

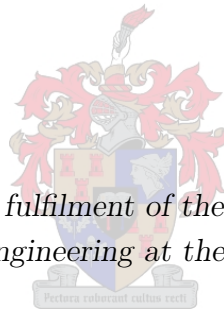


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A Cryogenic CMOS-based Control System for Testing Superconductor Electronics

by

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*Thesis presented in partial fulfilment of the requirements for the degree
of Master of Science in Engineering at the University of Stellenbosch*

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March 2008

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

Signature:

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Abstract

A Cryogenic CMOS-based Control System for Testing Superconductor Electronics

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Thesis: M.Sc.Eng. (E&E)

March 2008

A complete control system, with accompanying software, is designed to interface superconductive digital and sensory circuits for use in cryogenic vacuumed environments. It acts as an inter-mediator between superconductor electronics and room temperature electronics for research purposes.

In order to facilitate low bit-error rate communications with superconductive electronics, the system is designed to have ultra low-noise current and voltage sources for transmitting data to superconductor electronics. Very high sensitivity voltage inputs are also implemented for data extraction from superconductor electronics. It implements both digital as well as analog design components, including ADC and DAC devices. The data is transmitted via a USB cable connection at 1Mbaud to a computer where the data is processed by specially designed software and graphically displayed for user interfaced research.

Extensive research is done on the electronic components, such as CMOS devices, for functioning in an average temperature of 70 Kelvin inside cryogenic environments. This is done to reduce the thermal noise and heat transfer to superconductor electronics. An integrated temperature control system also ensures a stable environment for the electronics to operate at 70 K.

Uittreksel

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Maart 2008

'n Volledige beheerstelsel met meegaande sagteware is ontwerp om supergeleierlogika en sensorstroombane te toets in kriogeniese vakuumpoestande. Die beheerstelsel tree op as 'n tussenganger vir supergeleierelektronika en gewone kamertemperatuurelektronika vir navorsingsdoeleindes.

Om lae bisfout-tempokommunikasie te fasiliteer met supergeleierelektronika is die beheerstelsel ontwerp met ultra-laeruisstroom- en spanningsbronne vir data versending na supergeleierelektronikabane. Hoë sensitiewe spannings-intree kanale is ook geïmplementeer om data te onttrek van die supergeleierbane. Die ontwerp bevat digitaal en analoogkomponente, insluitend A/D en D/A omskakelaars. Data oordrag na 'n rekenaar word deur 'n USB-kabel teen 1 Mbaud gedoen, waar die data verwerk word deur die spesiaal-ontwikkelde sagteware. Hier word die data dan grafies voorgestel vir navorsings doeleindes deur die gebruiker.

Deeglike navorsing is ook gedoen op verskeie elektroniese komponente, soos CMOS-tegnologie, om in 'n kriokoeler by 'n temperatuur van 70 Kelvin te kan funksioneer. Dit word gedoen om termiese ruis- en hitte-oordrag te verminder. 'n Geïntegreerde temperatuurbeheerstelsel verseker 'n stabiele omgewing vir die elektronika om te werk by 'n temperatuur van 70 K.

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List of Abbreviations

AC	Alternating Current
ADC	Analogue to Digital Converter
A/D	Analogue to Digital
BeCu	Beryllium Copper
CDMA	Code Division Multiple Access
CMOS	Complementary Metal-Oxide Semiconductor
COSL	Complementary Output Switching Logic
CPU	Central Processing Unit
/CS	Chip Select Not
CT	Command Type
DAC	Digital to Analogue Converter
D/A	Digital to Analogue
DC	Direct Current
EM	Electro Magnetic
GBW	Gain Bandwidth
GND	Ground
GUI	Graphical User Interface
HF	High Frequency
IC	Integrated Circuit
I/O	Input/Output

ISP	In-System Programmable
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPF	Low Pass Filter
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
MUX	Multiplexer
OCR	Output Compare Register
Op-amp	Operational Amplifier
PCB	Printed Circuit Board
ppm	Parts per million
PWM	Pulse Width Modulator
RF	Radio Frequency
RSFQ	Rapid Single Flux Quantum
RX	Receive
SCE	Superconductor Electronics
SIS	Superconductor-insulator-superconductor
SMD	Surface Mount Device
SMT	Surface Mount
SO	Small Outline
SOIC	Small Outlined Integrated Circuit
SQUID	Superconducting Quantum Interference Device
/SS	Slave Select Not
TTL	Transistor-Transistor-Logic
TX	Transmit
USART	Universal Synchronous and Asynchronous Receiver Transmitter

List of Symbols

Constants:

n	nano, scale constant, 1×10^{-9}
μ	micro, scale constant, 1×10^{-6}
m	milli, scale constant, 1×10^{-3}
k	kilo, scale constant, 1×10^3
M	mega, scale constant, 1×10^6
G	giga, scale constant, 1×10^9
k	Boltzmann's constant = 1.38×10^{-23} J/K

Units of Measure:

A	Ampère
°C	Degrees Celsius
Hz	Hertz
J	Joule
K	Kelvin
Ω	Ohm
s	Seconds
min	Minutes
V	Volt
W	Watt

Variables:

ΔT	Temperature difference
T_C	Critical temperature of a superconductor

Chapter 1

Introduction

One of the great and important discoveries made in the previous century would be that of superconductivity. This field is rapidly expanding with various new and promising possibilities, especially in the field of electronics.

Superconductivity is generally described as the disappearance of electrical resistance at very low temperatures. This phenomenon happens when certain metals, for instance mercury or compositions such as niobium nitride or $\text{Yba}_2\text{Cu}_3\text{O}_7$ (YBCO), are cooled down to their critical temperatures, T_C . Due to the low values of T_C , they are cooled down in cryogenic environments. These environments are usually created by liquid helium cryostats or cryocoolers which produce very low temperatures. Below a temperature of T_C , the material takes on new electrical properties where the electrical resistance of the specific material drops to zero.

One example of implementing this technology is seen in superconductor Josephson Junctions [1, 2, 3]. These Josephson Junctions are used as building blocks in designing RSFQ logic devices, proposed by Likharev and Semenov [4], for designing sub-terahertz-clock-frequency digital systems. They are also used as building blocks in devices such as the SQUID magnetometer [5].

Other implementations of superconductors can be seen in the SIS mixer [6] for millimetre wavelength astronomy telescopes as well as in the superconducting hot electron bolometer [7] for measuring the energy of electromagnetic radiation.

Promising future applications for superconductor electronics (SCE) are in the telecommunications industry. Here RSFQ logic can be used to reduce interference in CDMA-based systems [8], and thereby allowing more users on the system. Wireless communications also benefit from this technology where RF front-ends [9] are designed with ultra fast superconducting analogue to digital converters (ADCs) [10].

Although the concept of SCE technology holds great potential for the future, it is still difficult to interface. The clock frequencies of SCE circuits can range from 10 GHz to 300 GHz and operate at very low amplitude input and output signals, typically in the lower millivolt range. Noise could easily clutter these signals. Measurement systems therefore need to be as noise free as possible

to extract valid data from SCE circuits.

For laboratory tests of SCE circuits, lower frequency inputs and outputs are required. SCE test equipment could be interfaced below 1 kHz, but to speed up bit-error rate measurements, test frequencies of around 100 kHz would be ideal. Test signals at much higher frequencies, carrying higher frequency noise, could easily interfere with the very sensitive RSFQ devices.

This thesis focuses on building a device for interfacing and testing SCE circuits, such as RSFQ [11] and COSL [12, 13, 14] devices.

A brief discussion of the following chapters are given below:

- Chapter 2 gives a background overview of why a cryogenic CMOS-based control system is needed, along with a specification list for designing such a system.
- Chapter 3 shows initial designs that explore three possibilities for designing a control system that would work at 70 K.
- Chapter 4 shows a detailed design for each subsystem that is implemented in the control system.
- Chapter 5 shows how all the subsystem building blocks fit together when implementing the control system. It also shows how the software was developed and implemented to control the system.
- In Chapter 6 results of various tests are given for evaluating the operation of the control system.
- Chapter 7 concludes this thesis, where recommendations are made and future prospects are discussed.

The appendix contains additional design information as well as developed software code. A calibration table for the calibrated PT1000 temperature sensor is shown and datasheet references are also given.

Chapter 2

Background and Specifications

As mentioned in Chapter 1, SCE technology holds great potential for the future, but critical research still needs to be done on this technology. Although expensive devices [15], such as Octopux [16] have been built for testing superconductive devices, this research attempts to design a simpler, cost effective interface for SCE devices. Octopux, designed at the State University of New York (SUNY), is also relatively slow, interfacing at approximately 1 kHz.

The necessity for designing a *cryogenic CMOS-based control system* will become clear when considering the meaning of the three separate terms.

2.1 Cryogenic Environments

Cryogenic is understood as producing very low temperatures such as those required for natural gas liquefaction.

Operating conditions for RSFQ and COSL families are not very favourable for normal semi-conductors. They usually operate inside vacuumed cryocoolers or liquid helium cryostats at very low temperatures. Niobium based RSFQ and COSL families operate at 4.2 K or below [11, 17].

At the University of Stellenbosch a *Cryomech PT405* cryocooler is used for testing SCE devices. This is a two-stage, 4 K cryocooler where the first stage reaches a temperature slightly less than 60 K. Unless otherwise noted, this cryocooler was used in this thesis for experiments and tests in cryogenic environments. A representation of such a cryocooler is given in Fig. 2.1.

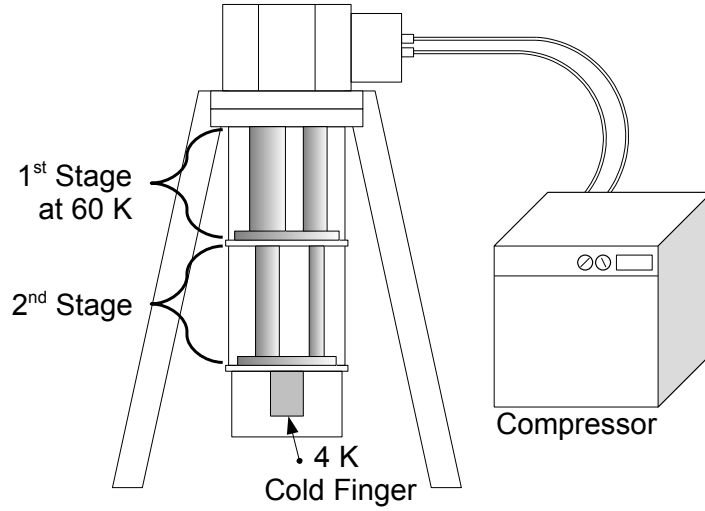


Figure 2.1: A two-stage, 4 K cryocooler.

A typical two-stage cryocooler delivers 0.5 W of cooling power at 4 K which must sustain this temperature against electric power dissipation, thermal radiation losses, poorly vacuumed space and heat transferring cables [18]. Multiple thermal shields and a good vacuum (10^{-5} atmosphere), significantly reduce heating, but the heat flow through cabling from the outside of the cryocooler still injects heat into the system.

The idea was proposed to test normal semiconductor electronic devices in the 1st stage of the cryocooler to see whether it is possible to implement a control system in this 60 K environment for interfacing SCE devices. The design also needs to be compact in order to fit into the very confined space of the 1st stage of the cryocooler.

The reason for lowering the operating temperature of the control system is to minimize the heat-load on the SCE devices. If the electronics of the control system is outside the cryocooler, the heat-load on the SCE circuits would be great because of the large temperature difference (ΔT) of 300 K between the outside and the inside of the cryocooler.

On the other hand, if the control system could be implemented inside the 1st stage of the cryocooler, thereby cooling down the semiconductor electronics, the heat-load on the SCE circuits would be significantly less, as the ΔT would minimize to approximately 55 K.

Cooling down the semiconductor electronics would also have another beneficial effect. Internal noise on a system is generated by various sources with thermal noise being one of these sources. A theorem by Nyquist, in Appendix A of [19], states that the mean-square noise voltage appearing across the terminals of a resistor of R ohms at temperature T Kelvin in a frequency band B hertz is given by

$$v_{rms}^2 = 4kTRBV^2, \quad (2.1)$$

where k = Boltzmann's constant, relating temperature to energy.

Thus, when temperature is reduced, the noise will also be reduced thereby creating a more sensitive measurement system.

2.2 CMOS Technology

Complementary metal-oxide-semiconductors (CMOS) are used in developing various semiconductor electronic devices. CMOS devices are developed with p-type and n-type MOSFETs for logic functioning.

One of the objectives of this thesis is to develop a system that can operate in cryogenic environments with great stability and integrity. CMOS technology has very low power dissipation and very high noise immunity, making it ideal for the given task of cryogenic operation.

Datasheets of manufactured semiconductor electronic devices usually specify that the absolute maximum rating for the operating temperature is between $-55\text{ }^{\circ}\text{C}$ (218 K) and $125\text{ }^{\circ}\text{C}$ (398 K). This is mainly because these devices are not tested and are not required to operate outside of these specifications. Various reports [20, 21, 22, 23] however indicate that CMOS technology can operate at very low temperatures. Several tests on CMOS components in cryogenic environments proved that CMOS technology has great potential for operation in very low temperatures.

Although there are different processes of developing different kind of CMOS devices, datasheets do not indicate which CMOS technology processes were used in the development of these devices. Therefore, in this thesis, off-the-shelf CMOS components were ordered and tested to implement in the control system.

2.3 Control System

SCE circuits operate at very low input and output amplitudes in the order of micro to millivolts. The difference between a logical '0' and '1' could typically be as low as $150\text{ }\mu\text{V}$ in RSFQ-to-DC converted outputs. It becomes difficult to distinguish the signals in this range from electrical noise. In order to minimize noise from external power supply sources, batteries should be used as independent power supplies for the control system. Regularly used bench power supply sources, used for driving normal semiconductor electronics, add HF noise to signals and should therefore be avoided.

A system needs to be developed to easily and accurately test SCE devices. A user should be able to manipulate data signals from a user interface on a computer and send this data signals to a SCE device. As signals are sent, data also needs to be sampled from the SCE outputs and graphically displayed on the computer for the user to interpret.

Therefore a software interface module needs to be developed to accommodate the designed hardware, combining them to form a control system to interface and test cutting edge SCE technology for research purposes.

2.4 Guidelines and Specifications

A complete USB-compatible hardware system with several input and output channels should be designed with the necessary amplification stages. Accompanying the hardware, a complete software package should be developed to enable a user to control a cryogenic SCE experiment.

In order to control SCE circuits, output channels should contain programmable current and voltage sources, implemented by DACs and analogue electronics. ADCs should also be implemented as part of the input channels to sample data from SCE circuits. An on-board microprocessor could be implemented to act as the system CPU and control the data signals to and from the SCE devices as well as the communication to and from the computer. The user should also be able to calibrate these channels.

Noise levels need to be kept to a minimum, therefore very low noise components should be implemented to ensure very high signal quality. In order to shield the control system from external HF noise, the necessary aluminium container packages could be designed to fit the designed electronic PCBs.

As discussed in Section 2.1, it would be ideal if the control system could be designed to operate in cryogenic environments with temperatures as low as 70 K.

A more detailed specification list is given below for the hardware design of such a control system:

- Adjustable positive and negative high current output channels between ± 500 mA.
- Adjustable bipolar low current output channels between $\pm 25\,000$ μA for sending DC or logic signals with step sizes of 1 μA .
- Adjustable bipolar low voltage output channels between $\pm 65\,000$ μV for sending DC or logic signals with step sizes of 2 μV .
- High sensitivity bipolar voltage input channels between $\pm 50\,000$ μV with a sensitivity of 2 μV .
- A computer interface via a USB port.
- Fibre optical communication connection to reduce external noise.
- Components cryogenically specified for operation at 70 K.
- Temperature read-out and on-board heater for temperature control around 70 K.
- Operation from battery pack to reduce external noise.
- Battery voltage & current sensing.

Chapter 3

Proposed Control System Configurations

Due to the extreme environment, and the lack of data for devices at cryogenic temperatures, several prototypes were built and tested.

In this chapter more than one design approach is considered and discussed. Each proposed design, with implementation and evaluation, will progress to the subsystems that will eventually be implemented in the final design. As the design concepts improve and evolve, new ideas force some of the specifications to slightly bend in a different direction, but brings with it a more refined specification list.

The complete design of subsystems for the final implemented control system will be discussed in Chapter 4.

3.1 Computer Interface and Communications

A quick and easily connectable interface always simplifies the usability of a design. The USB standard has become the most popular connectivity feature of the modern computer. For universal connectivity, a USB connectable interface has been designed.

3.1.1 USB Interface

In order to create the USB interface, a USB to RS232 converter has been implemented. The RS232 serial communication system is a widely used protocol for most data transferring devices, including the ATmega16 microcontroller, which is implemented and discussed in Section 4.5. This serial protocol is also easy to implement in the software programming of the design.

The FT232BM is a USB-USART device from *FTDI Ltd.*, which was chosen for the USB to RS232 conversion. It complies with the USB standard by interpreting the USB protocol and converting the signal to the well-known serial protocols such as RS232, RS422 or RS485. The USART concept is described in Section 3.1.2.

By installing the FTDI device on the USB port, the computer recognises it as an additional COM port. The user can then implement this port exactly as per normal COM port methodology and can programme the software accordingly.

Data can then easily be sent over this communication line with maximum speeds of up to 1 Megabaud (RS232) or 3 Megabaud (RS422/RS485), depending on the clock speed and setup of the communicated device.

An USB-RS232 converter has been designed on a small PCB, implemented with the FT232BM device. This board was used for testing the proposed configurations described in this chapter. It is quite easily implemented with a few additional components and is powered by the 5 V single supply rail of the USB connection.

The additional components that are required to implement the FT232BM device consists of an external 6 MHz crystal, an EEPROM memory device, some resistors and capacitors and a ferrite bead. Two optional LEDs can also be connected to assigned pins on the FTDI device to indicate when data is transmitted and received.

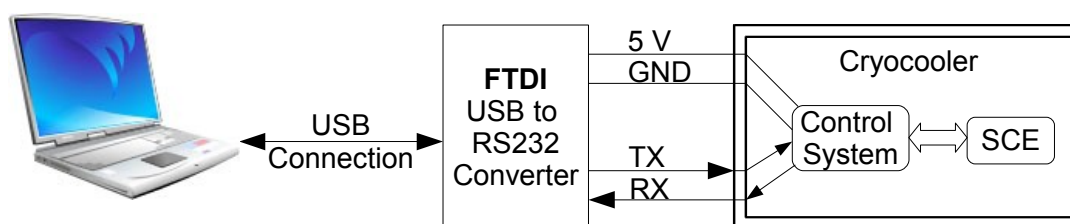


Figure 3.1: FTDI system implementation for first generation tests.

Fig. 3.1 shows the conceptual implementation of the FTDI interface that was used for communication with the control system in the cryocooler. The 5 V power is directly supplied by the USB port and can deliver up to 500 mA of current. This was used to deliver power to the prototype boards of the control system.

With this interface design, conceptual prototyping of a control system could be done, but it was found that external noise could also be coupled onto the system through the direct 5 V line as well as through the direct copper TX and RX lines. A better design, which provided more shielding, was required.

The single rail 5 V supply from the USB was inadequate for driving the *high current channels* of the design and a double rail power supply was also required for most of the operational amplifiers in the later designs.

The power supply was thus implemented by using batteries, shielded in a metal box, placed just outside the cryocooler. It was placed outside because the vacuum inside the cryocooler could cause the batteries to outgas. Outgassing happens when embedded gasses in a solid material is removed by the reduction of pressure.

Fibre optical cable provided a solution for shielding the data transfers. If data could be transferred into the cryocooler by means of fibre optical cable, then the control system would be completely shielded from any outside electrical noise sources.

Another advantage of using fibre optical cable is that it also prevents thermal conduction. It does not transfer heat as copper wires would. It reduces the heat transfer from the outside of the cryocooler to the control system at 70 K.

In Fig. 3.2, this more advanced conceptual design is illustrated. Data is sent from the computer via the USB connection, transformed to the RS232 UART protocol and then immediately converted to light signals travelling on the fibre optical cables. The data is then reconverted to electrical pulses on the inside of the cryocooler.

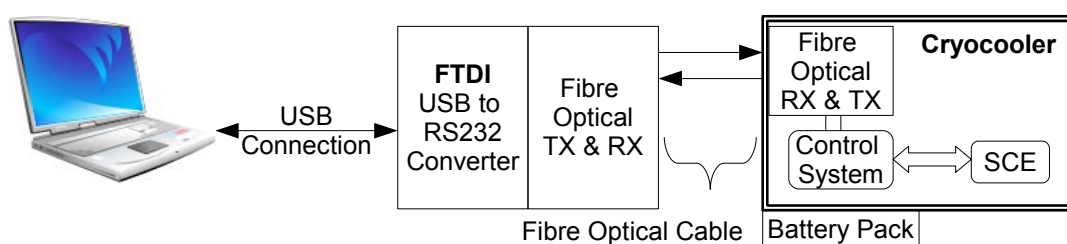


Figure 3.2: Fibre optical FTDI implementation for computer interface.

A more advanced USB-USART converter board has been built for the final design, using the newer FT232R device. The advanced board design is described in more detail in Section 4.2.

3.1.2 USART

By using the USB-RS232 COM port described in Section 3.1.1, the Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) communication system is used in communicating with the cryogenic control system. The asynchronous mode of the USART is used throughout this thesis. This means that no data is sent when the transmitting device has nothing to send, thereby reducing communication traffic.

The USART system operates with two data wires, one to send or transmit data and the other to receive data. In asynchronous mode, a transfer is started by sending a *start* bit, followed by five to eight data bits, an optional parity bit and a *stop* bit. These settings as well as the transfer speed are pre-configured, so that both devices know how and at what speed to interpret the received signal.

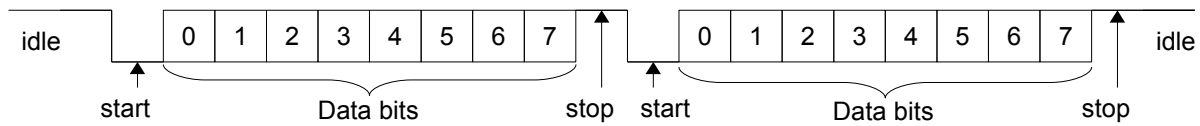


Figure 3.3: A UART serial transmission of two bytes.

Fig. 3.3 shows a typical transmission of two bytes, both having a *start* and *stop* bit, without the parity bit. With each *start* bit, the transmission is synchronized.

According to the pre-configured transfer speed, the receiving device will interpret each bit precisely halfway through the period assigned for each bit position to determine if the bit is a '1' or a '0'. If one of the clock frequencies of either the receiver or transmitter has an error of up to $\pm 2\%$ [24], the data will still be transmitted correctly, because each byte is synchronized with each *start* bit.

3.1.3 SPI Communication

The serial peripheral interface (SPI) is a protocol that uses three wires for high-speed synchronous data transfer between devices such as microcontrollers and ADCs. The three wires on the SPI bus are SCK, MOSI and MISO respectively, which will be clarified in this section. There is usually one master device with the possibility of one or more slave devices that are addressed.

A fourth wire is usually needed as a *slave select not* ($/SS$) or *chip select not* ($/CS$) control line to ensure communication with the correct device. This $/SS$ line must be selected and pulled down to a logic low before communication can begin. An unlimited amount of devices can thus be connected to the SPI bus as long as each slave device has its own $/SS$ line.

The master sends data to the slave device on the MOSI (Master Out Slave In) line, while at the same time data bits are transferred from the slave to the master on the MISO (Master In Slave Out) line.

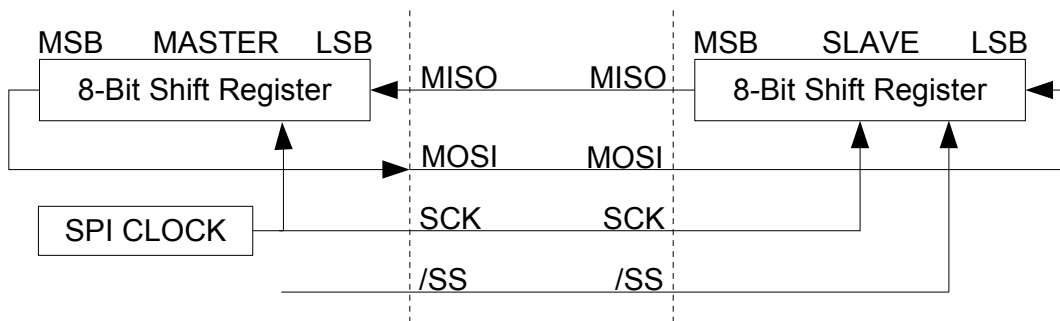


Figure 3.4: SPI master-slave interconnection.

As seen in Fig. 3.4, each device has its own 8-bit shift register. With each clock pulse on the SCK line, initiated by the master device, an exchange transaction is being done. Each device shifts out the most significant bit (MSB). This MSB is received by the other device and is saved in the least significant bit (LSB) position of the 8-bit shift register. After every 8-bit exchange, a new byte can be transmitted on the SPI bus.

It should be noted that the master device can be configured to start the SCK either on a logic high or a logic low. It can also be configured to transfer data either on the first or second edge of the clock. This all depends on how the slave device was built to operate, and therefore necessitates a careful design with the proper SPI configurations, done in software, for SPI communication.

3.2 Microchip PIC Control System

The first step towards designing a cryogenic control system was to test various CMOS devices inside the cryocooler to see what kind of technology would work in cryogenic environments.

The aim was to find a microprocessor to function as the system CPU, where data can be sent for interpretation and then redirected to specific output channels. These output channels would contain DACs to submit analogue data to SCE circuits. The data sent to the CPU would come from a personal computer by means of the interface described in Section 3.1.

The CPU would then also contain ADCs as input channels for reading in data from the SCE devices and then send each channel's data back to the computer for interpretation.

3.2.1 Component Choices

The PIC16F876A microprocessor from Microchip was used in previous designs and seemed to be a good candidate for cryogenic tests. It is specified as a 8-bit CMOS FLASH Microcontroller, thus some CMOS technology is definitely implemented in this device. The DIP package type was used.

The ADS7807U is a low-power ADC with 16-bit sampling capability using state-of-the-art CMOS structures. The only drawback is that this device is rather large because of the 28-pin SO package, containing only one sampling channel. Nevertheless, this device was chosen and tested.

For the DAC, the TLV5618A low power, 12-bit converter was chosen. This device is small with a 8-pin SOIC package and is also implemented with a CMOS process.

3.2.2 Initial Cryogenic Test Setup

A test setup was created by cooling down the PIC, DAC and ADC inside a 4-Kelvin, 2-stage *Gifford McMahon* cryocooler. An aluminium box was designed, as seen in Fig. 3.5, to contain the two PCB parts, with the PIC on one board and the DAC and ADC on another. They were

interconnected by a SPI bus. The pins of the DIP package of the PIC was soldered to the socket to ensure connectivity even at low temperatures.

The clock frequency of the PIC was produced by an external 11.0592 MHz crystal.

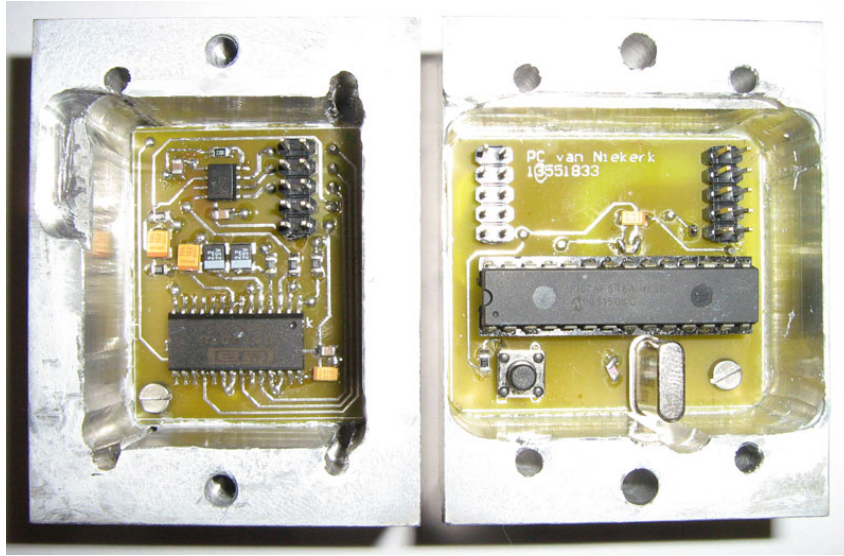


Figure 3.5: Test boards and aluminium boxes for the DAC and ADC (left) and the PIC16F876A (right).

The two parts of the box fit together to form a cube, where the metal provides shielding as well as heat transference away from the PCBs, as the electronic ground underneath the PCB is connected to the metal box.

A thermocouple was placed in a small hole on the outside of the metal box, with some heat sink thermal paste, to measure the temperature while the system cooled down. The *Dow Corning 340* heat sink compound was used on all thermal connection points for better heat transference. This compound does not have any oily substances or gasses and stays in a paste form at vacuumed cryogenic temperatures. Therefore this compound is preferred for the use in cryogenic environments above any normal heat sink compounds.

One of the PIC timers was programmed to interrupt and send data to the DAC, on the SPI bus protocol, to output a unity voltage. As seen in Fig. 3.6, this voltage was then immediately redirected back to the ADC and sampled.

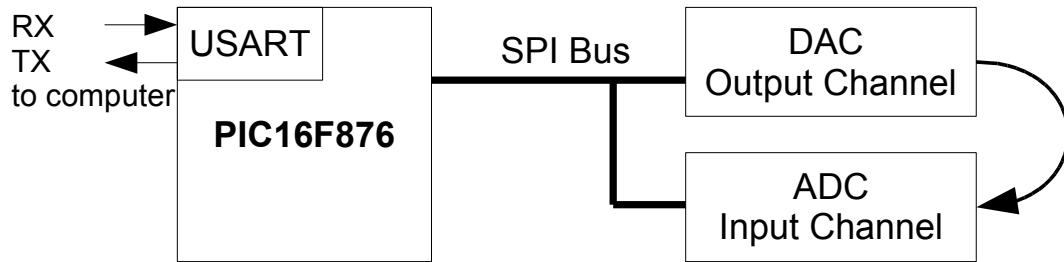


Figure 3.6: An illustration of the PIC test setup.

In turn, the SPI bus was used again by the PIC to read out the sampled voltage from the ADC to continuously send it back to the computer.

3.2.3 Results

Data from the ADC were recorded according to the temperature decrease and shown in Fig. 3.7. Here it can be seen that the ADC is quite stable as the temperature lowers to about 220 K, where it suddenly measured a higher voltage. Then at 160 K, the ADC measurement drops very steep and continues to drop down as the temperature lowers to 150 K.

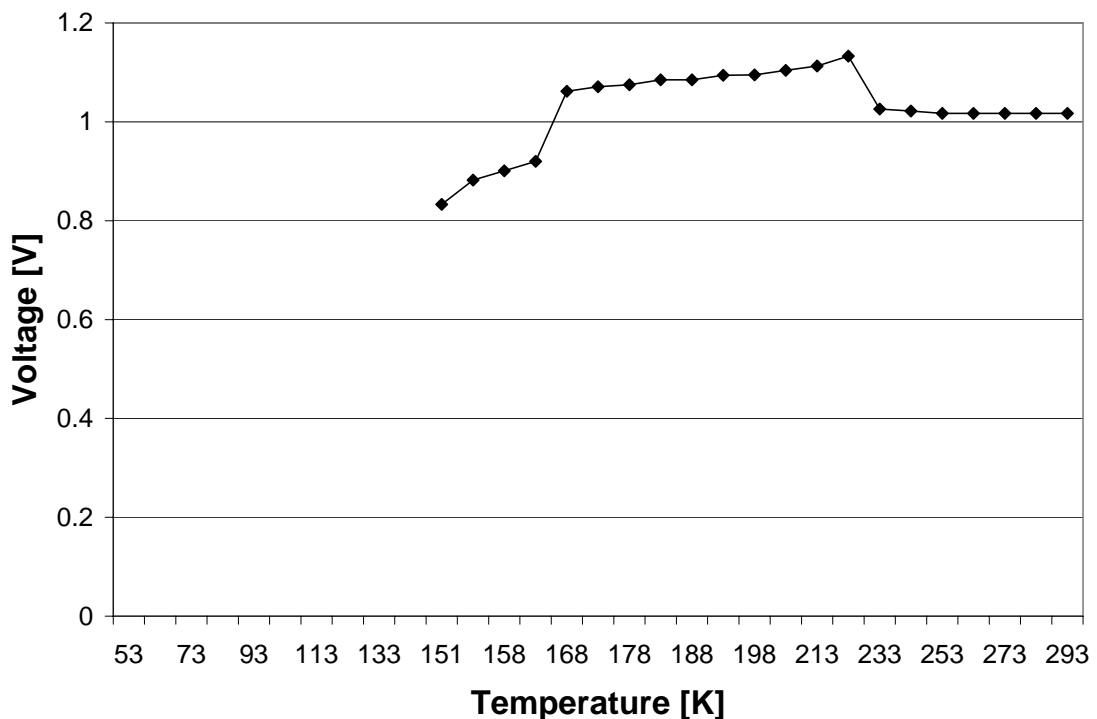


Figure 3.7: The ADS7807U ADC results while sampling 1 volt in cryogenic temperatures.

At this stage, the PIC microprocessor stopped functioning, failing to continuously transmit the ADC values. This could be observed by the non-responsive TX and RX LEDs on the FTDI interface that stopped blinking. Blinking of LEDs indicate that data is being transmitted and received and that the PIC is still active.

As the temperature was increased gradually, the PIC only started functioning again at a temperature of 198 K. The reason for this is that the temperature measured by the thermocouple on the outside of the metal box did not reflect the true temperature of the inside of the electronics. A temperature hysteresis could be observed.

This configuration was cooled down more than once with the same results for each test.

3.2.4 Conclusion

Upon closer inspection of the PIC data pages, it was observed that only the FLASH and EEPROM memories were implemented with CMOS technology and that the rest of the PIC, such as the inputs and outputs were implemented with TTL technology.

From these results it can be concluded that the PIC16F876A is not suitable for cryogenic operation. A new device was thus required.

Measured results have shown that the ADC showed a nonlinear response with temperature drop. The package type also proved too big for implementing more than one channel in a confined space such as in the cryocooler. Either a smaller single channel device or a multi-channel device is required and therefore the ADS7807U is not used further in this research.

Although the DAC worked fine, a higher resolution DAC is required. A 16-bit DAC would be ideal for real fine adjustments. Therefore the TLV5618A will not be used in the further design of the control system.

Positive results from this experiment were the verification of the SPI interface and the FTDI USB-RS232 computer interface, which were used in the experiments to follow.

3.3 ATMEL PWM Subsystems

In order to improve the design, the ATMEL AVR microcontrollers were considered. The AVR family devices are CMOS 8-bit microprocessors, based on the advanced RISC architecture.

Some of these devices have on-board pulse width modulators (PWM) which could be used for creating sine waves to send data to SCE devices.

A discussion of the component choices is given, followed by an overview of how the on-board PWM works. The ATMEL AVR devices as well as analogue components were tested in the cryocooler and the results are shown here. This is followed by a prototype control system design that was built and tested, where PWM signals were implemented. It is then concluded with a discussion of the results of the control system design.

3.3.1 Component Choices

The ATMEL AVR family has three basic groups of devices. They are the tinyAVR, megaAVR and more application specific AVRs such as LCD and USB controllers.

The tinyAVRs are more general purpose microprocessors with up to 8 kB of Flash program memory and 128 bytes of SRAM and EEPROM with limited peripherals.

The megaAVRs are more powerful with up to 256 kB of Flash program memory, 4 kB EEPROM and SRAM with an extensive peripheral set. Peripherals includes SPI and USART communication, PWMs and on-board ADCs and DACs.

Table 3.1: ATtiny selection options.

Devices	USART [Qty]	SPI [Qty]	PWM [Qty]	10-Bit ADCs [Qty]	RAM [Bytes]
ATtiny13	0	0	2	4	64
ATtiny26	0	1	2	11	128
ATtiny2313	1	0	4	0	128

Table 3.1 shows some ATtiny selection options. The ATtiny26 device was chosen because of the SPI functionality so that in-system programming could be done.

Two devices were considered for implementation of a system CPU for the control system. The one is the AT90USB128 device which offers a new USB 2.0 full-speed interface where greater transfer speeds could be attained. It later became clear that the computer side software programming, to connect with this device, was too complex and required expensive software packages to implement completely. Since a USB interface was already implemented by the FTDI device, the AT90USB128 was obsolete. A separate new project, apart from this thesis, was created to specifically implement the USB 2.0 full-speed interface and to report [25] on how it is to be implemented.

The other CPU option was the ATmega16 device. It was chosen because it has both SPI and USART communication ports, 32 I/O pins and can operate at an internal clock speed of up to 8 MHz. This device is described in more detail in Section 4.5.

3.3.2 Pulse Width Modulation

Pulse Width Modulation (PWM) is the creation of a square wave at a certain frequency, where the duty cycle can be changed to control the amount of power it produces. By changing or modulating the duty cycle, the average power of the signal is also changed. If the duty cycle is increased, meaning that the signal is high for longer than it is low, the average power will also be increased.

ATMEL AVR devices come standard with a feature to create an 8-bit PWM signal by toggling an I/O pin between a logic low, '0', and high, '1'. It is implemented with an 8-bit counter/timer

and an 8-bit output compare register (OCR). This OCR contains a value that is compared by the counter as shown in Fig. 3.8. This device also has a glitch-free transition if the OCR value is changed while in operation.

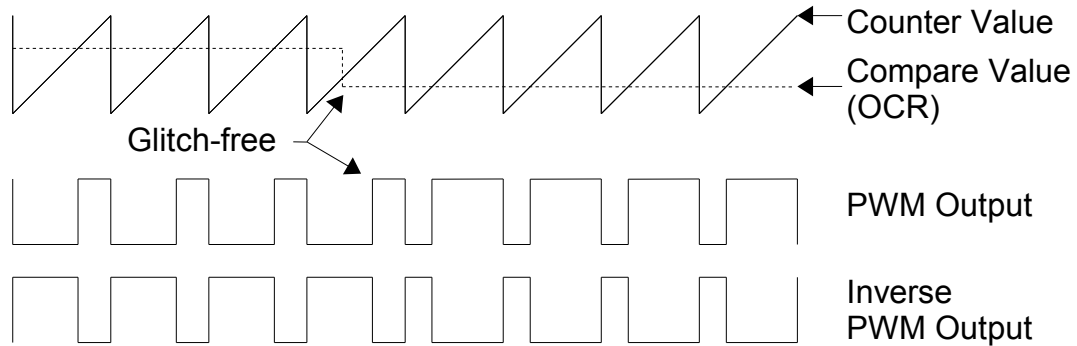


Figure 3.8: PWM example of an ATMEL AVR device.

The output of the I/O pin is low until the counter reaches the compared value, stored in the OCR. It then switches the I/O pin to high and keeps it high until the counter overflows and restarts the counting. The ATtiny26 device also has an inverse of this I/O pin, where the pin is kept high until the counter reaches the OCR value. It then switches the I/O pin value low and keep it low for the remainder of the period. When the counter overflows, the output of the I/O pins are reset and the process is started again.

Using this concept, a DAC can thus be implemented by filtering the PWM output with a low pass filter (LPF), consequently averaging the output. Likewise, a sine wave can be generated if the duty cycle is varied according to a sine wave formation, by changing the OCR value on each counter reset. An actual sine wave can then be extracted by this varying PWM signal if it is filtered by a LPF. The cut-off frequency of the LPF should be higher than that of the produced sine wave but lower than the 8-bit counter timer frequency of the square wave.

The PWM square wave frequency can be varied, but in this design it was set to the device's maximum of 250 kHz on the full 8-bit counter value. The sine wave frequency then depends on how many data points are used to create it. If only 10 data points are used and the OCR is changed on every counter reset, the sine wave frequency would then be 25 kHz. If more data points are used, the sine wave frequency would decrease but will result in a smoother signal output.

3.3.3 Cryogenic Tests

Before any system designs could continue, some cryogenic tests needed to be done. In this section ATMEL AVR devices, op-amps as well as some analogue components were tested in cryogenic environments to see what components could be used.

3.3.3.1 ATMEL AVR

An ATtiny26 DIP package was programmed in AVR Studio 4 in assembler language. It was programmed to use the on-board PWM to create a sine wave form, from a pre-calculated sine wave lookup table. The assembler code for this implementation can be found in Appendix C.1.

The device can be programmed to operate from an external crystal, with a maximum value of up to 16 MHz or an internal RC clock with a maximum value of up to 8 MHz. For this experiment the internal clock of the ATtiny26 was programmed for operation at 8 MHz.

This PWM signal was then filtered by a 1st order RC low pass filter (LPF) to obtain a sine wave. The cut-off frequency was calculated by choosing the RC values as in Eq. 3.2.

$$f = \frac{1}{2\pi RC} \quad (3.1)$$

$$= \frac{1}{2\pi(2.2 \times 10^3)(2.7 \times 10^{-9})} \quad (3.2)$$

$$= 26.8 \text{ kHz}$$

The sine wave had an amplitude of just less than 5 V with a DC offset of 2.5 V. No PCB was designed for this test. As seen in Fig. 3.9, the LPF was implemented by soldering a ceramic capacitor and a carbon resistor directly onto the pins of the microcontroller.

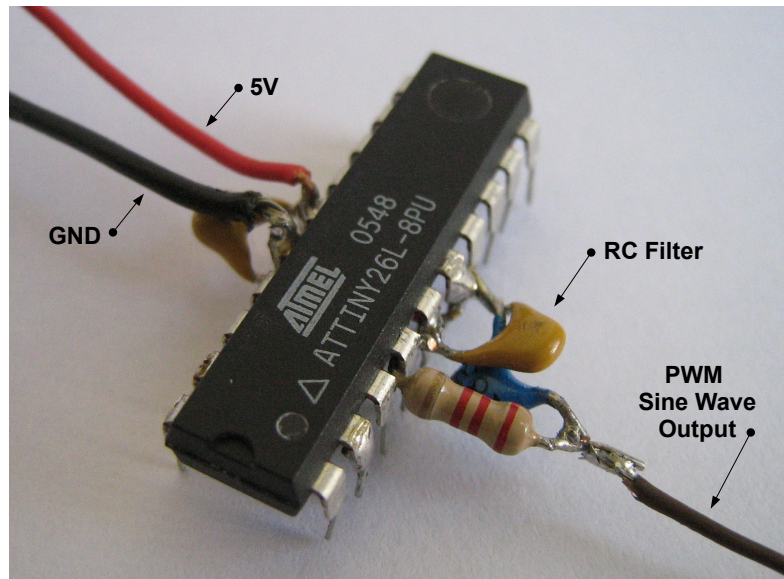


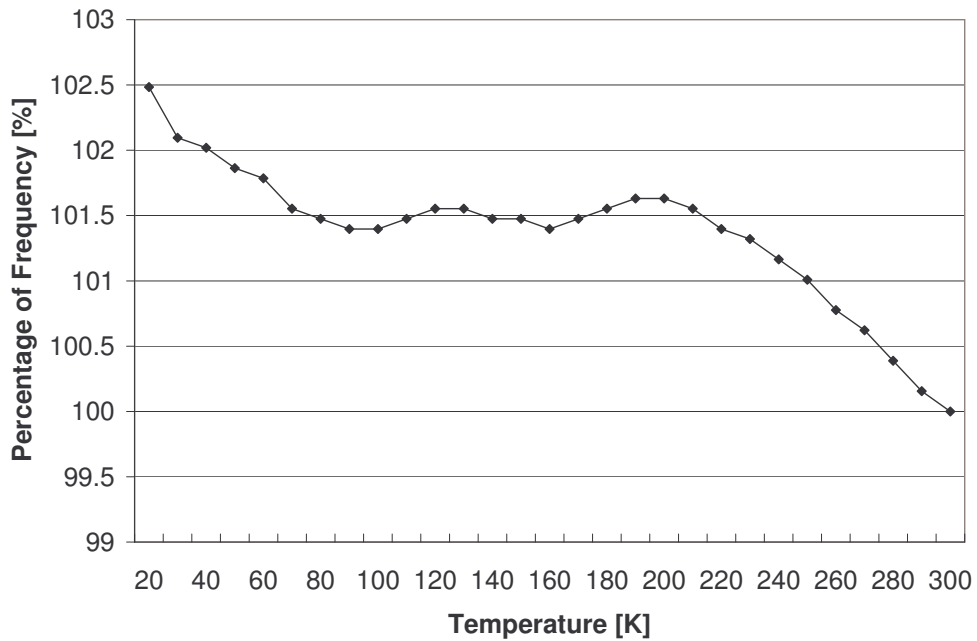
Figure 3.9: The ATtiny26 PWM connection wires for tests in the cryocooler.

Three wires were directly attached to the pins of the ATtiny26. One supplied a positive 5 V, another the ground of 0 V and the last was the output which produced the sine wave. The microcontroller was programmed to automatically initialize and set up the watchdog timer and then produce a constant sine wave.

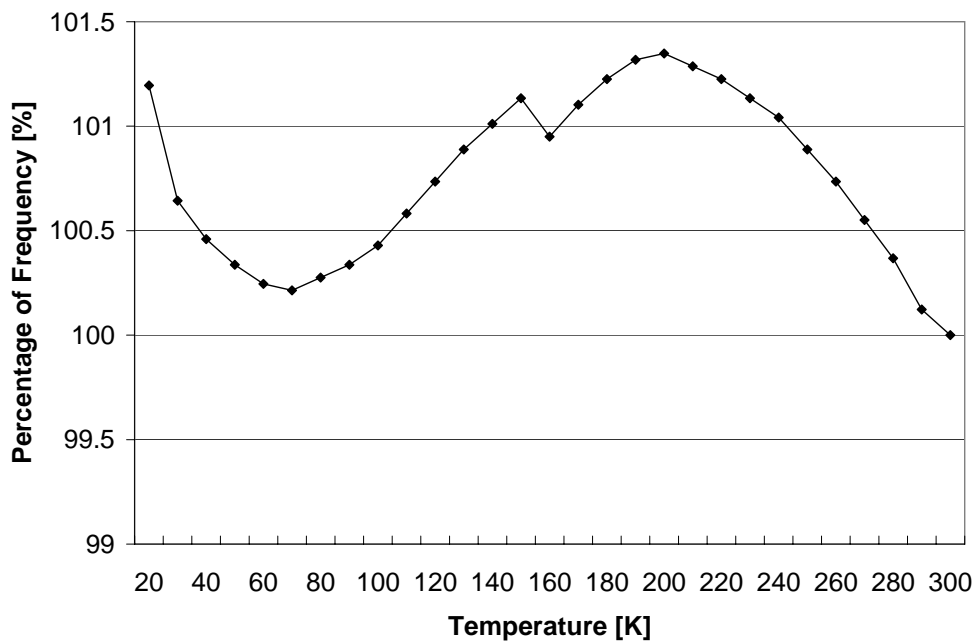
The function of the watchdog timer is to automatically reset the microcontroller if the normal sequence of the program is not executed. This function helped because every time the cryocooler started up, an EM spike was produced that disrupted the normal functioning of the ATtiny26. With the watchdog timer, the device could start up again and perform its programmed tasks.

The top of the ATtiny26 was tightly clamped down to the cold finger of the Cryomech. The cold finger is the metal part of the cryocooler that reaches a temperature of 4 K. Again some of the cryogenically tested *Dow Corning* thermal paste, described in Subsection 3.2.2, was placed between the ATtiny26 and the cold finger to ensure a good thermal connection. This ensured that the temperature measured on the cold finger would be very close to the temperature of the inside of the electronic device.

A digital frequency counter was used to measure the sine wave frequency, generated by the PWM. The data results of two experiments are shown in Fig. 3.10, where the measured frequency is displayed as a percentage of the desired frequency.



(a) ATtiny26 device 1



(b) ATtiny26 device 2

Figure 3.10: Internal clock frequency deviation of two ATtiny26 devices plotted against temperature drop.

At 300 K the devices produce a desired frequency of 100%. As the temperature lowers, the frequency of the device in Fig. 3.10(a) tends to stabilise at about 1.5% above the desired frequency. This means that the internal RC clock of the ATtiny26 device is clocking 1.5% faster

than its original value.

The frequency produced by the device in Fig. 3.10(b) does not deviate so much as the device in Fig. 3.10(a) with a maximum deviation of 1.4%. It then tends to return to the original frequency value at 70 K.

The sine wave output was quite noisy at the lower temperatures. This could be ascribed to the use of the ceramic capacitors in the LPF. As seen in Fig. 3.13, the ceramic type capacitor values lower at cryogenic environments. This caused the cut-off frequency of the LPF to rise, allowing more of the PWM square wave signal to filter through. The observed noise gave lead to further tests being done on other analogue components, shown below in this same section.

However, both microcontrollers actually worked to a temperature as low as 15 K, where it stopped to produce the sine wave. As the device was heated up again, it was reset by the watchdog timer and started working correctly at 20 K. This indicates that there was a temperature lag on the inside of the electronics of only about 5 K. This means that the electronics of the ATMEL AVR families can withstand very low temperatures and will still work well in cryogenic environments.

The USART communication transfer speed of the ATMEL devices is configured according to the clock frequency of the device. That means that the bit rate is directly influenced by the variation of the internal clock frequency of the device. This is not a problem because the USART communication can still function correctly even with a bit rate error of up to 2%, as showed in Subsection 3.1.2.

Even with this error, the ATMEL AVR devices can be reprogrammed to calibrate the internal RC clock to the desired frequency.

3.3.3.2 Amplifiers

Various types of operational amplifiers were placed inside the cryocooler to test their functionality in low temperatures. Table 3.2 shows seven op-amps that were tested in cryogenic environments.

Table 3.2: Lower Temperature Limit of Tested Op-amps.

Op-amp	Type	Gain-Bandwidth* [MHz]	Temperature [K]
LM412	BJT with JFET input	3	120
OPA277	CMOS	1	73
OPA727	CMOS	20	48
TLV2211	CMOS	0.056	30
LMC6064	Silicon-gate CMOS	0.1	63
LMC6462	CMOS	0.05	70
LMC7101	CMOS	1	44

*The specified gain-bandwidth product of the op-amp

These op-amps were tested in the inverting amplitude configuration, set with a gain of $A_V =$

10. The indicated failure temperature was measured where the output swing started to clip, gain-bandwidth (GBW) decreased, or the output latched to the rails [18]. The LMC7101 was chosen to implement in the rest of this thesis designs because it performs best with a 1 MHz GBW at reasonably low temperatures and is available in the small SOT-23 package.

3.3.3.3 Digital Potentiometer

The AD5262 is a 2-channel 8-bit digital potentiometer from Analog Devices. It comes in 20 k Ω , 50 k Ω and 200 k Ω versions and support dual supply operation. The 256 position potentiometer is digitally controllable via the SPI bus. It can be used for digital offset adjustments when calibrating the control system's output channels.

This device was placed on a small PCB. It was then fastened to the cold finger of the cryocooler for a cryogenic test. In order to change the resistance value of the digital potentiometer, it was connected to a micro processor on the outside of the cryocooler via a SPI bus. The micro-controller was programmed to change the value of the device every 5 seconds from its minimum to its middle value, and then to its maximum value, while it was cooled down. These values were measured and the results are shown in Fig. 3.11.

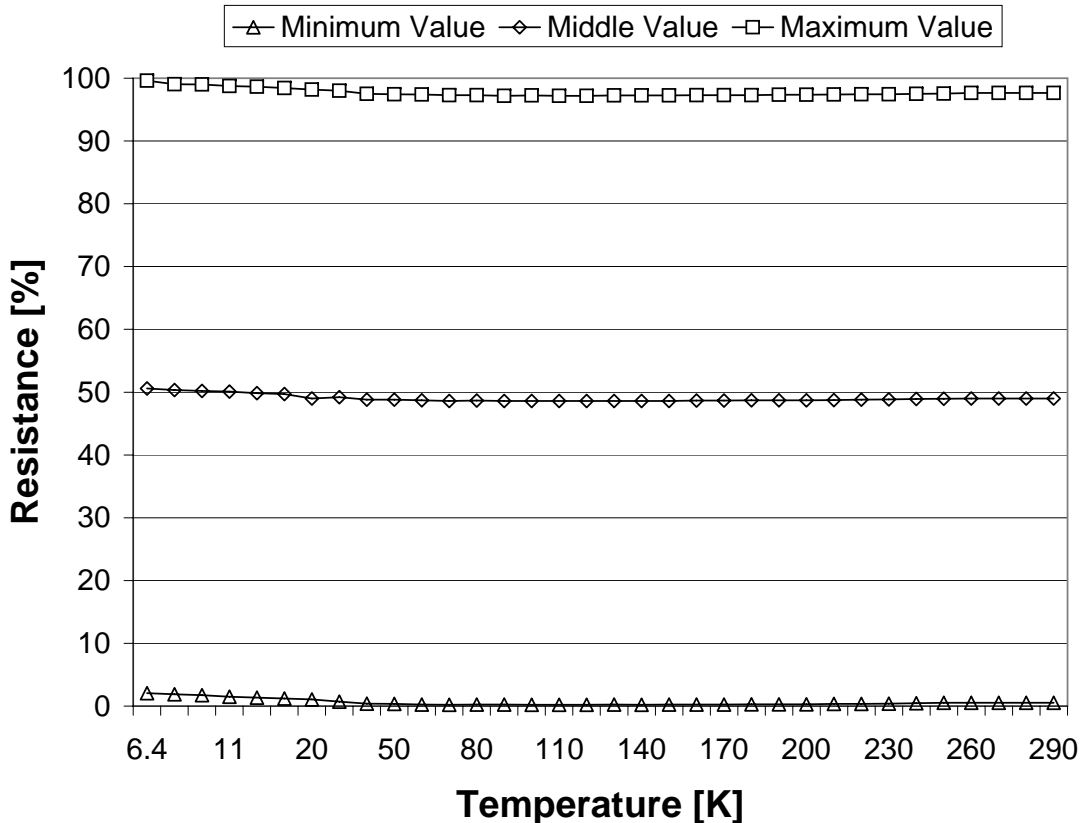


Figure 3.11: The AD5262 digital potentiometer cryogenic test results.

This device actually performed very well. At 290 K it is just 2% below its specified top value. Thus it has a small offset. This offset stays the same as the temperature lowers to about 40 K. Most remarkable was that its values stayed quite linear to a temperature as low as 6.4 K.

3.3.3.4 Analogue components

Two types of resistors were tested [18], one is a radial carbon composition resistor and the other a 0.25 watt SMD carbon film resistor.

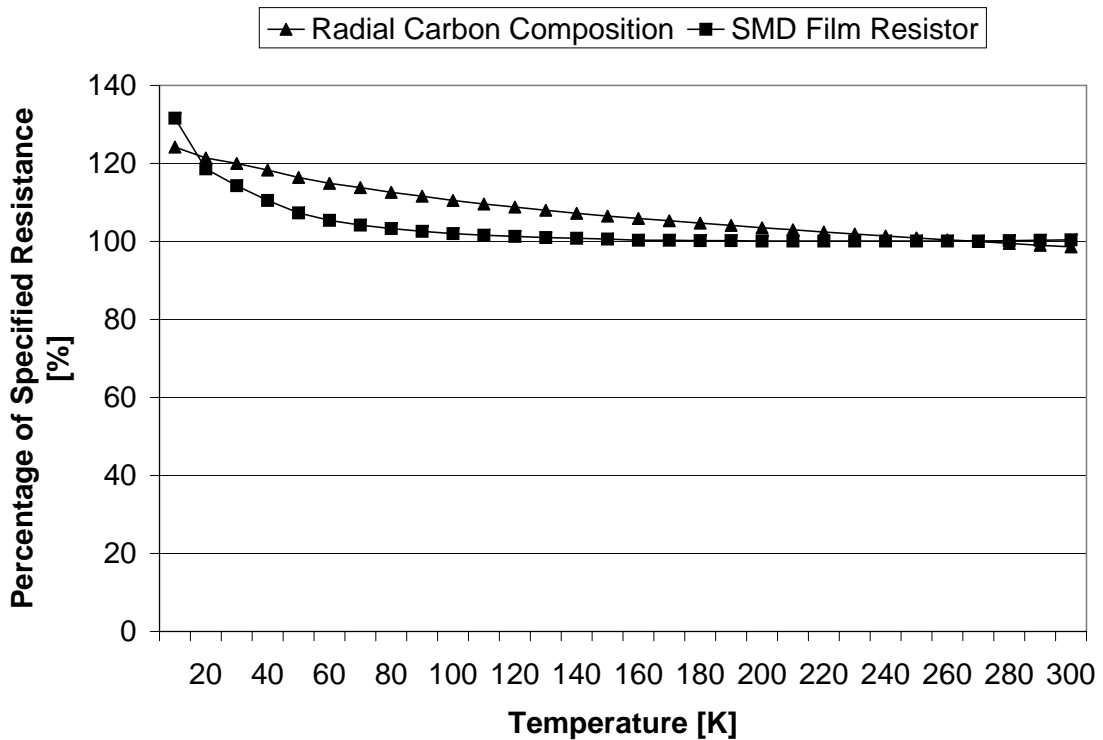


Figure 3.12: Tested resistor types with characteristic plots against cryogenic temperature range.

From the characteristics in Fig. 3.12 it can be seen that the SMD film resistor is more suitable. Apart from being small, it varies only with about 5% from its original value at 70 K as opposed to 15% variation of the carbon composition resistor at 70 K. The control system is thus implemented with the SMD film resistor types.

Fig. 3.13 shows eight different types of capacitors that were tested [18] inside the cryocooler.

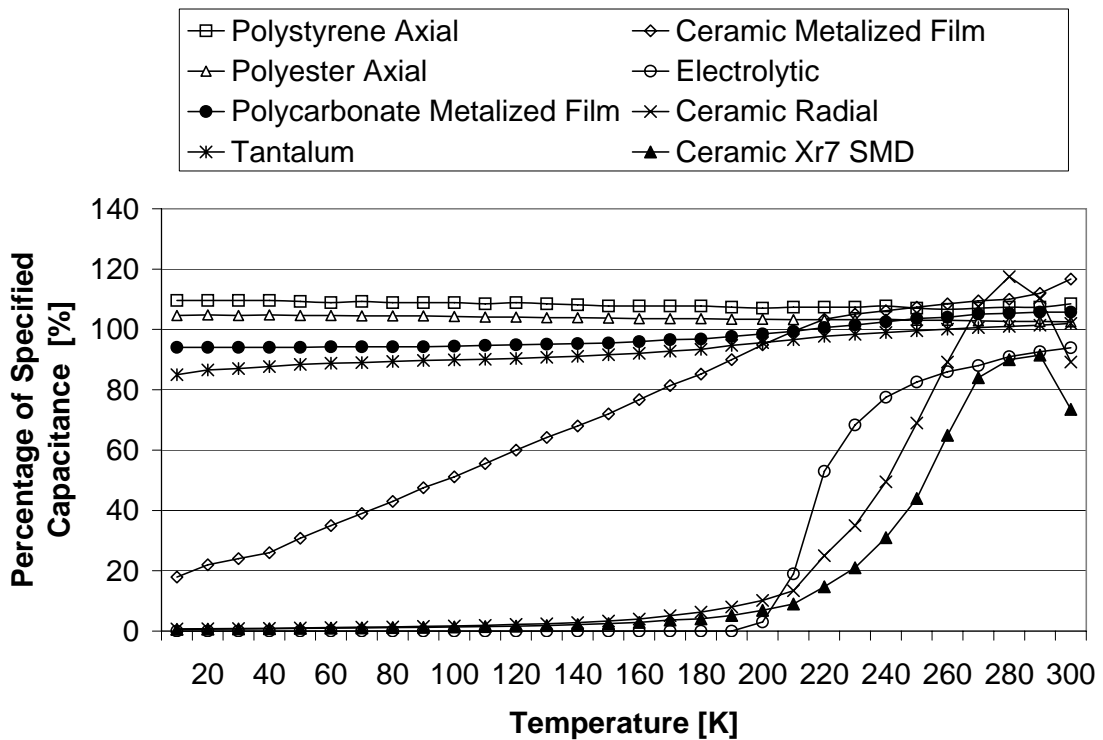


Figure 3.13: Tested capacitor types with characteristic plots against cryogenic temperature range.

These results indicate that the polystyrene, polyester, polycarbonate and tantalum capacitor types offer the most acceptable performance. Of these four types, the axial polyester capacitor has the best performance with only a 4.6% capacitance rise at 70 K while the tantalum capacitor has the greatest capacitance deviation. It drops to 88% of the specified capacitance at 70 K. However, the tantalum capacitor can still be used in cryogenic environments by choosing a slightly larger capacitance to compensate for the capacitance drop.

In the control system, the tantalum capacitor is preferred above the polyester capacitor because it is manufactured in SMD package types which take up less space, opposed to the axial type capacitors. It also is mainly used as decoupling capacitors which do not require precision capacitor values.

3.3.4 System Design

3.3.4.1 Overview

Since the cryocooler takes approximately 90 minutes to cool down to 4 K, and even longer to warm up (see Appendix E), it would be convenient if the software on the control system microcontrollers inside the cryocooler could be updated while in the cryocooler. The ATMEL AVR devices are in-system programmable (ISP). They can therefore be programmed, or reprogrammed while already implemented in a system or on a manufactured PCB through a SPI serial interface.

With the new information about the ATMEL AVR family devices which can operate in cryogenic environments, a new system implementation was proposed and can be seen in Fig. 3.14.

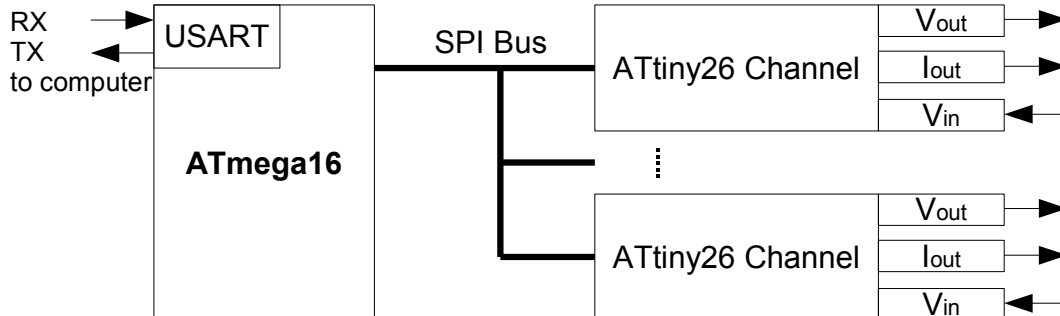


Figure 3.14: The ATtiny26 PWM subsystems.

It was decided that a channel should be implemented by an ATtiny26 device, where each channel would consist of a voltage output, a current output and a voltage input stage. The ATtiny26 has enough on-board ADCs to sample incoming data while the D/A conversions could be done by using the PWM as described in Section 3.3.2. With this PWM DAC the voltage output, current output as well as sine waves can be controlled.

The ATmega16 would operate as the system CPU as well as the local ISP programmer for the ATtiny26 subsystem controllers. The advantage of this system is that the channels could be reprogrammed while inside of the cryocooler, without having the trouble of opening up the cryocooler to retract the hardware for programming.

3.3.4.2 Implementation

GUI software as well as hardware code for the ATmega16 were written for implementing this ISP. An in depth study [26, 27] was done to understand the protocol for ISP programming of the ATtiny26 device through the SPI bus. Each compiled hex file was read into the software, interpreted and sent to the ATmega16 programmer to program the ATtiny26 channels as desired.

Although each ATtiny26 device was connected to the 3-wire SPI bus, each device needed to be connected with a /SS and a /RESET wire. The /RESET wire is specifically used when the device is programmed, while the /SS is used to select the device for data communications.

Each ATtiny26 channel was designed onto its own small PCB. As seen in Fig. 3.15, these boards were then placed in parallel, closely above the ATmega16 motherboard and connected to it with soldered-on ribbon cables. The ATtiny26 SMT SOIC packages and the large square axial polyester capacitors can be seen. The smaller tantalum capacitors are also visible.

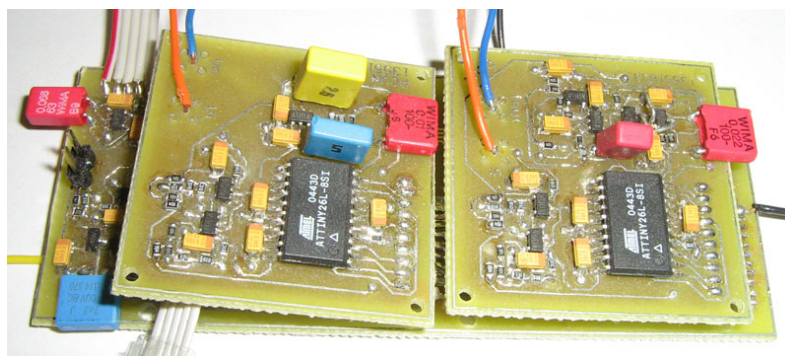


Figure 3.15: Prototype system with ATtiny26 subsystem boards.

The ATtiny26 devices were programmed to produce a maximum PWM frequency of 250 kHz. When filtered, it could produce a sine wave with a maximum frequency of 25 kHz. This is done by only repeating 10 data points to form a sine wave from a lookup table as described in Subsection 3.3.2.

System observations showed that some high frequency noise coupled onto the power supply rails. The high frequency noise came from the PWM sine wave generation and influenced the op-amps on the output channels. This high frequency noise is unacceptable for RSFQ circuits which operate internally with very low power pulses. These pulses occupy a very wide bandwidth, which makes the RSFQ circuits very susceptible to noise. Any HF noise on RSFQ input signals could couple into the RSFQ circuits and cause erroneous pulses.

However, the *low current and voltage channel* designs on this system did work well and will be described in more detail in Chapter 4.

Also the ribbon cable connections were very difficult to solder underneath the boards and did not allow for easy interchangeable designs. Therefore a system redesign was necessary.

3.3.5 Conclusion

It was decided to discontinue the ISP PWM subsystem design as high frequency noise coupled onto the power supply rails. This caused low voltage noise on the outputs to the SCE devices. This high frequency noise is unacceptable for RSFQ circuits. Therefore only the amplitude-controlled logic signals would be implemented in testing RSFQ circuits in this control system.

Although the sine wave functionality of this system could not be implemented, the *low current and voltage channel* designs on this system did in fact work and was used and improved upon in the next design.

3.4 Final Proposed Cryogenic Control System

The Cryomech PT405 cryocooler, used at Stellenbosch, was designed so that the 2nd stage at the cold finger would be easily accessible to insert SCE test circuits. However, opening up and

getting to the 1st stage of the cryocooler is a complex and time consuming procedure. It is opened up from the 2nd stage at the bottom of the cryocooler, layering off all the parts up to the 1st stage. As mentioned, this part is a very confined space which leaves little room for electronics.

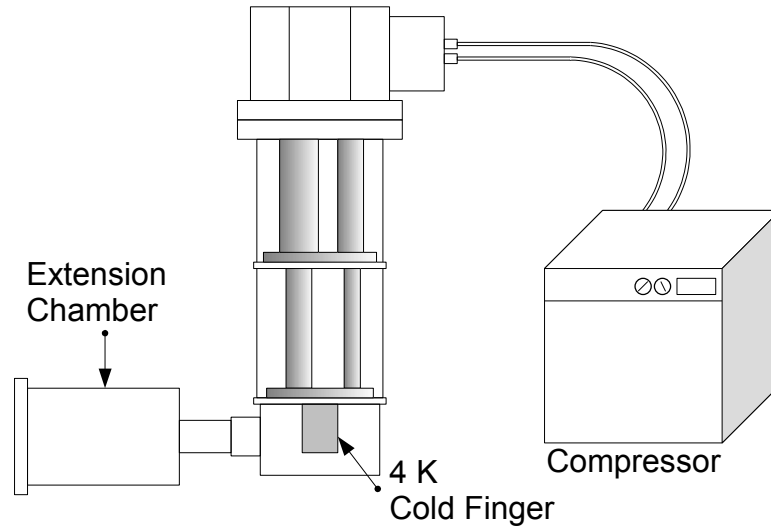


Figure 3.16: Cryocooler stages with extension chamber.

Stellenbosch technicians added a container that expands the vacuum of the cryocooler, as illustrated in Fig. 3.16. This container forms part of the cryogenic vacuum environment. It extends from the 2nd stage of the cryocooler for easy access to the SCE devices on the cold finger. This was designed so that electronic measurement devices could easily fit into it, without having to un-mount all of the cryocooler parts to get to its 1st stage. Even though this forms part of the cryogenic vacuum environment, it will not reach cryogenic temperatures.

A final design for a cryogenic control system was proposed where a motherboard, which contains the ATmega16 system CPU, would have plug-in slots for input and output channel daughterboards. Each daughterboard would then have its own ground plane that would be separated from the interfering digital logic ground plane of the microprocessor.

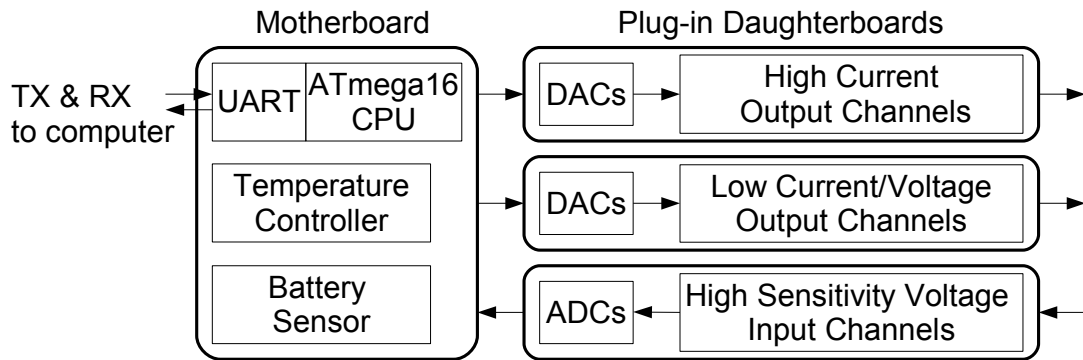


Figure 3.17: Motherboard with input and output daughterboards.

The daughterboards would then plug into the motherboard at 90 degree angles. This design would then be very versatile and adaptable, because the user would be able to choose which output channels are needed for the experiment and swap channels as needed. If channel modifications are needed, these daughterboards can be redesigned and plugged into the same slots in the motherboard, without redesigning the whole system.

The space inside the 1st stage of the cryocooler would not be enough to fit this system. Even though the temperature in the extension chamber will not reach a low of 70 K, it was decided to place the final design in the extension chamber of the cryocooler. All the necessary tests were done to design a system that would work at 70 K so the design concept was proven. This add-on chamber forms part of the cryogenic vacuum and is shielded against external noise sources.

The original problem with heat-load from 300 K electronics to the 4 K SCE was mitigated by using long, thin wires that are thermally grounded to the cooling stages of the cryocooler at 60 K, ± 35 K and then 4 K.

3.5 Conclusion

In this chapter various system implementations were considered. Three basic designs were proposed, studied and implemented. They were tested to evaluate their functionality in cryogenic environments and to find the best possible solution for the given system specifications.

The PIC device from Microchip failed to operate well in cryogenic environments. New devices were tested in the cryocooler upon which the ATMEL AVR family returned very promising results. These ATMEL devices were used throughout this thesis.

Cryogenic tests were also done on different digital devices as well as analogue components to ensure stable building blocks for designing a *cryogenic CMOS-based control system*.

The ATtiny26 PWM subsystem channels produced too much noise. This concept was abandoned.

Finally, a system was designed to operate in an extension chamber of the cryocooler. This design implemented the ATmega16 microprocessor as the system CPU on a small motherboard. This motherboard has plug-in slots to fit various input and output channels for data transfer tests with SCE devices.

In the next chapter, the design of all the various subsystems of this final system design will be explained.

Chapter 4

Design of Subsystems

The final system configuration was decided upon. This system configuration is designed and consists of various subsystems that eventually make up the whole design. In this chapter the detailed design of each sub-block will be given and its functionality will be explained.

This chapter starts off with the backbone of power circuitry which supplies the power to the rest of the system. It is then followed by the fibre optical USB converter that links the user with the control system. The implementation of various SMT devices are discussed whereupon the temperature control system and the various channel designs will follow. This chapter will conclude with the discussion of the daughterboard identification system.

4.1 Power Circuitry

This section of the design enables the whole control system to function at the correct power levels. The power supplied to the control system should be very stable and unsusceptible to external noise components. Therefore the control system is designed to operate from shielded battery sources to avoid EM interference and external noise from light emitting sources, bench power supplies or any other 50 Hz humming.

Implemented voltage regulators are discussed as well as the utilization of some voltage references. System current consumption monitor circuits as well as battery voltage level check-up circuits are described, as this control system is battery operated and these levels need to be monitored.

4.1.1 Voltage Regulation

The ATmega16 microprocessor, and most of the other implemented devices, were designed to operate from a 5 V power source. The op-amps however, operate on a dual rail power supply of ± 5 V in order to implement the bipolar channel designs of the control system.

Four normal AA, 1.5 V batteries are used in series to create a 6 V power supply. Another four batteries are used to create a negative rail of -6 V. Over time, the voltage level of batteries

lowers as power is drawn from them. In order to create a stable and consistent power supply, the voltage from the batteries needs to be regulated.

Two regulators, the LP3872 and the LM2990, both from National Semiconductor, were chosen to regulate the dual rail power supply. The LP3872ES-5.0 is a 1.5 A ultra-low dropout linear regulator that regulates a precision output voltage of 5 V. It has a low dropout voltage of 0.38 V at 1.5 A. This means that it will still support the control system with a steady 5 V supply even if the 6 V battery voltage drops to 5.38 V. This regulator, capable of delivering 1.5 A, will ensure that the *high current channels* of the control system as well as the rest of the electronic devices will be supplied with enough power.

Fig. 4.1 shows the basic connection configuration of the regulators. A 10 k Ω resistor is used as a pull-up resistor on the shut-down not (/SD) pin of the LP3872 to enable the regulator. 10 μ F tantalum capacitors are implemented as decoupling capacitors, one on the input and one on the output of the regulator.

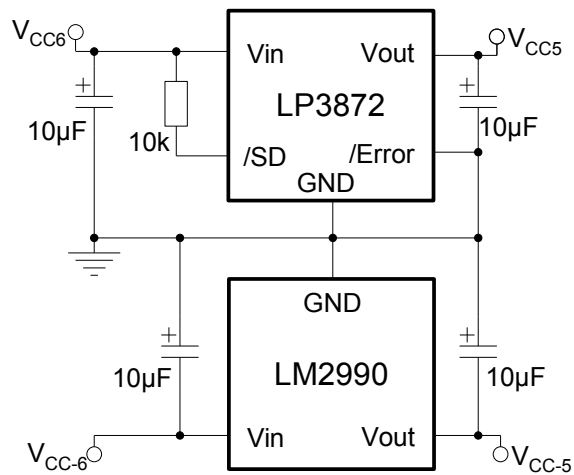


Figure 4.1: Regulator configurations

The LM2990S-5.0 is a negative low dropout linear regulator that will ensure a negative voltage rail of -5 V. It has a dropout value of 0.6 V at the maximum load current of 1 A. The configuration for this device is also shown in Fig. 4.1. It is a simple three pin device implemented with decoupling tantalum capacitors, also 10 μ F, on the input and output.

These regulators are short circuit protected, so no additional short circuit prevention electronics were required.

4.1.1.1 Additional Regulator

The maximum supply voltage of the INA322 instrumentation amplifier is 7.5 V. The total of 10 V regulator rails described above is thus too large for this device. Therefore another voltage

regulator was implemented to regulate a negative voltage of -1.25 V. The UCC284-ADJ is a negative adjustable regulator which can deliver 0.5 A with only a 0.2 V dropout voltage.

By using this regulator in conjunction with the 5 V regulator, a total of 6.25 V can be supplied to the instrumentation amplifier. This is done so that the INA322 can measure very small, millivolt, bipolar inputs around 0 V.

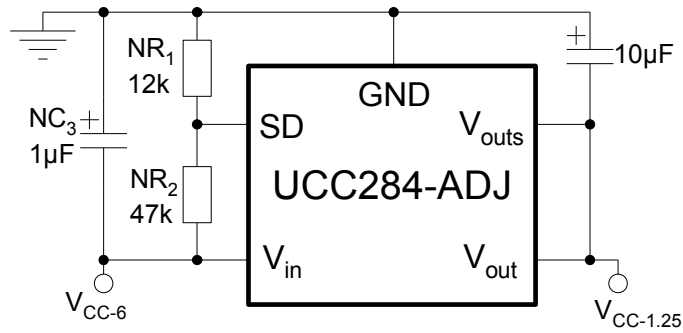


Figure 4.2: The UCC284-ADJ negative regulator setup.

The particular regulator setup for -1.25 V can be seen in Fig. 4.2. If a different voltage adjustment is required, two resistors can be added. A resistor R_1 should then be placed between V_{outs} and V_{out} and a resistor R_2 should be placed between V_{outs} and GND. The output voltage, V_{out} , can then be represented by

$$V_{out} = -1.25 \times \left(1 + \frac{R_1}{R_2}\right). \quad (4.1)$$

In this case, V_{outs} was directly connected to V_{out} to produce a voltage of -1.25 V.

A 1 μ F decoupling capacitor is required on the input and a 10 μ F capacitor is placed on the output of the device. The regulator can be shut down when pin SD is pulled above -0.7 V. In order for it to operate this pin requires to be kept between -0.7 V and -1.6 V. Therefore, a 0.1 μ F tantalum capacitor in conjunction with a resistor network was placed on the SD pin to supply a constant voltage of -1 V to keep it in operational mode.

4.1.2 Voltage References

The DACs, ADCs and the INA322 instrumentation amplifiers require accurate voltage references to operate correctly. Two voltage reference devices, the REF3225 and REF3212 from Texas Instruments, were implemented. They are both of the CMOS family type. The REF3225 supplies a voltage of 2.5 V while the REF3212 supplies a 1.25 V reference.

They have excellent ultra-low drift of 20 ppm/ $^{\circ}$ C which relates to only a 0.46% voltage drift over a wide temperature range down to 70 K.

Both references operate from the 5 V supply with only a 0.1 μF tantalum capacitor on the input and output of each device.

4.1.3 Current Sensing

A current sensing circuit has been designed to monitor the current drawn from the batteries. It can measure the current of both power supply rails and display these measured values on the user interface software on the computer.

The hardware of the current sensor is implemented with a INA322 instrumentation amplifier, as the basic design shows in Fig. 4.3(a). It operates from a 5 V single supply rail and therefore the measured 6 V battery voltages need to be downscaled. The battery voltages are divided by a factor of 2, using two 100 k Ω resistors.

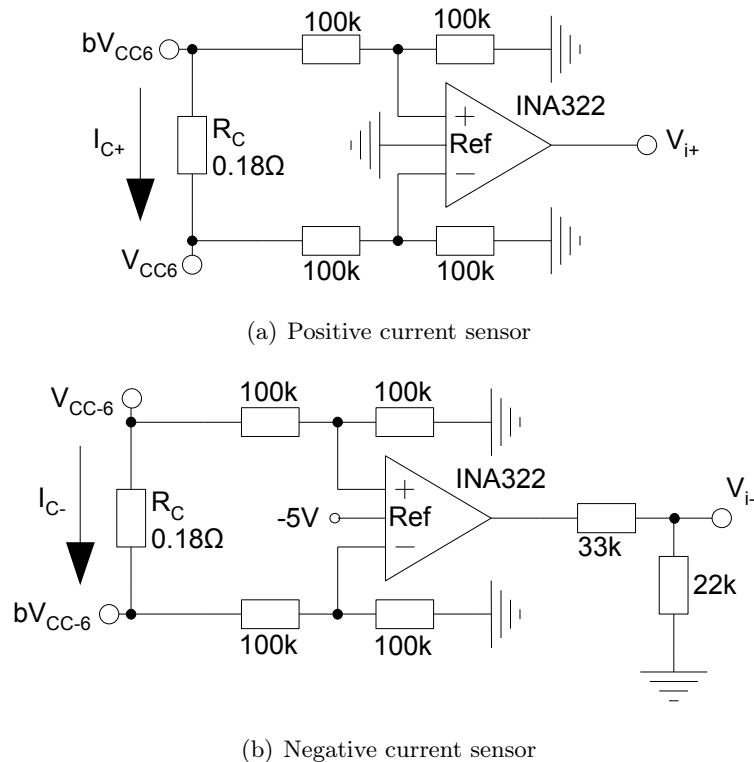


Figure 4.3: Current sensing circuits

bV_{CC6} is connected directly to the 6 V battery supply and V_{CC6} is the value that is supplied to the regulators, thereby measuring all the current drawn from the batteries.

R_C is a specially designed low ohmic, high power, current sensing resistor. It is a SMT resistor from Meggitt CGS. The current, I_{C+} , is measured by detecting the voltage drop over

this resistor and then calculating it by Ohm's law as follows

$$I_{C+} = \frac{bV_{CC6} - V_{CC6}}{R_C}. \quad (4.2)$$

A high amplification factor of 50 of the INA322 limits the maximum voltage difference that can be measured to 0.2 V. This implies that the maximum current that can be measured is 1.11 A. The resistor has a power rating of 1 watt and a value of 0.18 Ω . By using the power formula

$$P = I_C^2 R_C, \quad (4.3)$$

where P is the power in watts, the maximum allowed current through R_C is calculated as 2.35 A.

Although not indicated in the figure, amplification by the INA322 can be set by connecting two external resistors. In this case the amplification is set to a factor of 50. The device measures the voltage difference over R_C , amplifies the difference by 50 and produces a voltage, V_{I+} on the output. This value is relative to the reference voltage of the INA322. The reference is connected to ground because, in this case, the measured voltage difference will always be positive and therefore above the reference.

In measuring the negative current, the same basic principals are used, but with minor modifications. Here the voltage rails of the INA322 are between -5 V and 0 V, where the -5 V is the new virtual ground for this device. This is done to be able to measure the negative voltage from the batteries. The current sensor on the negative rail was designed that as the current flows back to the batteries at bV_{CC-6} , shown in Fig. 4.3(b), the measured voltage difference across R_C would always be positive. This is only positive, relative to the voltage reference of the INA322 that is connected to virtual ground (-5 V). Therefore the output of the INA322 will be between -5 V and 0 V. As seen, voltage division is done at the output. This is done in order to scale the output value between -2 V and 0 V and to fit the ADC's measurement range. The same voltage division is also performed on the positive current measurement in order to fit the 0 V to 2 V measurement range of the ADC.

These measurements are sampled by the MAX186, a 12-bit, 8-channel ADC, which is discussed in Subsection 4.3.3. This device is also used in detecting the voltage levels of the batteries in the voltage sensing subsection.

4.1.4 Voltage Sensing

The voltage of the batteries that supply the power to the control system can be measured and their values displayed on the user interface software on the computer. This is done in order to see when the batteries need replacement or recharging.

Measurement of the voltage levels are done by using the MAX186. This device has 8 channels available for 12-bit A/D sampling. Two of these channels are used to measure the current consumption described in Subsection 4.1.3. Another two channels are used for voltage sensing.

The MAX186 is implemented here with its internal 4.096 V reference as described in Subsection 4.3.3. It runs on a dual rail power supply of ± 5 V. It is configured to sample data in bipolar mode, causing the reference voltage to divide by a factor of 2. The available references for sampling both the positive and negative currents and voltages are therefore ± 2.048 V. Thus, in order to sample the battery voltage levels, the ± 6 V needs to be downscaled. This is done by normal resistor voltage division as shown in Fig. 4.4.

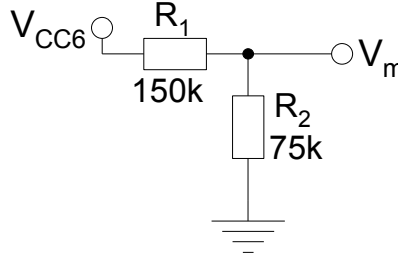


Figure 4.4: Battery voltage measurement adjustment

Here the sampled voltage, V_m is calculated by

$$V_m = V_{CC6} \left(\frac{R_2}{R_2 + R_1} \right). \quad (4.4)$$

High resistor values are chosen to limit the current that is dispensed. The maximum current flowing through these resistors is calculated by

$$\begin{aligned} \frac{V_{CC6}}{R_2 + R_1} &= \frac{6}{75 \times 10^3 + 150 \times 10^3} \\ &= 26.6 \mu A. \end{aligned} \quad (4.5)$$

The battery voltages are measured inside the cryocooler to assure that the right voltage levels are actually supplied to the control system.

4.1.5 Summary

A thorough design of the power circuitry was given, where the necessity of 3 regulators were discussed. The implementation of two voltage references were also given and discussed. As this control system will operate from batteries, the current consumption as well as the battery voltage levels are monitored and the designs of these circuits were given.

4.2 Fibre Optical USB Connection

As mentioned in Section 3.1.1, a USB-USART computer interface was implemented using a device from FTDI Ltd.

In this section, the design of the implemented FT232R device as well as the fibre optical data conversion design is discussed.

4.2.1 FT232R

The USB-USART computer interface has been designed using the FT232R device. This device interprets data signals from the USB port. The USB cable has 4 shielded wires coming from the computer. They are $D+$, $D-$, 5 V and GND, where $D+$ and $D-$ carries the transmitted USB data while the 5 V is used to power the FT232R device. The data lines can be connected directly to pins $USBDP$ and $USBDM$ on the FT232R device. It converts the signals to RS232 protocol and sends the serial data out on the RXD and TXD pins. The voltage levels of these pins can be set between 1.8 V and 5 V to directly interface with other IC devices. This is done with an external wire connection. In this case the value was set to 5 V by connecting the V_{CCIO} pin to the 5 V power supply.

The device was set up to draw power from the USB up to 100 mA, because only the FT232R device needs to be powered from the bus. On the FT232R device, pin $C0$ was configured to drive the TX data LED while pin $C1$ was set to drive the RX data LED to indicate that data is transmitted or received.

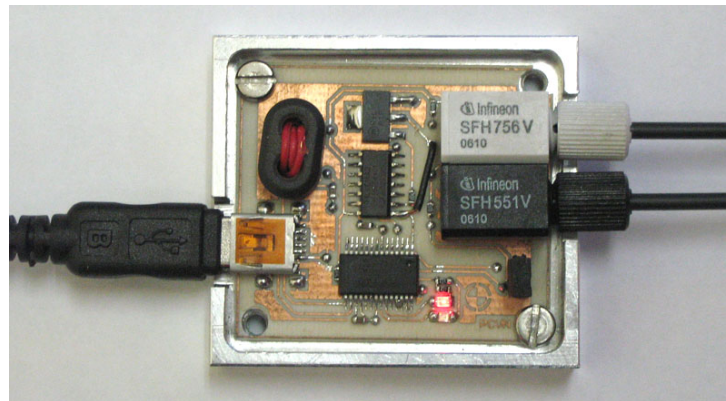


Figure 4.5: The FTDI USB-USART to fibre optical converter.

To implement this device, a small separate PCB layout, shown in Fig. 4.5, was designed. It has a USB mini-B connector on one side for computer communication and two fibre optical connectors on the other side going to the control system in the cryocooler. This PCB was placed in an aluminium cover. The design for this cover is given in Appendix B.

4.2.2 Fibre Optical Conversion

In order to communicate via fibre optical cables, the TX data needs to be converted or modulated into light signals. Also, a receiver is required to demodulate the RX light signals.

The TX signal is modulated by implementing the SFH756V, a special fibre optical transmitter diode. It has an anode and cathode pin for driving the diode. For RX light demodulation, the SFH551/1-1V photo detector receiver is implemented. Both of these devices have a light tight housing that ensures interference free transmissions. The maximum specified transfer rate for these devices is 5 Mbit/s.

A design was proposed in Fig. 4.6(a) for driving the TX diode by switching a transistor. When the USART is idle and not transmitting data, the logic state of the TX pin is high as described in Subsection 3.1.2. In this state, the inverter output is zero, causing the transistor to shut down so that there will be no current flowing into the collector pin. Therefore no current will flow through the transmitter diode which implies that no light is emitted by the diode. When data is transmitted, the TX signal goes low causing the transistor to switch on hard and allowing current to flow through the transmitter diode. Light is therefore emitted on a logic 0 and vice versa. A 40 mA current limit was designed by placing a $100\ \Omega$ resistor at R_1 . The maximum allowed current specified by the device is 50 mA.

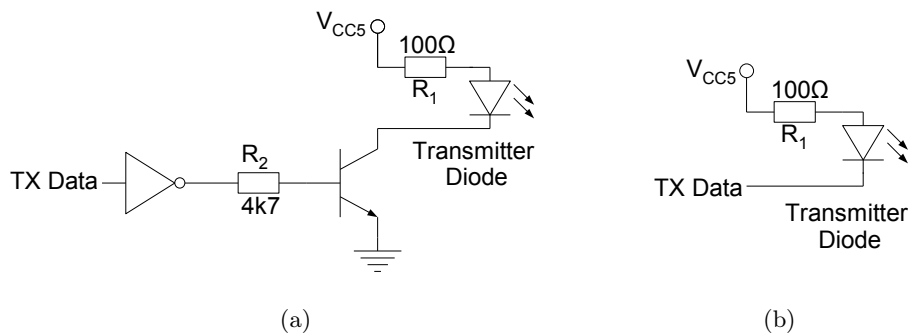
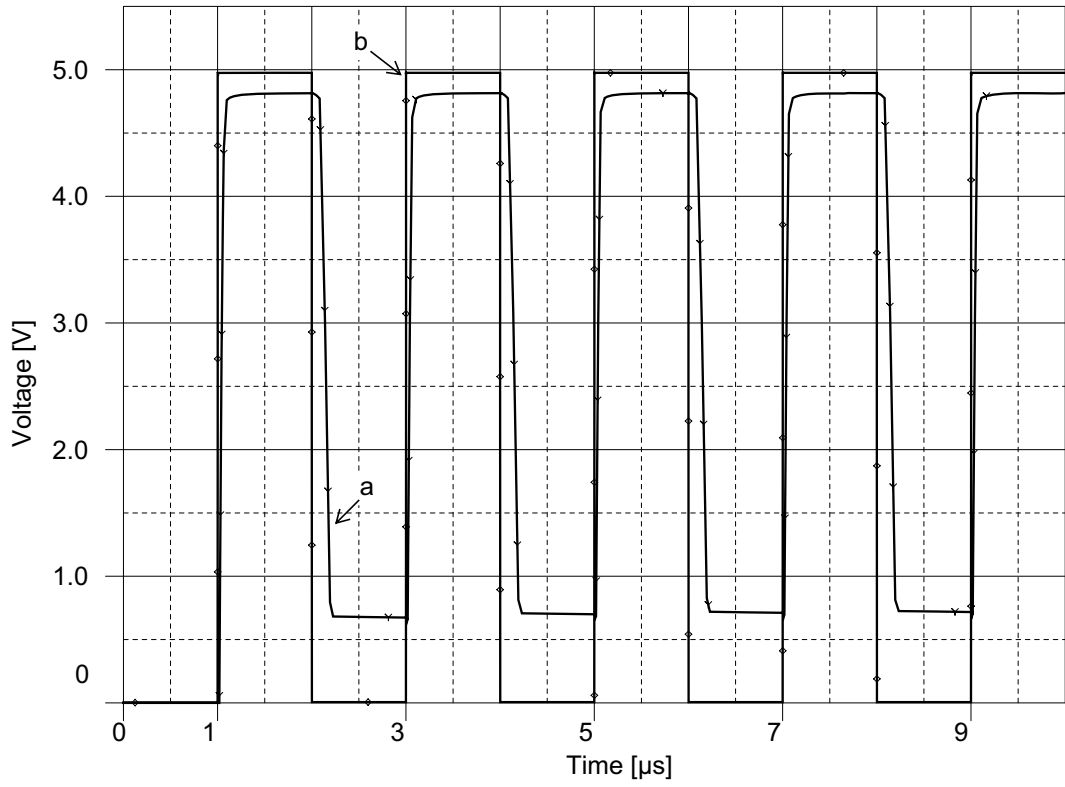


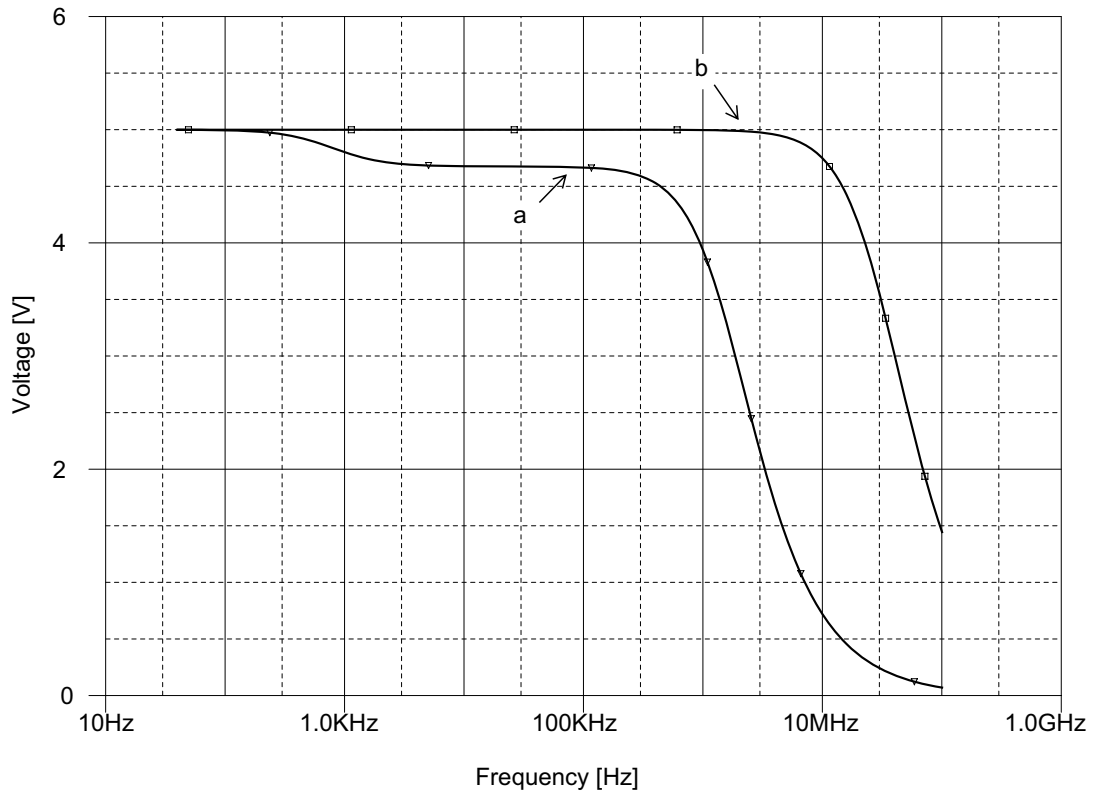
Figure 4.6: (a) The proposed circuit design and (b) the implemented circuit design for modulating the TX signal.

The design in Fig. 4.6(a) works for transmitting data at low baud speeds of up to 250 kbaud. However, when transmitting data above 250 kbaud, data is lost. This can be explained by the combination of the inverter with the transistor that causes the transmission to lag and not switch on the diode with hard edges. A simulation of this design at 1 Mbaud, is shown in Fig. 4.7(a), where the voltage across R_1 and the transmitter diode is measured. It can be seen that the signal is slightly deformed, especially when the signal is a logic low. The perfect square wave is the simulation of the design without the transistor, where the voltage across R_1 and the transmitter diode is also measured. A frequency sweep of the transistor gain is also given in Fig. 4.7(b) where

it has a lower frequency range than the design without the transistor. The design in Fig. 4.6(b) is thus more efficient.



(a) Time domain



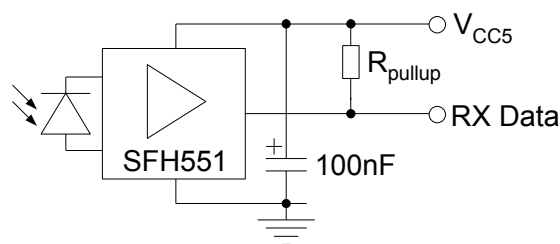
(b) Frequency sweep

Figure 4.7: Simulations of the light modulator signals for the designs shown in Fig. 4.6(a) and (b).

The more basic design, shown in Fig. 4.6(b) was implemented. With this design transfer speeds of up to 1 Mbaud could be attained. It was also designed to only allow a maximum of 40 mA through the diode with $R_1 = 100 \Omega$.

With the USART in idle mode, TX data will be a logic high, causing no voltage drop over the diode so that no light is transmitted. A logic low will cause a voltage drop over the diode and thereby sending a light signal across the fibre optical cable.

On the RX side, the light is demodulated by the SFH551/1-1V photo detector receiver. This device is connected as shown in Fig. 4.8. It has three pins, one for power, one for ground and one for the RX data signal.



(a)

Figure 4.8: The SFH551/1-1V photo detector connection diagram.

When light is received on the photo detector, it will give out a logic low. It is pulled high by the R_{pullup} resistor of $10 \text{ k}\Omega$ when no light signal is detected. Logic data is thus switched between 0 V and 5 V to interface with the USART I/O pins on the microprocessor.

Both the transmitter and receiver are implemented on the USB-USART PCB as well as at the receiving end of the control system.

4.2.3 Summary

Data from the computer is sent through this USB-UART converter and transformed into light signals that travel via fibre optical cables into the cryocooler. The hardware design of the implementation of this converter, as well as the operation of light modulation are documented.

4.3 Implemented D/A and A/D Converters

Different DACs and ADCs were used in the design of this control system. A description follows of which type of converters were used in specific applications and how they were implemented. It starts off by showing a DC stabilization circuit for filtering HF noise on the power supply rails.

4.3.1 DAC and ADC Voltage Rails

For greater stability, a $10\ \mu\text{H}$ SMT inductor is placed on the $5\ \text{V}$ supply voltage of every DAC and ADC as an RF choke. This is then followed by a low pass RC filter as shown in Fig. 4.9. The LPF has a cut-off frequency of $3.15\ \text{kHz}$. This combination blocks out HF noise and will ensure a stable DC power supply.

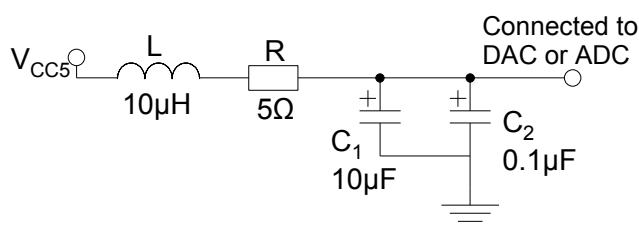


Figure 4.9: DC power filter for each implemented DAC and ADC.

4.3.2 Digital to Analogue Converter

4.3.2.1 DAC8555

The DAC8555 is used to implement a voltage controllable *high current channel*, described in Section 4.7. It is also used to implement voltage controllable *low current and voltage combination channels* in Section 4.8.

This device uses CMOS technology. It is a four channel 16-bit DAC with a SPI interface. It can be preset to start from the zero-scale or mid-scale value on the power-on reset. In Fig. 4.10, the device is configured for use in the *high current channel* design where the $RSTSEL$ pin is connected to GND for a power-on zero-scaled value output on the channels. If $RSTSEL$ is connected to V_{CC5} , as is the case with the *low current and voltage channels*, the device will start on a mid-scale value. The $/RST$ pin can be used for an external reset of the device, but is not used in this design and is therefore permanently connected to V_{CC5} .

Each output channel daughterboard is implemented with one of these DACs. The *high current board* uses two of its channels, while the *low current and voltage daughterboards* use all four of its channels.

The $5\ \text{V}$, inductor filtered, power supply, described in Subsection 4.3.1, is connected to pin AV_{dd} .

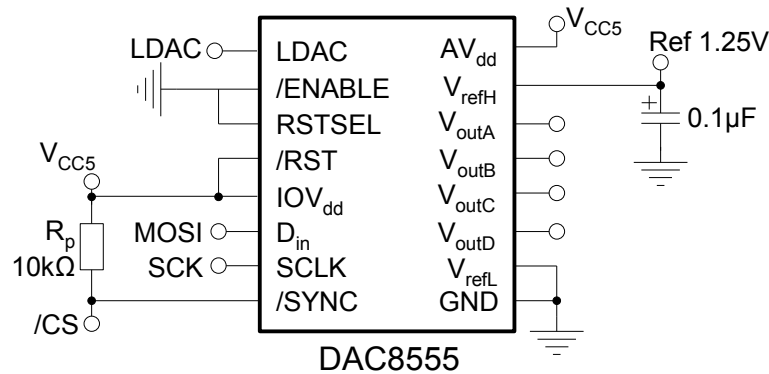


Figure 4.10: The DAC8555 circuit configuration for the *high current channel*.

As no data will be read from this device, *SCLK* and D_{in} are the only pins that are required to connect to the SPI bus.

The */SYNC* pin is used as the */CS* and is pulled high by a 10 k Ω pull-up resistor, R_p .

The ATmega16 microcontroller controls the */CS* lines but its I/O pins are low at startup before the device is properly programmed via the SPI bus. The pull-up resistors then prevent all the SPI interfaced devices from interfering on the SPI bus when the microcontroller is being programmed.

The references on this DAC are configured to scale the output value between 0 V and 1.25 V. However, for the *low current and voltage channels*, the reference is set to 2.5 V.

In order to set the output values, new data values are loaded into the output registers of the device. By sending a rising edge pulse, the LDAC pin can be used to latch all the outputs at once. The LDAC pin on all the DAC8555 devices are connected and controlled by one I/O pin on the microprocessor. If no values for the DAC were updated, the output values stay the same as before the device was latched. This is done to synchronize all the new output voltages on all the different DACs, particularly on the *low current and voltage channels* for sending data to SCE devices.

4.3.3 Analogue to Digital Converters

4.3.3.1 ADS8325

The ADS8325 is used for measurements at the *high sensitivity input channels*, described in Section 4.9 and is also used for sampling the upgraded temperature sensor in Subsection 4.6.4.

This device is a 16-bit micro-power ADC, also made with CMOS technology. It comes in a small 8-pin package with a differential input and a SPI interface. This device is very sensitive to digital noise and should be placed as far as possible from the microprocessor, especially for ground plane connection.

The pin configuration and implementation for this device is shown in Fig. 4.11.

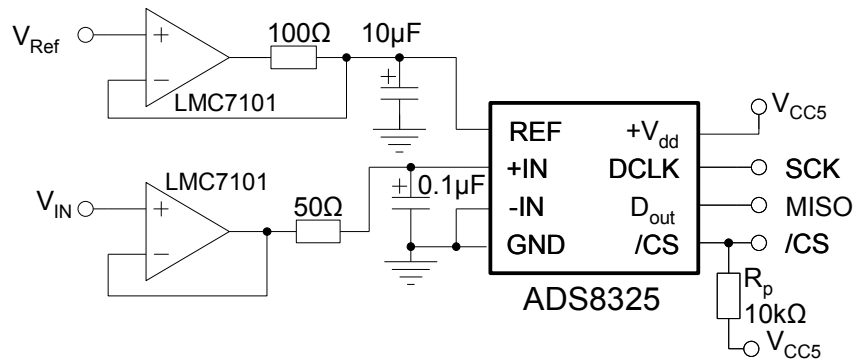


Figure 4.11: The ADS8325 implementation circuit.

The inductor filtered power supply of 5 V is connected to pin +V_{dd}.

SCK and MISO are the only two wires of the SPI bus which are required to connect to the device because no commands need to be sent to it. When /CS is pulled low, the V_{IN} is sampled and the 16-bit data conversion can be extracted via the SPI bus after the 6th clock pulse of SCK. A pull-up resistor, R_p , is also required on the /CS pin.

A 10 μF tantalum capacitor is placed on the REF pin to ensure a stable reference voltage. The device datasheet indicates that if a high output impedance reference source is used, an additional operational amplifier with a current limiting resistor must be placed in cascade with the 10 μF capacitor. This is done as shown in the figure. A reference of 2.5 V at V_{Ref} is used for the temperature sensor, while a reference of 5 V is used when implemented for the *high sensitivity input channels*.

The sampled input voltage, V_{IN} , is buffered with an op-amp and filtered with a low pass RC filter to improve sampling quality.

The -IN pin can only detect values between -0.3 V and +0.5 V and is therefore only used to sense a remote signal ground that may move slightly with respect to the local ground. The -IN pin is therefore connected to GND.

4.3.3.2 MAX186

Another ADC that was implemented is the MAX186. It is used for feedback measurements on the output channels for calibration purposes as well as for measuring the battery voltages and currents.

This is a high quality 12-bit device with 8 sampling channels. It support a dual rail power supply of ±5 V and can therefore sample bipolar signals which makes it ideal for monitoring the bipolar output channels as well as reading the negative voltage rails. This device is software configurable for unipolar or bipolar operation.

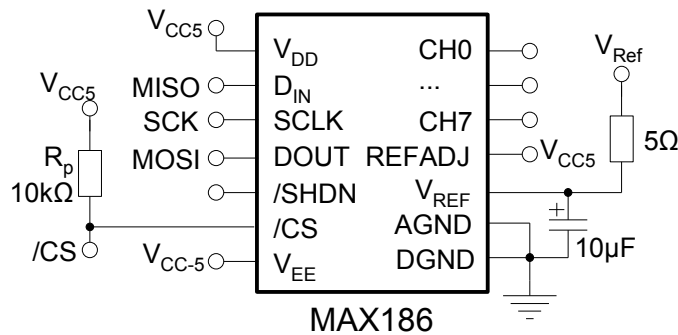


Figure 4.12: The MAX186 configuration circuit.

The inductor filtered positive power supply is connected to V_{DD} and the negative rail is connected to V_{EE} .

The reference is RC filtered for stability with a $10\ \mu\text{F}$ tantalum capacitor and a $5\ \Omega$ series resistor.

Again, a pull-up resistor, R_p , is connected to the $/CS$ pin.

When the $/SHDN$ pin is left floating, the external reference at the V_{REF} pin is used. When $/SHDN$ is pulled high, the internal reference of 4.096 V is used. An external 2.5 V reference at V_{Ref} is used with the *low current and voltage channel feedback*, while the internal reference is used for the sampling of the battery voltages.

The $REFADJ$ pin is the input to a reference buffer amplifier which is not used in this design, therefore it is connected to V_{CC5} to disable it.

In this case the analogue ground is connected to the digital ground because it is implemented on the *low current and voltage channel daughterboard* which has its own ground that is separated from the microcontroller.

4.3.4 Summary

In this section the implementation of a specific DAC and two ADCs were discussed. Some of their main features were also highlighted.

The 16-bit CMOS DAC8555 was chosen to be implemented on the output channels of the control system. It was chosen because it has four output channels implemented in a small package size.

The ADS8325 is a highly sensitive 16-bit CMOS ADC. It was chosen to be implemented on the highly sensitive input channels as well the temperature measurement circuit for accurate measurements.

The MAX186 is another ADC that was implemented in the control system. It is a 12-bit ADC, implemented with 8 input channels. The multiple inputs of this device makes it ideal for

the various feedback voltages that requires sampling, as described in Subsection 4.8.5. It is also used for battery status monitoring.

4.4 Multiplexed Chip Select Lines

The ATmega16 microprocessor does not have enough I/O pins for all the /CS lines to enable all the implemented devices. Therefore the MAX398 multiplexer from MAXIM is utilized for extra /CS lines. The operation of this device is discussed here.

4.4.1 MAX398

A circuit diagram of the implementation of the MAX398 is given in Fig. 4.13.

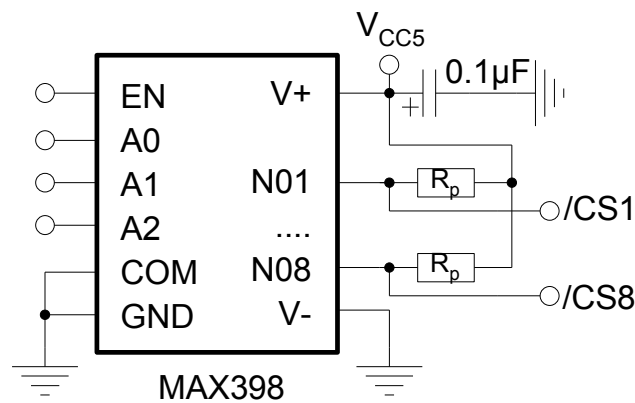


Figure 4.13: Implementation of the MAX398

By using 3 address pins ($A0$, $A1$, $A2$), an input signal at the COM pin can be connected to any of the 8 output channels ($N01..N08$). The outputs are low when the device is not enabled, therefore each output should be pulled high by a pull-up resistor. The address pins are selected, or programmed, before the device is enabled. The device is enabled by pulling the EN pin high, but is disabled when no /CS pins are used.

The input pin, COM , is connected to GND so that when the device is enabled, the specific output pin will be pulled low while all the other pins would still be pulled high by the pull-up resistors. The $V-$ pin is connected to GND and $V+$ is connected to V_{CC5} and sustained with a $0.1\mu\text{F}$ tantalum decoupling capacitor.

When a device needs to be selected with a /CS line, the correct address for that device is programmed to the MUX. It is then enabled where it will pull the correct /CS line low. When the /CS needs to go high again, the MUX is simply shut down and the output pins are pulled high by the pull-up resistors.

4.4.2 Conclusion

The MAX398 multiplexer is operated with four I/O pins by the microprocessor. With 8 output channels, this device then effectively doubles the amount of I/O pins that can be used as /CS lines. Thus, more devices can be addressed on the daughterboards whereby more channels can be implemented for testing SCE devices.

4.5 Microprocessor

The microprocessor runs the entire control system. As mentioned in Chapter 3, the ATmega16 microcontroller was chosen as the control system microprocessor. In this section this device is discussed and its hardware implementation is described in detail.

4.5.1 ATmega16

The ATmega16 microprocessor is part of the ATMEL AVR CMOS RISC family architecture. These devices performed well at low cryogenic temperatures as the results have shown in Sub-section 3.3.3.

The square TQFP package of the microprocessor was implemented in this design. The schematic design which displays the circuit implementation of the microprocessor is shown in Appendix A.1. There it shows how $0.1 \mu\text{F}$ decoupling capacitors are used on the voltage rails.

This device was programmed to operate from its maximum internal RC clock of 8 MHz. It has serial communication abilities, like the USART and SPI channels as well as the in-system programming (ISP) capability for programming the device. The ISP is done via the SPI bus which is connected to a 6-pin header for external programming by means of the STK500 development kit from ATMEL. The use of this development kit as well as the programming for the microprocessor is described in more detail in Section 5.2.

The microprocessor functions as the SPI master device when addressing other devices on the SPI bus. It also has multiple I/O pins to address various external devices. Table 4.1 gives a clear pin connection summary for what each pin on this device was implemented for.

Table 4.1: Pin connections of the ATmega16 microprocessor.

Pin No.	Pin Name	Connection	Function
1	MOSI	ISP header MOSI pin	SPI programming data input
2	MISO	ISP header MISO pin	SPI programming data output
3	SCK	ISP header SCK pin	SPI programming clock
4	/RESET	ISP header /RESET pin	Reset /SS pin for ISP
5,17,38	VCC	5 V supply	Power supply
6,18,28,39	GND	Circuit ground	Device ground
7,8	XTAL1..2	-open-	Internal clock used
9	PD0	RXD	USART RX pin
10	PD1	TXD	USART TX pin
11	PD2	ADG619 IN pin	Temperature sensor enable switch
12	PD3	ADS8325 /CS pin	ADC for temperature reading
13	PD4	IRLML5103 gate pin	Heater enable switch
14	PD5	MAX186(bU1) /CS pin	ADC for battery monitoring
15	PD6	ADG619 IN pin	Output channel protection switch
16	PD7	MAX186(ID-U1) /CS pin	ADC for daughterboard ID
19..22	PC0..3	ADG619 IN pins	V/I Output board 2 channel select
23..26	PC4..7	ADG619 IN pins	V/I Output board 3 channel select
27	AVCC	5 V supply	Analogue power supply
29	AREF	-open-	On-board ADC not used
30..33	PA4..7	ADG619 IN pins	V/I Output board 1 channel select
34	PA0	MAX398 EN pin	Multiplexer(U3) enable
35..37	PA1..3	MAX398 pins A0..A2	Multiplexer(U3) address pins
40	PB0	MAX398 EN pin	Multiplexer(U4) enable
41..43	PB1..3	MAX398 pins A0..A2	Multiplexer(U4) address pins
44	PB4	LDAC	Latch DAC devices

4.5.2 Summary

The implementation of the ATmega16 microprocessor was discussed in this section, where some of its features were highlighted. A full pin connection table for this device also gives the entire pin functionality of the designed system.

The full software implementation for this microprocessor is given in Subsection 5.2.1.

4.6 Temperature Control System

The SCE control system was designed to operate in the first stage of the cryocooler where the temperature reaches approximately 60 K. As the cryocooler is active for long periods of time, this temperature could drop even more. It would be more desirable for the electronics to operate at a fixed temperature of 70 K to eliminate the effects of drifting temperature on electronic devices. A temperature control system is required to regulate a stable temperature. In order to keep the temperatures at a certain preset value, the temperature needs to be measured and a heater control system needs to be implemented.

Therefore a temperature sensor and heater system was integrated with the SCE interface hardware design. This is done to regulate the temperature control system electronics on the motherboard and to keep them from freezing out.

Two temperature sensor circuits were designed and are discussed here. The implementation of the heater design is also shown.

4.6.1 Temperature Sensor

There are different kinds of temperature sensors but few has the ability to measure low cryogenic temperatures. The cryocooler has its own Si diode thermometers to measure temperature to near absolute zero on the cold finger.

In this thesis design, experiments were done with resistor thermometers. Platinum temperature sensors, specifically the PT100 and PT1000 sensors were tested. Their resistance changes with varying temperature. The PT100 sensor has a value of 100 Ω where the PT1000 is 1 000 Ω at 0 $^{\circ}\text{C}$. The resistance of these sensors lower with decreasing temperature and increase with rising temperature. Their values change quite linearly and are usually specified in lookup tables between -200 $^{\circ}\text{C}$ and 800 $^{\circ}\text{C}$ (or between 73 K and 1 073 K).

Only two wires are needed to measure the resistance, but as a small current is pushed through the resistor to measure it, a lead resistance can cause inaccurate measurements. These platinum sensors can therefore be used in two, three or four wire modes. Two temperature designs are discussed in this section where the four wire mode is used in the second design in Subsection 4.6.4.

4.6.2 Design Procedure

An amplification circuit was needed to measure the resistance of the sensors. A bridge circuit design was used to detect the varying PT100 resistance. In Fig. 4.14 the resistors R_1 , R_2 and R_3 forms part of the bridge circuit with the PT100 sensor as the fourth resistor in the bridge.

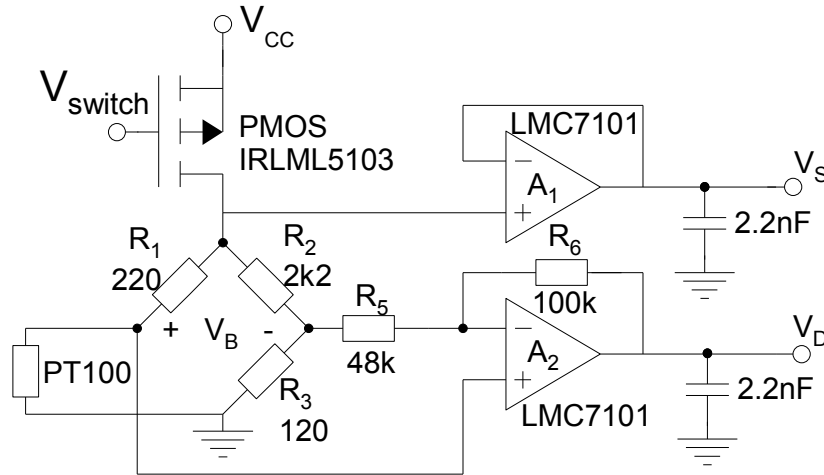


Figure 4.14: PT100 temperature sensor bridge.

A 3.3 V regulated voltage at V_{CC} was used as the supply voltage for the bridge. This supply could be turned on and off by the use of a PMOS transistor. With V_{switch} at a logic low, the transistor is switched on, with only a very small voltage drop of a few millivolts over the transistor. In order to measure the PT100 sensor, current is sent through the resistors. As the resistor values are quite low, the current through them can cause the sensor to heat up and increase the PT100 resistance value. Therefore, to avoid an incorrect temperature measurement, the temperature sensor only needs to be enabled for a short while whilst being measured.

Two voltages were sampled to calculate the value of the PT100 sensor. The first is V_D , which is the amplified voltage difference, V_B , across the bridge circuit. This voltage is only amplified by a factor $A_{A2} = R_6/R_5 = 2.08$, by op-amp A_2 . It is not necessary for any more amplification because of the great resistance variation in the sensor that causes a great voltage difference range with varying temperatures.

Since V_B is directly proportional to the supply voltage, the 3.3 V supply rail is also sampled at V_S . It goes through a voltage follower buffer at A_1 . The difference between these two samples is then used in finding the correct temperature. For these measurements, two 10-bit ADCs on the ATmega16 microcontroller were used. Calibration software was developed to map the 10-bit values against the highly sensitive Si diode sensor of the cryocooler and then store these calibrated values in a lookup table. The temperature could then be measured by using this calibrated lookup table.

With this bridge circuit design and 10-bit ADC, a resolution of 0.3 K per bit could be attained.

4.6.3 PT100 Calibration

The PT100 sensor was placed inside the cryocooler for calibration on the cold finger, next to the Si diode temperature sensor. The designed electronic measuring circuit for the temperature

sensor was placed outside the cryocooler. Two long wires were thus used to connect to the PT100 sensor in two wire mode.

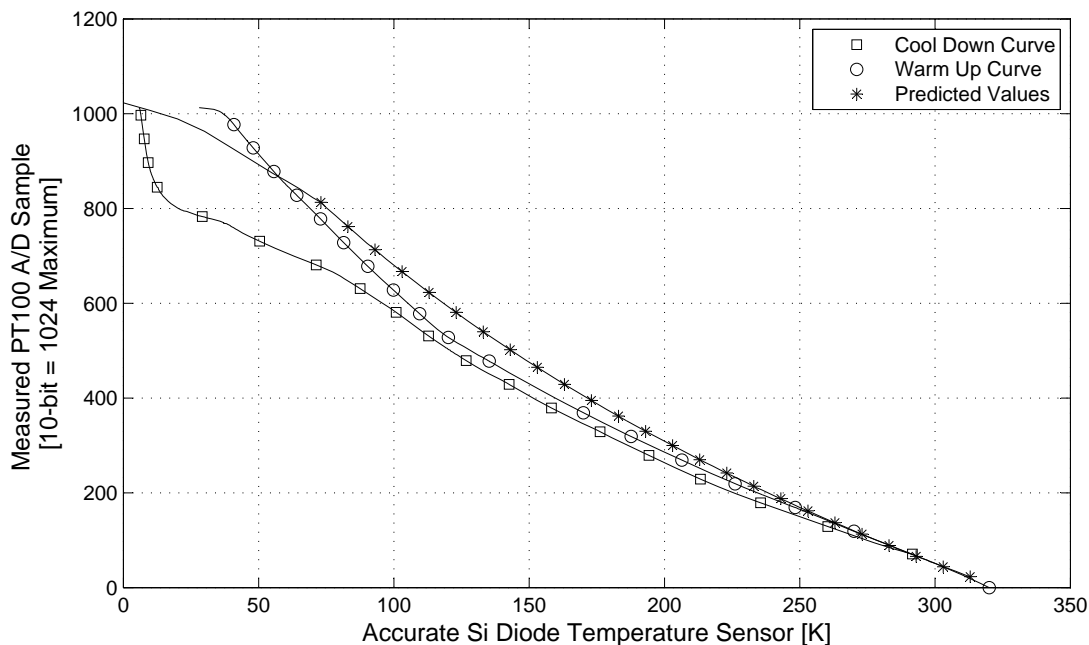


Figure 4.15: PT100 calibration plots.

As the results in Fig. 4.15 shows, the PT100 has two characteristic plots. The first measurement was done while the cryocooler cooled down. As mentioned, this process takes approximately 90 minutes. The second data plot was taken while the cryocooler warmed up naturally over a period of about 8 hours.

These two plots stayed close to each other down to about 73 K, where the cool down curve started showing a large temperature lag. A few factors contribute to this behaviour. Firstly, the PT100 sensor was in a cylindrical stainless steel sheathing tube. Therefore a very small area of the stainless steel tube actually touched the flat metal surface of the cold finger. That caused a temperature lag, as the stainless steel is not a very good conductor of heat at those low temperatures. The temperature of the stainless steel sheathing needed to cool down first before the PT100 sensor could indicate the temperature decrease.

Another factor is the two-wire measuring system, where the same wires are used for sending current as well as measure the voltage of the sensor. The lead wires has their own lead resistance. The lead resistance causes a larger measured voltage drop over the PT100 sensor resulting in a higher than expected temperature measurement.

Although the warm up curve data resembles a more accurate temperature, the temperature lag on the sensor still poses a problem. Therefore a new system was designed using the PT1000 sensor with a four-wire measurement system.

4.6.4 PT1000 Improvements

A new design concept was implemented with a thin film PT1000 sensor. This sensor was ordered without the stainless steel sheathing tube. This would eliminate the stainless steel temperature buffer that caused the lag effect on the the PT100 measurement. The flat thin film sensor can thus be placed directly on the temperature measurement surface.

A constant current source was designed so that when the sensor is measured, the same amount of current would always flow through it. It was also designed to be switched on or off for the same heating problem as the previous sensor although this sensor would not dissipate that much heat as it was designed with less current flowing through it with each measurement.

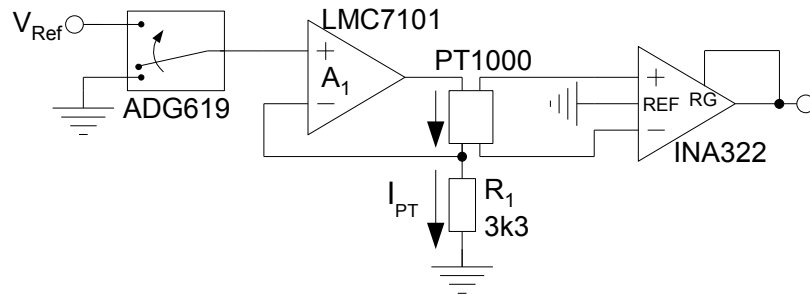


Figure 4.16: PT1000 measurement circuit.

In Fig. 4.16, a 1.25 V reference supply at V_{Ref} was used to measure the PT1000 sensor. It is digitally switched on and off with the ADG619 switch. A more detailed design of this switch is given in Subsection 4.8.2. It was implemented to switch between ground and the 1.25 V reference upon measurement. The op-amp, A_1 , is implemented as a voltage follower. Here the inverting pin on the op-amp will follow the non-inverting pin as closely as possible. That will cause the voltage over R_1 to always be 1.25 V upon measurement, resulting in a predicted current through it of

$$\begin{aligned}
 I_{PT} &= \frac{V_{Ref}}{R_1} & (4.6) \\
 &= \frac{1.25}{3300} \\
 &= 378 \mu A.
 \end{aligned}$$

The current drawn from the op-amp has no other path as to flow through the PT1000 sensor. A predicted constant current will therefore always cause an accurate measurement of the PT1000 sensor.

As shown, the 4-wire mode was implemented, where two separate wires were used to purely measure the voltage drop over the PT1000 sensor without the effect of the extra lead wire resis-

tance. This is measured using the INA322 differential amplifier, set with a default amplification factor of 5.

These components are all CMOS devices as the temperature sensor would eventually be integrated with the control system inside the cryocooler.

The ADS8325, discussed in Subsection 4.3.3, has been used to improve the temperature control design. With 16-bit resolution, this ADC allows for more accurate measurements to be taken. With this configuration, a wide temperature range of 0 K to 350 K can be measured. That gives a theoretically temperature accuracy resolution of 0.005 K per bit measured, which is 60 times finer than with the PT100 sensor design.

4.6.5 PT1000 Calibration

The PT1000 thin film sensor was mounted on the cold finger of the cryocooler while the control system was positioned outside of the cryocooler. Thus, 4 wires were taken into the cryocooler to measure the resistance of the PT1000 sensor as described in Subsection 4.6.4. The measured PT1000 values shown in Fig. 4.17 were calibrated against the accurate Si diode sensor of the cryocooler.

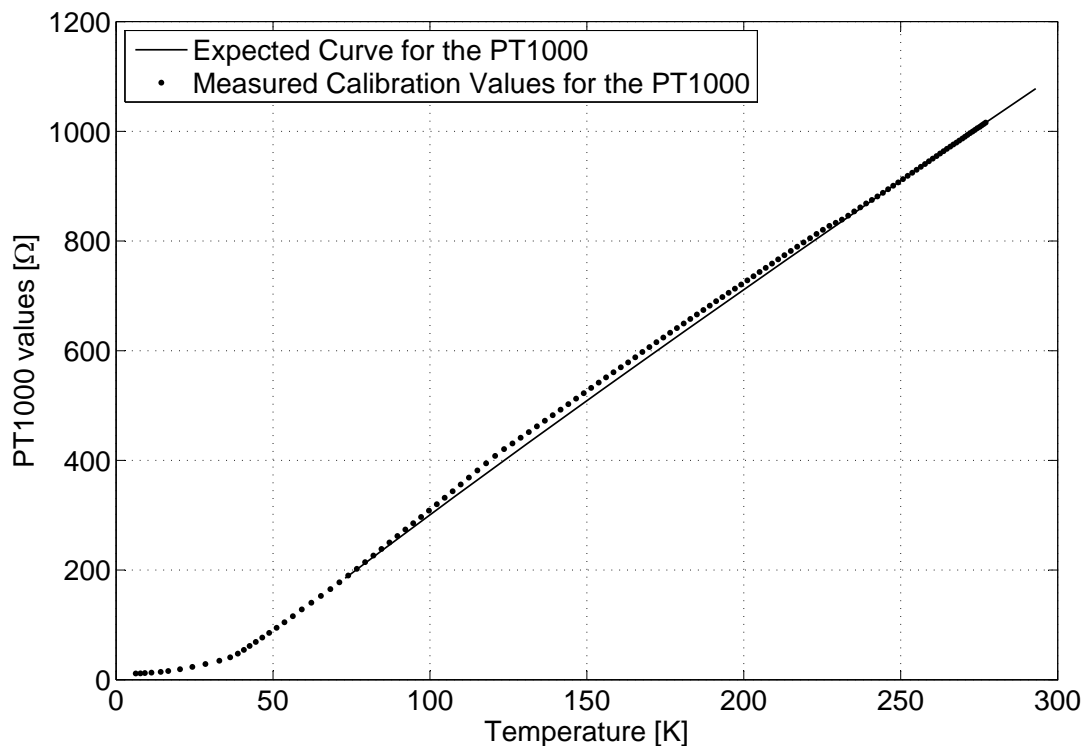


Figure 4.17: PT1000 calibrated values.

The PT1000 stays very close to the expected linear values. At room temperature and at about 75 K, the measured PT1000 values are almost exactly on the expected curve. The lowest expected

value for the PT1000 is only specified to a temperature of 73 K (-200 °C). The measured value of the PT1000 still drops linearly to a temperature of about 40 K. Here the PT1000 temperature sensor shows a non-linear response as it approach 0 K. This PT1000 sensor was calibrated to a temperature of 6 K. These calibrated values for the PT1000 can be found in Appendix D.

4.6.6 Heater Design

This heater system was designed to be automatically switched on or off by the control system software. As the motherboard of the control system would cool down below a specific preset boundary, the heater would be turned on to produce heat to the system ground of the PCB. Since the ground plane is connected to every part of the system design, the heater is mounted onto this plane of the PCB.

As Fig. 4.18 shows, the heater is implemented with a PMOS switch and a high power resistor. The 22 Ω high power resistor has a metal surface to transfer the generated heat to the PCB.

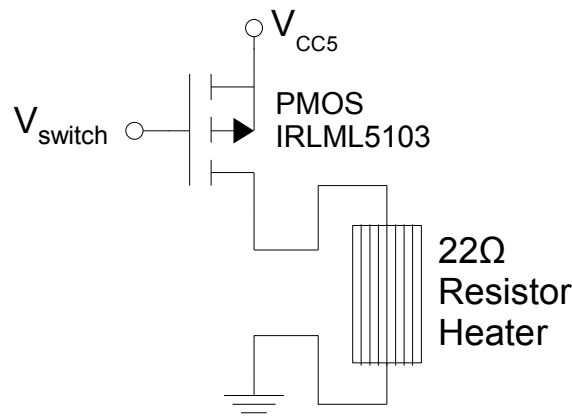


Figure 4.18: The resistor heater implementation.

When V_{switch} is pulled low, the heater system is enabled, where 5 V power is applied across the resistor. With 227 mA of current through it, a total power of 1.14 watt is dissipated by this resistor. The produced heat is transferred to the PCB, thus heating up the control system.

4.6.7 Conclusion

Two designed temperature sensor circuits, as well as the designed heater implementation were discussed.

The PT100 sensor is specified in lookup tables between 73 K (-200 °C) and 1073 K (800 °C). Below this temperature the sensor is less accurate and shows a non-linear behaviour. It is not advised to use it in lower temperatures with the stainless steel sheathing. A platinum sensor without the stainless steel sheathing, with only the thin film front end, is much more accurate.

It is also advised to rather implement the platinum sensor using the three- or four-wire mode to eliminate the lead wire resistance, which has a large effect, especially in cryogenic environments.

In cryogenic environments below 40 K, the platinum sensor has a non-linear response, but with a calibrated lookup table, the sensor would still indicate an accurate measurement.

4.7 High Current Channels

As the control system will be implemented inside the cryocooler extension, the need for a CMOS design is not crucial. Therefore the *high current channel* that was designed was implemented with an NPN-transistor. This design was tested inside the cryocooler at 60 K and worked very well, but for uniformity, a PMOS transistor current channel was also designed and discussed here for future implementations.

Each *high current daughterboard* consists of two *high current channels*. One is a current source and the other a current sink. Each channel is controlled by a 16-bit DAC, as discussed in Subsection 4.3.2. These *high current channels* were designed to source and sink up to 500 mA and are used as DC power supplies for certain SCE devices.

4.7.1 Implemented Design

A design for a voltage controlled current source [28] is shown in Fig. 4.19. It is implemented with a two op-amp feedback system, an NPN-transistor and controlled by a DAC. Dual rail power supply of ± 5 V is implemented for operation.

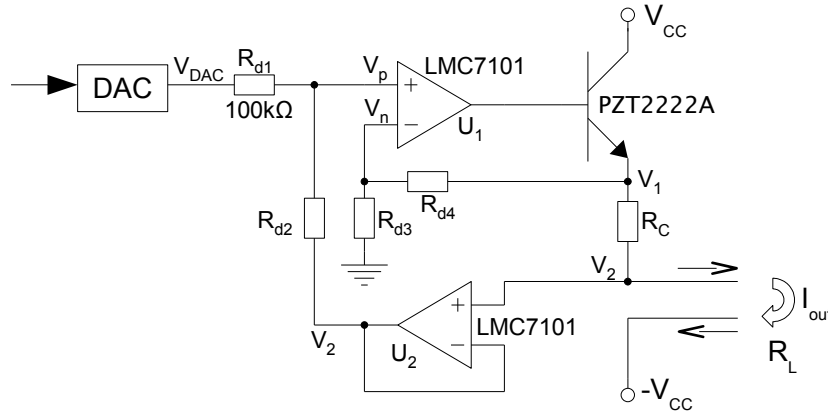


Figure 4.19: The implemented high current source circuit.

The PZT2222A device is a small SMT NPN transistor, allowing for a peak collector current of up to 1 A. The transistor amplifies the base current drawn from the op-amp, U_1 , while the voltage over R_C ,

$$V_{Rc} = V_1 - V_2, \quad (4.7)$$

controls the output current, I_{out} .

All of the R_d resistors are 100 k Ω . At U_1 , the non-inverting input, V_p , is equal to V_n . By resistor voltage division it is found that

$$V_n = \frac{V_1}{2} = V_p. \quad (4.8)$$

Now, the current through R_{d1} is equal to the current through R_{d2} , which results in

$$\frac{V_{DAC} - V_p}{R_{d1}} = \frac{V_p - V_2}{R_{d2}}. \quad (4.9)$$

Eq. 4.9 could be simplified by cancelling out the two equal resistances and by substituting V_p with Eq. 4.8 to produce

$$V_1 = V_{DAC} + V_2. \quad (4.10)$$

Now, Eq. 4.10 can be substituted into Eq. 4.7 and can be rewritten as follow

$$\begin{aligned} V_{Rc} &= (V_{DAC} + V_2) - V_2 \\ &= V_{DAC} \end{aligned} \quad (4.11)$$

Thus the output current can be represented by

$$I_{out} = \frac{V_{Rc}}{R_C} = \frac{V_{DAC}}{R_C}, \quad (4.12)$$

therefore I_{out} is directly controlled by the output voltage of the DAC.

The current sink is implemented exactly as the current source channel, except that the pins on the output of the channel are switched in order to draw current.

In order to dissipate minimal power, R_C is constructed by placing six 10 Ω SMT resistors in parallel. Thus the resistance, R_C , decreases to 1.66 Ω , thereby reducing the power dissipation ($P = VI = RI^2$), and increasing the amount of power it can handle. Six 0.125 mW resistors in parallel can handle power of up to 750 mW. With $R_C = 1.66 \Omega$, the total amount of power dissipation for a maximum of 500 mA, would be 417 mW.

As the PSPICE simulation shows in Fig. 4.20, the current channel can deliver 500 mA with a load resistor, R_L , of up to 14 Ω . If R_L increases, the current will peak at a lower value. However, if R_L decreases, the current channel can produce even more than the maximum desired current of 500 mA.

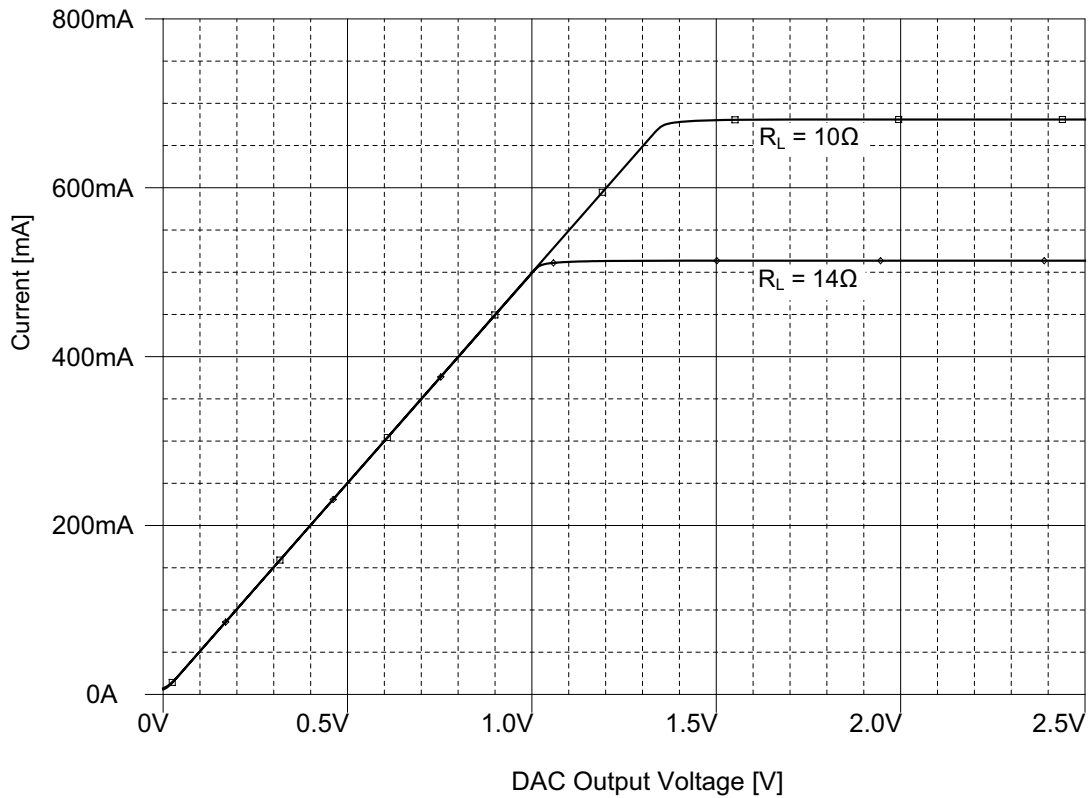


Figure 4.20: Simulation results of the *high current source*.

Each of these channels is voltage controlled by a digitally controllable 16-bit DAC. With the reference of the DAC placed on 1.25 V a maximum of 625 mA can be achieved and can therefore be incremented or decremented in steps of about $10\ \mu\text{A}$. The user interface software will however limit the maximum current output to 500 mA.

Fig. 4.21 displays the measured results of an implemented prototype *high current channel*.

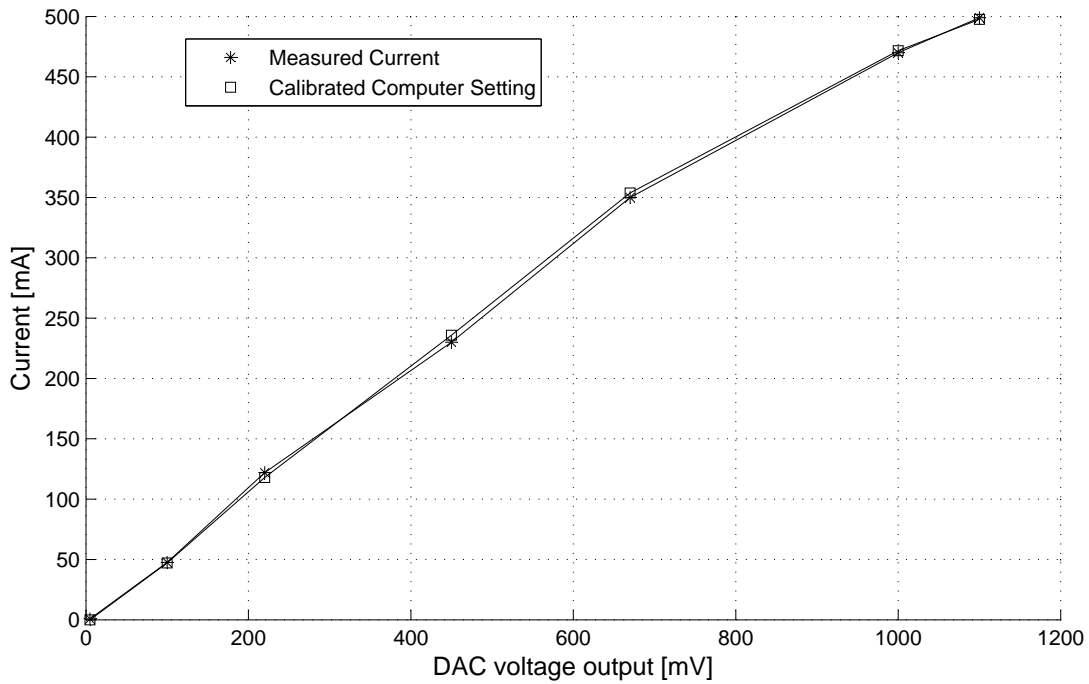


Figure 4.21: Measured results of the *high current channel*.

These measurements were done with a large R_L of $13\ \Omega$. The current source responds quite linearly except at the maximum value where the large R_L starts to slightly suppress the current at 500 mA. The current channel is calibrated in software to produce a maximum of 500 mA.

4.7.2 PMOS Design

The basic circuitry for a PMOS design current source [29] is shown in Fig. 4.22. It relies on a PMOS transistor and an op-amp in conjunction with a DAC. This system produces a current on the output channel that can be varied by means of a voltage adjustable DAC.

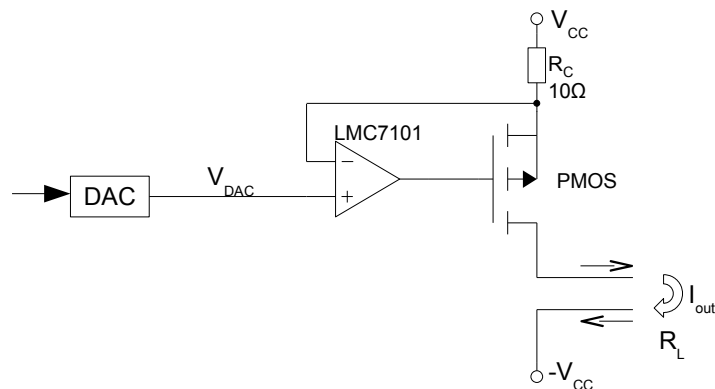


Figure 4.22: High current channel.

In order to reach a maximum output of 500 mA over the full 16-bit DAC spectrum, the V_{CC} and $-V_{CC}$ should be connected to 5 V and -5 V respectively. The op-amp should also be connected to this dual rail and will enable the transistor to operate in its linear region to control the current through it.

The LMC7101 op-amp can be used as a voltage follower in this design. As the DAC voltage, V_{DAC} , decreases from 5 V to 0 V on the non-inverting pin of the op-amp, the voltage of the inverting pin will follow. This will cause an increase in the voltage drop across resistor R_C , whereupon the current through it will also increase. Thus the current through R_C that is equal to the output current, I_{out} , can be calculated by

$$I_{out} = \frac{V_{CC} - V_{DAC}}{R_C}. \quad (4.13)$$

It is designed that $R_C = 10 \Omega$ in order to produce a maximum current of 500 mA when $V_{DAC} = 0$. This is only possible if both the resistor R_C and the PMOS transistor can handle the associated power dissipation ($P = VI = RI^2$). Thus, the power through R_C is $10 \times 0.5^2 = 2.5 W$ and should be considered when choosing a resistor.

The PSPICE simulation results in Fig. 4.23 shows how the current increases to 500 mA as the DAC output voltage decreases to 0 V.

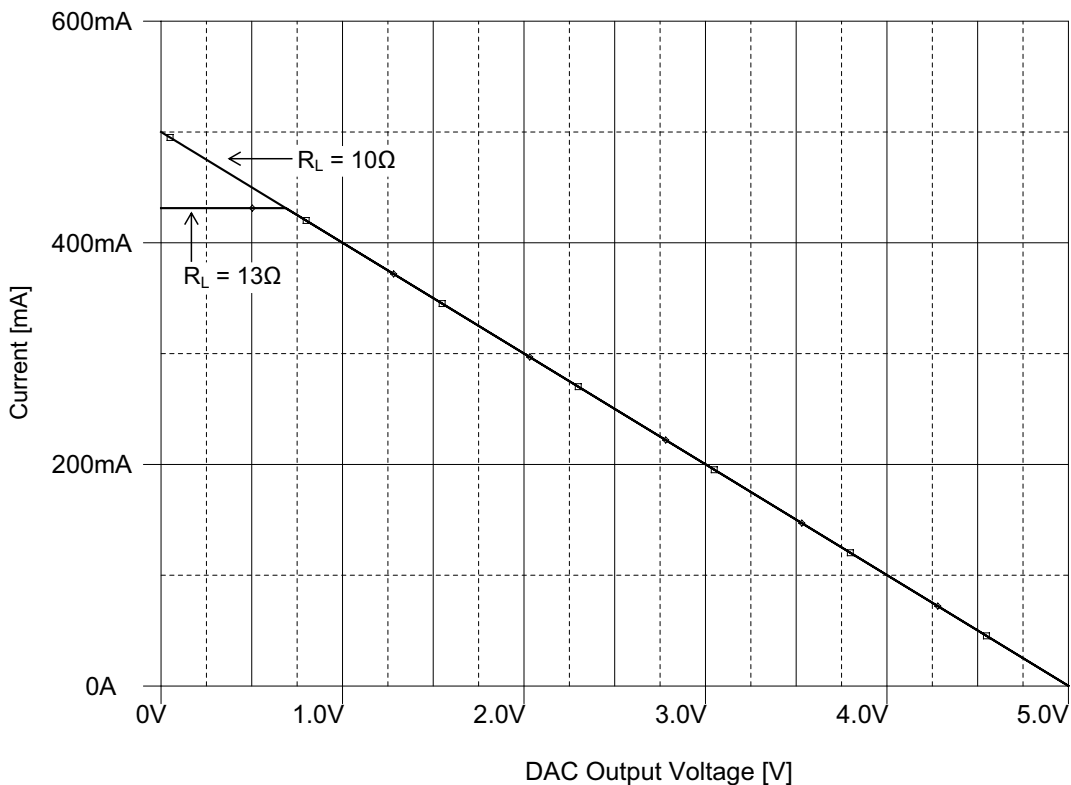


Figure 4.23: Simulation of the PMOS design current channel.

Two load resistors were used in the simulation. This design only allows for a load resistance R_L of up to $10\ \Omega$. If the R_L is bigger than $10\ \Omega$ the maximum deliverable current would be suppressed at a lower value than $500\ \text{mA}$, as seen in Fig. 4.23.

Assuming that the reference of the DAC is equal to V_{CC} , the current could then be adjusted over the full 16-bit range of the DAC. The current could therefore be adjusted in precision steps of $7\ \mu\text{A}$.

A suggestion for this design is to rather use a digital potentiometer instead of a DAC for the voltage control. With a system start-up, the hardware configuration of the DAC only allows it to be set to start from either $0\ \text{V}$ or from a mid-scaled value, thereby creating a current pulse on the output of the current channel.

With a digital potentiometer which is connected between $0\ \text{V}$ and $5\ \text{V}$, the wiper can be set to always start with $0\ \Omega$ on the $5\ \text{V}$ side at startup. That will cause a $5\ \text{V}$ control signal on the channel with no current flowing through the current channel.

4.7.3 Conclusion

In this section, two types of *high current channels* were considered. The NPN-transistor design was implemented for the current channel in the control system. The reason for this choice is that it dissipates less power than the PMOS design because of the current flowing through the control resistor, R_C . The former design can also accommodate a larger load resistance of up to $14\ \Omega$ for the maximum desired current.

On the other hand, the PMOS design can be more finely adjusted with the full range of the DAC. It is also implemented with less components than the NPN-transistor current circuit. Therefore the PMOS design can be considered for future designs.

4.8 Low Current and Voltage Output Channel Combination

This channel was designed to be digitally switched between a current and a voltage source. Fig. 4.24 shows how any one of these channels can be independently switched from the computer, by two switches in unison, to be a current or a voltage source. The channels are voltage controlled by a 16-bit DAC, discussed in Subsection 4.3.2. The DAC is followed by a bipolar conversion block which converts a unipolar signal, ranging between $0\ \text{V}$ and V_{Ref} , to a scaled bipolar signal, ranging between $\pm V_{Ref}$.

Right at the end of the output channel, another switch is implemented. At the system power-up, this switch is connected to ground by default and acts like a safety mechanism that prevents any transient voltage spikes or currents going to the SCE circuits.

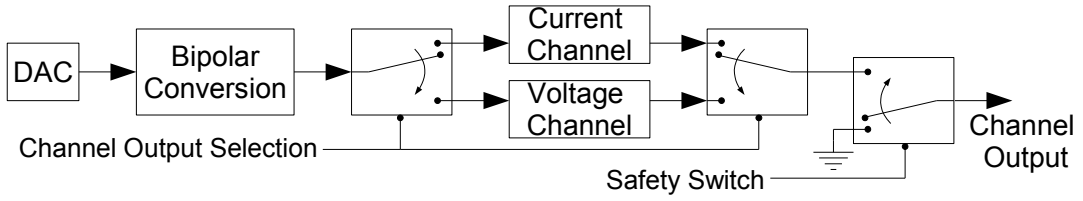


Figure 4.24: Low current and voltage channel combination.

In this section, the bipolar conversion and both the current and voltage channel designs are discussed. It will be followed by a discussion of the hardware implementation of a feedback monitoring system to calibrate these channels.

4.8.1 Bipolar Conversion

The bipolar conversion is done with a simple op-amp circuit, shown in Fig. 4.25.

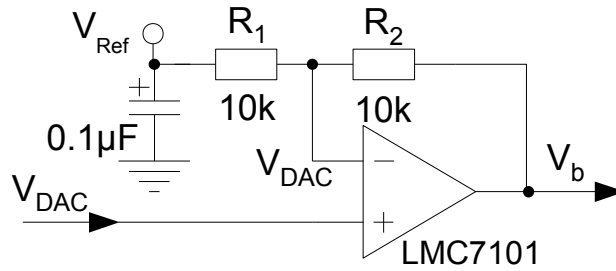


Figure 4.25: The bipolar conversion circuit.

The design is based on the normal inverting amplifier configuration [30], where the amplification is calculated by

$$A_V = -\frac{R_2}{R_1} = -1. \quad (4.14)$$

With V_{Ref} fixed by a 2.5 V reference, this voltage is amplified by a factor of -1 with respect to the non-inverting pin reference of the op-amp. The controlled voltage from the DAC, V_{DAC} , is connected to this reference pin on the op-amp and can be varied between 0 V and 2.5 V. Now, the inverting pin on the op-amp will follow the non-inverting pin, and the current through R_1 is equal to the current flowing through R_2 . The current equation through the resistors can be written as

$$\frac{V_{Ref} - V_{DAC}}{R_1} = \frac{V_{DAC} - V_b}{R_2}. \quad (4.15)$$

The two resistor values are equal, so the equation simplifies to

$$V_b = 2V_{DAC} - 2.5. \quad (4.16)$$

As V_{DAC} varies between 0 V and 2.5 V, the output, V_b , will vary between ± 2.5 V. This is done to enable bipolar signals on the output channels.

4.8.2 Digital Switch

The ADG619 is a single-pole, double throw, CMOS switch. It conducts current in both directions equally well and is bipolar compatible. The voltage rails are therefore connected to ± 5 V, each with a $0.1 \mu\text{F}$ decoupling capacitor, as shown in Fig. 4.26.

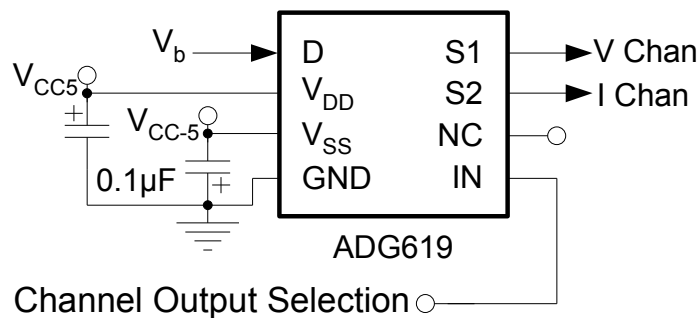


Figure 4.26: The ADG619 switch circuit.

The input signal, V_b , from the bipolar converter, is received at pin D . Depending on the channel output selection on the IN pin, this signal is connected to either the voltage channel, at S_1 , or the current channel at S_2 . With the IN pin on a logic low (low is equal to GND on this device), D is connected to pin S_1 , and with a logic high, D is connected to pin S_2 . The *channel output selection* line is also connected to the second switch in this system as shown in Fig. 4.24 so that both switches are switched in unison.

The series resistance through this device is 4Ω , but could reach a maximum of 6Ω and should be taken into consideration in the design process.

4.8.2.1 Safety Switch

When only the positive power rail is switched on, the negative power rail is 500 mV above the system ground. The inverse is also true, when only the negative power rail is connected to the control system, the positive rail on the op-amps is measured with an offset of -500 mV. This has an implication on the output of these *low current and voltage channels*. An offset of 300 mV is measured on the output when only one of the power supply rails is connected. This is quite large when considered that the *low voltage output channel* was only designed and specified to output a maximum voltage range of ± 65 mV.

Fig. 4.27 shows how this offset is created when a dual rail power supply is powered on.

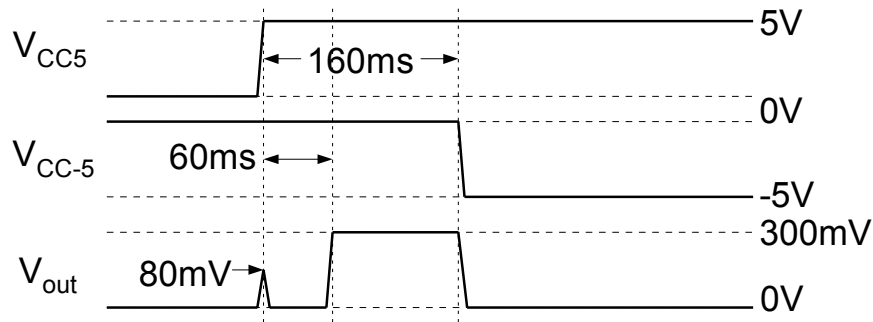


Figure 4.27: Measured offset voltage on output channel with unsynchronized voltage rails.

When the bench power supply was switched on, the negative power rail had a delay of 160 ms before it was turned on. On V_{out} , an 80 mV spike was observed followed by the 300 mV offset. It returned to ground when both power supply rails were switched on.

By installing the safety switch at the end of this output channel, as shown in Fig. 4.24, this offset is eliminated, because the switch is set to ground by default, on a system reset. Only a small 80 mV spike is produced on the output as the rails are switched on. This spike was damped by installing a small 1 nF capacitor at the output of this channel. Note that the voltage spike was only observed on an open circuit. When a load resistance of 50 Ω was connected to the output channel, no voltage spike could be observed.

4.8.3 Low Current Channel

Voltage usually drops over a specific length of wire as a result of the lead resistance. Since the length of the wire, over which the voltage is applied, can usually not be determined beforehand, it is better to implement a current source than a voltage source for SCE inputs. If the load impedance is known and a specific current is sent through it, the exact voltage could be applied over that load impedance. SCE inputs have very low resistances of about 10 Ω . Current loops also have low impedance values, thereby reducing noise sensitivity.

The designed current channel circuit is displayed in Fig. 4.28.

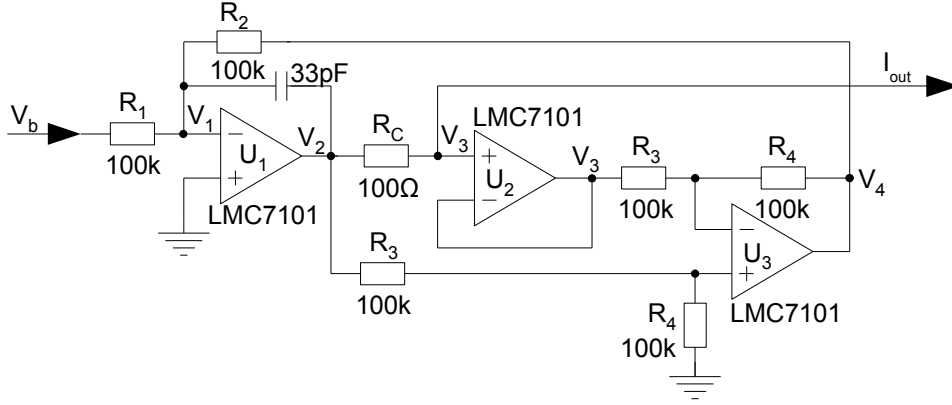


Figure 4.28: Low current channel.

The output current, I_{out} , is calculated by the voltage difference across the current control resistor, R_C , by

$$I_{out} = \frac{V_{Rc}}{R_C}, \quad (4.17)$$

where $V_{Rc} = V_2 - V_3$.

Op-amp U_2 is a normal voltage follower and U_3 is implemented in a difference amplifier design where its output can be calculated by

$$V_4 = (V_2 - V_3) \frac{R_4}{R_3}, \quad (4.18)$$

thus with $R_3 = R_4$, eq. 4.18 could be simplified to

$$V_4 = V_{Rc}. \quad (4.19)$$

Op-amp U_1 is implemented as an inverting amplifier with the feedback resistor at R_2 . Thus, the current passing through R_1 equals the current through R_2 and can be represented by the following equation

$$\frac{V_b - V_1}{R_1} = \frac{V_1 - V_4}{R_2} \quad (4.20)$$

$$= \frac{V_1 - V_{Rc}}{R_2}. \quad (4.21)$$

Here the voltage at V_1 is equal to the ground potential, thus $V_1 = 0 \text{ V}$, and with $R_1 = R_2$, eq. 4.21 can be simplified to

$$V_{Rc} = -V_b \quad (4.22)$$

thus, by substituting eq. 4.22 into eq. 4.17, the output current can be represented by

$$I_{out} = -\frac{V_b}{R_C}. \quad (4.23)$$

When simulating the circuit, using PSPICE, the results in Fig. 4.29 were obtained, with V_b ranging between ± 2.5 V. With the chosen current control resistor, $R_C = 100 \Omega$, the total output current range is designed for an output between ± 25 mA.

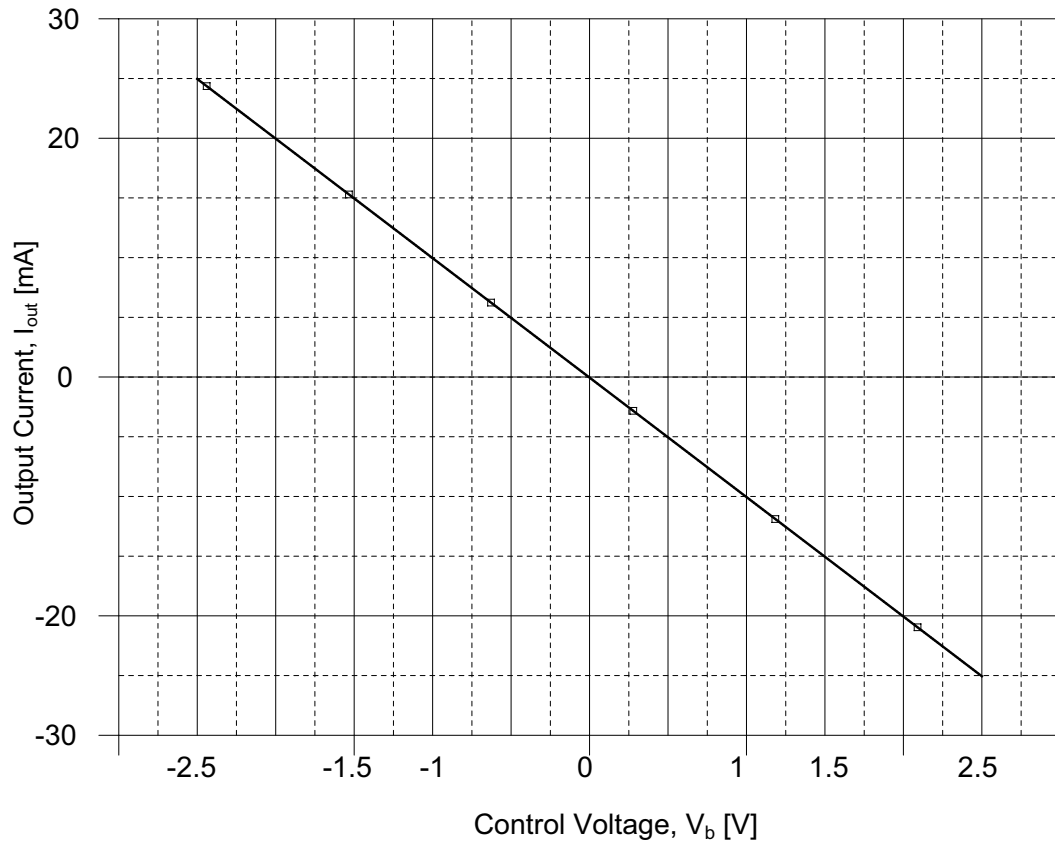


Figure 4.29: Simulation of the output from the *low current channel*.

The output will supply this very linear current for a load resistance of up to 50Ω . Measured results from the implemented *low current output* design are shown in Chapter 6.

With the current ranging between $\pm 25\,000 \mu\text{A}$ and with a 16-bit DAC as the voltage control, the output current can be adjusted in precision steps of $0.8 \mu\text{A}$ per bit.

The 33 pF capacitor in conjunction with the $100 \text{ k}\Omega$ feedback resistor functions as a pas-

sive LPF. The -3 dB cutoff frequency is calculated by

$$\begin{aligned}
 f_c &= \frac{1}{2\pi RC} \\
 &= \frac{1}{2\pi(100 \times 10^3)(33 \times 10^{-12})} \\
 &= 48.2 \text{ kHz}.
 \end{aligned}
 \tag{4.24}$$

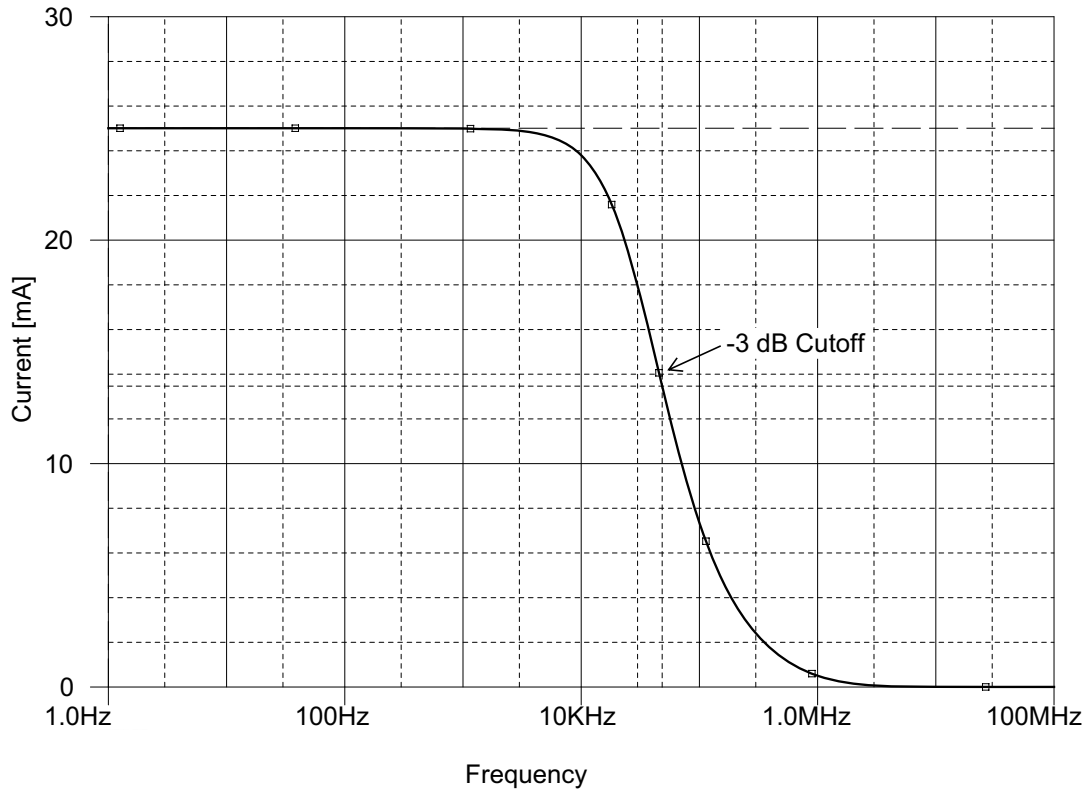


Figure 4.30: AC sweep simulation of the current source with the LPF.

Fig. 4.30 shows the AC sweep simulation of the current source where the cutoff frequency is at 48 kHz. This is designed to filter any high frequency noise that might interfere with the data signals.

4.8.4 Low Voltage Channel

In order to create a small output value in the millivolt range, voltage division is used, and is then buffered by a voltage follower op-amp, as shown in Fig. 4.31.

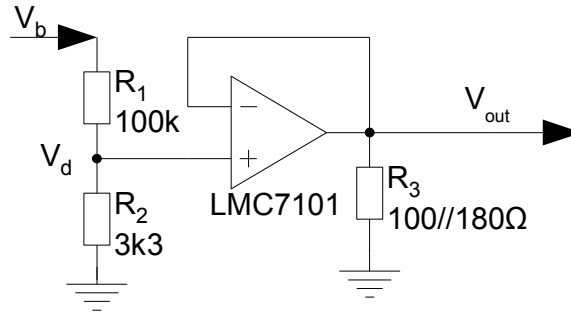


Figure 4.31: Low voltage channel.

This output channel is designed for a load resistance of 50Ω . It must supply the desired voltage to this load, but it has to go through two digital switches of 4Ω each. The resistance of these switches could add up to a maximum of 6Ω each. This will cause a slight voltage drop before it reaches the load. It is therefore designed to produce a larger voltage to compensate for this. For a desired maximum output range of $\pm 65 \text{ mV}$, the output current with a 50Ω load is calculated to be $\pm 1.3 \text{ mA}$. By using this current, the voltage drop over the two series switches at maximum resistance of 6Ω each would then be 15.6 mV . The desired maximum voltage at V_d should then be designed to be $65 + 15.6 = 80.6 \text{ mV}$. With the bipolar control voltage, V_b , varying between $\pm 2.5 \text{ V}$, the voltage division resistors R_1 and R_2 were chosen to be $100 \text{ k}\Omega$ and $3.3 \text{ k}\Omega$ respectively. The division voltage, V_d , is calculated by

$$\begin{aligned}
 V_d &= V_b \left(\frac{R_2}{R_2 + R_1} \right) & (4.25) \\
 &= \pm 2.5 \left(\frac{3.3 \times 10^3}{3.3 \times 10^3 + 100 \times 10^3} \right) \\
 &= \pm 79.86 \text{ mV}.
 \end{aligned}$$

This should be sufficient to produce the desired output, but it might not be exactly 65 mV and therefore a voltage monitoring feedback system is designed to measure exactly what the output voltage is after the safety switch so that the software can be calibrated accordingly. This design is discussed in Subsection 4.8.5.

The switch at the bipolar voltage side would not have any noticeable effect because of the large R_1 and R_2 choice, and can therefore be neglected in the calculations.

As the output voltage amplitude is controlled by a 16-bit DAC, it can therefore be finely adjusted in steps of about $2 \mu\text{V}$ per bit.

This channel was also designed so that the resistance seen from the load side, should be 50Ω . The output impedance of the LMC7101 op-amp is about 100Ω , so two more resistors were placed in parallel with it at R_3 to create a total of 39Ω . When the resistance of the two series switches are added, a total resistance of between 47Ω and 51Ω is seen from the load.

4.8.5 Output Current and Voltage Monitoring

A feedback system has been implemented to monitor the currents and voltages that are actually transmitted to the SCE circuits. This is then used to calibrate the user software according to the maximum and minimum output range per output channel. Any offset on a channel can also be detected and is also calibrated in the software.

The ADC used for these measurements is the MAX186, which is described in Subsection 4.3.3. For this application, the ADC was implemented to have a bipolar voltage input range of ± 1.25 V.

The current is measured by sampling the voltage over R_C , at V_4 in Fig. 4.28 where $V_4 = V_{R_C}$. With the known value of R_C , the current can then be calculated.

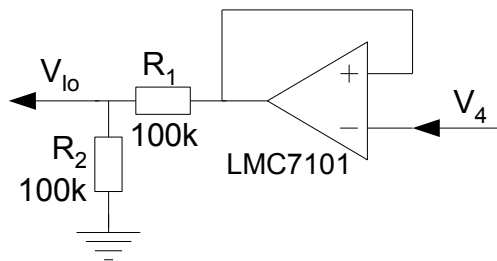


Figure 4.32: Current monitor feedback system.

The voltage at V_4 is buffered by a voltage follower op-amp and then adjusted by voltage division as shown in Fig. 4.32. This is done to scale the V_{R_C} value of ± 2.5 V in order to fit the input range of the ADC.

In order to monitor the voltage channel, the output is measured right at the end of the channel after the safety switch, so that the actual output voltage of the channel is measured. It is measured by the circuit in Fig. 4.33 with the switch connected to R_1 .

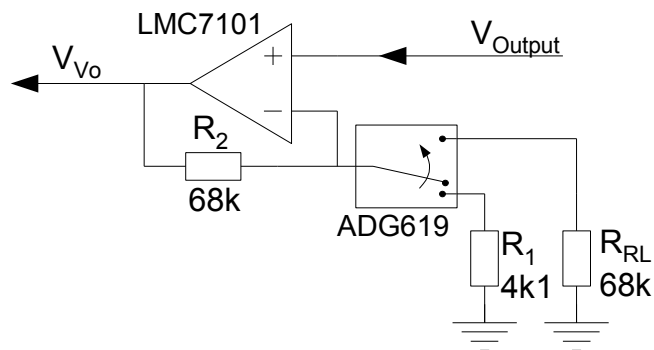


Figure 4.33: Output voltage monitor feedback system.

The maximum bipolar output voltage of about ± 65 mV is amplified by this non-inverting op-amp circuit [30]. The gain is calculated by

$$V_{Vo} = \left(1 + \frac{R_2}{R_1}\right)V_{Output} \quad (4.26)$$

$$= \left(1 + \frac{68}{4.1}\right)V_{Output} \quad (4.27)$$

$$= (17.59)V_{Output}. \quad (4.28)$$

This will adjust the measurement to ± 1.14 V to fit the voltage range of the ADC, with an extra margin left for when the output voltage is a little bit larger than expected. The DAC can then detect an output voltage of up to 71 mV and adjust the software accordingly.

The value of the load resistance can also be sensed by sending a 5 mA signal on the output channel and measuring the feedback voltage across it. In order to do this, the switch in Fig. 4.33 is switched to R_{RL} . This will change the gain calculation to

$$V_{Vo} = \left(1 + \frac{R_2}{R_{RL}}\right)V_{Output} \quad (4.29)$$

$$= \left(1 + \frac{68}{68}\right)V_{Output} \quad (4.30)$$

$$= 2V_{Output}. \quad (4.31)$$

This smaller gain is used because the voltage on the output is much larger when the current channel is enabled. With the maximum DAC read-in value at 1.25 V, and the sense current at 5 mA, a maximum load resistance of 125 Ω can be sensed. However, the maximum load resistance will not exceed 60 Ω . If the maximum value is measured, this will indicate that the measurement has hit the top rail and that there is an open circuit with no load resistance attached to the channel.

This can be used to detect if something is wrong in the cryocooler, for instance if one of the channels to the SCE device is accidentally disconnected, caused by a broken wirebond or bad connection. This will then trigger an alarm in the user software and warn the user.

4.8.6 Summary

A *low current and voltage channel* is designed to interface directly with SCE devices. In this section, a detail design is given of how one such channel is implemented. A safety switch is also designed to protect SCE circuits from initial startup pulses. The interchangeability of the two types of outputs on one channel is also discussed. Other important designs that are shown here are the voltage and current monitoring feedback systems that are used for calibrating the output channels.

4.9 High Sensitivity Voltage Input Channels

The *high sensitivity voltage input channels* are designed to sample and read out data from SCE devices. These signals are disguised in very low voltages and need to be amplified in order to detect them. A precision operational amplifier is used to detect the signals and a 16-bit ADC is utilized to sample these amplified signals and send the data via the SPI bus to the microcontroller. The implementation and operation of the instrumentation amplifier are discussed first, followed by the specific design details of the control system. Noise figures on this channel are also looked at.

4.9.1 Instrumentation Amplifier

The INA322 instrumentation amplifier from Texas Instruments is used to amplify the input signal. This device comes in an 8-pin MSOP package. It is a micro-power CMOS device with bipolar power supply operation that offers very low noise amplification. Its quiescent current is $40 \mu\text{A}$ and when in shutdown mode the device consumes less than $1 \mu\text{A}$ by pulling the shutdown pin low.

The instrumentation amplifier can only support a maximum supply voltage between V_+ and V_- of 7.5 V . Therefore the positive power supply of this device is connected to the 5 V rail with the negative supply connected to the additional -1.25 V regulator, as described in Subsection 4.1.1. This is done so that the INA322 would be able to detect small bipolar signals around 0 V .

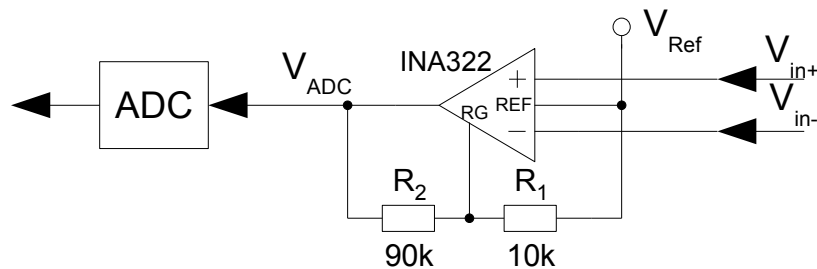


Figure 4.34: Voltage input channel.

This device has differential inputs that amplifies the difference on these inputs with an internal amplification factor of 5. The gain can also be increased by two external resistors, as seen in Fig. 4.34, up to a gain factor of 1000. The gain, G , is set by

$$G = 5 + 5\left(\frac{R_2}{R_1}\right). \quad (4.32)$$

If the internal gain of 5 is required, resistor R_1 should be omitted, leaving an open circuit, while the resistor R_2 should be replaced by a short circuit between the RG pin and the output pin of the device.

The *REF* pin sets the offset of the output by adding the DC voltage of V_{Ref} to the amplified signal. The output that is fed to the ADC is thus represented by

$$V_{ADC} = V_{Ref} + G(V_{in+} - V_{in-}). \quad (4.33)$$

4.9.2 Implementation

In implementing the INA322, the resistors, R_1 and R_2 , were chosen to be 10 k Ω and 90 k Ω respectively in order to establish a gain of 50. The gain was designed to accommodate a bipolar input voltage range of ± 50 mV. This maximum input range will be amplified to ± 2.5 V around the V_{Ref} , which is also set to 2.5 V. This will fill the full ADC reference range which has been set to 5 V.

The ADS8325 is used for the A/D conversions. The specific implementation of this ADC is described in Subsection 4.3.3.

With the 16-bit ADC and with a maximum bipolar input of $\pm 50\,000$ μ V, this channel can detect a voltage variation of 1.5 μ V per bit. According to the data page of the instrumentation amplifier, the expected noise with a DC signal would be 20 μ V_{PP}. The noise would be 500 nV/ \sqrt{Hz} for 10 Hz and 100 nV/ \sqrt{Hz} for 10 kHz. Between these frequencies the noise would thus vary from 1.58 μ V to 10 μ V. This is bigger than the 1.5 μ V sensitivity of the input channel, but by averaging multiple samples, the noise would be reduced. According to the data page of the ADC, the noise can be reduced by $\frac{1}{\sqrt{n}}$ where n is the amount of averages. If an average of 4 samples are taken, the noise would then be reduced to between 0.79 μ V and 5 μ V.

This would increase the accuracy of the sampled data, thus a high sensitivity input channel is created.

4.9.3 Summary

The implementation of the specific *high sensitivity input channel* design is discussed in this section. This channel is used to read in very low voltage signals at various different levels. The amplification stage was discussed whereupon the detail design was given. Some noise figures are also given to show the sensitivity of this input channel.

4.10 Daughterboard Identification System

A daughterboard identification system was designed so that the user can see what boards are connected and ready for use. The design is looked at in this section.

4.10.1 Unique Identification

The daughterboards are detected by a DAC where each daughterboard type has its own unique voltage level identification. The motherboard can automatically identify whether a daughter-

board is plugged into a slot and what type of board it is. Fig. 4.35 shows a simple diagram of how the identification of the different boards is achieved.

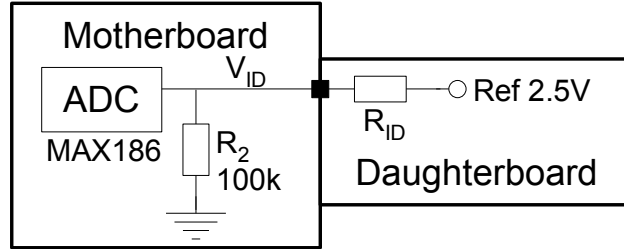


Figure 4.35: Implementation of the daughterboard identification system.

Each daughterboard type has its own identification resistor, R_{ID} , where it is connected to a 2.5 V reference. The other end of the resistor is connected to the edge of the daughterboard where it will connect with the motherboard. A fixed resistor, R_2 , on the motherboard will be connected to the daughterboard identification resistor, forming a voltage division network that will be sampled by the MAX186 ADC. The ID voltages are then calculated by

$$V_{ID} = 2.5 \left(\frac{R_2}{R_2 + R_{ID}} \right). \quad (4.34)$$

Table 4.2 shows the different R_{ID} values and their equivalent ID voltages that is used for identifying the daughterboards.

Table 4.2: Daughterboard identification table.

Daughterboard Type	$R_{ID}[\text{k}\Omega]$	$V_{ID}[\text{V}]$
High Current	short	2.5
Low Current and Voltage	100	1.25
High Sensitive Input	56	1.6
No Board	open	0

With the *high current board*, the connection is short circuited to the 2.5 V reference and when no board is connected, the input to the ADC will be pulled low by R_2 causing a 0 V input.

4.10.2 Conclusion

A design was given of a daughterboard identification system. The detail is given of how to sense these boards.

This daughterboard ID feature makes it easier to utilize the control system, as the user interface software will detect the the daughterboards automatically.

4.11 Conclusion

In this chapter, every aspect of each designed sub-block is discussed in great detail.

This chapter starts with all the necessary power circuitry to supply the control system with the right power levels. It includes voltage regulation as well as battery monitoring circuitry.

This is followed by the description of how the USB-USART was implemented for data transfers with the special fibre optical extension design.

Various implemented SMT devices are discussed, including the microprocessor implementation which functions as the system CPU.

A temperature control design follows, where the necessity of such a subsystem is discussed.

A detail design of the various output and input channels is discussed to give the user an in depth understanding of the operation of these channels.

This chapter concludes with a design discussion of the daughterboard identification system in order to automatically identify a plugged-in daughterboard.

Chapter 5

System Implementation

All the different subsystems of the *cryogenic CMOS-based control system* have been designed and tested. Every part now needs to be integrated into one whole system.

In this chapter hardware and software overviews are given. It starts with the hardware implementation of how the subsystems fit together and how the different hardware blocks are connected to each other.

Furthermore, a design for the control system software is given. It shows how the software was created in order to operate the control system. This includes the hardware programming of the motherboard microprocessor with a description of the designed protocol for data transfers. This chapter ends with the implementation of the graphical user interface.

5.1 Hardware Implementation

This section starts with a discussion of fibre optical feedthroughs and the necessary connections to the cryocooler. An overview is then given of how the control system fits together. This is followed by a detailed discussion of which connectors were utilized in this design. It then concludes with the structural integration of how the motherboard and daughterboards were implemented and how they connect to each other.

5.1.1 Fibre Optical Connections and Overview

One proposal was to allow fibre optical cable for data transfer into the cryocooler in order to limit heat transference from the outside and to isolate the control system from any external electrical noise that could couple with the data wires. Currently, the cryocooler has no optical fibre feedthroughs. It is only equipped with a 10-pin aviation standard Souriau connector for electrical connections entering the cryocooler.

Research was done to find vacuum-tight fibre optical feedthroughs for data transfers. Such a feedthrough, shown in Fig. 5.1(a), was found at Oxford Electronics Ltd. who specializes in

vacuum fibres and feedthroughs. They supply options of connecting the fibre optical cable with either an SMA connectors or with a straight ferrule connector, as seen in Fig. 5.1(b).

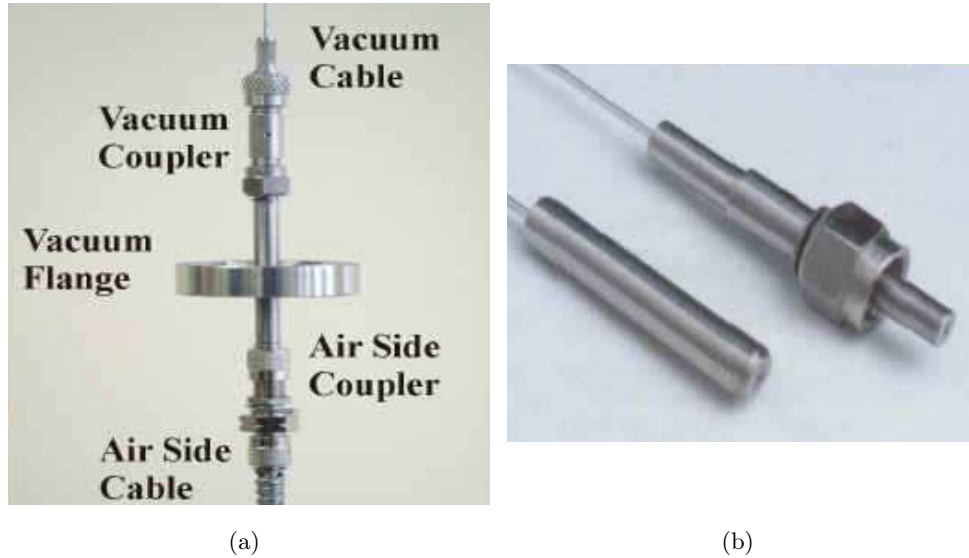


Figure 5.1: (a) Fibre optical vacuum feedthrough with (b) the SMA and straight ferrule connector options.

The fibre optical feedthrough is weldable into a variety of standard flanges. It also allows disconnection at either side of the vacuum chamber. The fibres are metal coated and are thus epoxy free to prevent outgassing of the cables in the cryocooler.

A quote on these feedthroughs and specially mounted fibre optical cables are specified in Table 5.1

Table 5.1: Oxford Electronics price quote for fibre optical accessories.

Type	Description	Length [m]	Price [£]
CF16VF600	Vacuum feedthrough on CF16 flange	n/a	304.00
VC600IR-100-SMA	Vacuum fibre optical SMA cable	0.1	212.00
EC1000-1 IR	External fibre optical cable	1	159.60
EC1000-5 IR	External fibre optical cable	5	366.00
EC1000-10 IR	External fibre optical cable	10	624.00

This feedthrough system is quite expensive, especially if two feedthroughs are needed, one for the TX and one for the RX line. It was decided not to implement this fibre optical feedthrough system, since the extension chamber of the cryocooler, in which the control system is positioned, does not reach cryogenic temperature levels. Thus, the temperature transference through cabling was not relevant anymore, however effective shielding was still a priority. Therefore the VPSTP,

a specially shielded cable from SAMTEC [31], was used to connect from the power box to the cryocooler. This cable is described in Subsection 5.1.2.

A broad overview of the final implemented system is given by Fig. 5.2.

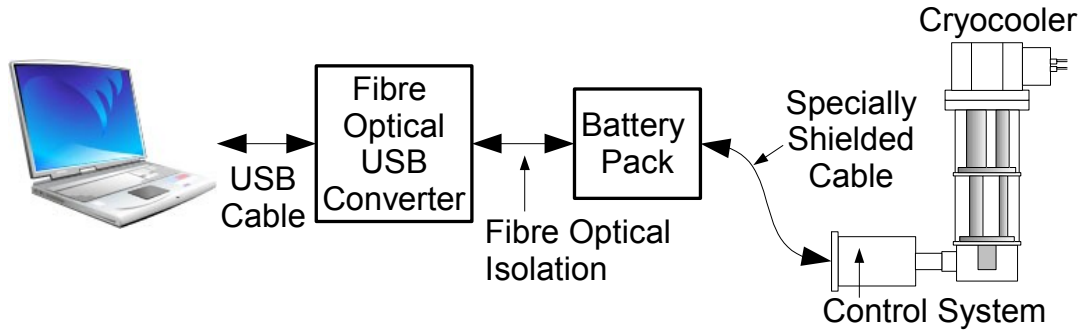


Figure 5.2: Hardware connection overview diagram.

The detail of the first part of the diagram, up to the fibre optical converter, was already discussed in Subsection 4.2. From here the data is transferred through the fibre optical cables to the shielded battery pack where it is demodulated. The fibre optical cables electrically isolate the control system from the outside. From here it uses its own battery power source. The data, as well as the necessary power are transferred through the specially shielded cable to the control system, which is inside the extension chamber of the cryocooler.

5.1.2 Outside Connections

An aluminium box was designed to contain the batteries for the power supply of the control system. The detail of the designed aluminium boxes are given in Appendix B. An accompanying PCB was also designed to fit inside this power box. It contains the ± 5 V regulators as well as the voltage and current measuring circuits, described in Subsection 4.1. This box has a double pole, double throw, external switch for switching both power rails at the same time. If one power rail is switched before the other, the dual rail op-amps would produce a voltage offset on the output channels, which could be large enough to damage some SCE devices. This effect is described in Subsection 4.8.2 where digitally controlled safety switches were implemented to avoid this problem.

Fig. 5.3 shows the implemented power box with the inputs and outputs.



Figure 5.3: Aluminium power box for the batteries.

On the left, the fibre optical cables can be seen where the USART signals are received from the computer and demodulated to normal electrical signals, as described in Subsection 4.2.2. At the top right corner, the connected VPSTP shielded cable from SAMTEC can be seen. This cable carries the electrical RX and TX signals into the cryocooler.

This VPSTP cable has exceptionally good shielding. It is specified to allow data transfers at rates of up to 1 GHz. As seen in the magnified insert in Fig. 5.4, the wires in this cable are all grouped in pairs, with each pair having its own grounded shielding. The VPSTP cable and its appropriate VRDPC mate connector can also be seen in Fig. 5.4.

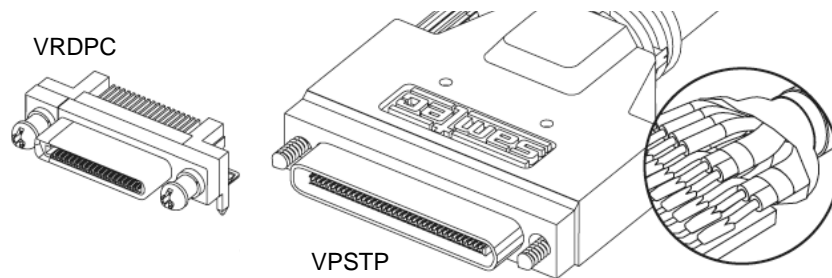


Figure 5.4: The shielded VPSTP cable with its accompanying VRDPC connector from SAMTEC.

A VPSTP cable with 8 twisted pair wires was used. All 8 of these twisted pair wires are utilized. One of each of the twisted pair wires are connected to ground. Table 5.2 summarizes what the 8 remaining wires are utilized for.

Table 5.2: VPSTP shielded cable wire usage.

Name	Function
TX	USART transmit data line
RX	USART receive data line
V_{CC6}	6 V battery potential
V_{CC-6}	-6 V battery potential
V_{CC5}	Regulated 5 V power rail
V_{CC-5}	Regulated -5 V power rail
V_{I+}	Measured current usage from 6 V battery
V_{I-}	Measured current usage from -6 V battery

The battery potentials and the measured current usage are sampled inside the cryocooler by the MAX186 on the motherboard, as described in Subsection 4.3.3.

5.1.3 Mechanics

5.1.3.1 Edge Connectors

The MEC1 edge connectors from SAMTEC was selected for connecting the daughterboards to the motherboard. It is a mini edge-card socket especially suited for daughterboard extensions.

The contacts on the MEC1 are made of beryllium copper (BeCu). BeCu is a copper alloy containing up to 2.7% beryllium which strengthens the material. BeCu is one of the strongest copper alloys available. There are two main types of beryllium copper alloys in use. They are known as the *high strength* and *high conductivity* alloys. The high conductivity alloys contain a beryllium concentration that varies between 0.2% and 0.7%. The strength of the alloys increase as the beryllium content increases. By combining the strength and conductivity features, these alloys make good electronic connectors and spring contacts. They also do not become brittle in cryogenic temperatures [32], thus maintaining their strength and flexibility at low temperatures.

For this design, an 8-position MEC1 connector, polarized at position 3, as seen in Fig. 5.5, was used. This leaves 7 positions that has a connector at each side. Thus, with edge connectors on both sides of the slot-in PCB, a total of 14 connections can be made through this connector. The polarized feature prevents the user from inserting the daughterboard in the wrong way.

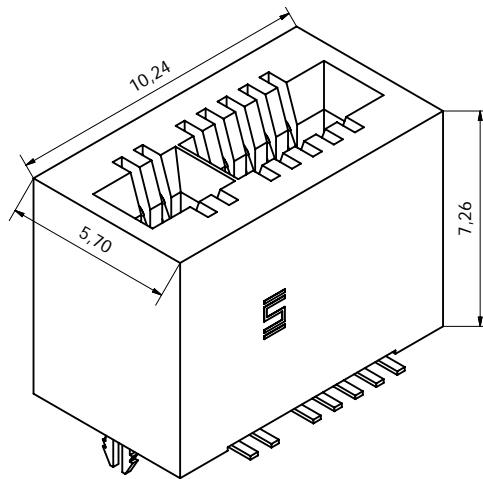


Figure 5.5: The MEC1 connector (Dimensions in mm).

With the surface mount MEC1 on the motherboard, the daughterboards are plugged in at 90 degree angles.

The MEC1 edge connectors are designed to mate with a PCB that has a thickness of between 1.55 mm and 1.60 mm.

5.1.3.2 PCB Construction

For the final PCB design of the control system, the motherboard with all the daughterboards were designed to be manufactured with a 4-layer process. All the layout diagrams of the PCBs were done in Protel DXP and are given in Appendix A.2.

The PCB layout was done on a 4-layer PCB. Fig. 5.6 shows the side view of the construction of a 4-layer PCB.

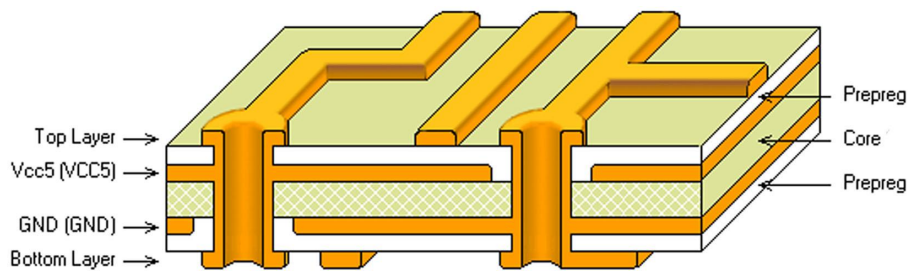


Figure 5.6: Side view of a 4-layer PCB constructed at TraX.

The core is made of the FR4 material on which the rest of the board is constructed. The V_{CC5} and GND layers are the two power planes that were etched onto the core. Both sides of the board were covered with prepreg isolation whereupon the top and bottom layer tracks

were etched onto. The manufactured boards were ordered in a 1.55 mm thickness so that the daughterboards would fit into the MEC1 connectors, described in the previous subsection.

As a limitation, set by TraX Interconnect [33] where the designed PCBs were manufactured, only *through hole vias* as opposed to *blind vias* were allowed in the design. *Through hole vias* go through all the layers of the PCB as seen in Fig. 5.6, where *blind vias* only connect 2 layers at a time.

Care was taken in designing the PCBs [34, 35] with adequate track widths. This was done to accommodate for the required current of up to 500 mA per *high current channel*. The cross-sectional area, A , of the track, measured in mils² is calculated by

$$\text{Internal Tracks : } I = 0.015 \times dT^{0.5453} \times A^{0.7349} \quad (5.1)$$

$$\text{External Tracks : } I = 0.0647 \times dT^{0.4281} \times A^{0.6732}, \quad (5.2)$$

where I is the maximum current in Ampère and dT is the temperature rise above ambient in °C.

After solder masks were placed on the boards, they were finished off with immersion gold. This is more correctly called Electroless Nickel/Immersion Gold (ENIG). Only the exposed contacts and vias were covered with this process. This is a solderable finish for SMT devices. It was done to help protect sliding edge connectors against wear. The gold covering also prevent oxidation on the edge connectors that effectively ensures better connectivity to the motherboard.

5.1.4 Motherboard Construction

The motherboard was manufactured at TraX Interconnect, as described in Subsection 5.1.3.2.

The implemented connectors on the motherboard are discussed here and followed by an overview of the motherboard layout.

5.1.4.1 Connectors

A few connectors on the motherboard are required for communicating with external devices. A list of 3 types of ports that are implemented on the motherboard, are described here and displayed in Fig. 5.7. They are:

- A normal 6-pin header: The motherboard contains a 2-row, 6-pin ISP header for programming the ATmega16. This is a normal header connection as the device will only be programmed in room temperature conditions. It can be seen at the bottom of Fig. 5.7.
- A 10-pin micro mate header: This is a TFM micro mate header from SAMTEC and can be seen at the left bottom of Fig. 5.7. It is used for the incoming data from the battery pack, as listed in Table 5.2. This header mates with a 10-wire SFSD cable socket, also from SAMTEC. The contact material implemented in this socket is also made of the BeCu alloy to ensure a good connection in cryogenic environments. The wires at the other end of this cable is soldered to the aviation standard Souriau connector at the flange of the cryocooler.

- Nine MEC1 connectors: Three of these connectors are utilized for input daughterboards as seen at the right bottom of Fig. 5.7. Two MEC1 connectors are implemented for each output board. This would enable the motherboard to connect a total of three output daughterboards. There are two types of output daughterboards and they are interchangeable on the same connectors, since the control system will automatically recognize the type of output boards.

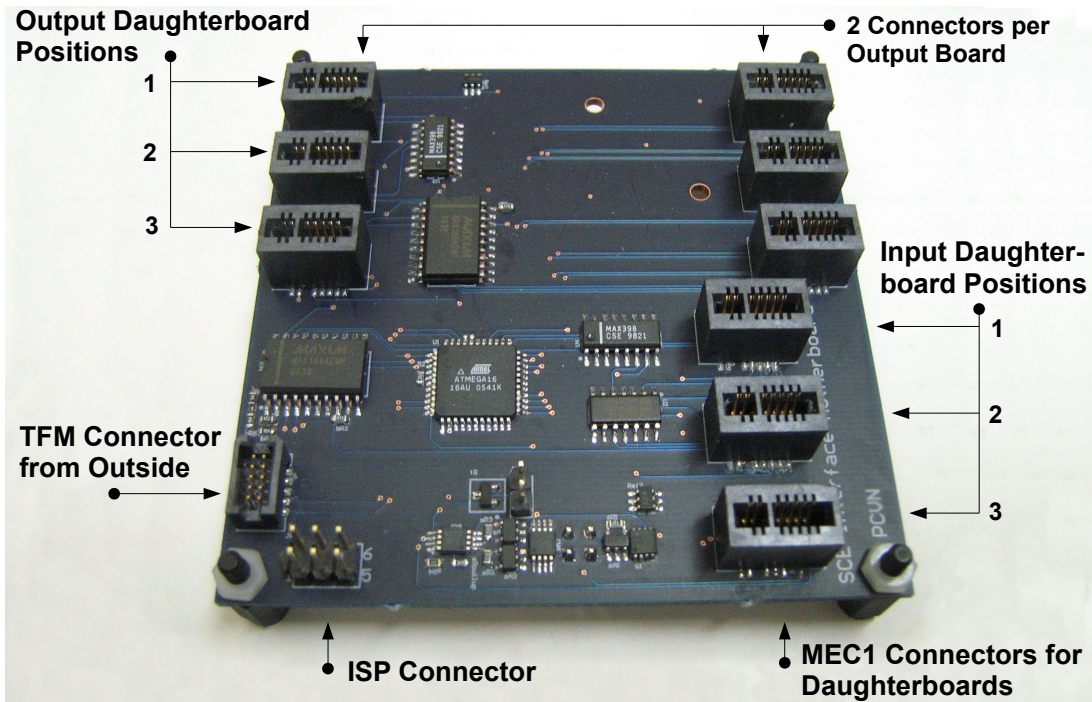


Figure 5.7: Motherboard with the indicated connectors.

5.1.4.2 Device Coordination

The heater is fastened underneath the motherboard with two small M3 screws and nuts. Thermal paste, inserted between the motherboard and heater, ensures thermal conductivity to the control system PCB. The PT1000 temperature sensor is also mounted underneath the motherboard to measure its own temperature.

This board contains the ATmega16 microprocessor, two MAX186 ADCs, one for battery monitoring and one for the daughterboard ID system. It also implements the two multiplexers for the /CS expansion system, described in Section 4.4. The two voltage reference devices, described in Section 4.1.2 are also implemented on the motherboard.

5.1.5 Daughterboard Constructions

These boards were also manufactured at TraX Interconnect and were constructed as described in Subsection 5.1.3.2.

The *high current boards* and the *low current and voltage boards* are the two types of output daughterboards. They have the same edge connector layouts and can plug into the same MEC1 sockets on the motherboard. Each output daughterboard uses two MEC1 connectors, one at each side of the board, while the input daughterboard only uses one MEC1 connector.

5.1.5.1 High Current Boards

The *high current board* has two output channels as described in Section 4.7. The implemented board layout is shown in Fig. 5.8 with the high current source, HC+, at the top and the high current sink, HC-, at the bottom.

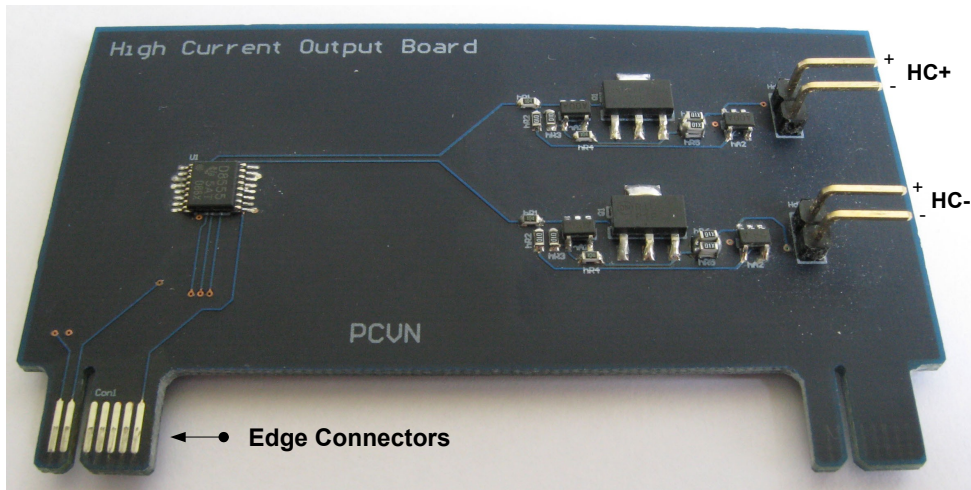


Figure 5.8: High current daughterboard with two channels.

Since there are only two channels to control, this board needs less control wires. Only the left edge connector is implemented for connection to the motherboard. The electrical connection layout to the edge connector is given in the schematics in Appendix A.1. The two edge slide-in connectors are placed far from each other to support the board for greater physical stability when inserted into the motherboard.

Channel input and output connections for all the daughterboards are implemented with 90 degree angled header pins. In order to ensure connectivity in cryogenic environments, twisted pair wires with BeCu female crimp terminals could be used to connect the channels to the SCE devices.

5.1.5.2 Low Current and Voltage Boards

Each *low current and voltage board* has four output channels, as shown in Fig. 5.9. The polarity of each channel is also given, with the positive terminal at the top of each channel. The hardware programming for the microcontroller was done to implement channel 1 at the bottom and channel 4 at the top of the board. The control system was designed to be very adaptable. If the sequence of the channel numbering needs to be changed, it can be done by reprogramming the ATmega16 microcontroller.

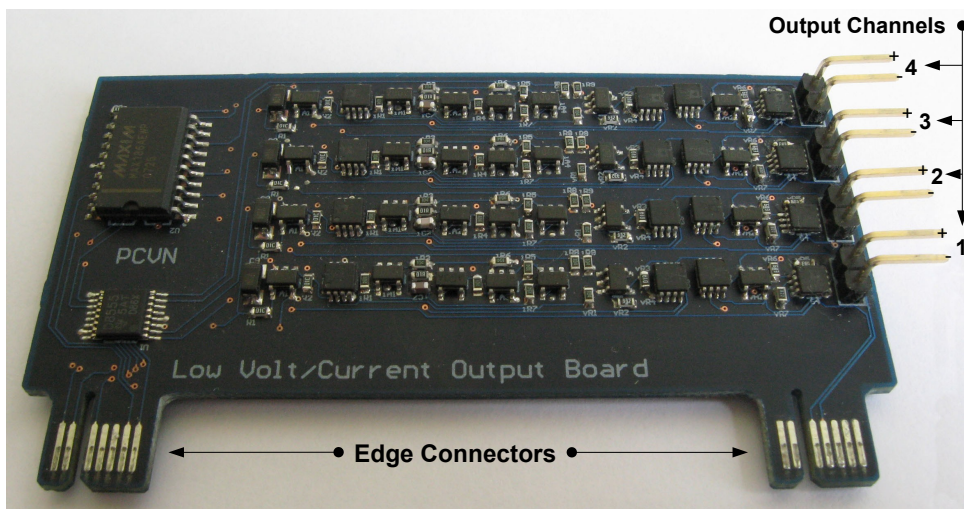


Figure 5.9: Low current and voltage output daughterboard with four channels.

Each channel can be switched independently between a low current or a low voltage source, as described in Section 4.8. This board also contains the hardware for the voltage and current monitoring feedback system to calibrate the output channels, described in Subsection 4.8.5.

This board connects to the motherboard through the two indicated edge connectors. The electrical connection layouts to the edge connectors are given in the schematics in Appendix A.1.

5.1.5.3 High Sensitivity Voltage Input Boards

A *high sensitivity voltage input board* is shown in Fig. 5.10. The two differential input channels are shown with the positive terminal at the top of each channel. Channel 1 is at the bottom and channel 2 at the top. This can also be changed by reprogramming the microcontroller, if so desired.

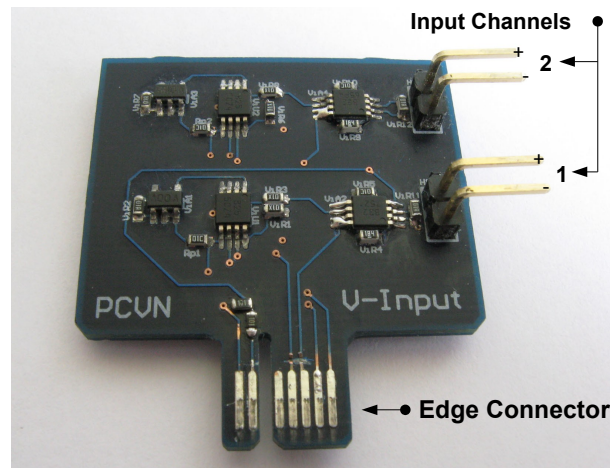


Figure 5.10: High sensitivity voltage input daughterboard.

As seen, this board is smaller than the other daughterboards and therefore only one edge connector was implemented for this board. Twisted pair wires with BeCu female crimp terminals could be used to connect the SCE devices to the header inputs.

The INA322 instrumentation amplifiers as well as the 16-bit ADCs are implemented on this board as described in Section 4.9.

5.1.6 Conclusion

In this section, the hardware implementation is discussed. An overview is given of how the *cryogenic CMOS based control system* fits together. Attention is focused on the different connectors, implemented to connect the different subsystems.

The preference of BeCu alloys for interconnections in cryogenic environments is discussed. It was chosen for its strength, flexibility and electrical conductivity at very low temperatures.

The motherboard and all the different daughterboards are shown where the physical layout and channel positions of these boards are discussed. This is done to show the user how the hardware correlates with the implemented software.

5.2 Software Implementation

Embedded firmware as well as a graphical user interface (GUI) were developed for the control system. These two developments are interdependent on each other where data from the GUI is interpreted by the embedded firmware and vice versa.

The control of the system is done from the computer where the GUI is utilized to graphically input data signals for each channel. Each channel has its own data frame of a user-defined bit length. In order to test SCE, the data need to be uploaded to the firmware, where it is interpreted by the microcontroller in order to control each channel. Configuration data for the control system as well as the experimental data frames are sent to the ATmega16 via the USB-RS232 connection. As the USART is used in asynchronous mode, the data frames are first stored in the SRAM of the microcontroller and are not directly sent on the output channels. This is done in order to send all the channel data in parallel and to attain a maximum test frequency by the microcontroller. Once the frames are saved, they can then be sent to the output channels by a command from the user.

In this section, the programming structure for the embedded firmware is described first. It is then followed by the GUI software development in Subsection 5.2.2.

5.2.1 Embedded Firmware Development

In this section, the program flow for the ATmega16 microprocessor is described. It starts with how the developed code is uploaded to the microprocessor. The firmware operations are then described where the concepts are depicted in flow diagrams. Furthermore, all the necessary commands are given for interfacing the hardware from the GUI.

This section ends with a time assessment of the speed with which the data can be processed by using the implemented commands for the microcontroller.

5.2.1.1 In-System Programming

The hardware programming was done in C with *AVR Studio 4.12*. This program compiles the written code and generates a *.hex file. This program is also used to upload this *.hex by means of the *STK500* development kit from ATMEL. The code that was developed for the ATmega16 microcontroller is given in Section C.2 in the appendix.

In-system programming is done by connecting the *STK500* to the 6-pin SPI header on the motherboard as described in Subsection 5.1.4.1.

5.2.1.2 Main Procedure

When initialized, the main procedure on the ATmega16 microprocessor waits for the user software for instructions before any operations are executed. It initialize all the necessary ports and variables and then waits for an execution flag before a command is executed. A command is

received by an instruction set from the user interface via the USART port in the *USART interrupt procedure*. This interrupt procedure, described in Subsection 5.2.1.3, sets an execution flag when an instruction set was successfully received.

Fig. 5.11 shows the flow diagram of the main procedure as it waits for instructions.

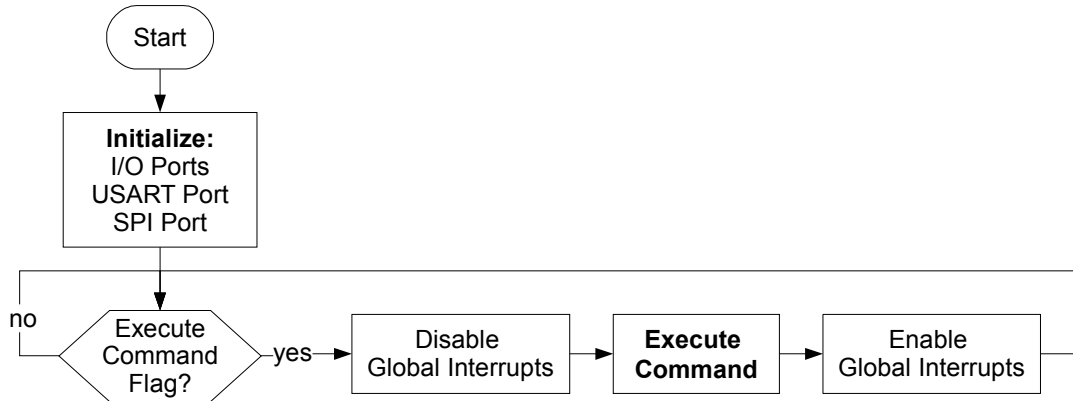


Figure 5.11: The main program on the ATmega16 microprocessor.

While a command is being executed, the global interrupts are disabled. This is done to prevent the *USART interrupt procedure* from altering the global variables that are used when executing a command. The global interrupts are enabled again after the command execution is completed.

The command execution and list of instructions are discussed in Subsection 5.2.1.4.

5.2.1.3 USART Interrupt Handling

The USART interrupt is programmed to receive instructions from the user software on the computer. It interrupts the main procedure with each byte received. An instruction set could consist of 1, 3 or 4 bytes while a special instruction set of 2 bytes enables the USART to receive a string of data bytes. This special instruction set enables the upload of all the data frames to the microprocessor for the different output channels. These data frames are stored in the SRAM of the microprocessor.

Fig. 5.12 shows the flow diagram of how the instruction sets and the data frames are received and stored.

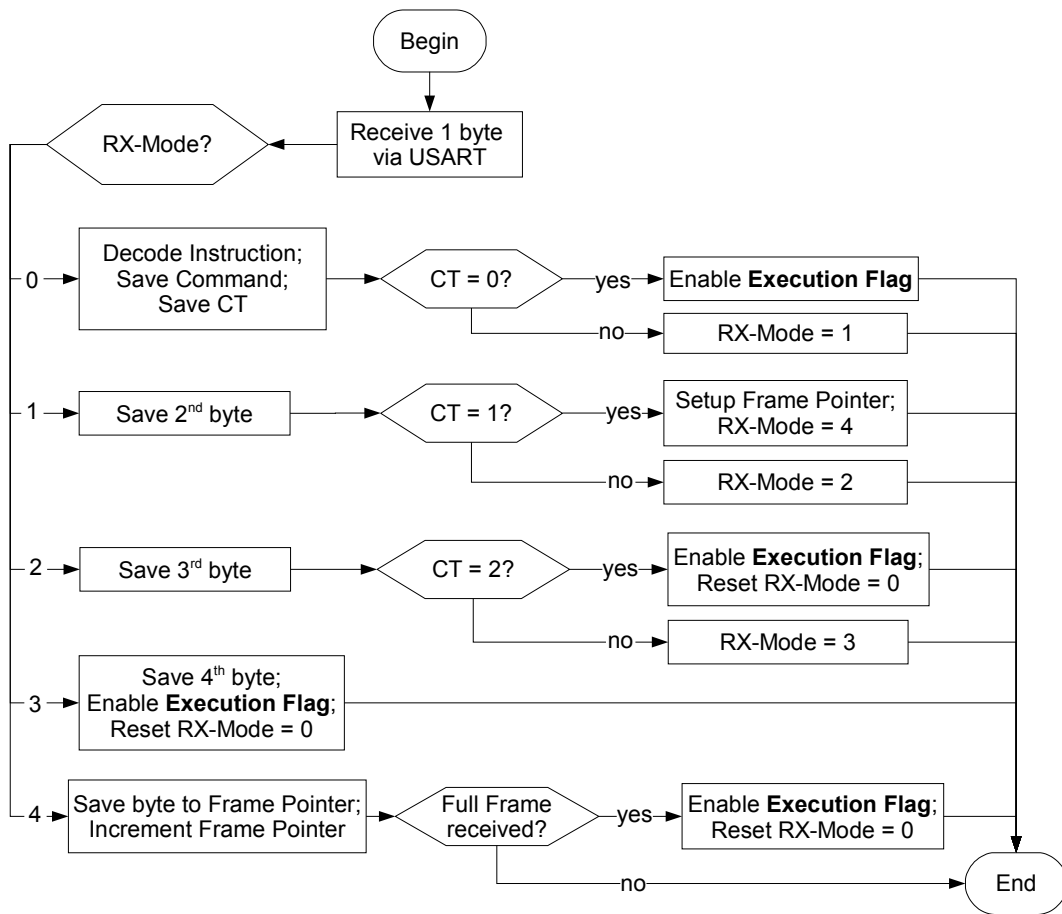


Figure 5.12: Receiving a command through the USART interrupt procedure.

The *RX-Mode* is always zero (0) when the 1st byte of an instruction set is received. The 1st instruction byte contains the command as well as the command-type, CT, while the 2nd, 3rd and 4th bytes usually contain configuration data for the daughterboards. The CT consists of 2 bits that are placed in the two most significant bit (MSB) positions of the 1st instruction byte, as shown in Fig. 5.13.

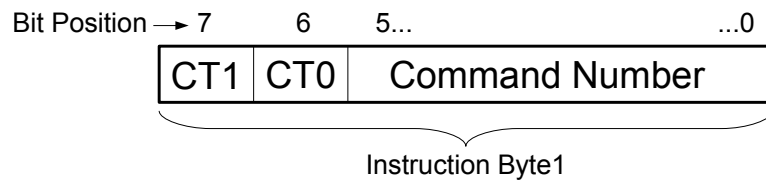


Figure 5.13: The bit layout of the 1st instruction byte.

This CT indicates how many bytes the instruction set consists of, so that the *USART interrupt procedure* knows how many bytes to receive. A description list for CT is given in Table 5.3.

Table 5.3: Command-type bit description.

CT1	CT0	Command-type Description
0	0	1 byte instruction
0	1	2 byte instruction set, followed by n amount of data bytes
1	0	3 byte instruction set
1	1	4 byte instruction set

When a 2 byte instruction set is received, the 2nd byte contains the value n to specify the amount of data bytes that is to be received by the USART. When the full instruction is received by the USART, the *RX-Mode* is reset to zero (0) and an *execute command* flag is set. The command will then be executed from the main procedure, as described in Subsection 5.2.1.2

5.2.1.4 Command Execution

Every command that is successfully received by the USART will be executed from the main procedure by calling a command execution sub-routine. This sub-routine will only execute the specific command and return to the main procedure.

All the different commands for the *cryogenic CMOS-based control system*, with a description, is listed in Table 5.4. These are the commands that can be performed by the ATmega16 microprocessor on the control system. The command numbers are given by C# in the table. Where applicable, the number of return bytes from the microcontroller, with descriptions, are also given.

Table 5.4: ATmega16 microcontroller command descriptions and return values

C#	Command Description	Returns	Return Description
1	Detect daughterboards	6×2 bytes	6×12-bit ADC values for daughterboard identifications
2	Activate specified output channels	n/a	n/a
3	Toggle specified output channel between voltage and current	n/a	n/a
4	Upload positive amplitude of channel	n/a	n/a
5	Upload the frame size and the number of input samples/bit	n/a	n/a
6	Enable all output channels	n/a	n/a
7	Disable all output channels	n/a	n/a
8	Read the voltage feedback values of the specified channels	$ch \times 2$ bytes	$ch \leq 4$; 12-bit ADC values
9	Read the current feedback values of the specified channels	$ch \times 2$ bytes	$ch \leq 4$; 12-bit ADC values
10	Switch heater on	n/a	n/a
11	Switch heater off	n/a	n/a
12	Read battery status	4×2 bytes	12-bit ADC values for \pm voltage and \pm current measurements of batteries
13	Read temperature	2 bytes	16-bit ADC value for temperature reading
14	Activate specified input channels	n/a	n/a
15	Upload negative amplitude of channel	n/a	n/a
16	COM port scan	1 byte	Returns the command+1
17	Output a DC value on specified channel	n/a	n/a
18	Upload output data frames	n/a	n/a
19	Send and receive a data frame for all active channels	x bytes*	Returns the 16-bit sampled input values
20	Loop the send and receive data frames	x bytes*	Returns the 16-bit sampled input values
21	Stop the send and receive loop	n/a	n/a
22	Read the value of each active input channel	$ch \times 2$ bytes	$ch \leq 6$; Return 16-bit values of each active input channel
23	Upload average numbers for input channels and temperature sensor	n/a	n/a

*These commands and return values are discussed in Subsection 5.2.1.5.

All the 12-bit and 16-bit return values that are shown in Table 5.4, are returned in a two-byte format. The value is split between bit 7 and bit 8, as seen in Fig. 5.14. The most significant byte (MSByte) is returned first and is followed by the least significant byte (LSByte).

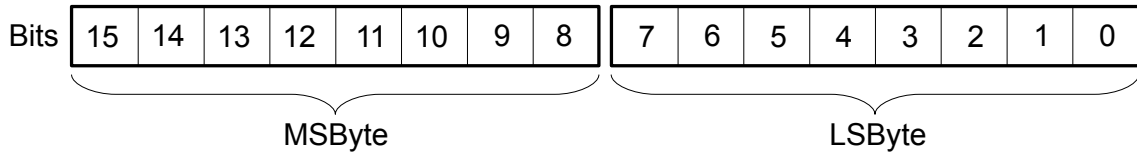


Figure 5.14: Two-byte return value format.

The various commands are explained underneath. For easy reference, the command numbers, C1 to C23, will be used when referring to specific commands.

C1 will detect the daughterboard identification voltages as described in Section 4.10. The 12-bit ID values of all 6 boards will be returned in the two-byte format. The return sequence of these values will firstly be the output daughterboards from 1 to 3 followed by the input daughterboards 1 to 3.

C2 will activate the specified channels on a specific output daughterboard. The channels and board numbers are specified in the instruction set in Table 5.5. This command will only activate the channels on one daughterboard at a time.

C3 is used to toggle the specified channels on a specific output daughterboard between a current source and a voltage source as described in Section 4.8. Only one daughterboard can be set at a time.

C4 is used to upload the maximum value of a logic 1 for a specific channel.

Using C5, the data frame size and the number of input samples per output bit can be set. This command is explained in more detail in Subsection 5.2.1.5.

C6 and C7 are used to toggle the safety switch that enables or disables the output channels on the *low current and voltage daughterboards* as described in Section 4.8.

C8 and C9 will respectively read the voltage feedback and current feedback values of the specified channels on a specific output daughterboard, as described in Subsection 4.8.5. The 12-bit values of the requested channels will be returned in ascending channel order.

C10 and C11 are used to toggle the heater on and off.

The C12 command reads the battery status. It returns four 12-bit values. The first return value is the positive rail battery voltage which is followed by the negative rail battery voltage. This will be followed by the positive and then the negative current values drawn from the batteries.

C13 will return a 16-bit ADC temperature value, sampled from the PT1000 temperature sensor as described in Subsection 4.6.4. When averaging is enabled, the averaging will be done on the microprocessor so that only a single 16-bit value will be returned.

C14 can be used to activate the input channels on all the input daughterboards. The channel selection is shown in Table 5.5.

C15 is used to upload the minimum value of a logic 0 for a specific channel.

C16 is reserved for when the user software detects whether the ATmega16 is active and on-line. The microprocessor responds to this command by returning $17(\text{command} + 1)$ to the user software. This is done when the user software executes a port scan to automatically identify on which COM port the microprocessor is located, and whether it is ready for operation.

C17 will send either a DC current or DC voltage value on a specified channel, depending on which state the channel was selected.

C18 uploads the data frames to be sent on each channel. Each channel has its own data frame of $8 \times n$ bits, where n is the amount of bytes per frame. All the data frames need to be uploaded for each active channel. Only the data frames for the active channels should be uploaded consecutively by this command, in ascending output board and channel order.

C19 to C21 will be explained in Subsection 5.2.1.5.

C22 is a single command instruction which will return one 16-bit value for each active input channel, also in ascending input channel order.

C23 uploads the number of values to be sampled for averaging the input channel values and temperature values respectively.

In order to execute these commands, the instruction set protocol for each command is given in Table 5.5.

Table 5.5: Command instruction set protocol.

CT	C#	RXByte2	RXByte3	RXByte4
00	1	n/a	n/a	n/a
10	2	OutBoardNr	OutChansSel	n/a
10	3	OutBoardNr	OutChansSel	n/a
11	4	OutBrdNr OutChNr	Ampl(HB)	Ampl(LB)
10	5	FrameSize	SPB	n/a
00	6	n/a	n/a	n/a
00	7	n/a	n/a	n/a
10	8	OutBoardNr	OutChansSel	n/a
10	9	OutBoardNr	OutChansSel	n/a
00	10	n/a	n/a	n/a
00	11	n/a	n/a	n/a
00	12	n/a	n/a	n/a
00	13	n/a	n/a	n/a
10	14	InChansSel	0	n/a
11	15	OutBrdNr OutChNr	Ampl_HB	Ampl_LB
00	16	n/a	n/a	n/a
11	17	OutBrdNr OutChNr	Ampl_HB	Ampl_LB
01	18	FollowBytes	byte1	byte2... etc.
00	19	n/a	n/a	n/a
00	20	n/a	n/a	n/a
00	21	n/a	n/a	n/a
00	22	n/a	n/a	n/a
10	23	TempAverage	InputAverage	n/a

The C# value forms part of the 1st byte of the instruction set. It should be noted that the CT value must be added to the command values as shown in Fig. 5.13. RXByte1, 2 and 3 make up the rest of the instruction set which is received by the ATmega16 microprocessor. Naturally, where the n/a (not applicable) is listed, no data need to be sent for that byte. It should also be noted that a '0' value should be included at C14 in RXByte3 to complete the instruction set.

An alphabetical ordered description is listed below for the abbreviated words in Table 5.5.

Ampl_HB: This is the high byte of a 16-bit integer value to set either the maximum or minimum amplitude of an output channel.

Ampl_LB: This is the low byte of a 16-bit integer value to set either the maximum or minimum amplitude of an output channel.

FollowBytes: This is an integer value to specify the amount of data bytes that are to follow the 2-byte instruction set.

FrameSize: This is an integer value to set the number of bytes per frame size.

InChansSel: This is a register for selecting input channels on selected input daughterboards.

Fig. 5.15 shows the bit positions for the specific channels.

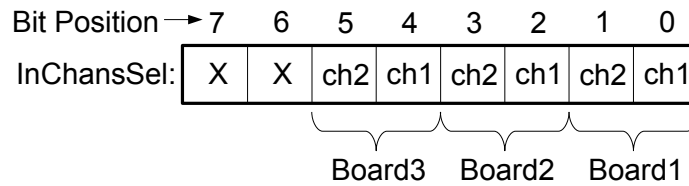


Figure 5.15: Bit positions of *InChansSel* for selecting specific input channels.

Bits 0 and 1 represent channels 1 and 2 on input board 1, bits 2 and 3 represent channels 1 and 2 on board 2, and bits 4 and 5 represent channels 1 and 2 on board 3.

InputAverage: This is an integer value to specify the number of values to be sampled on an input channel, to calculate one average input value.

OutBoardNr: This integer value can be 1, 2 or 3 to specify the output board number.

OutBrdNr|OutChNr: This byte contains two values as seen in Fig. 5.16.

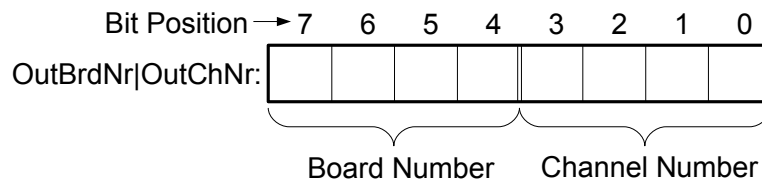


Figure 5.16: The byte allocation of *OutBrdNr|OutChNr* for selecting a specific board and channel number.

The upper 4 bits in this byte represent the board number (1 to 3) and the lower 4 bits in this byte represent the channel number (1 to 4). As an example, if the hexadecimal value of this register is 0X34, then channel 4 on output board 3 is selected.

OutChansSel: This is a register for selecting the output channels on an output daughterboard as shown in Fig. 5.17.

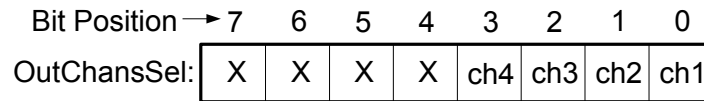


Figure 5.17: Bit positions of *OutChansSel* for selecting a specific output channel.

Bit positions 0 to 3 of this register represent channels 1 to 4 on an output daughter-board. If a bit is set to 1, that specific channel is selected while a 0 will deselect that specific channel.

SPB: Samples Per Bit - This is an integer value, indicating the number of values to sample per input channel for every bit sent on the output channel.

TempAverage: This is an integer value to specify the number of values to be sampled, to calculate one average temperature value.

5.2.1.5 Send and Receive Frames

Before any data frames can be sent or received on the channels, the necessary configuration commands of the control system should be done. The essential configuration commands that need to be executed are, C2 to C6, C14 and C15. These commands activate the specified output and input channels, upload the minimum and maximum amplitudes per output channel, and set up the frame size and input samples per output bit. The frame size is set up by allocating enough SRAM memory with pointers to store each active output channel frame. All the output channels are also enabled by switching the safety switch with C6.

After the configuration is done, the frames for each channel can be uploaded. This is done by using C18. The frame size should be updated each time an output channel is activated or deactivated. Subsequently, the output data frames need to be updated as well.

The data frames are stored in SRAM and are accessed by pointers, while the amplitudes of the output signals are stored in arrays for each separate channel. Each channel has its own logic data frame ready when a send and receive command is given. It also has its own maximum and minimum values. These are the logic 1 and logic 0 values for the specific channel.

After the data frames are uploaded, the send and receive instructions, C19 or C20, can be given to the microprocessor in order to send and receive the data frames on the activated channels. This process is illustrated in Fig. 5.18.

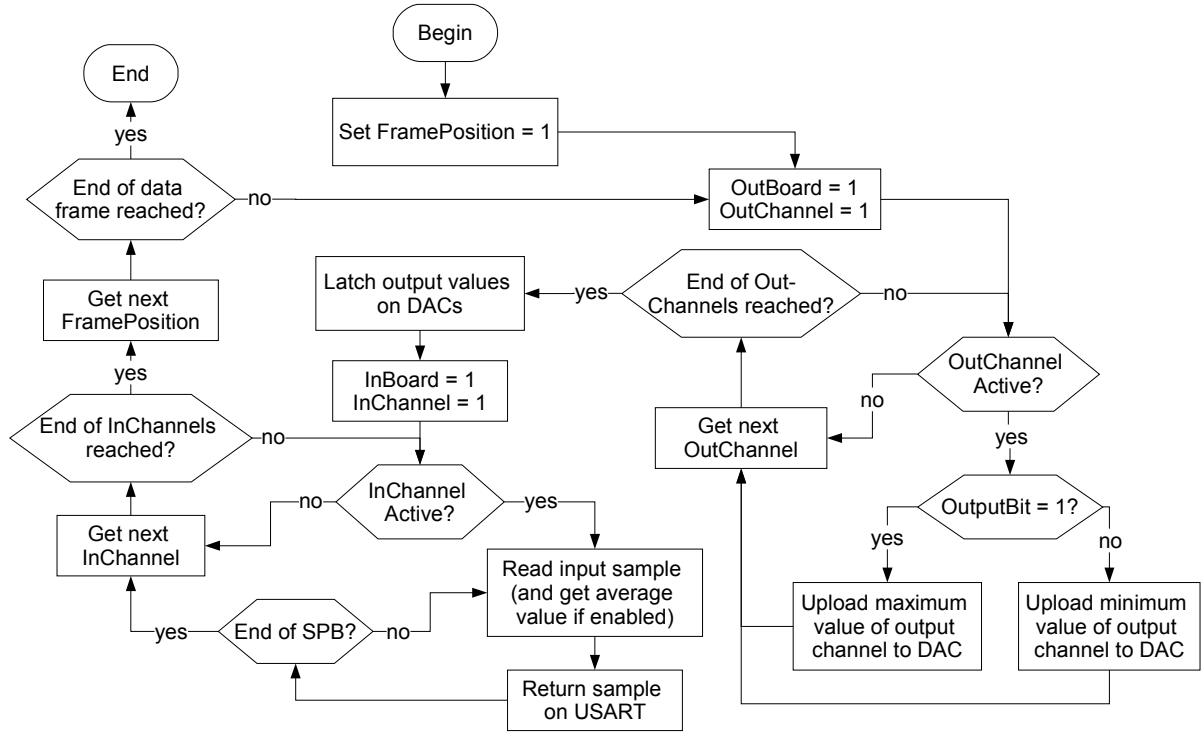


Figure 5.18: Send and receive of the data frames.

Every bit value of each channel is uploaded to the specific DAC. If the bit value is a 1, the stored 16-bit maximum value of that specific channel is uploaded. When the bit value is 0, the stored 16-bit minimum value is uploaded. After every bit value has been uploaded for each active channel, the DACs are latched to update all the new uploaded values on the output channels in unison. This is done for every bit in the output data frame, but before the next data bits are uploaded to the DACs, every active input channel is sampled. The samples per bit (SPB) value specifies how many samples are taken for a specific input channel before the next active input channel is sampled. As the voltage input channels are sampled, they are not stored in SRAM, but are immediately sent to the user interface on the USART.

According to the simulation of the microprocessor software, it takes more time to store the 16-bit sampled values in SRAM, and send them after each completed output frame, than to send them immediately on the USART after each input channel has been sampled.

The number of bytes that are sent back to the user interface can be calculated by the frame size and the amount of samples taken per output bit. The user can thus calculate the amount of returned 16-bit values by

$$\#InputValues = InCh \times (FrameSize \times 8) \times SPB, \quad (5.3)$$

where $InCh$ is the amount of active input channels and SPB is the amount of samples per bit.

The frame size is specified in amount of bytes.

The global interrupts are enabled when the frame loop is requested. This is done in order to receive the stop command from the user interface, and thus stop the loop when requested.

5.2.1.6 Time Assessment

The code that was written for the microcontroller can be simulated on the computer by the *AVR Studio* programming software. The simulation clock speed of the microprocessor was set to 8 MHz. The software can sequentially step through the code, showing the time that each line of code takes to execute.

The timing diagram in Fig. 5.19, gives the execution times of the different commands on the microprocessor.

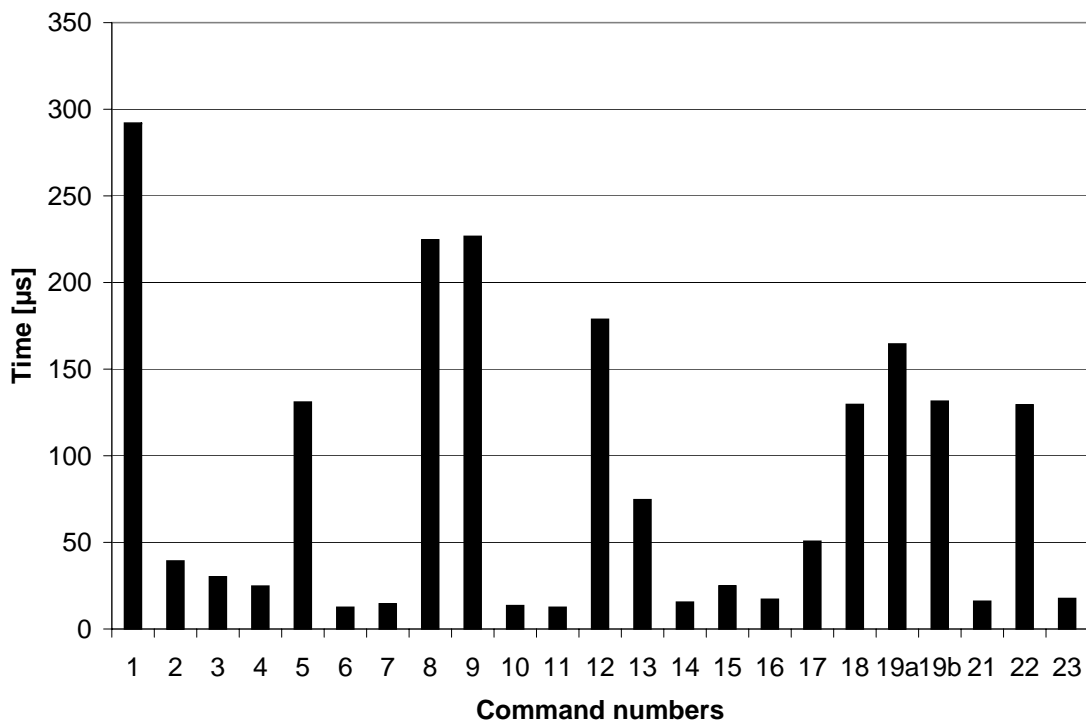


Figure 5.19: Timing diagram for command execution on the ATmega16 microprocessor.

Except for C18, the time values for the commands does not include the USART interrupt timing for uploading the commands to the microprocessor. However, the USART transfer times are included for when the microprocessor returns values to the user interface.

C18 was simulated for uploading a 6-byte data frame to the microprocessor via the USART. According to the simulation, each 12-bit ADC value takes approximately 34 μ s to be sampled.

This time is limited by the SPI SCK frequency, f_{SCK} , that is set at a maximum speed of

$$f_{SCK} = \frac{f_{OSC}}{2}, \quad (5.4)$$

where f_{OSC} is the clock speed of the microprocessor. This makes up the time for C1, C8, C9, and C12, where more than one 12-bit ADC value is sampled.

The frame size set-up of C5 is done with for-loops and a record array for all active output channels.

C19a shows the time required to set one output bit on one active output channel, while C19b indicates the time required to sample one 16-bit value from an input channel.

The steps for making up the time for C19a and C19b is given in Tables 5.6 and 5.7.

Table 5.6: The time needed for sending one data bit in a data frame.

Description (for C19a)	Time [μ s]
Select active channel	8.625
Read logic bit from frame and set /CS on MUX	16.5
Upload amplitude to DAC via SPI	40
Check for more active outputs then latch all DACs	99.375
Total	164.5

Table 5.7: The time needed for sampling one data bit in a data frame.

Description (for C19b)	Time [μ s]
MUX setup for /CS	5.75
Read ADC via SPI	41
Save in temporary variable	7.625
TX data on USART	12.75
Check for more active inputs	56.625
Total	131.5

The largest part of the processing time is taken up by the overhead programming for running loops to check whether any more active channels should be updated. These overhead loops are illustrated in Fig. 5.18.

With this timing analysis, the maximum output frequency for one channel can be calculated to be approximately $1/0.0001645 = 6.07 \text{ kHz}$. The maximum input sampling frequency for one channel that can be done by the microprocessor is approximately $1/0.0001315 = 7.6 \text{ kHz}$.

Practically measured frequencies for data frames on output channels are shown in Fig. 6.8 and Fig. 6.13 in Chapter 6 where the frequency for a '01' bit-pattern was measured to be 2.155 kHz

for two bits. Thus a frequency of 4.31 kHz was attained per output bit. This is lower than the simulation values shown here because the SPI frequency with those measurements was set to a lower value than the maximum SPI frequency. When simulating the code with this lower SPI frequency, the simulation results corresponded with those measured in Chapter 6.

5.2.1.7 Conclusion

An oversight was given of the code that was implemented to operate the ATmega16 microprocessor. Flow diagrams of the main procedure, the USART interrupt handling and data frame handling are given. All the instructions are given to interface the designed hardware of the *cryogenic CMOS-based control system*.

Data for each output channel are sent to the hardware in frames and stored in SRAM on the microprocessor. This is done in order to output the data of each channel in parallel. The time for each instruction was measured in simulations whereupon an estimate could be calculated for the maximum transfer rate of the data frames. These simulated transfer rate frequencies correspond to the measured transfer rate frequencies in Chapter 6. A maximum frequency of 6.07 kHz could be attained for sending data on an output channel. Although this is lower than the anticipated transfer rate, it is still faster than Octopux, as mentioned in Chapter 2.

Much of the processing speed is used up with high level language such as *C*. Higher frequencies could possibly be obtained when programming the microprocessor in assembler.

5.2.2 User Interface Software Development

An executable GUI was developed to interface with the *cryogenic CMOS-based control system*. This is a test platform that enables the user to implement the control system for testing SCE devices. From here various SCE test setups can be controlled.

The GUI is a user-friendly application where data can easily be edited in graphical format. The layout is presented in a digital oscilloscope style view where the output and input channels are graphically displayed.

The presented of the GUI is grouped by various functionality of the control system and is displayed on different pages. It is divided into five sections. There is a setup page and a channel calibration page. Two different output channel pages are implemented. A separate page is assigned for the implemented temperature control and battery status monitoring.

The GUI was developed using *Borland Delphi*. The code for the GUI is given in Section C.3 in the appendix.

In this section, a description of the program flow gives insight into how the GUI operates. The implementation of each channel calibration is described whereupon the data frame *send and receive* functionality is also given. The software implementation of the temperature control and battery monitor systems are also discussed.

5.2.2.1 Program Flow

Upon program execution, a COM port scan is done in the *form create* procedure. When the application is executed, it will automatically detect whether the hardware of the control system is connected to any COM port and if it is ready for operation. As described in Section 4.2, the USB port is used for communication to the hardware of the control system, but the software interprets this port as a normal COM port.

The GUI application responds to user interface actions. It waits for user input before any code is executed. Buttons on the GUI are linked to specific code snippets that execute when the buttons are pressed. An example of the developed GUI is shown in Fig. 5.20. Here the COM port can be configured manually when a different custom baud rate is required. The daughterboards on the motherboard can also be detected and verified.

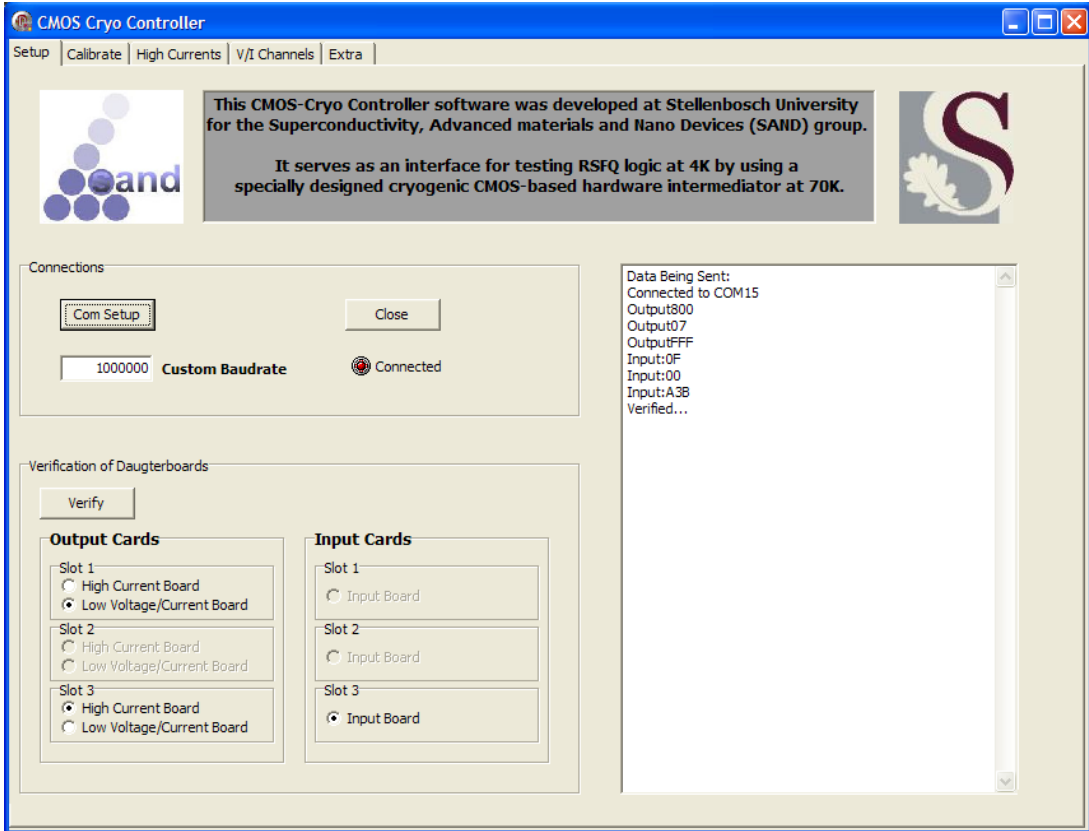


Figure 5.20: An example of the GUI application for the control system.

As seen at the top of Fig. 5.20, different tabs are implemented for the different functions of the control system.

All the interfacing with the control system hardware is done by utilizing the firmware commands that are described in Subsection 5.2.1.

5.2.2.2 Channel Calibration

Both the low power output and input channels can be calibrated. The calibration of the *low current and voltage output channels* are done by using the feedback monitor system described in Subsection 4.8.5. Because the minimum and maximum output values of the output channels could vary slightly, these values are also measured by the feedback system to limit the user to these boundaries. The minimum and maximum voltage feedback values are stored in V_{min} and V_{max} , while the offset of the voltage channel is stored in V_{offset} . Each calibrated data value sent to the DAC on the control system is then calculated by

$$DAC\ value = \left(\frac{(V_{user} - V_{offset}) + (V_{max} + |V_{offset}|)}{2V_{max} + 2|V_{offset}|} \right) (2^{16} - 1), \quad (5.5)$$

where V_{user} is the user specified voltage output value. This formula is used because the middle value of the DAC is transformed to the zero value on the output channel by the bipolar conversion, explained in Subsection 4.8.1.

Also discussed in Subsection 4.8.5 is the measurement of the load resistance, R_L . This is done along with the calibration. The GUI application utilizes the feedback system in order to measure the value of R_L . If no R_L is connected to the output channel, this will be detected to warn the user that the channel to the SCE device might be disconnected.

The DC offset calibration of a highly sensitive voltage input channel is done by connecting one of the output channels to the input channel. The user software does the calibration by disabling the output channels, in other words, grounding the output. This is then used as a reference for the input channel to know how much DC offset is measured by the specific input channel. The offset is measured and stored. When an input channel is calibrated, this offset value is used by simply subtracting the offset from the measured input value for that specific input channel.

5.2.2.3 Output and Input Channels

Only the settings for the verified daughterboards, detected on the motherboard, are displayed in the control system software.

The *high current channel* control page is separated from the *low current and voltage output* control page as it performs a different function on the SCE circuits.

In the *low current and voltage output* page, data frames can be entered into the GUI for each channel for sending bit-patterns to the SCE circuits. These bit-patterns are displayed graphically, almost like a digital analyzer, for each active output channel as shown in Fig. 5.21. As seen, each channel can be selected to be either a voltage or a current output. The frame size, input samples per output bit and averaging can also be set. Each minimum and maximum output value that is sent to the DAC is calculated by Eq. 5.5.

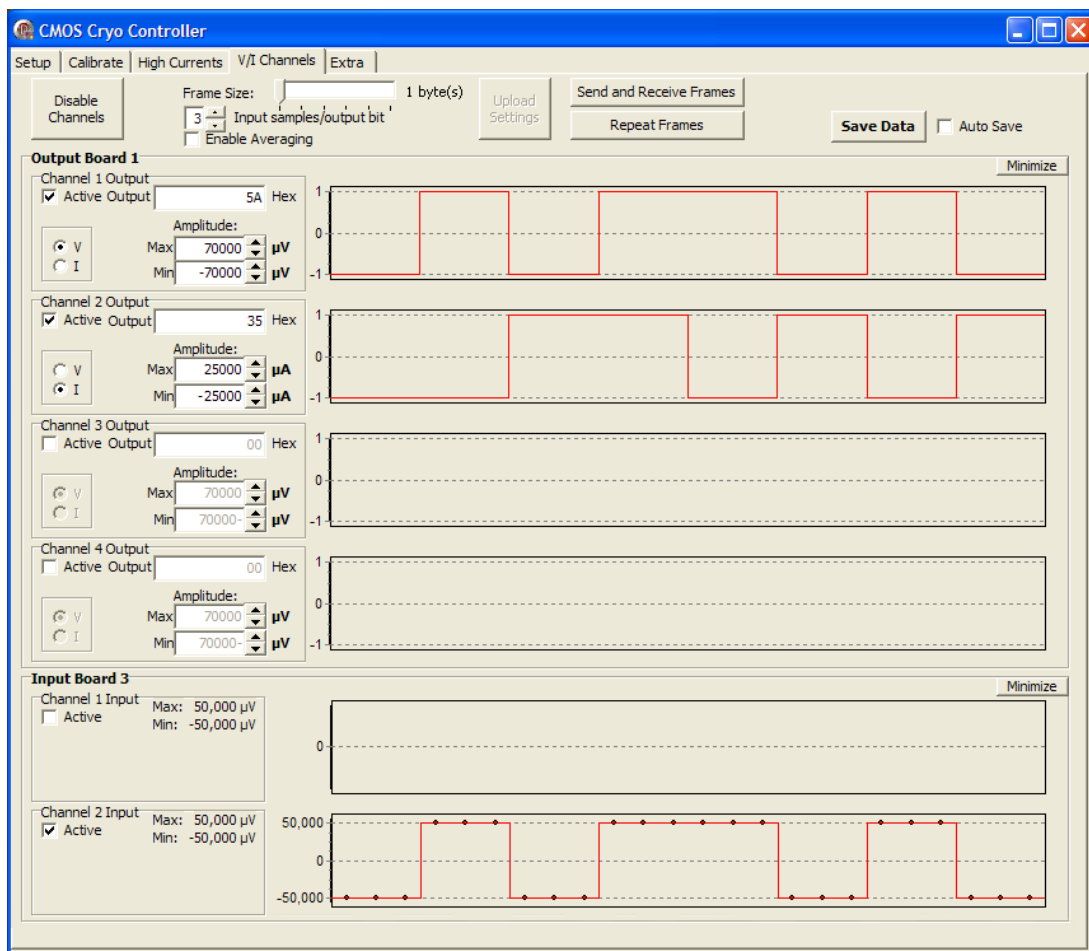


Figure 5.21: Output and input channel settings.

Most of the configuration commands, described in Subsection 5.2.1.4, are sent to the hardware as the buttons are clicked. Only the frame data and amplitude settings need to be uploaded before a send and receive test can be done.

The GUI for the control system will receive and display all the activated input channel values. These values are displayed in a digital oscilloscope style. All these input values can be stored to a file for data interpretation at a later stage. Both the output and input data values are saved to a *.m file so that data plots can be done in Matlab as well.

5.2.2.4 Temperature Control System

The temperature control system operates on a timer interrupt, set to read the temperature every 500 ms. It is enabled by a button on the GUI, that could be pressed by the user, as seen in Fig. 5.22.

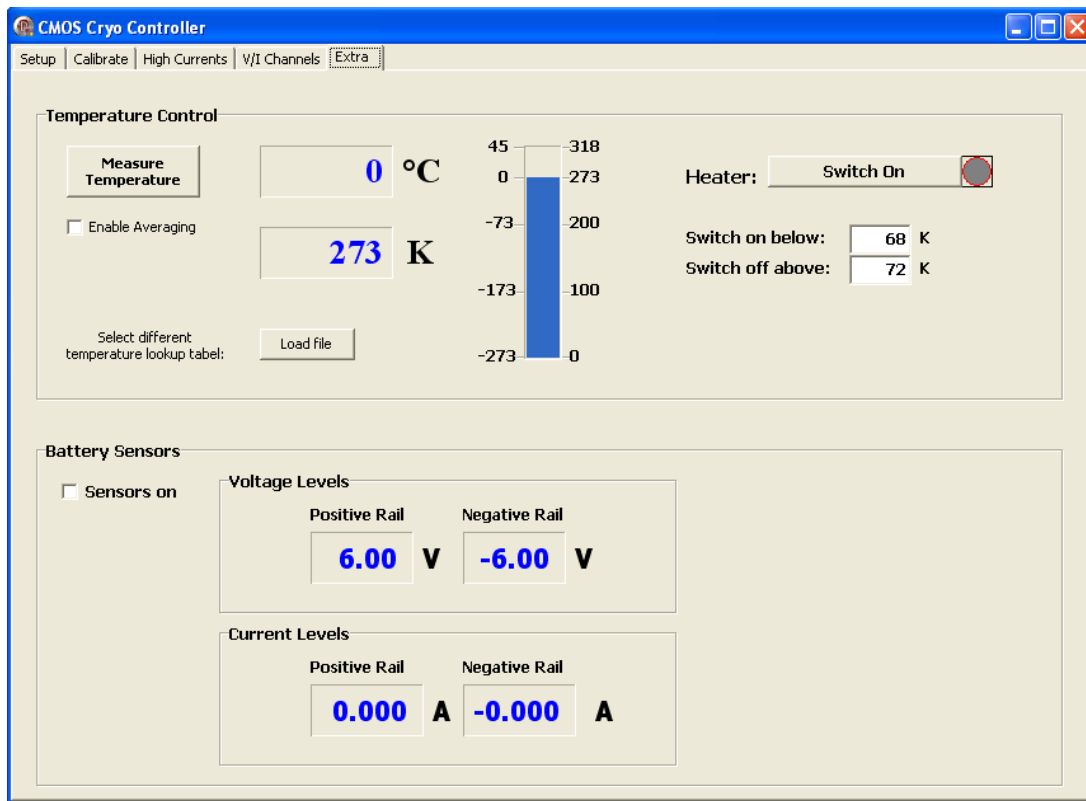


Figure 5.22: GUI for the temperature control system and battery status monitor.

Although the heater is linked with the measurement of the temperature sensor, it can be activated by a separate button. If the temperature measurement is activated it will check whether the heater should be enabled or disabled on each timer interrupt. If the temperature is below a predetermined value and the heater is off, it will be enabled. If the temperature is above another predetermined value and the heater is on, it will be switched off.

A flow diagram of the temperature control sequence is given in Fig. 5.23.

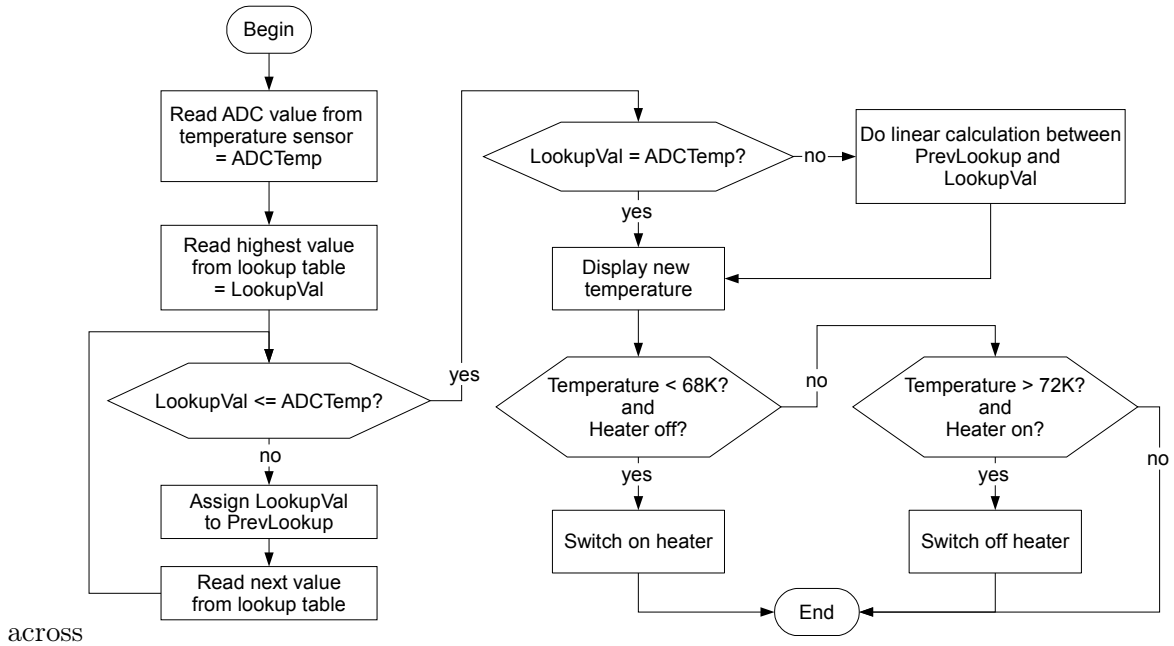


Figure 5.23: The flow diagram for the temperature control system.

With each timer interrupt, the temperature value is calculated by sampling a 16-bit ADC value from the temperature sensor on the motherboard. It then uses this value to find the correct corresponding temperature value in a lookup table. The lookup table is a text file with a *.tpr extension, consisting of two columns. The first column contains the 16-bit ADC values while the second column contains the corresponding calibrated temperature value. There can be between 2 and $2^{16} - 1$ entries in the lookup table. The first value should be the largest 16-bit value (65 535) and the last value should be the smallest (0). If the exact ADC value is not present in the table, a linear approximation will be calculated for the temperature, T , by

$$T = \left(\frac{ADCTemp - LookupVal}{PrevLookup - LookupVal} \right) (PrevTemp - Temp) + Temp, \quad (5.6)$$

where $LookupVal$ is the 16-bit lookup value that is just smaller than the measured ADC value, $ADCTemp$, and $PrevLookup$ is the 16-bit lookup value that is just larger than $ADCTemp$. $PrevTemp$ and $Temp$ are the corresponding temperature values of $PrevLookup$ and $LookupVal$ respectively.

5.2.2.5 Battery Monitor System

The battery monitor system is implemented to monitor the battery voltage and current levels. This is also done on a 500 ms timer interrupt sequence. With this system the batteries can be monitored to see when battery replacement or recharge is required. It also detects the current drawn from the batteries. The values are graphically displayed as shown in the bottom of

Fig. 5.22.

The battery monitor system is implemented by the GUI by sending the command for reading the battery status as described in Subsection 5.2.1.4. The hardware will then return the correct 12-bit ADC values which are interpreted by the GUI and displayed for the user. The ADC value for the voltage monitoring of the battery is decoded with the following equation

$$V_{Battery} = 3 \times \left(\frac{Value_{ADC}}{(2^{12} - 1)} \right) V_{Ref}. \quad (5.7)$$

The detected voltage value is multiplied by 3 because the 6 V from the batteries are divided by 3 so that the ADC can detect the value in the range of the reference voltage, V_{Ref} .

The current calculation is more complex and is derived from the current sensing circuit design in Subsection 4.1.3.

$$\frac{I_{Battery} \times R_C}{2} \times G_{amp} \times \left(\frac{22}{22 + 33} \right) = V_{ADC} \quad (5.8)$$

$$I_{Battery} = \frac{5 \times V_{ADC}}{G_{amp} \times R_C} \quad (5.9)$$

Here the battery current, $I_{Battery}$, is calculated with the measured ADC voltage

$$V_{ADC} = \frac{Value_{ADC}}{2^{12} - 1}.$$

G_{amp} is the gain of the instrumentation amplifier and R_C is the value of the special resistor for measuring the current through it.

5.2.3 Conclusion

A graphical user interface (GUI) design is proposed and its functionality is discussed.

Specific routines on how the GUI was implemented gives insight into the operation of the software. The operation of the GUI is mainly based on the commands that were created for the hardware interface. As specific commands are sent to the control system hardware, data values are received back from the hardware. These values are interpreted by the GUI to update the user display. Valuable data results can also be stored to data files for later interpretation.

Special features such as the temperature control system and the battery monitor system are also discussed.

This GUI can be used to do controlled tests on SCE circuits.

5.3 Summary

In this chapter the full system implementation was discussed. It starts with how the hardware of the cryogenic CMOS-based control system is implemented and how every subsystem fits together. All the connections are discussed and shown.

The second part of this chapter discussed the detail of software development and implementation. All the software interface commands are given for the user to understand the operation of the software.

Chapter 6

Control System Tests and Results

The final *cryogenic CMOS-based control system* was designed, built and implemented as shown in Chapter 5. This control system was then put through a sequence of tests to evaluate its performance at normal room temperature as well as in cryogenic environments.

A modification was made to the control system for measurements in cryogenic environments. An external 8 MHz TTL clock was connected to the ATmega16 from the outside of the cryocooler. This was done because the internal RC clock on the ATmega16 microcontroller became unstable below 190 K. Although the RC clock speed did not vary by more than 2%, the instability caused a communication loss on the USART. The cryogenic tests were done in the *Gifford McMahon* cryocooler at a temperature of 85 K. Due to the lack of Helium pressure, this cryocooler could not produce any lower temperatures. The control system motherboard with its daughterboards did not fit in the *Cryomech PT405* cryocooler, so the tests could not be done at a lower temperature. All these tests were done on the control system while operating from its own battery power supply.

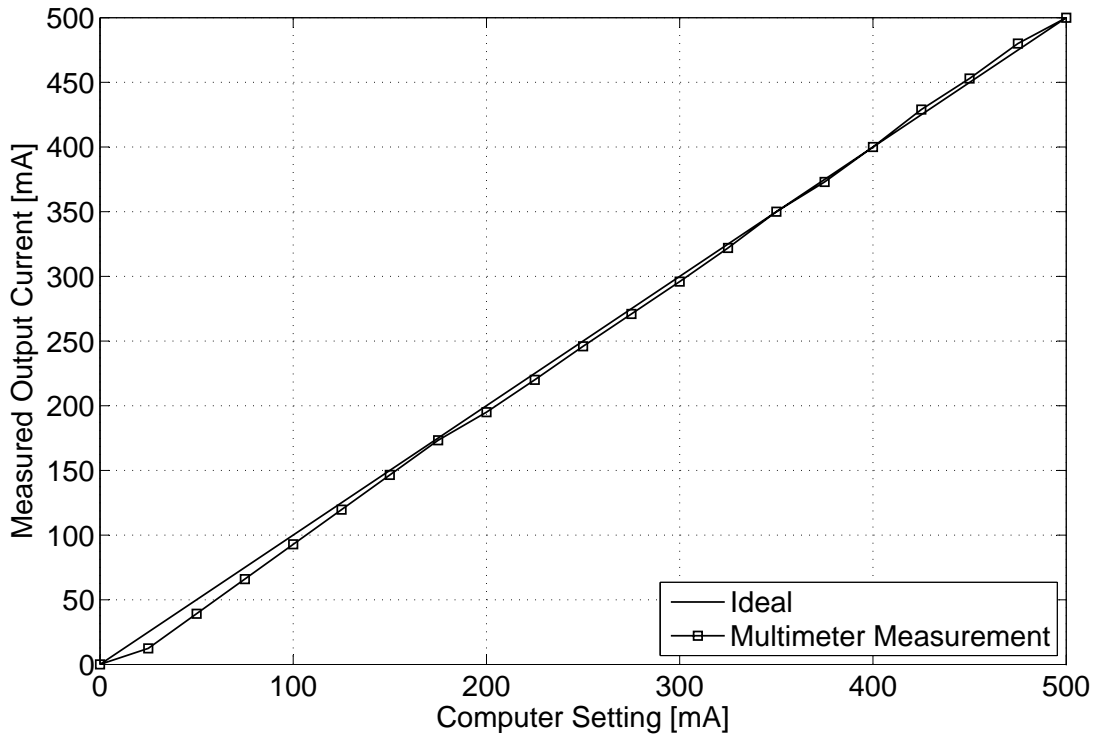
The results were measured with a multimeter and a *Tektronics* digital oscilloscope.

Tests on each channel type are discussed where a result analysis is given. This chapter is concluded with a summary of the power usage of each part of the control system.

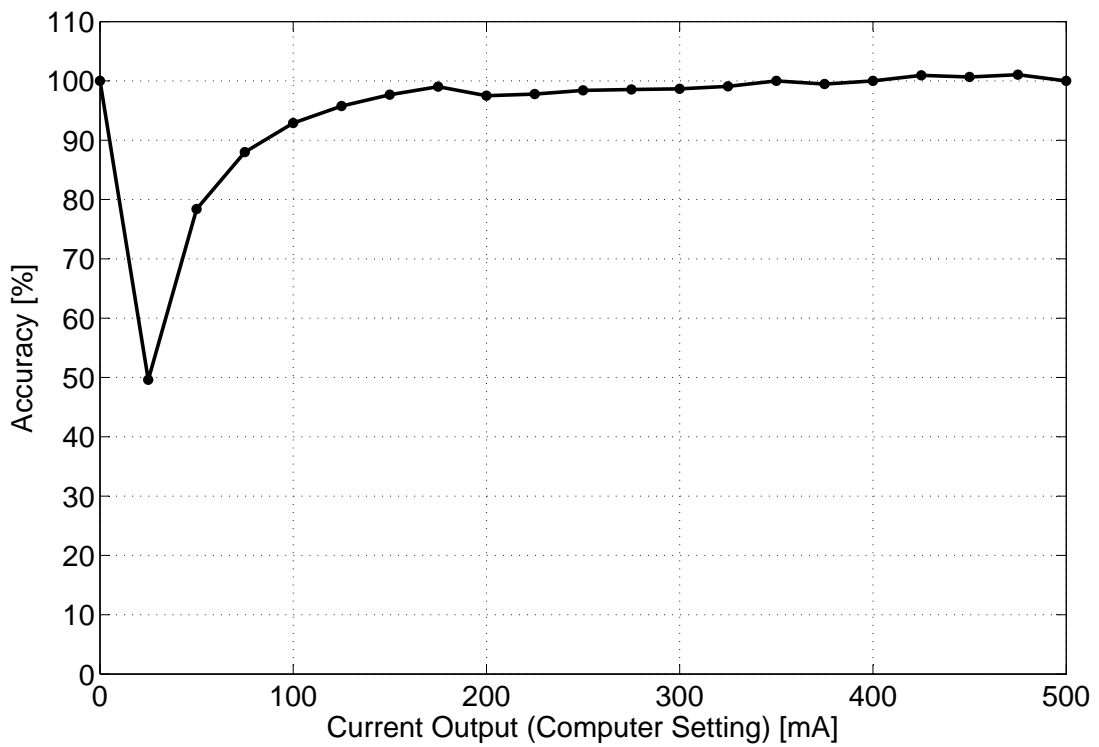
6.1 High Current Output Channels

6.1.1 Linearity and Accuracy

A linearity test was done on the *high current output channel*. The output channel was connected to the maximum load resistance, $R_L = 13\Omega$, to test if the maximum current value of 500 mA could be achieved, as the simulations showed in Section 4.7. The results of these tests done at room temperature are given in Fig. 6.1 with the cryogenic tests shown in Fig. 6.2.

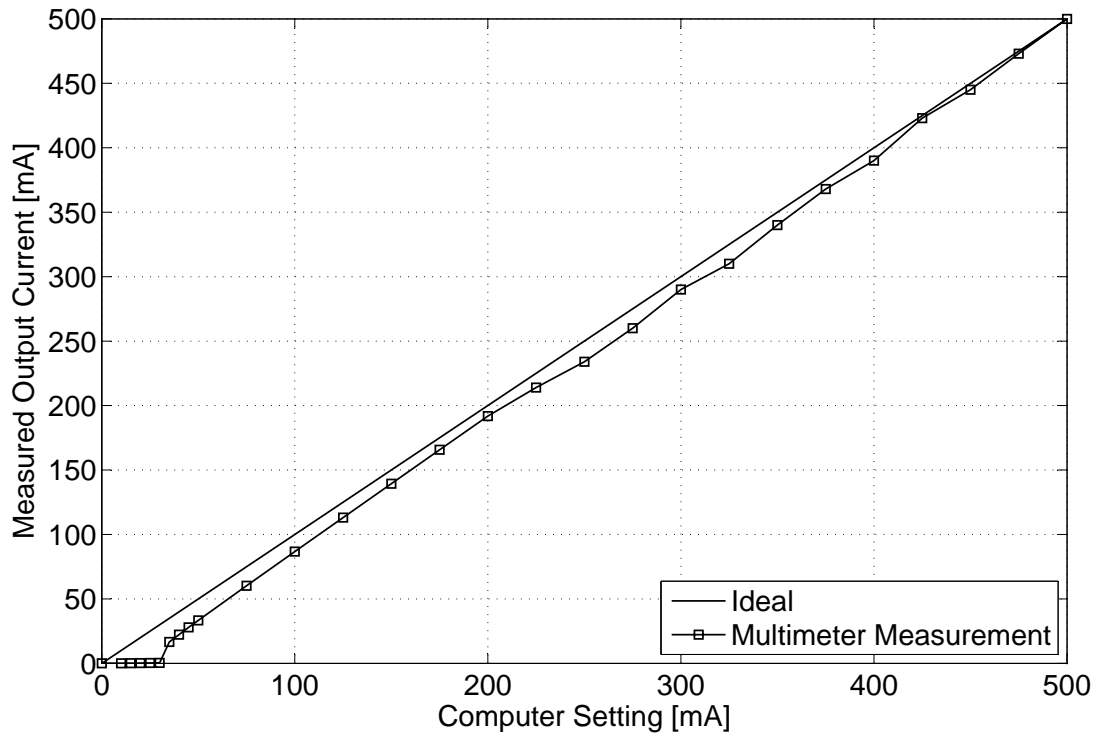


(a) Linearity

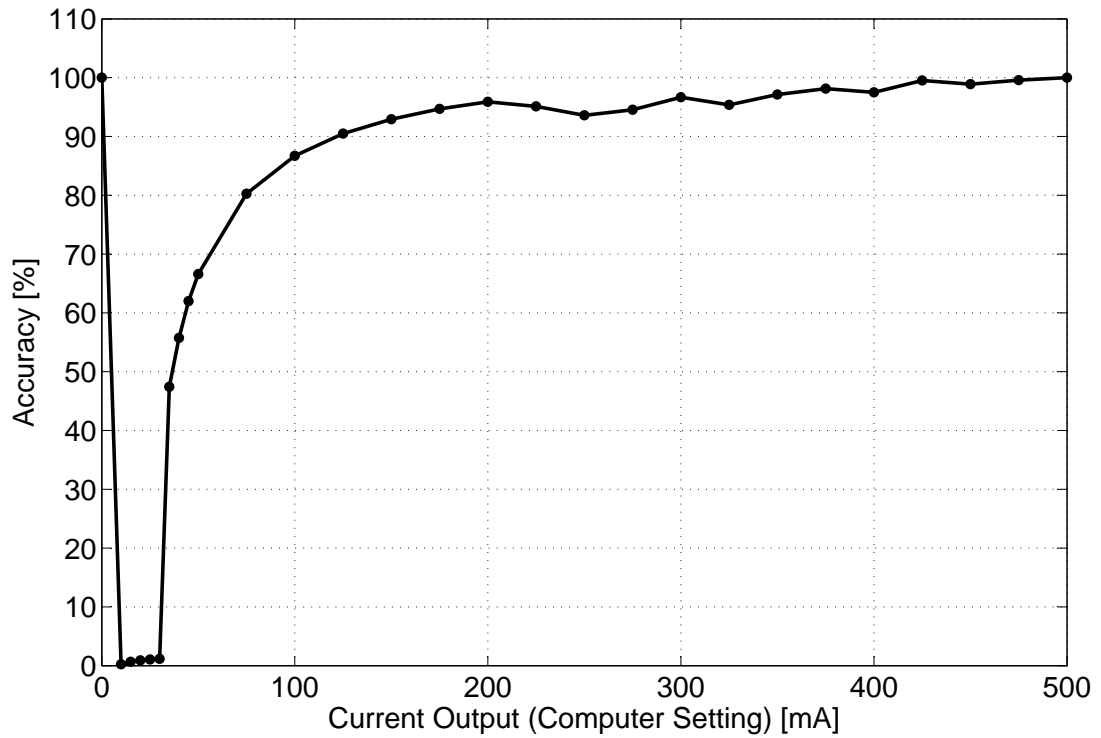


(b) Accuracy

Figure 6.1: The (a) linearity and (b) accuracy of the *high current channel* output at 300 K.



(a) Linearity



(b) Accuracy

Figure 6.2: The (a) linearity and (b) accuracy of the *high current channel* output at 85 K.

Fig. 6.1(a) and Fig. 6.2(a) show the linearity of the output against the desired values of the computer setting. The accuracy of the linearity tests are given in Fig. 6.1(b) and Fig. 6.2(b). The accuracy values were calculated by

$$I_{Accuracy} = \left(\frac{I_{MM}}{I_C}\right)100, \quad (6.1)$$

where I_{MM} is the actual measured multimeter reading and I_C is the desired computer setting.

The maximum current value of 500 mA is achieved with great accuracy. As seen, finer measurement increments at the lower current outputs were taken from the tests done in the cryocooler. The multimeter measurements are not very accurate, as it can only measure in steps of 10 mA for values larger than 200 mA. The results indicate that the *high current channel* in the cryocooler delivers slightly less current as in room temperature conditions. This might be caused by the output offset voltage drift with varying temperature of the LM7101 op-amp used in this design. The input offset voltage drift for this device is specified to be $1 \mu\text{V}/^\circ\text{C}$.

Although the measurements are quite linear from approximately 30 mA upwards, both were lower at smaller current settings than what was anticipated at first. On closer inspection of the simulation of this channel in Subsection 4.7.1, a non-linearity was found at the lower current output values. The transistor used in this design as described in Subsection 4.7.1, will cause the output current to follow the curve as shown in Fig. 6.3(a). This will cause the current channel to have an offset of 7 mA at $V_{DAC} = 0$.

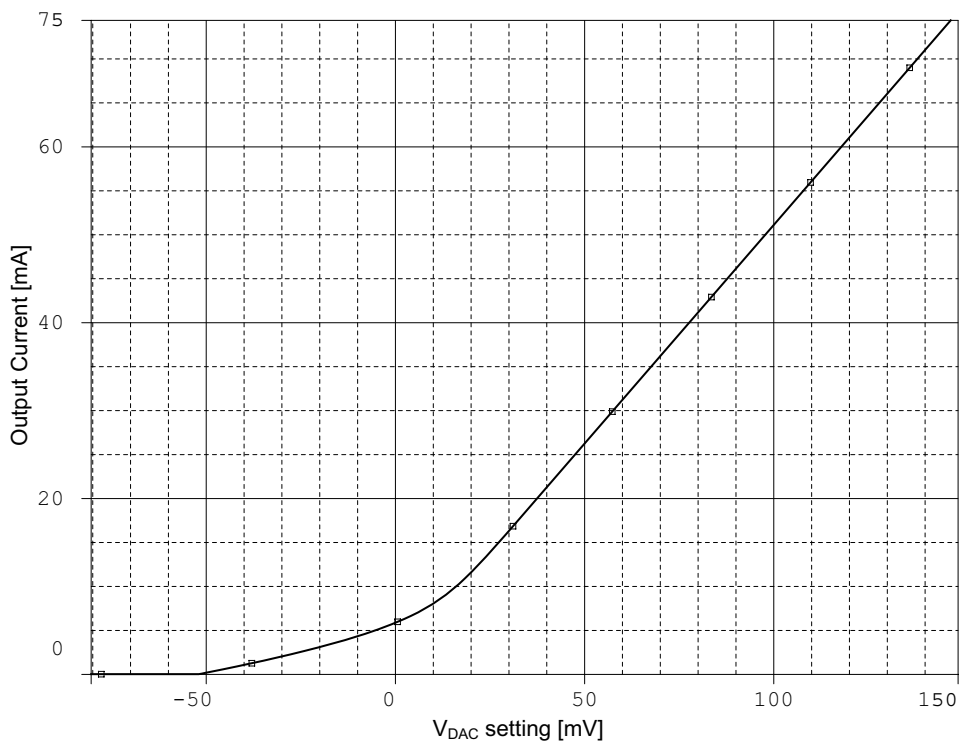
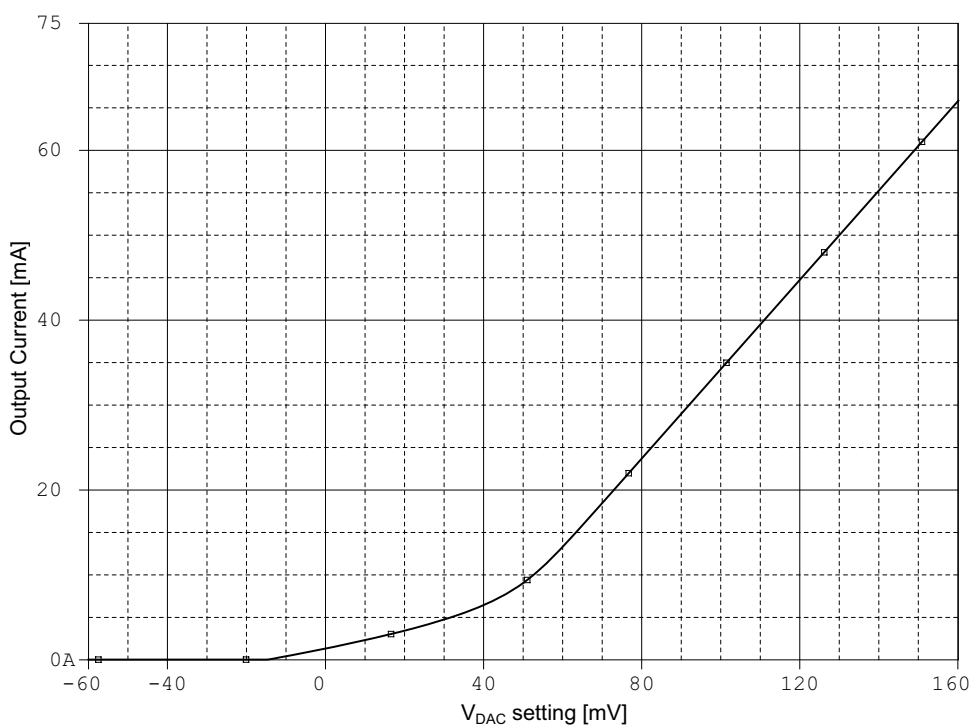
However, when the R_d resistors (Fig. 4.19) are not exactly equal to each other, this function can shift left or right as shown in Fig. 6.3(b). An offset of 2 mA can be observed in this simulation at $V_{DAC} = 0$. The simulation was done with the actual measured R_d values in Table 6.1 for the tested *high current channel* shown in Fig. 6.1.

Table 6.1: The actual measured values of the R_d resistors in a *high current channel*.

Resistor	Value [k Ω]
R_{d1}	100
R_{d2}	99.4
R_{d3}	99.4
R_{d4}	100.3

This then explains the inaccuracies in the measurement of the high current channel at the lower current settings.

The simulations were done with $R_L = 13 \Omega$.

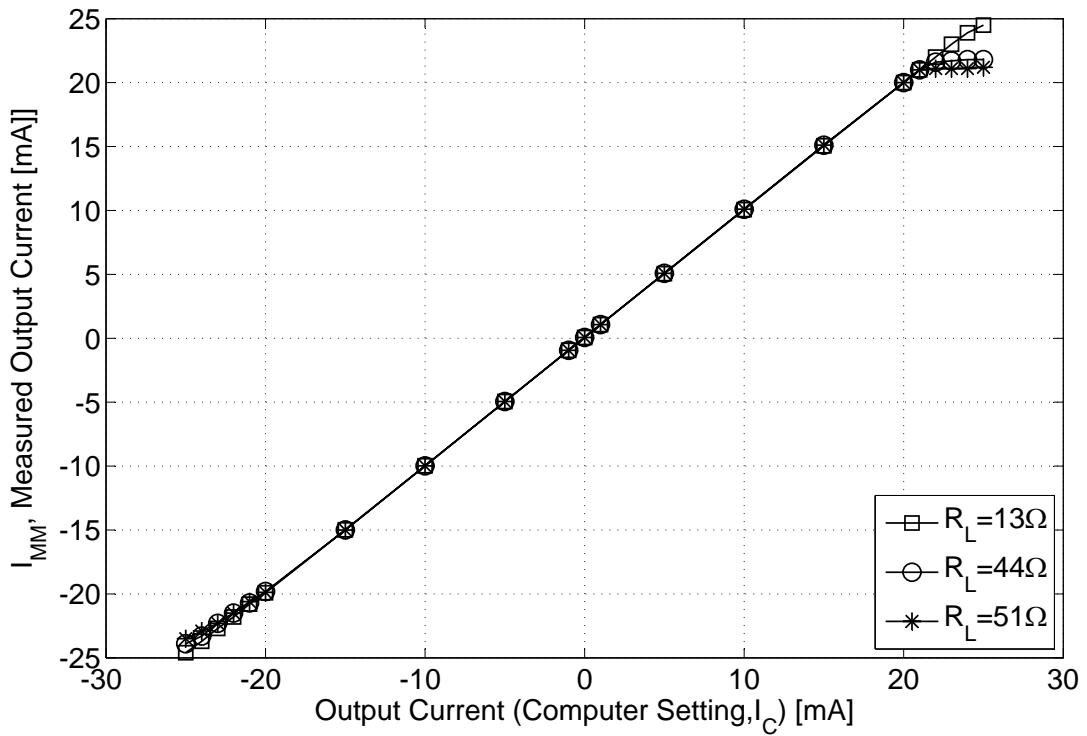
(a) With all R_d values equal to 100 k Ω .(b) With actual measured R_d values.**Figure 6.3:** Simulations of the *high current channel*, showing the non-linear response at low output values.

6.2 Low Current Output Channels

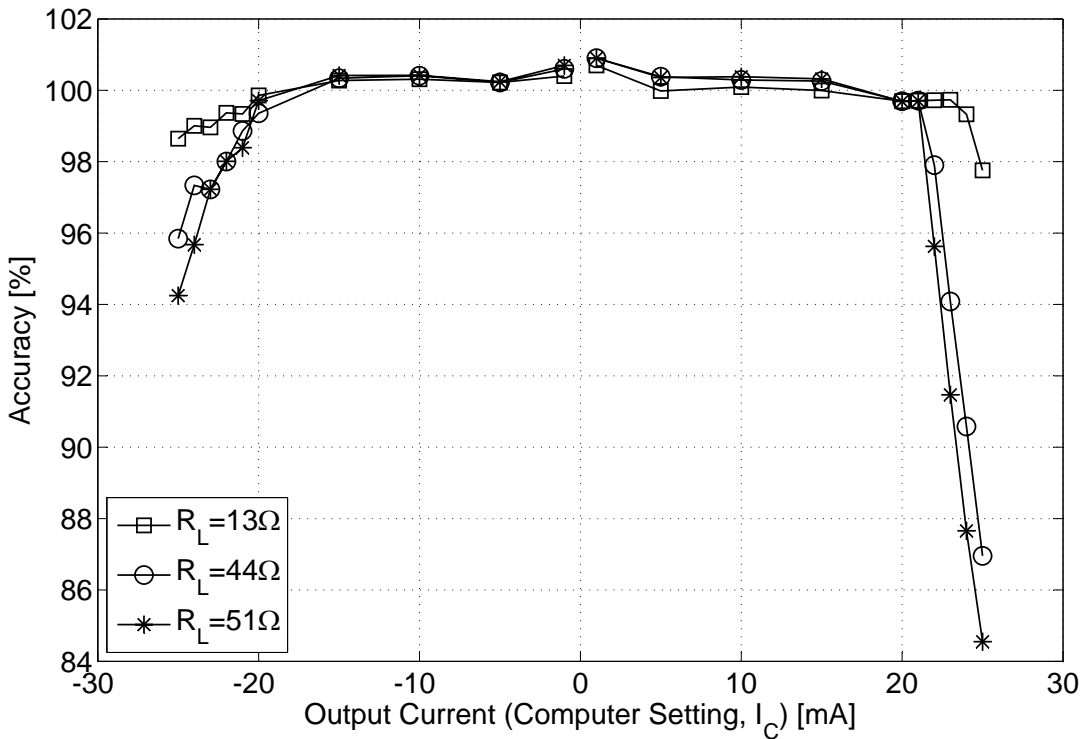
6.2.1 Linearity and Accuracy

The linearity of the *low current output channels* were measured with different load resistance values (R_L). Room temperature measurements are shown in Fig. 6.4 with the cryocooler measurements in Fig. 6.5. With lower R_L values, the output channels produced the expected full current range of ± 25 mA. However, with larger R_L values of up to 51Ω , the output current was suppressed at approximately 22 mA in room temperature conditions. The negative values were suppressed slightly less. The reason for the suppression is that the output voltage on the op-amp increases with a larger R_L in order to maintain the same desired current output level. With this larger output voltages, the positive power rail starts to clip the signal.

Also the data page of the LM7101 op-amp used in this design, indicates that when operating on a single 5 V power supply, the maximum output current is about 20 mA. However, this design was implemented with dual rail ± 5 V power supply rails, thus slightly more current could be drawn from the op-amps.

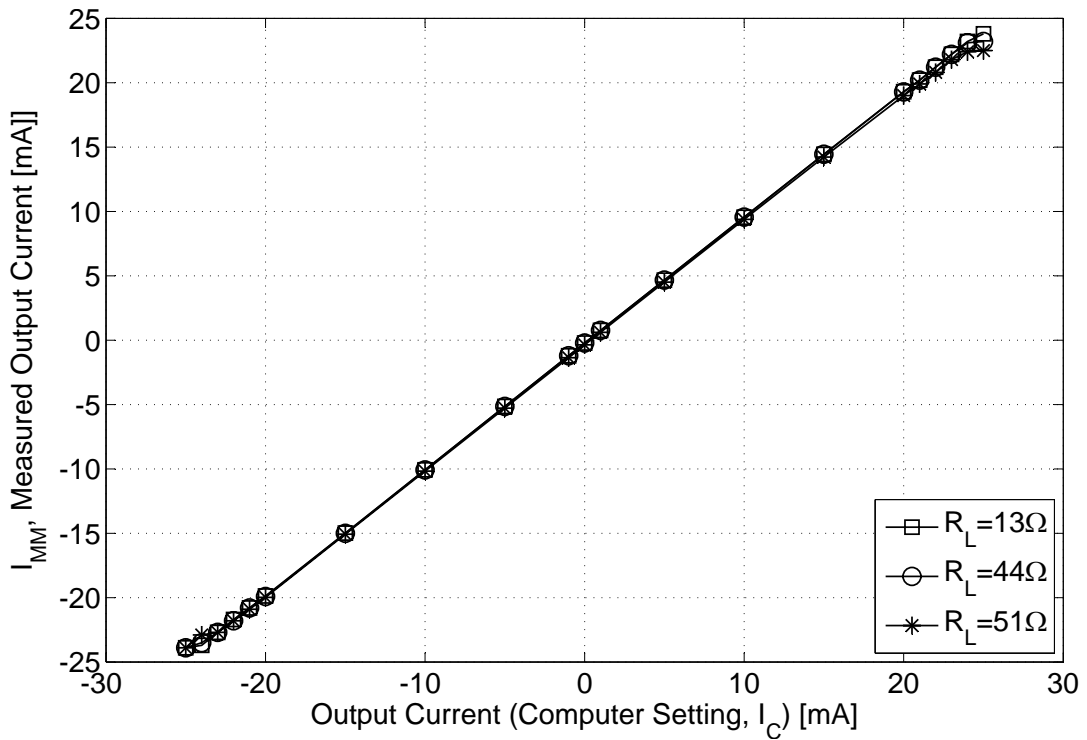


(a) Linearity

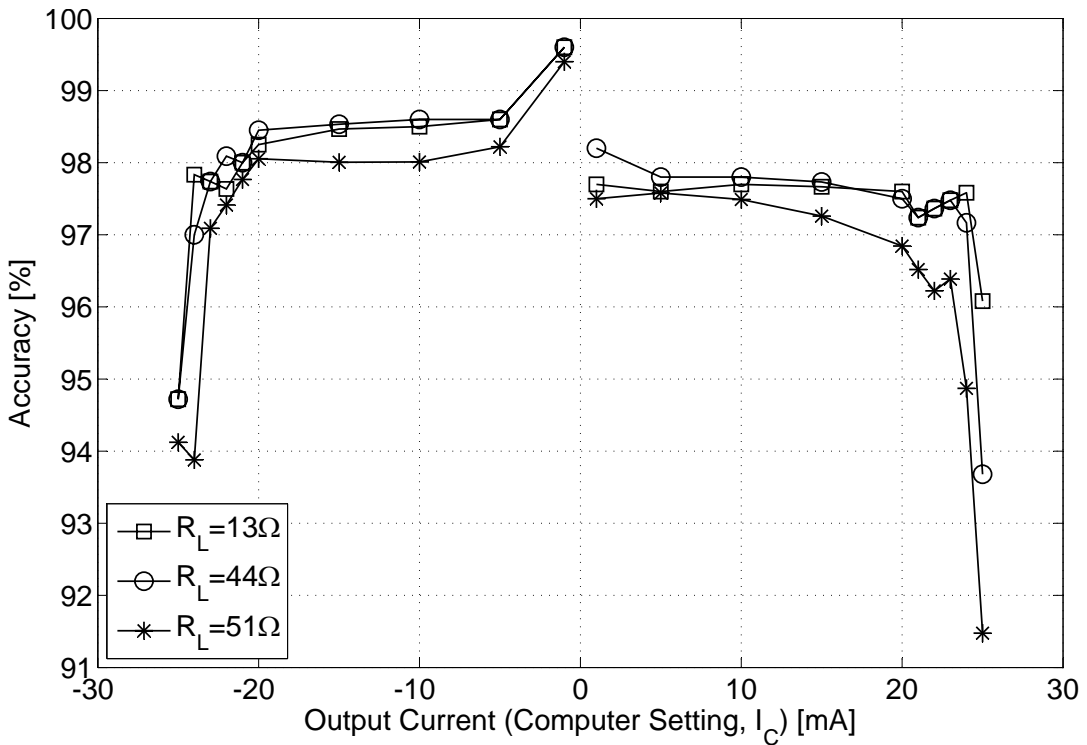


(b) Accuracy

Figure 6.4: The (a) linearity and (b) accuracy of the *low current channel* outputs for different load resistances at 300 K.



(a) Linearity



(b) Accuracy

Figure 6.5: The (a) linearity and (b) accuracy of the *low current channel* outputs for different load resistances at 85 K.

Fig. 6.4(b) and Fig. 6.5(b) indicate the accuracies with which these channels can be adjusted. Again, this also shows the output suppression with larger R_L values. The offset of these channels were set to 0 mA, thus at the 0 mA computer setting, the accuracy would be 100%. The accuracy values were then calculated by

$$I_{OutAccuracy} = \left(\frac{I_{MM}}{I_C}\right)100, \quad (6.2)$$

where I_{MM} is the multimeter measurement and I_C is the computer setting.

As with the *high current channel*, these *low current channel* accuracy measurements in Fig. 6.5(b), show that less than the desired current is produced in cryogenic environments, which might be caused by the output offset voltage drift over temperature of the LM7101 op-amp.

6.2.2 Feedback Monitor Accuracy

The current feedback monitor values, I_{FB} , were also recorded. These values were compared to the actual measured multimeter measurements, I_{MM} , from a calibrated channel. Fig. 6.6(a) shows the difference of these two signals at room temperature, which is calculated by

$$Feedback\ Deviation = I_{FB} - I_{MM}. \quad (6.3)$$

The same measurements were taken in cryogenic environments in Fig. 6.7.

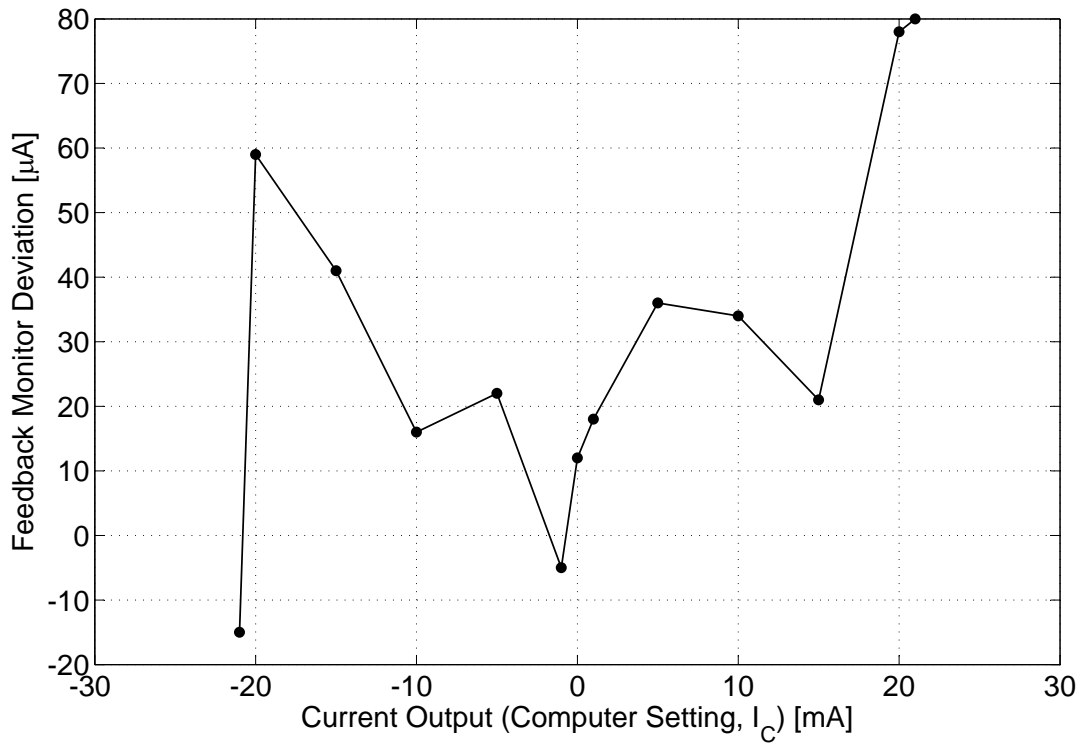
Fig. 6.6(b) and Fig. 6.7(b) show the accuracy of the current feedback monitor calculated by

$$\begin{aligned} I_{FB\ Accuracy} &= 100 - Error \\ &= 100 - \left(\frac{I_{FB} - I_{MM}}{I_{MM}}\right)100. \end{aligned} \quad (6.4)$$

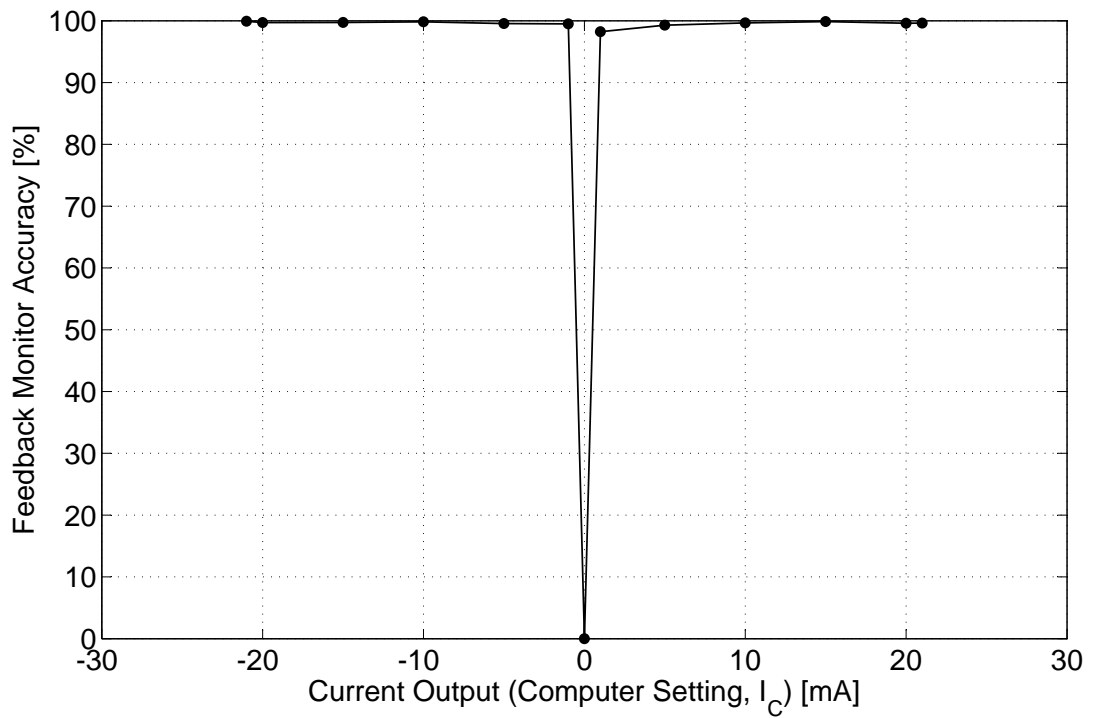
The 0% accuracy in Fig. 6.6(b) at 0 mA is caused by $I_{FB} = 24\mu A$ and $I_{MM} = 12\mu A$ where the difference between them is exactly equal to I_{MM} .

An R_L value of 51 Ω was connected to the output as part of these measurements. The measurements greater or equal to 20 mA are less accurate, because for these values, the multimeter can only give readings in steps of 0.1 mA.

The deviation of the feedback monitor results, measured in the cryocooler, increases with larger output currents. It is assumed that this is caused by the output offset voltage drift with temperature of the op-amps. Another probability is that the references, discussed in Subsection 4.1.2, could also drift, causing a lower than expected reading on the ADC devices. These devices are specified to drift with 20 ppm/ $^{\circ}C$, which would cause a 10 mV decrease on 2.5 V over a 200 $^{\circ}C$ temperature range.

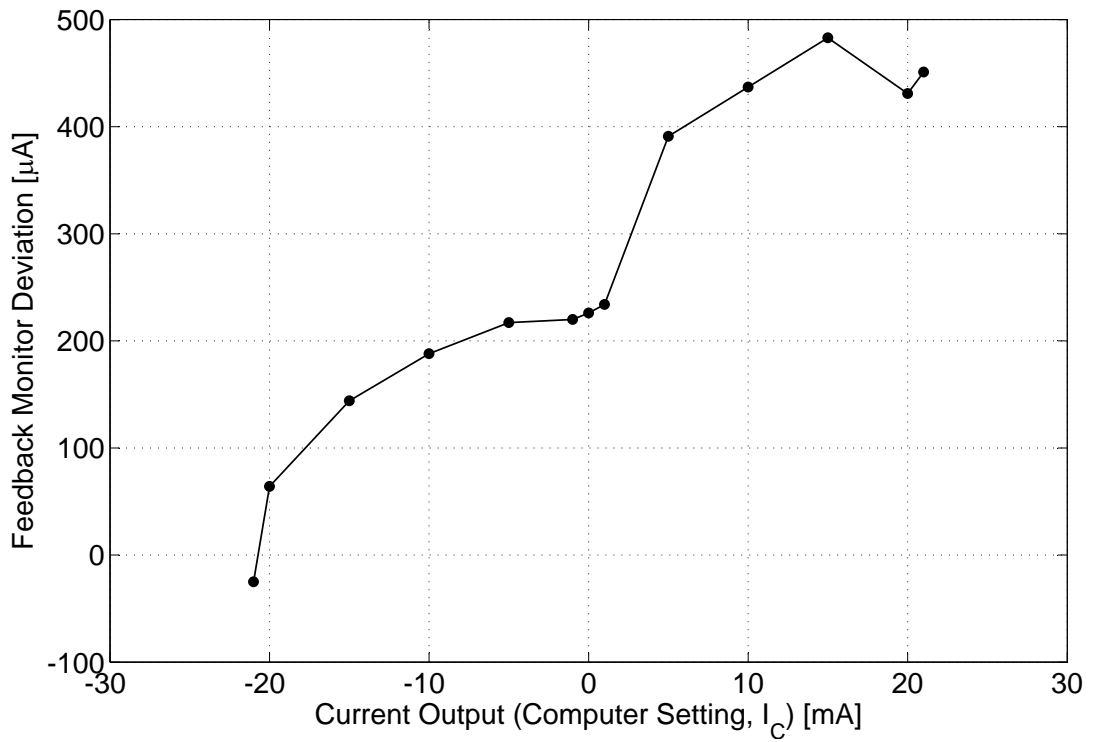


(a) Deviation

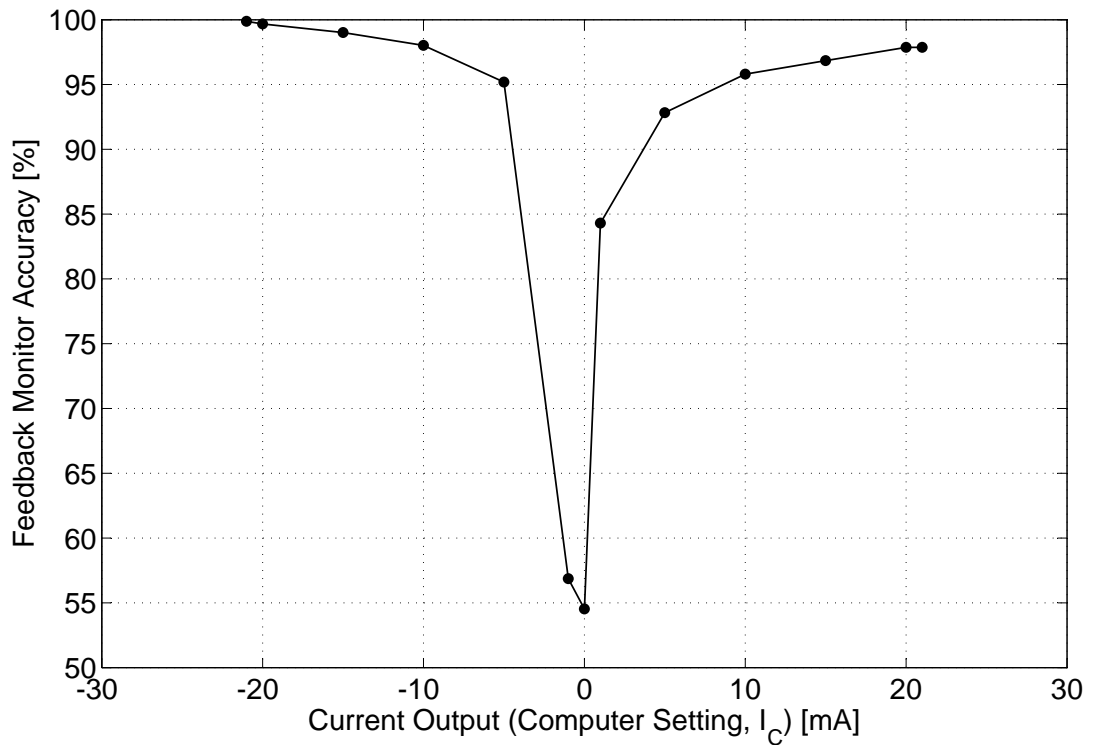


(b) Accuracy

Figure 6.6: The feedback monitor (a) deviation from actual measurement, and (b) accuracy at 300 K.



(a) Deviation



(b) Accuracy

Figure 6.7: The feedback monitor (a) deviation from actual measurement, and (b) accuracy at 85 K.

6.2.3 Oscilloscope Measurements

An oscilloscope measurement was also taken and is shown in Fig. 6.8. It shows the oscilloscope measurement of a repeated '01' bit-pattern, sent on the current output channel. The minimum and maximum values were set to be ± 21.6 mA. The minimum and maximum amplitudes of the output channels can be set independently and does not need to be symmetrical around 0 as in the following test procedure. The current channel was connected to $R_L = 51\Omega$ with the probes measuring the voltage over R_L .

The frequency of this two-bit bit-pattern is measured to be 2.155 kHz which indicates a bit frequency of 4.31 kHz. This is lower than the simulated timing frequencies in Subsection 5.2.1.6, because at this stage of the testing procedures, the SPI setting on the firmware was not yet set to its maximum frequency.

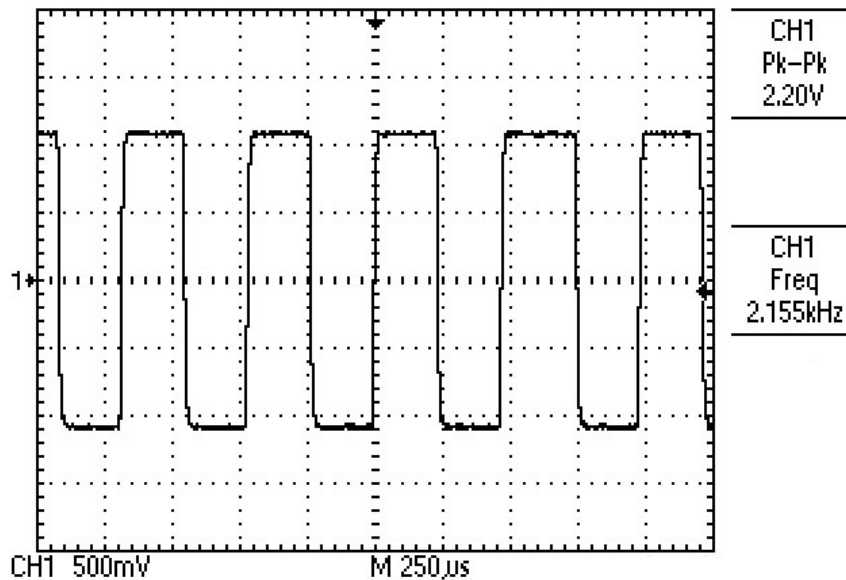


Figure 6.8: ± 21.6 mA bit-pattern sent on the current channel.

From this measurement the current can be calculated by using the maximum value of $2.2/2 = 1.1V$ by

$$\begin{aligned}
 I_{Out} &= \frac{V}{R} & (6.5) \\
 &= \frac{1.1 \times 10^3}{51} \\
 &= \pm 21.568 \text{ mA}.
 \end{aligned}$$

6.3 Low Voltage Output Channels

6.3.1 Linearity and Accuracy

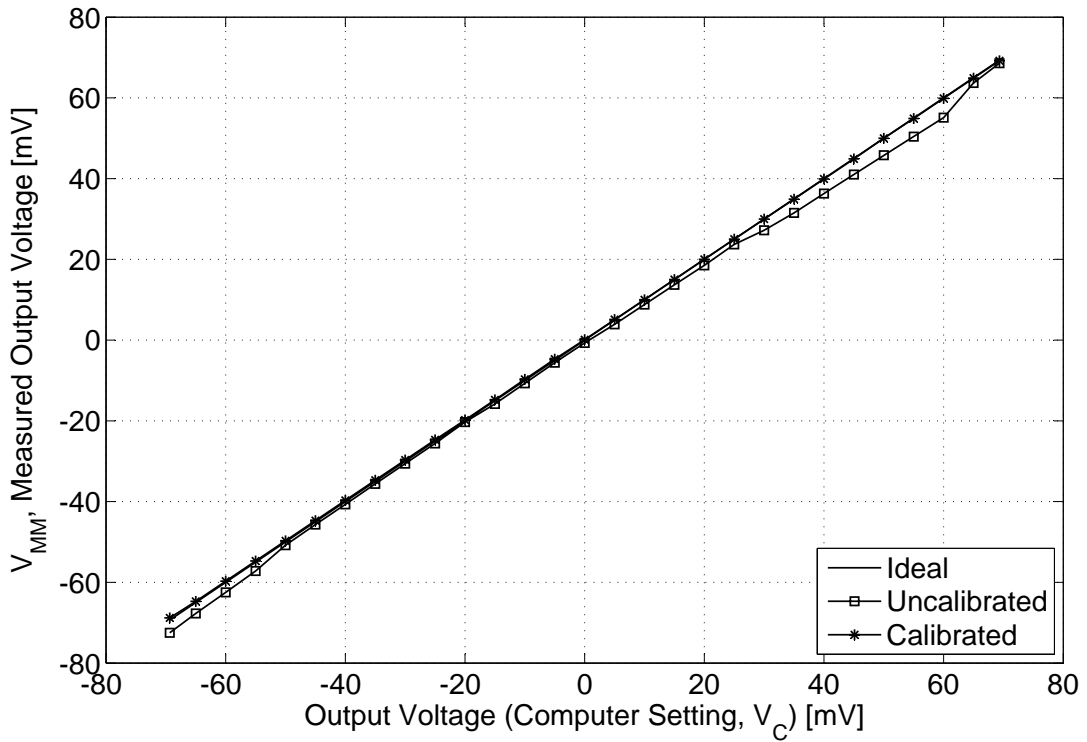
The same type of tests were done on the *low voltage channels* as with the *low current channels*. The multimeter that was used to measure these results can only measure in steps of 0.1 mV.

The linearity tests are shown in Fig. 6.9(a) and Fig 6.10(a). Uncalibrated channel output values as well as calibrated channel output values are presented. A slight offset can be seen by the uncalibrated data plot in room temperature conditions, whereas in cryogenic environments, the uncalibrated channel offset is less than the calibrated measurements. The reason for this is that the feedback monitor circuits have the same offset effect as the output channels and does not detect the real offset of the channel. This could also be caused by offset voltage drift of the op-amps or references at low temperatures.

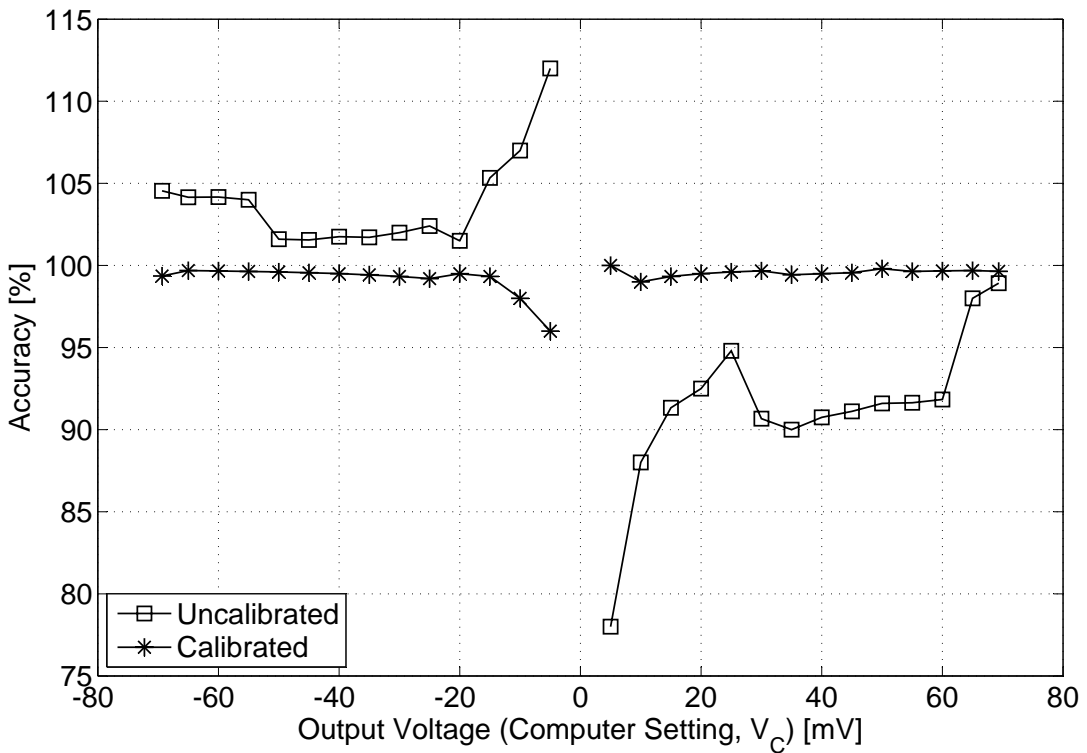
The accuracy plot in Fig. 6.9(b) shows the negative offset of Fig. 6.9(a) more clearly. These values are calculated by

$$V_{OutAccuracy} = \left(\frac{V_{MM}}{V_C}\right)100, \quad (6.6)$$

where V_{MM} is the multimeter measurement and V_C is the computer setting.

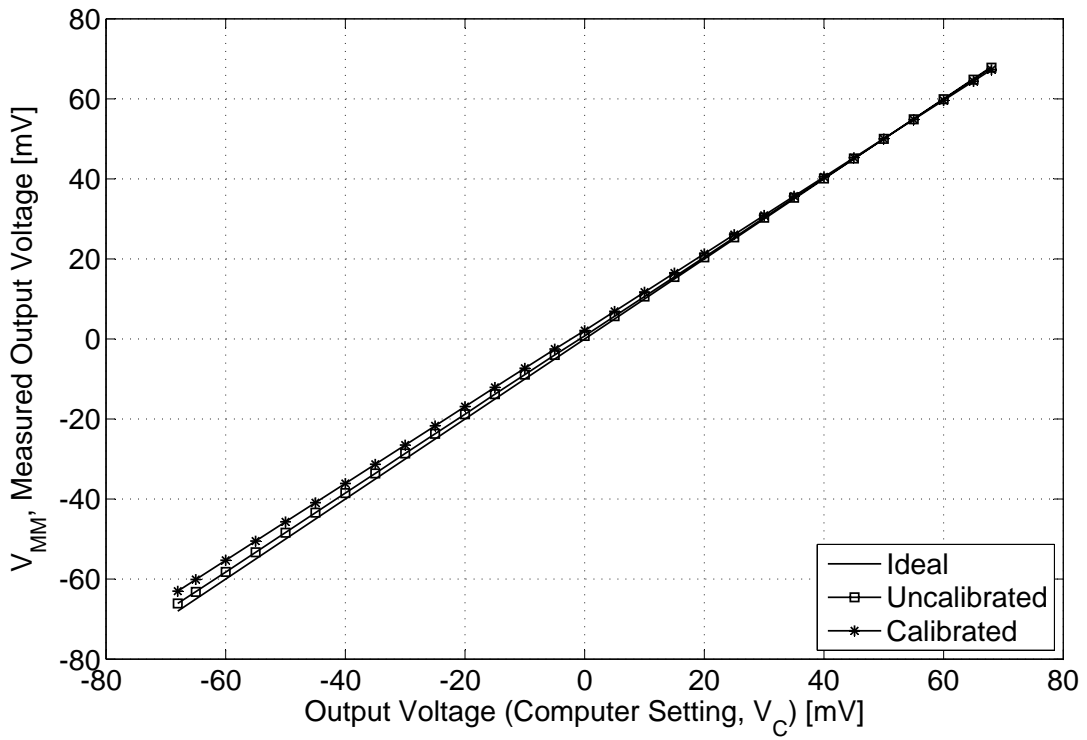


(a) Linearity

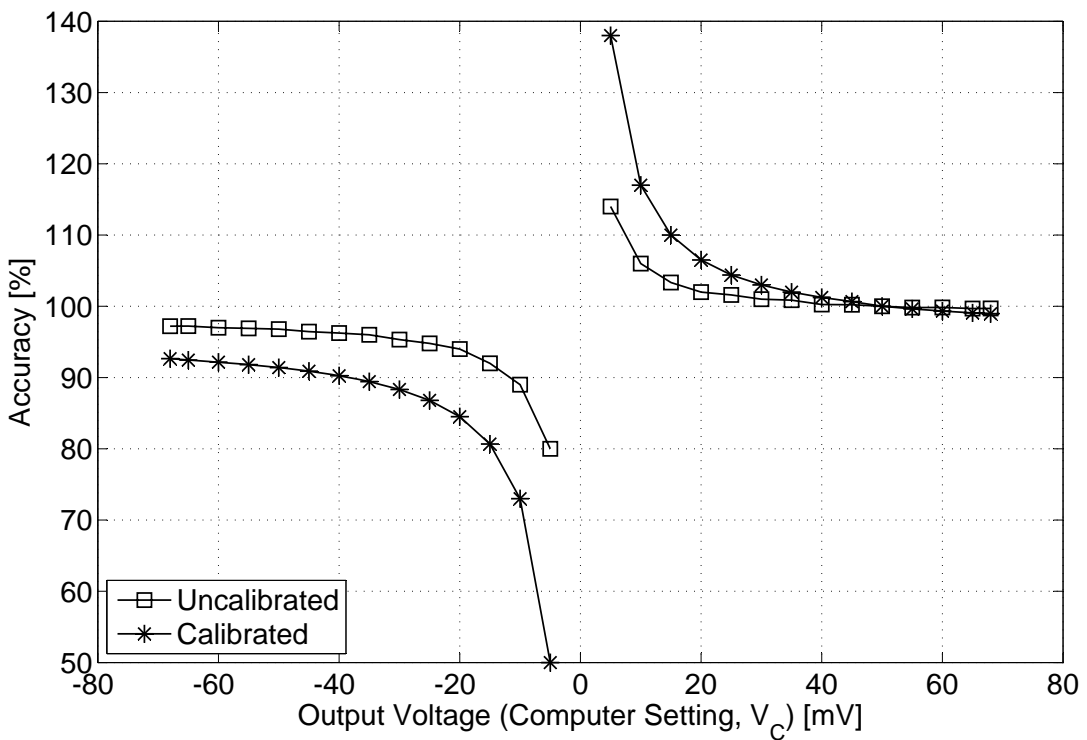


(b) Accuracy

Figure 6.9: The (a) linearity and (b) accuracy of the low voltage channel outputs at 300 K.



(a) Linearity



(b) Accuracy

Figure 6.10: The (a) linearity and (b) accuracy of the low voltage channel outputs at 85 K.

6.3.2 Feedback Monitor Accuracy

The voltage feedback monitor results at room temperature conditions can be seen in Fig. 6.11, while the measurements done in the cryocooler are presented in Fig. 6.12. The voltage feedback, V_{FB} , is compared to the multimeter measurement, V_{MM} , where the deviation is calculated by

$$\text{Feedback Deviation} = V_{MM} - V_{FB}. \quad (6.7)$$

These results are shown in Fig. 6.11(a) and Fig. 6.12(a). An offset on the feedback measurements of up to $500 \mu\text{V}$ at room temperature can be seen at the lower negative output values. The feedback op-amps might have a slightly larger offset at negative values which could cause this effect. This error is enlarged in cryogenic environments which would explain the inaccurate calibration on this channel, shown in Fig. 6.10(a).

With the V_{MM} offset value equal to 0, the accuracy of the feedback is calculated by

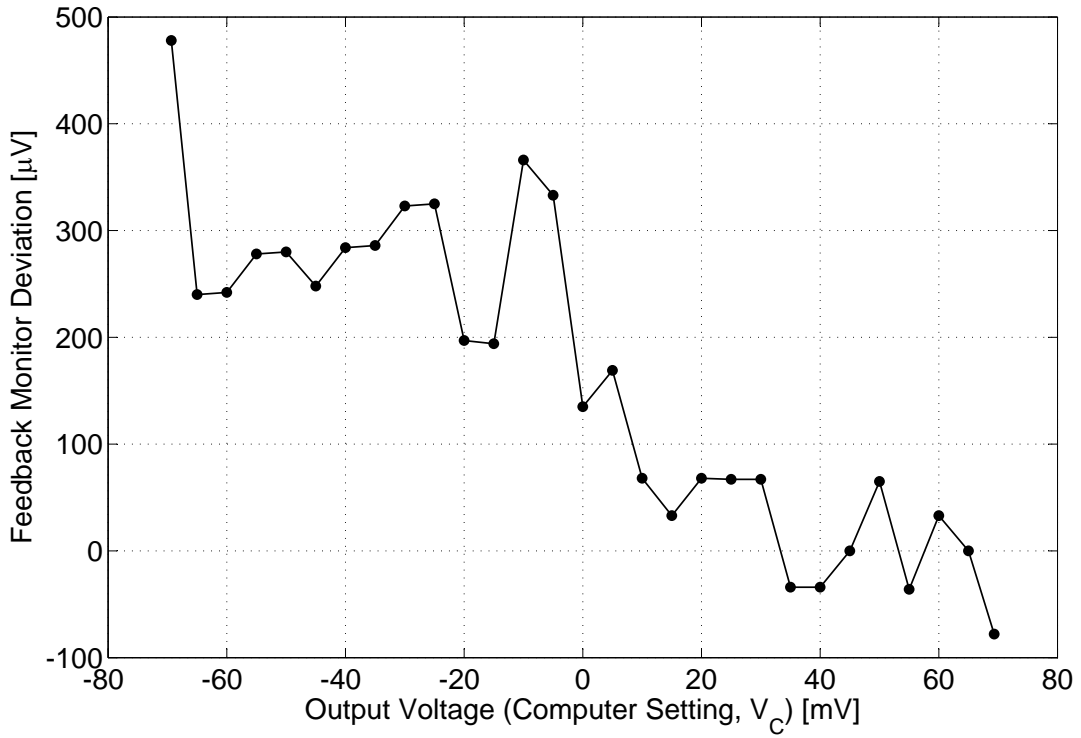
$$\begin{aligned} V_{FB \text{ Accuracy}} &= 100 - \text{Error} \\ &= 100 - \left(\frac{V_{FB} - V_{MM}}{V_{MM}} \right) 100 \end{aligned} \quad (6.8)$$

and is displayed in Fig. 6.11(b).

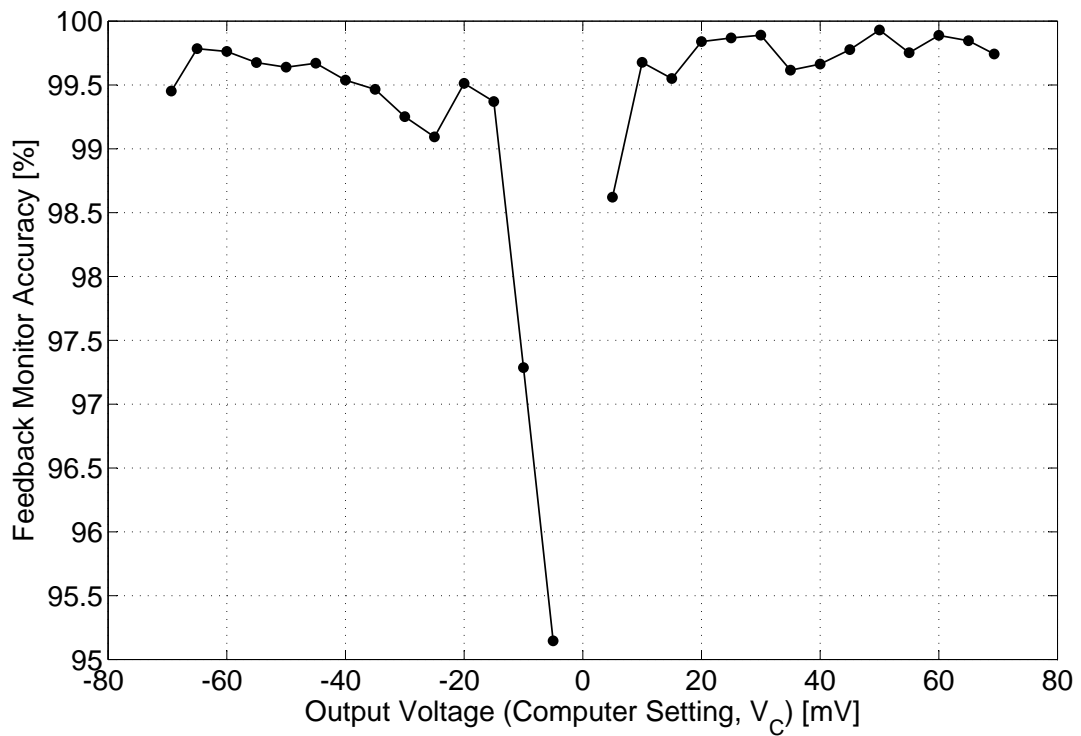
As mentioned, the multimeter only measures in steps of 0.1 mV. This would explain the slightly less accurate values near 0 mV in Fig. 6.11(b) and 6.12(b). As V_{MM} reaches 0 mV, any slight deviation in V_{FB} would cause a larger error calculation.

If the offset drift is known at specific temperatures, this could also be calibrated out in the software module of the control system.

The feedback system is used to calibrate the offset of the output channels, but the feedback op-amps might have a slight offset themselves. Thus, a more accurate feedback system with higher order ADCs and lower offset op-amps would also improve the calibration of these channels.

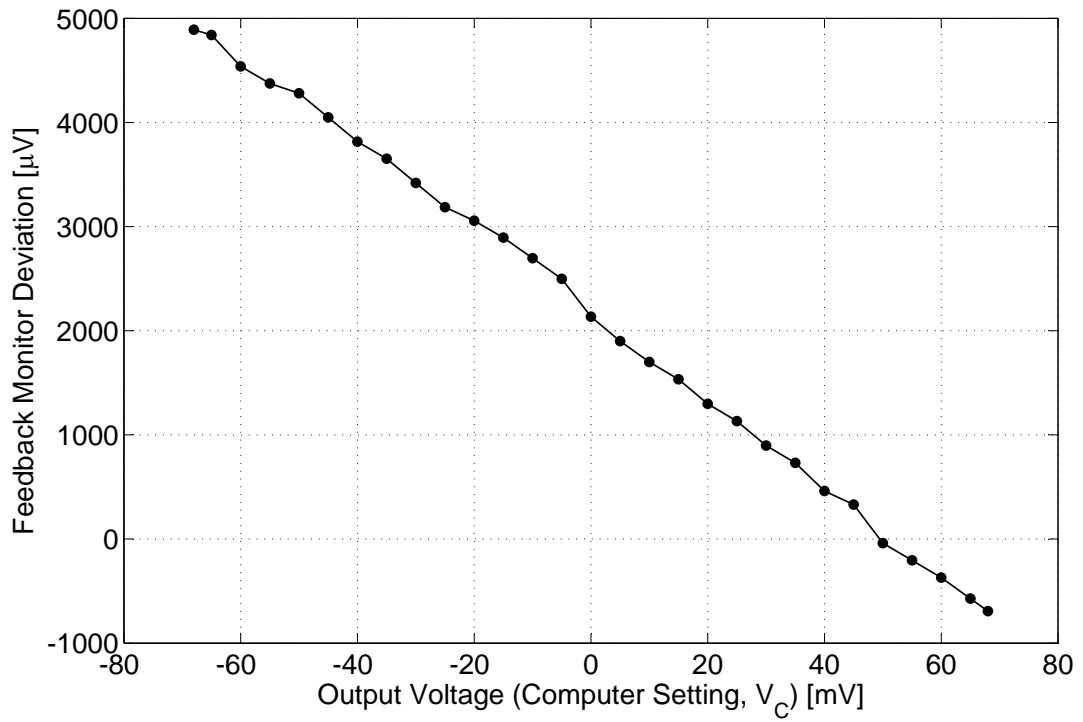


(a) Deviation

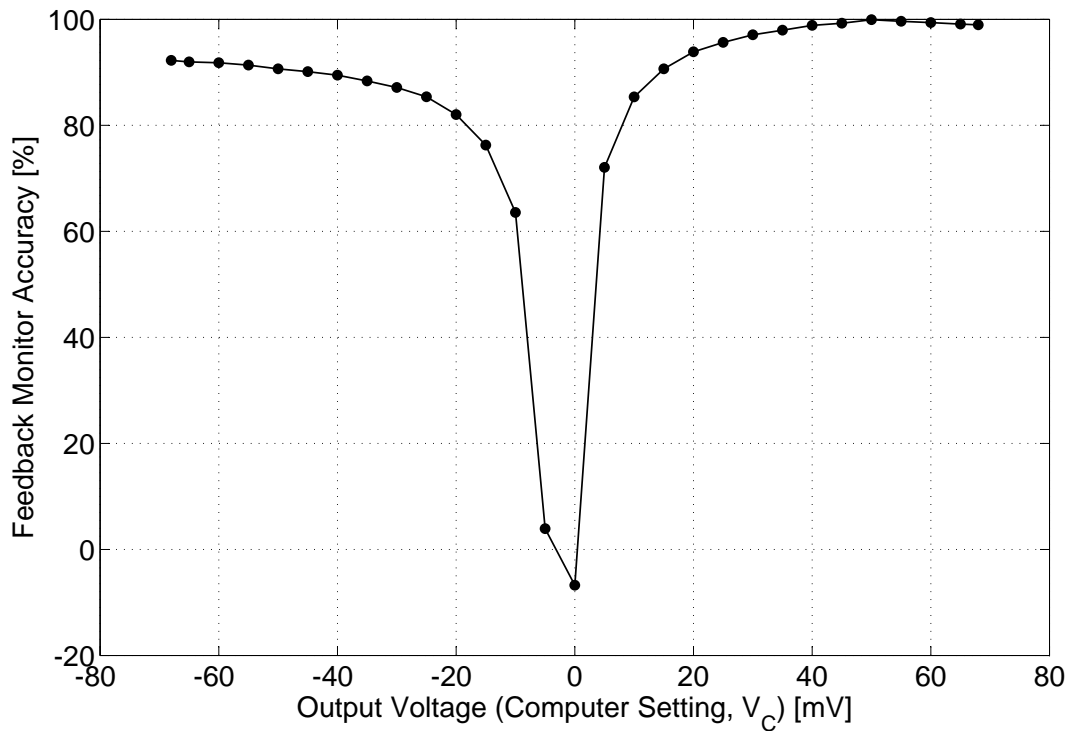


(b) Accuracy

Figure 6.11: The (a) deviation and (b) accuracy of the low voltage output feedback monitor at 300 K.



(a) Deviation



(b) Accuracy

Figure 6.12: The (a) deviation and (b) accuracy of the low voltage output feedback monitor at 85 K.

6.3.3 Oscilloscope Measurements

A sequential bit-pattern of 0 and 1 was transmitted on the voltage output channel. Its minimum and maximum values were set to ± 70 mV. Again, the minimum and maximum amplitudes of the output channels can be set independently and does not need to be symmetrical around 0 as in the following test procedure. The oscilloscope measurement of this signal is shown in Fig. 6.13. When measuring small signals like these, the oscilloscope adds its own internal noise of about 3 mV to the signal as can be seen on top of the square wave. That is why the signal is a bit larger than the set value.

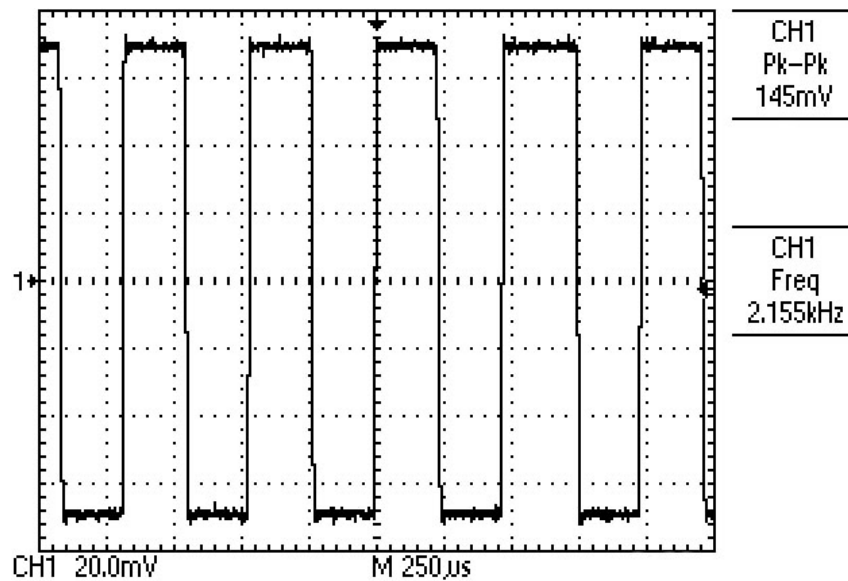


Figure 6.13: ± 70 mV bit-pattern on the voltage output channel.

The frequency of this signal is measured at 2.155 kHz.

6.4 High Sensitivity Voltage Input Channels

The results for the *high sensitivity voltage input channel* are only given for measurements taken in room temperature conditions. The INA322 instrumentation amplifiers, implemented on the input channels, latched to the positive rail at temperatures below 150 K. Therefore measurements on this channel could not be performed at 85 K.

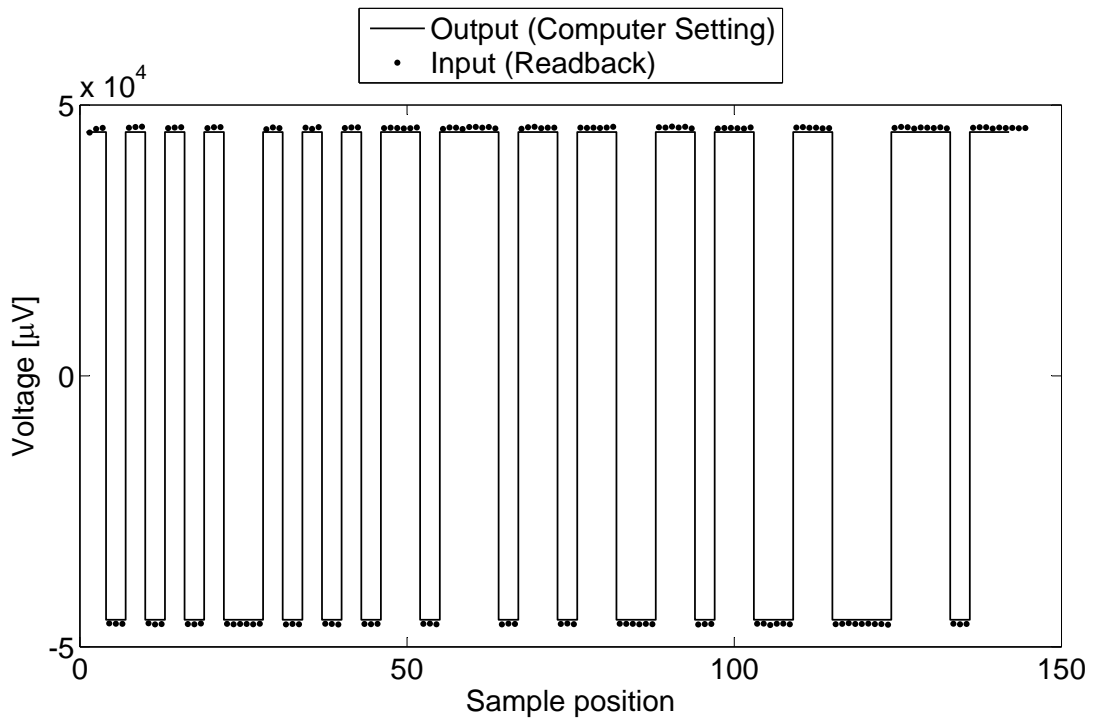
Room temperature measurements were done on a calibrated input channel. An output channel of the control system was set to produce a bit-pattern at two different amplitudes as shown in Fig. 6.14, with the output data frame size set to 6 bytes. This output channel was then connected to the input channel for data measurements.

For each test, the minimum and maximum output values were set to $\pm 45\,000\ \mu\text{V}$ and $\pm 1\,000\ \mu\text{V}$ respectively. Again, the minimum and maximum amplitudes of the output channels can be set independently and does not need to be symmetrical around 0 as in these test procedures.

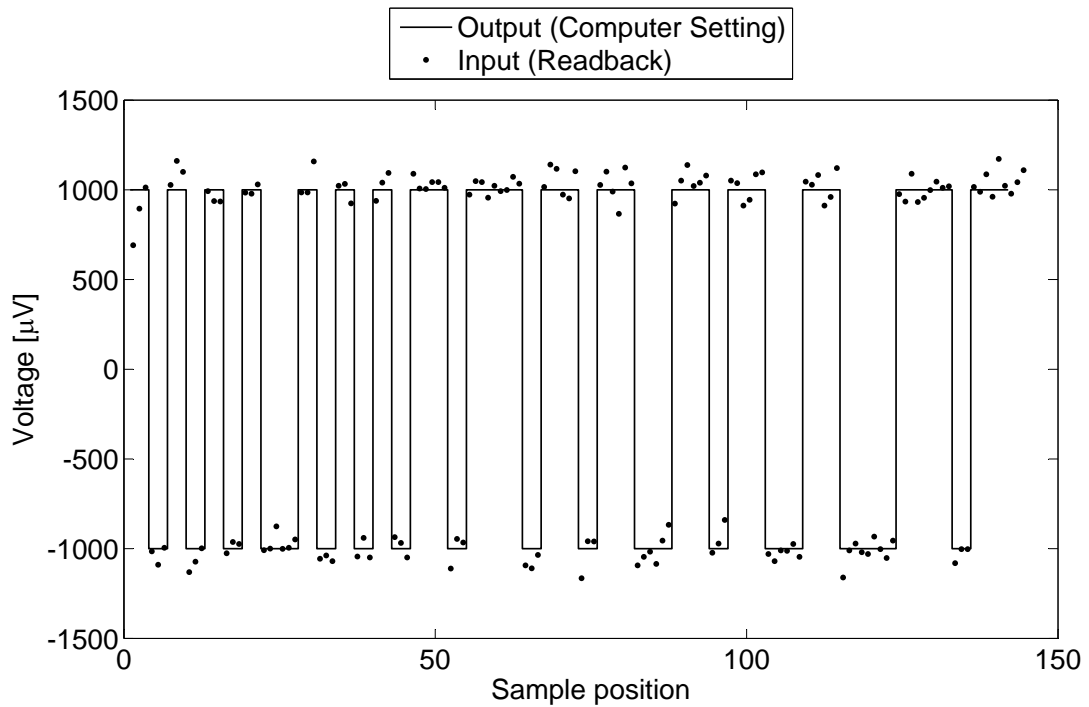
The input measurements were set to sample 3 values per output bit. These input values, along with the output values, were saved to a file and plotted in Matlab.

The input data values in Fig 6.14(a) represent the the input signal very accurately. Only slightly larger values than the settings on the output channel could be observed. The influence of noise could be observed with the smaller signal inputs as seen in Fig. 6.14(b) and Fig. 6.15. The control system was measured in an unshielded environment at room temperature.

Due to a design error on the input daughterboard, a critical error modification was done on the negative rail of the sensitive A/C converter. The necessary UCC284 negative regulator was not implemented as described in Subsection 4.1.1.1. Voltage division was done by two $100\ \Omega$ resistors to establish a negative voltage rail. This caused an unstable negative voltage rail and would explain the more than expected noise on the measurements.



(a) Hexadecimal logic data: 0xAA55BB66CC77



(b) Hexadecimal logic data: 0xAA55BB66CC77

Figure 6.14: *Input channel sampling of output channel bit-patterns, with different amplitudes of (a) $\pm 45\,000 \mu\text{V}$ and (b) $\pm 1\,000 \mu\text{V}$. Measurements were taken at 300 K.*

Fig. 6.15 shows the measurement of a grounded input channel at $0 \mu\text{V}$. Transient effects at the beginning of each frame measurement could be observed, where the ADC device has a DC offset of about $-500 \mu\text{V}$. This effect could either be corrected in software, or by disregarding the first few values of the ADC before taking a measurement on the input channel. The observed noise is less than $300 \mu\text{V}$.

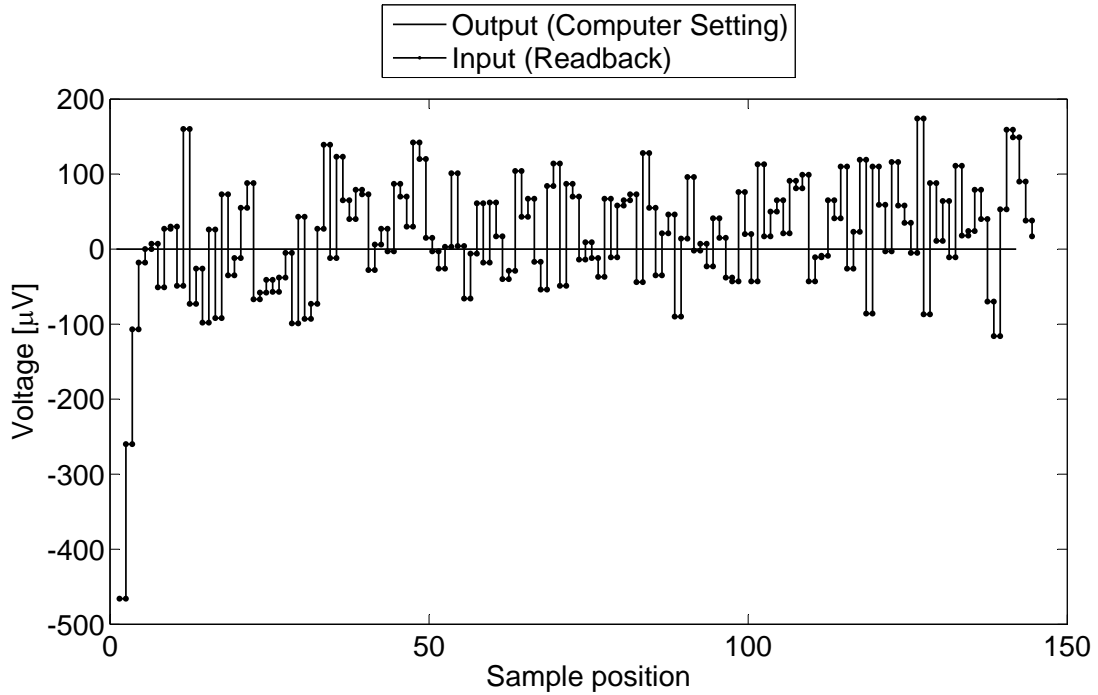


Figure 6.15: Grounded *input channel* measurement at 300 K.

6.5 Temperature Control System

The integrated heater and PT1000 temperature sensor was tested in the Gifford McMahon cryocooler to determine its effectivity. The 22Ω high power resistor heater and temperature sensor was placed directly on the cold finger of the cryocooler.

With the cryocooler in operation and the heater switched off, the temperature decreased at a rate of 3.49 K/min . When the heater was switched on, producing 1.14 W of power, the temperature decrease rate was measured to be only 1.74 K/min .

The effect of the heater was also measured as the cryocooler was switched off and warming up. With the heater switched off, the temperature rise rate was measured to be 0.6 K/min . The rise rate when the heater was switched on was measured to be 1.84 K/min . That means that the cryocooler will heat up 3 times faster when the heater is switched on.

With this cryocooler at a temperature of 85 K , the heater could increase the temperature of the control system at a rate of 1.75 K/min . A more effective temperature control system, which

produce more power, could be implemented by connecting the heater to the 6 V battery supply instead of the regulated 5 V supply. The power is calculated by

$$P = \frac{V^2}{R} \quad (6.9)$$

For even more heating power, a resistor with a lower resistance value could also be implemented.

6.6 Control System Power Usage

A quiescent current analysis of all the components for the different PCBs are given in Tables 6.2 to 6.7. The values were taken from the different datasheets of the devices.

Table 6.2: Current drawn by the regulators on the battery PCB.

Components	Qty	Typical [mA]	Maximum [mA]
LM2990	1	1.000	9.000
LP3872	1	5.000	15.000
INA322	2	0.120	0.140
Total		6.120	24.140

Table 6.3: Current drawn by the *motherboard*.

Components	Qty	Typical [mA]	Maximum [mA]
ATmega16	1	12.000	15.000
Ref3225 & Ref3212	2	0.200	0.240
MAX398	2	0.002	0.002
MAX186	2	0.200	0.240
ADS8325	1	0.900	1.500
ADG619	1	0.001	0.001
LMC7101	3	0.300	0.360
INA322	1	0.060	0.070
Total		13.663	17.413

Table 6.4: Current drawn by the *high current daughterboard*.

Components	Qty	Typical [mA]	Maximum [mA]
DAC8555	1	0.650	0.950
LMC7101	4	2.000	3.800
Total		2.650	4.750

Table 6.5: Current drawn by the *low current and voltage daughterboard*.

Components	Qty	Typical [mA]	Maximum [mA]
DAC8555	1	0.650	0.950
MAX186	1	0.100	0.120
LMC7101	28	14.000	26.600
ADC619	12	0.012	0.012
Total		14.762	27.682

Table 6.6: Current drawn by the *voltage input daughterboard*.

Components	Qty	Typical [mA]	Maximum [mA]
LMC7101	2	0.200	0.240
ADS8325	2	1.800	3.000
INA322	2	0.120	0.140
Total		2.120	3.380

Table 6.7: Current drawn by other devices.

Description	Current [mA]
Resistors connected to ground	0.590
PT1000 (when enabled)	0.378
Heater (when enabled)	227.27
Total	228.238

Current measurements were taken of the control system and are given in Table 6.8.

Table 6.8: Measured currents of the *cryogenic CMOS-based control system*.

Board	Positive Rail [mA]	Negative Rail [mA]
Battery PCB and motherboard	18.6	0.2
High current daughterboard	3.4	2.8
Low current and voltage daughterboard	14.3	18.4
Voltage input daughterboard	28.4	30.1
Total	64.7	51.5

The measured current values correspond with the theoretical current values of the datasheets. The only deviation is found on the voltage input daughterboard. As mentioned, a design error on the PCB forced the designer to do a critical error modification. The necessary UCC284 negative regulator was not implemented as described in Subsection 4.1.1.1. Voltage division was done by two 100 Ω resistors to establish a negative voltage rail. This modification causes the large current consumption of the voltage input daughterboard.

The total power drawn by the quiescent control system with each board type implemented would then be

$$P = VI \quad (6.10)$$

$$\begin{aligned} P_P &= 6 \times 0.0647 \\ &= 388.2 \text{ mW} \end{aligned} \quad (6.11)$$

$$\begin{aligned} P_N &= 6 \times 0.0515 \\ &= 309.0 \text{ mW}, \end{aligned} \quad (6.12)$$

where P_P is the power drawn from the positive power rail and P_N is the power drawn from the negative power rail.

6.7 Conclusion

In this chapter the cryogenic CMOS-based control system was put through accuracy and linearity tests at room temperature as well as in cryogenic environments. All the channel types were measured and displayed here.

The *high current channel* gives a linear output from 100 mA to the maximum designed 500 mA with great accuracy. With the current values below the 30 mA setting, the output shows a non-linear response.

The designed *low current output channel* is very linear with great accuracy. The positive current maximum limits are suppressed though and will only give up to 22 mA, which is 3 mA less than designed for.

The low *voltage output channel* has a small negative offset, but is adjusted well by the feedback calibration system at room temperature. The output of this channel is also quite linear.

The outputs of these channels are all slightly lower than expected in cryogenic environments, but are still quite accurate.

The feedback monitor systems of the current as well as the voltage channels are reasonably accurate at room temperature, but shows larger offsets in cryogenic environments. For greater accuracy, a 16-bit feedback ADC with less offset could be implemented.

Accurate *input channel* values are displayed. Only about 280 μV noise is detected on the input which is caused by unshielded control system measurements and the effect of an unstable negative rail.

The implemented heater effectivity was measured and shown. The tests and results chapter is concluded by a current and power analysis drawn by the control system.

Chapter 7

Conclusion, Recommendations and Future Prospects

In this chapter conclusions are made about the design of the *cryogenic CMOS-based control system*. Recommendations for improving the control system are also given. This chapter ends with a discussion of the future prospects for testing SCE devices at the University of Stellenbosch.

7.1 Conclusion

This thesis presents the design and development of a *cryogenic CMOS-based control system*. A complete USB compatible hardware system with several input and output channels was developed. This was developed using off-the-shelf CMOS components to implement a computer controlled test facility for SCE circuits such as RSFQ and COSL technology.

The appropriate firmware for the ATmega16 microcontroller was developed to implement the hardware of the control system. A user can control this hardware by means of a specially developed graphical user interface software package.

A list of the fulfilled specifications for the control system is given below:

- Adjustable positive and negative high current output channels were developed, delivering up to ± 500 mA of current in incremental steps of $10 \mu\text{A}$.
- Adjustable bipolar low current output channels, delivering approximately $\pm 22\,000 \mu\text{A}$ in incremental steps of $0.8 \mu\text{A}$, were developed for sending DC or logic signals to SCE circuits.
- Adjustable bipolar low voltage output channels between $\pm 70\,000 \mu\text{V}$ were developed for sending DC or logic signals to SCE circuits in steps of $2 \mu\text{V}$.
- High sensitivity bipolar voltage input channels were developed to measure $\pm 50\,000 \mu\text{V}$ input signals from SCE devices. With the proper design, the sensitivity of these channels would be less than $20 \mu\text{V}$.

- Reasonably accurate calibration systems were created for calibrating all the low power output and input channels.
- A graphical user interface was created to control the SCE tests from a computer.
- The user interface connects with the control system hardware at a speed of 1 Mbaud via a USB port that was implemented with a USB-RS232 converter.
- Fibre optical communication connections were installed to shield the control system from HF noise from the computer or any external power sources.
- Various devices were tested at 70 K and were implemented in the control system.
- An accurate temperature sensor and on-board heater for temperature control was implemented.
- The control system was implemented to operate from a battery source to reduce external noise.
- Battery voltage and current sensing were also done to indicate the battery status of the control system.

Although the control system was designed to operate in cryogenic environments, it could not be used at those low temperatures. The reason for this is because the 1st stage of the cryocooler is too small to contain the designed control system. It could be implemented in a specially designed container that extends the cryocooler. By placing the control system in this extension of the cryocooler, as described in Chapter 5, it could be used to test RSFQ and COSL circuits at the University of Stellenbosch. The heating problem, stipulated in Chapter 2, is overcome by using long, thin wires that are thermally grounded to the cooling stages of the cryocooler at 60 K, ± 35 K and then at 4 K respectively.

Tests on SCE devices could not be performed because the cryocooler does not yet have the proper EM shielding that is necessary.

7.2 Recommendations

A few recommendations are made in designing an improved SCE test control system for future purposes.

- For attaining faster transfer speeds between the computer and the control system, a microprocessor that can handle full USB speeds could be implemented. For faster interfacing frequencies with SCE devices, the microprocessor could be programmed in assembler to reduce the large processing time caused by the overhead high level language. A faster external clock or crystal could also be used for faster processing times. The possibility

of implementing an FPGA device could also be researched to see if greater testing speeds could be achieved.

- Fibre optical cables electrically isolates the control system. It is recommended that these cables be used for shielding the control system from HF noise from the computer or any power sources.
- In order to eliminate any large voltage or current spikes with a system start-up, a safety ground switch should be implemented on the output channels (as discussed in Subsection 4.8.2).
- In overcoming the starting value offset of the *high current source*, a new PMOS *high current source* could be implemented (as discussed in Subsection 4.7.2).
- The op-amps used in the offset calibration feedback systems have their own offset values, causing slightly inaccurate calibrations. More accurate devices could be implemented for this functionality with higher resolution ADCs and op-amps with less offset on the outputs.
- A battery measurement system could be implemented on the outside of the cryocooler, directly on the battery box with its own processor. Thereby the batteries could be measured without interfering with the communication of the control system. It would also increase the processing power of the control system. The values of the battery voltage and currents could be displayed on an LCD screen.

A few more recommendations can be made when designing any further electronic systems for operation in cryogenic environments.

- BeCu is a strong alloy that keeps its conductivity and flexibility at low temperatures. These alloys can be used for spring contacts in connectors in cryogenic environments.
- The PT1000 thin film temperature sensor, without the stainless steel sheathing, can be implemented at very low temperatures. In order to measure this sensor, a 4-wire measurement system should be implemented to eliminate lead resistance that influence the measurements.
- The internal RC clock of the ATmega16 does not produce a stable clock frequency at low temperatures, therefore an external clock is advisable.
- Although the INA322 is specified to be a CMOS device, it does not function well at cryogenic temperatures. Another operational amplifier should be researched or designed to operate at lower temperatures.
- The tantalum SMT capacitors were used throughout this design because of its small package size and stability in cryogenic environments. The axial polyester type capacitors, which

also performed well in cryogenic environments (Fig. 3.13), were too large to implement on the small surface mount PCB structure. However, WIMA [36] fabricates small SMT metallised polyester capacitors. These polyester capacitors could perform very well in cryogenic environments. These specific capacitors were difficult to obtain and were therefore not tested in cryogenic environments. Because of its small package size and predicted stability in cryogenic environments, it is recommended to test these capacitors for future implementation in cryogenic environments.

7.3 List of Contributions

A list of contributions made by this thesis is given below:

- This thesis contributes to the superconducting interface environment by presenting the first detailed specification list for a computer controlled testing facility for RSFQ and COSL circuits. This is a stepping stone for developing more refined specifications for testing SCE circuits.
- A computerized control system was developed for easy interface and testing of SCE devices.
- A system was developed, allowing up to 12 low current/voltage output channels and up to 6 high sensitivity voltage input channels to interface and test RSFQ logic circuits at cryogenic environments.
- Valuable tested SCE data can be saved in electronic format.
- A calibration of the PT1000 temperature sensor was done between 6 K and 300 K.

7.4 Future Prospects

Currently, research at the University of Stellenbosch includes experimentation with different types of CMOS technologies in order to implement amplifiers directly at 4.2 K. Specific technologies that are explored are HiCMOS II [21], and CMOS fabrication processes below $0.35 \mu\text{m}$ [20]. The p-HEMT transistors [37] are also considered in interfacing RSFQ circuits at 4.2 K.

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Appendix A

PCB Designs

The PCB designs for the *cryogenic CMOS-based control system* are given in this appendix. The schematics as well as the PCB layouts were done in *Protel DXP*.

A.1 Schematics

The following section contains the designed schematics of the control system. Included are the battery and power board schematics, the *motherboard* schematics with sub-schematics, all the daughterboard schematics and the *FTDI USB-RS232* optical fibre converter schematics.

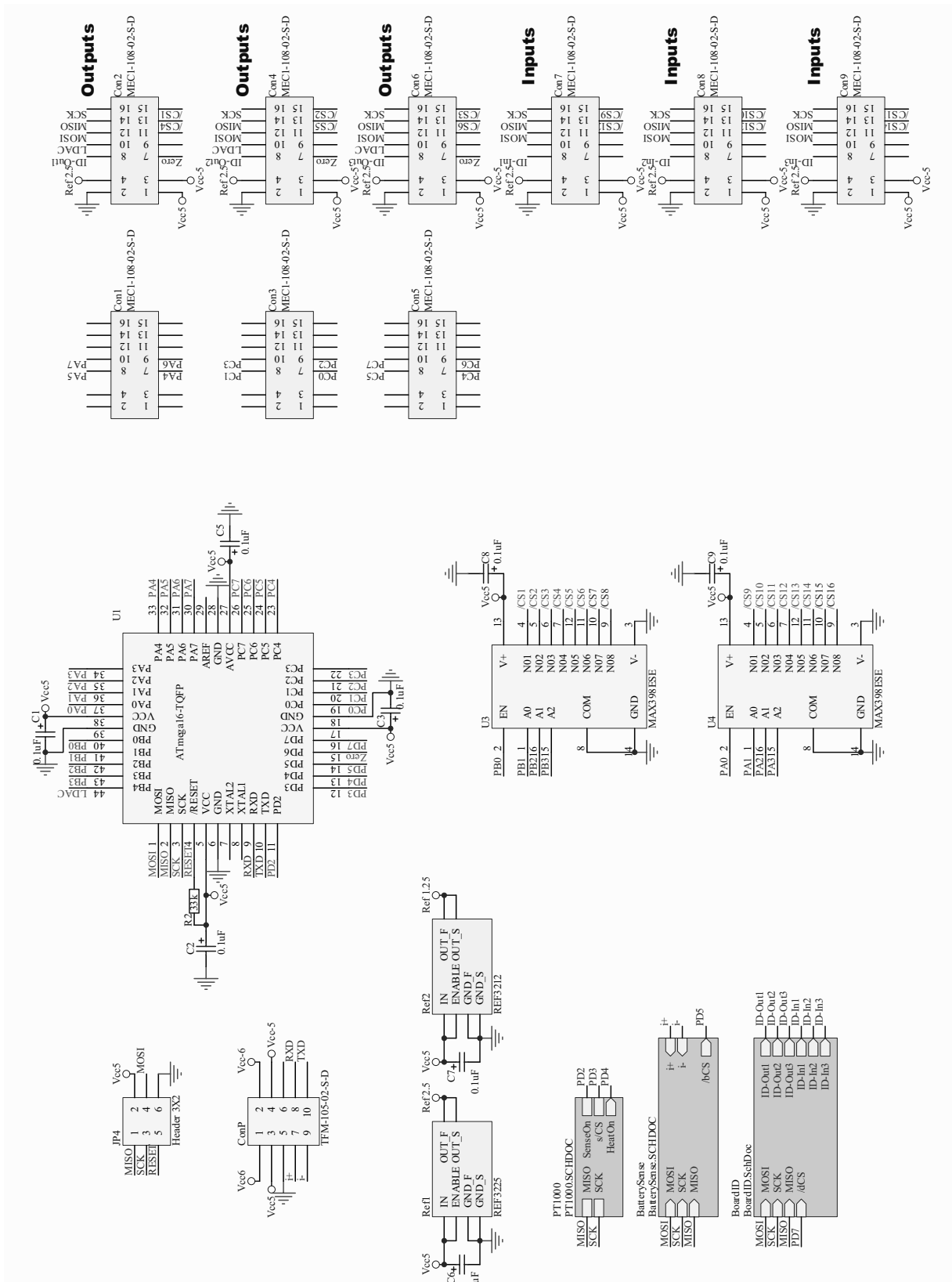
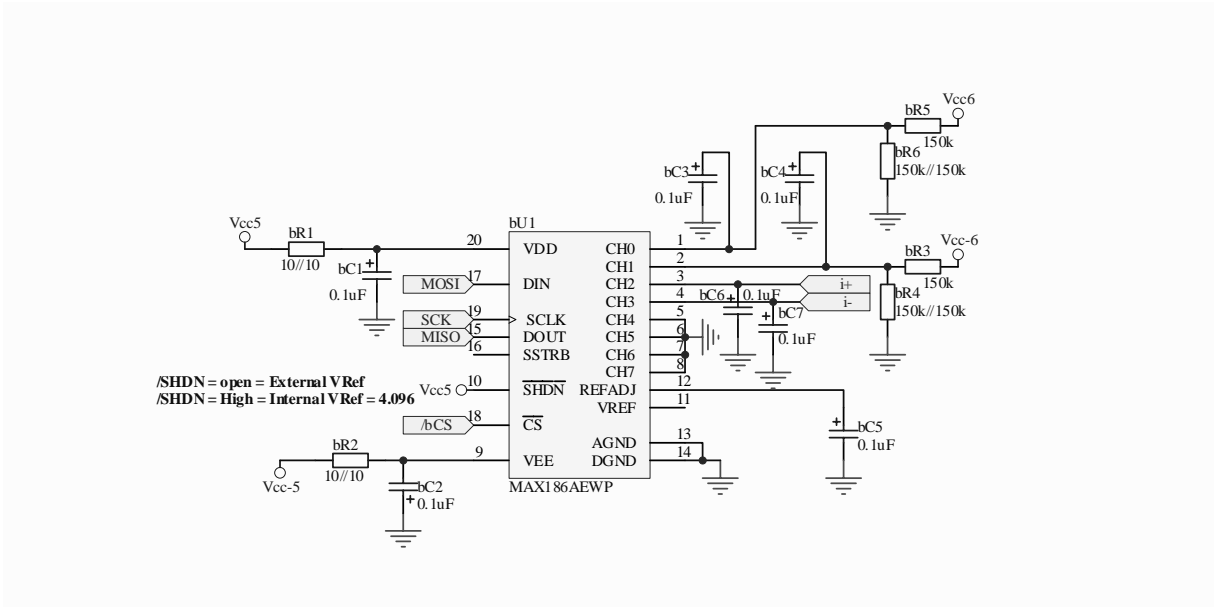
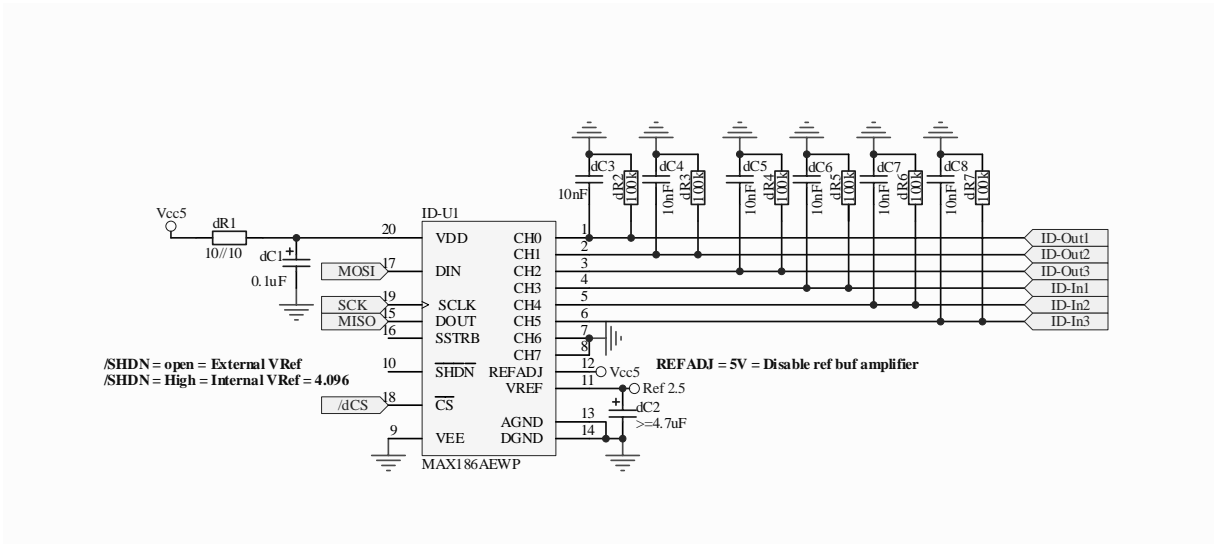


Figure A.2: The motherboard PCB schematic, including 3 sub-schematics.

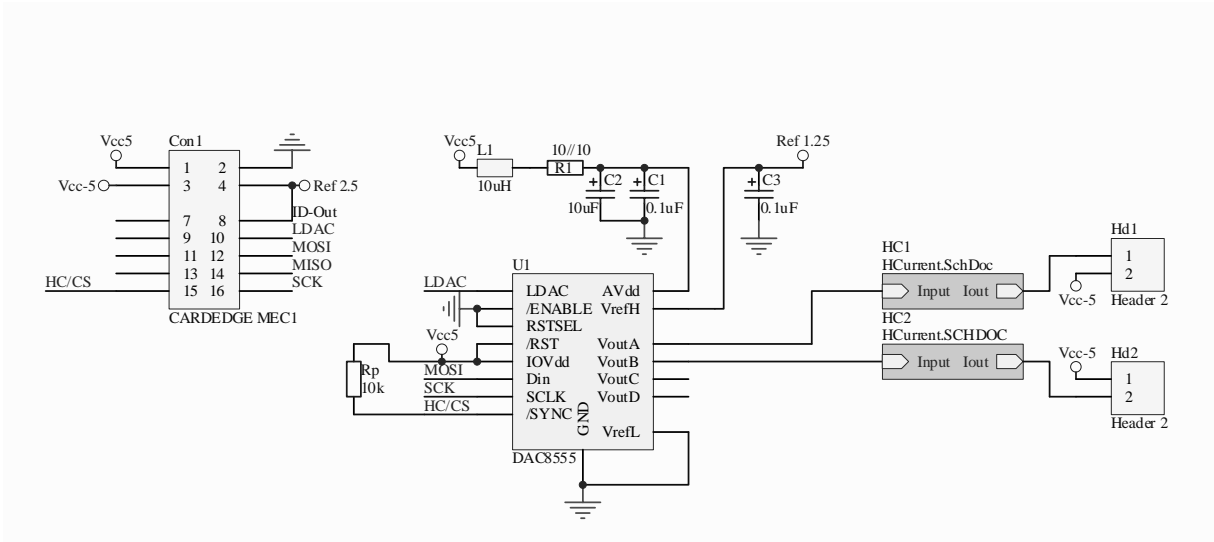


(a) BatterySense

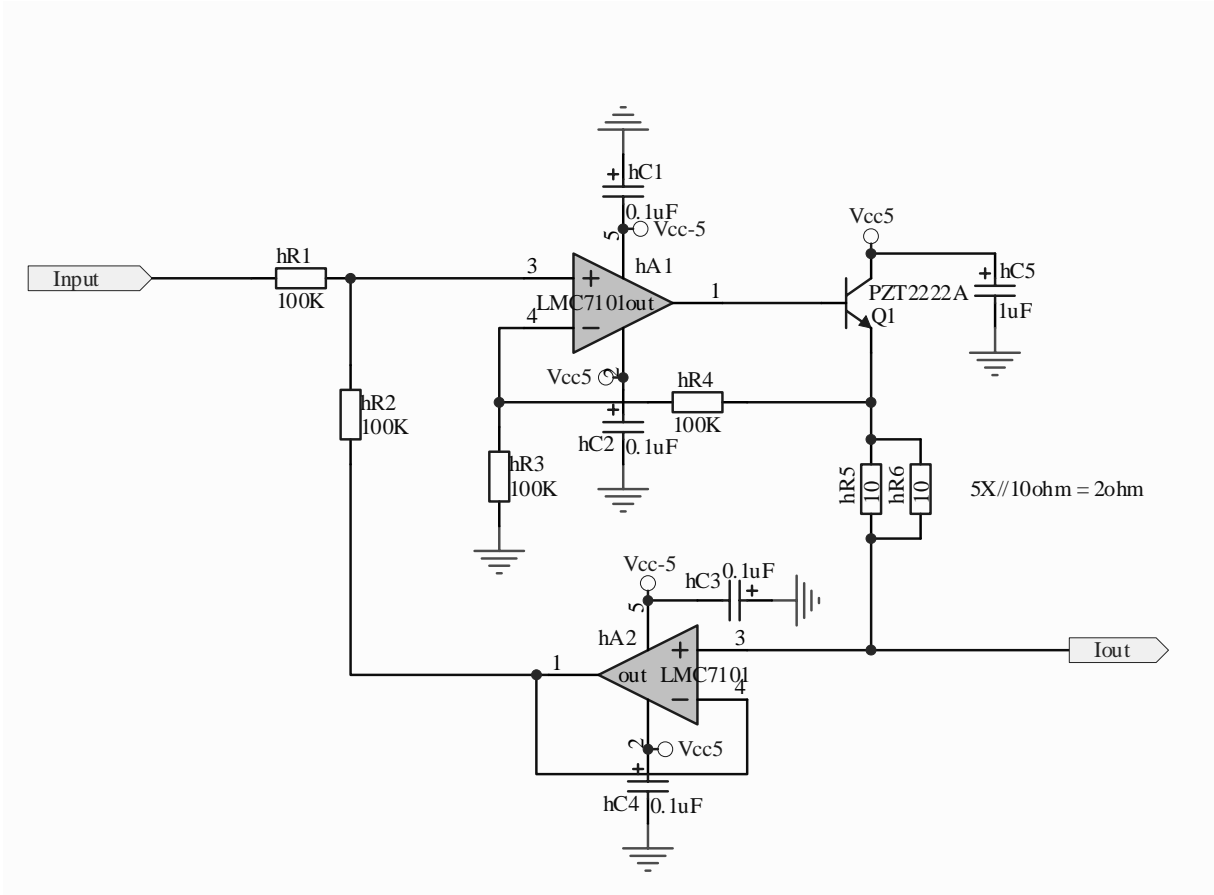


(b) BoardID

Figure A.3: The (a) *BatterySense* and (b) *BoardID* sub-schematics included on the *motherboard* schematic.

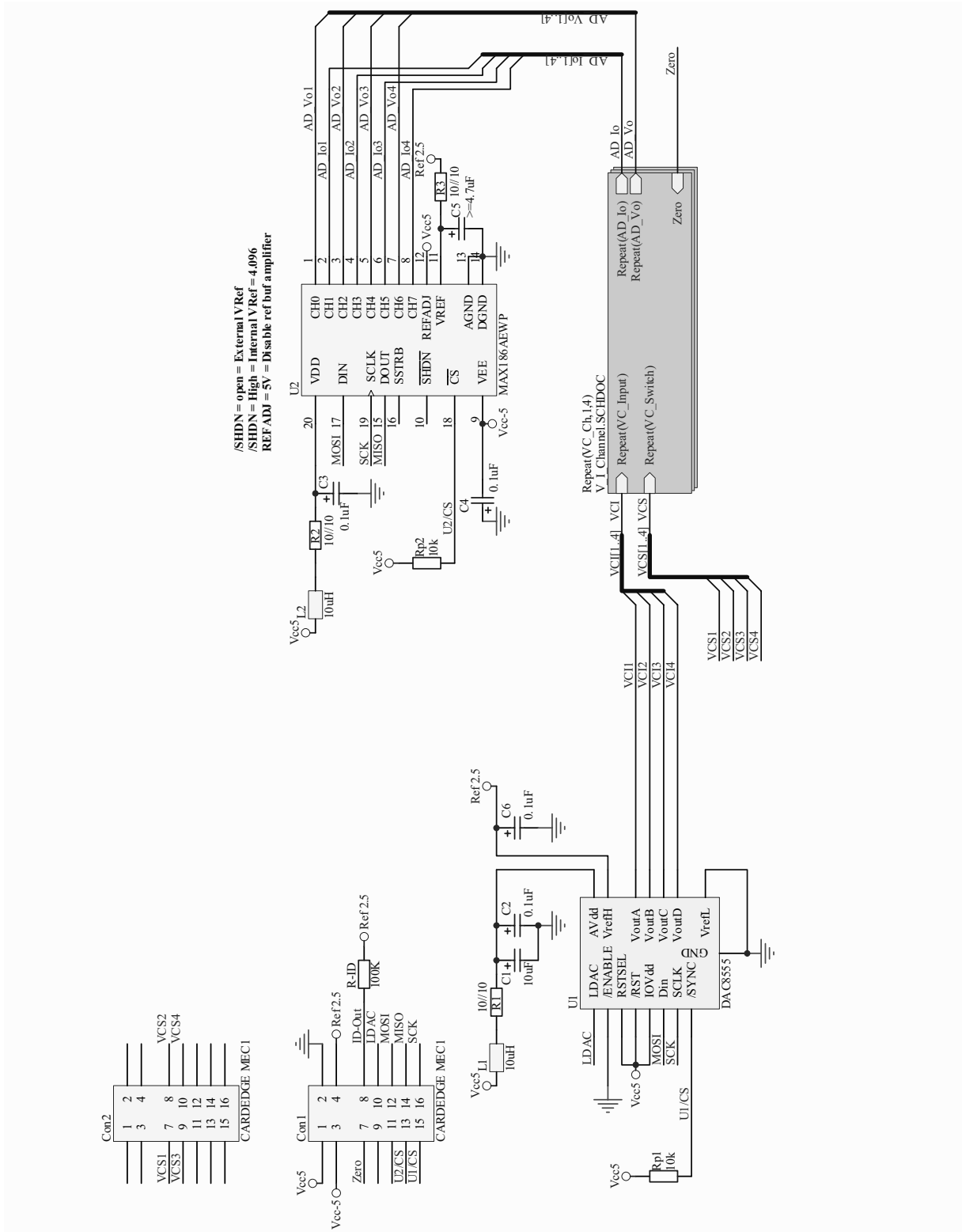


(a) Two channels on the *high current daughterboard*



(b) Implemented *high current channel*

Figure A.5: The (a) *high current channel daughterboard* and (b) the detail of one *high current channel*.



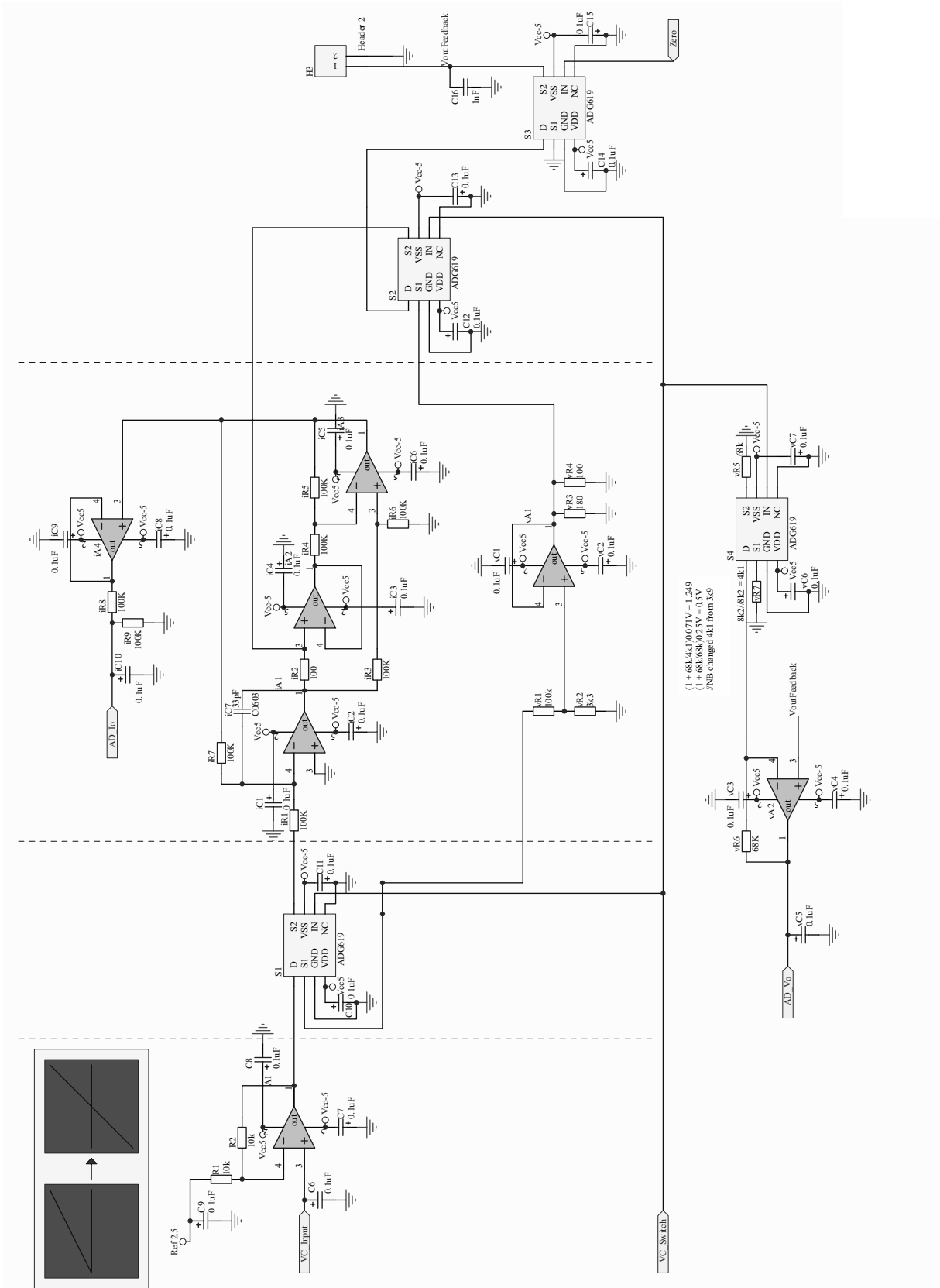


Figure A.7: The low current and voltage channel schematic.

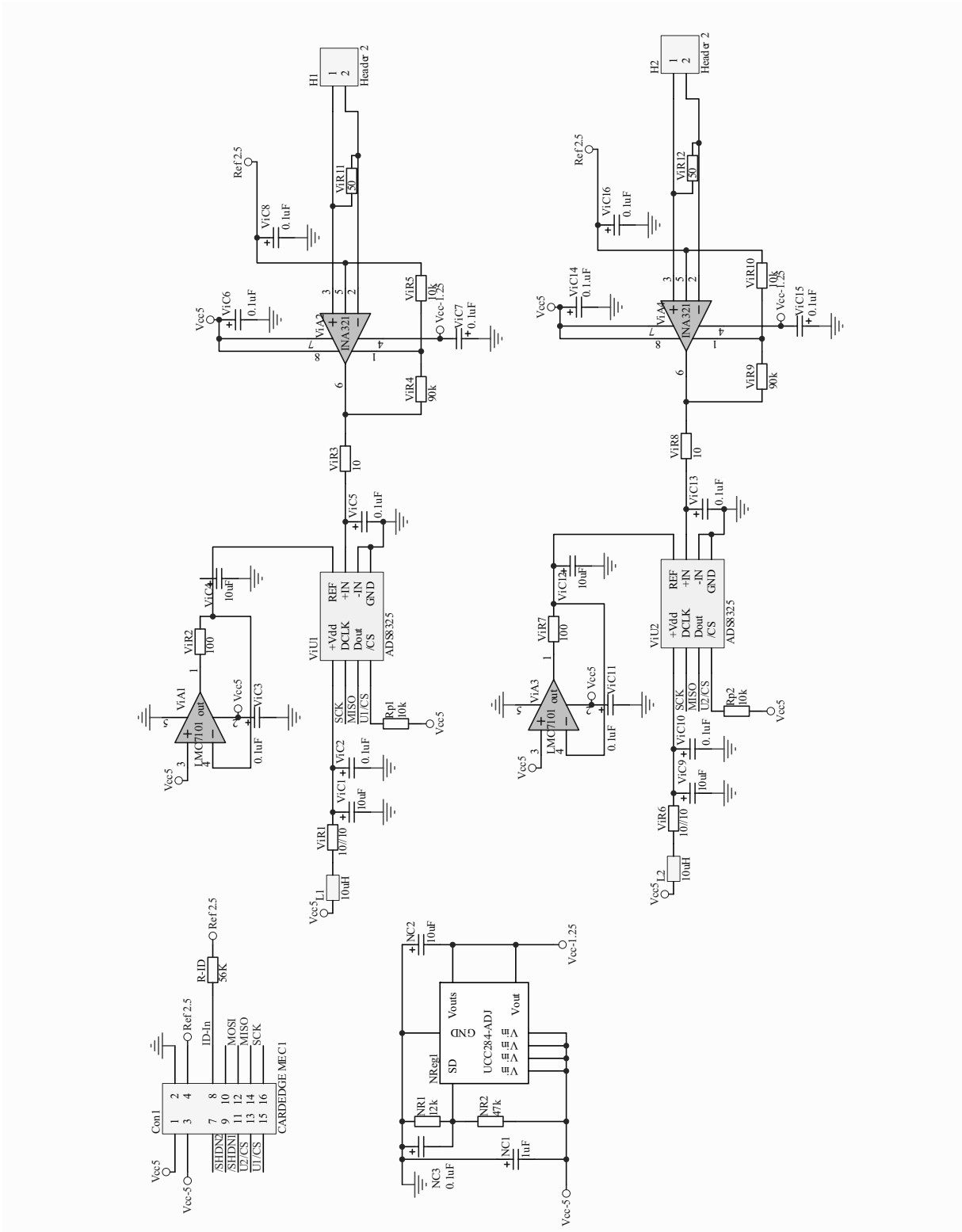


Figure A.8: The high sensitivity voltage input daughterboard schematic.

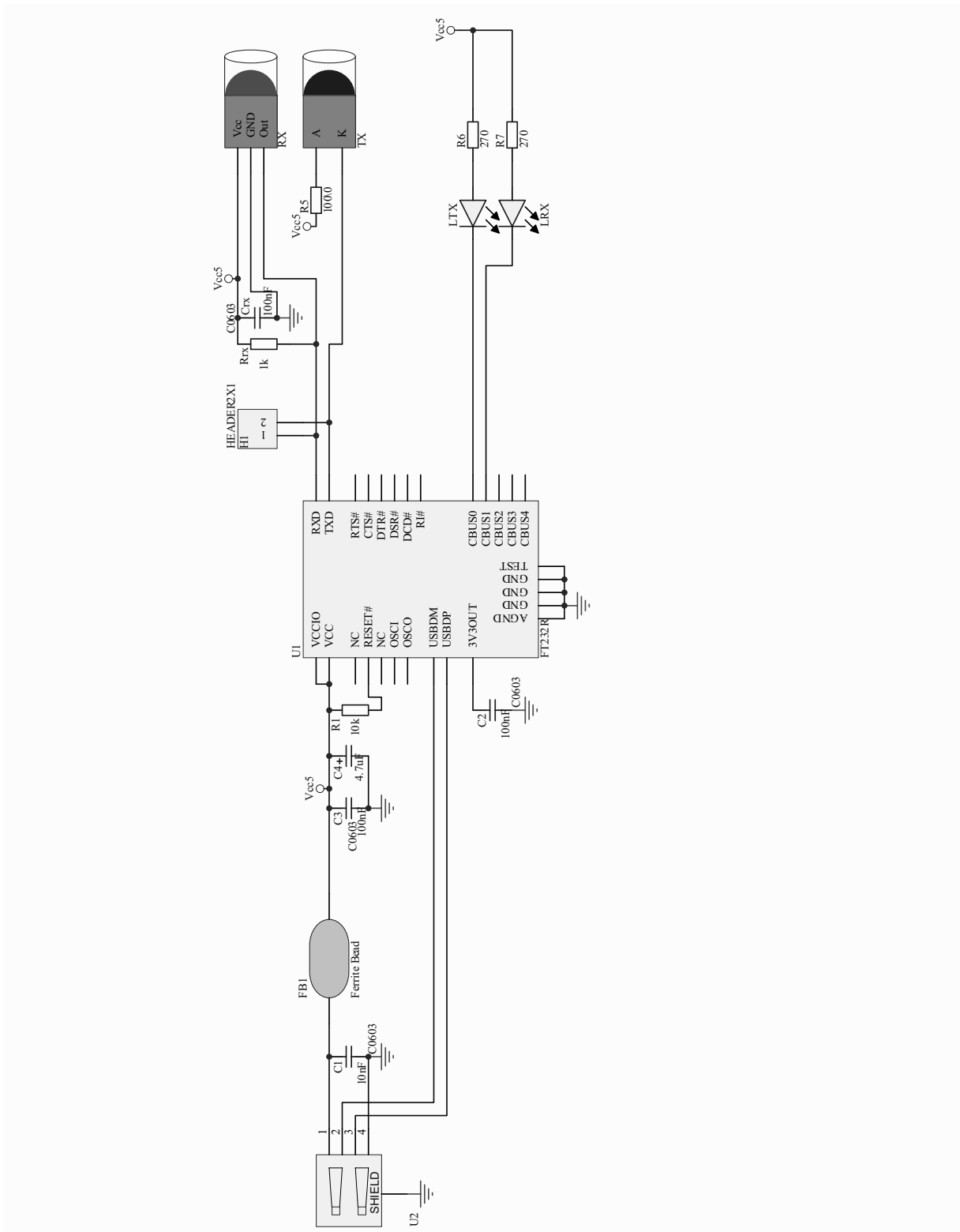
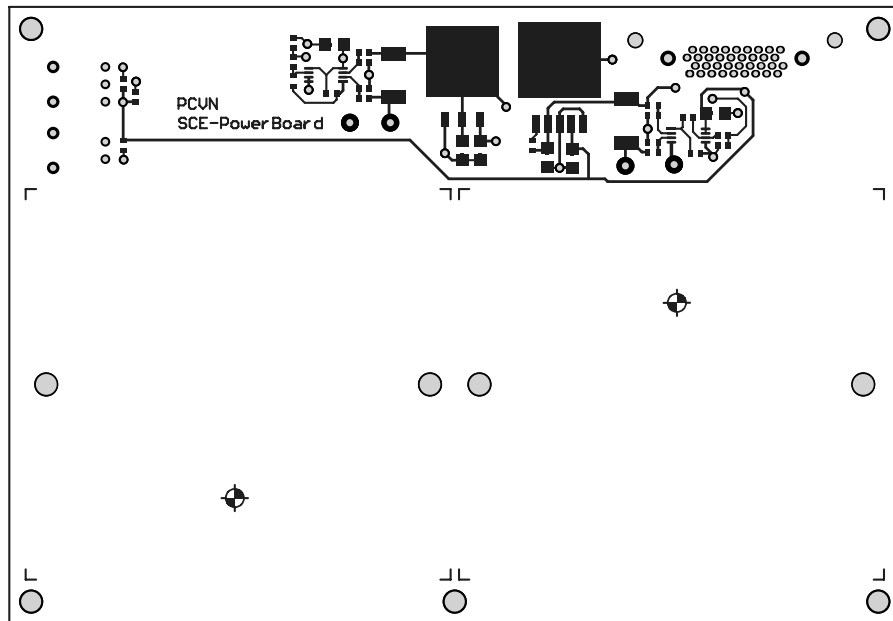


Figure A.9: The FTDI USB-RS232 fibre optical converter schematic.

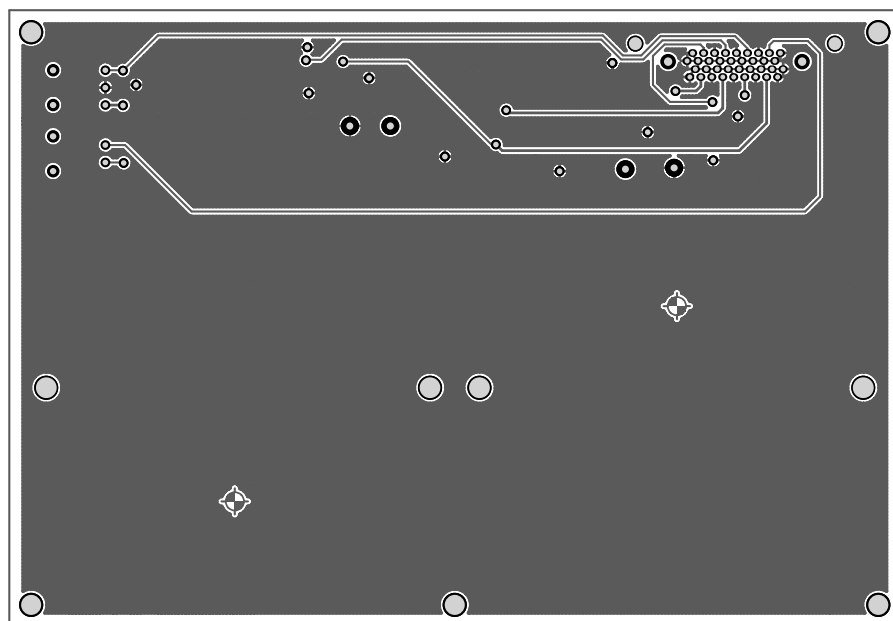
A.2 PCB Layouts

The following section contains the PCB layouts of the control system. Both the front, component side, as well as the bottom side of the PCBs are given.

The PCBs in Fig. A.10 and Fig. A.16 were created at the Stellenbosch University PCB manufacturing facilities, while the PCBs in Fig. A.11 to Fig. A.15 were manufactured at TraX Interconnect [33].



(a) Component side



(b) Bottom side

Figure A.10: The (a) component side and (b) bottom side of the power board PCB, containing the battery holders, regulators, fibre optical converters and current sensing circuitry.

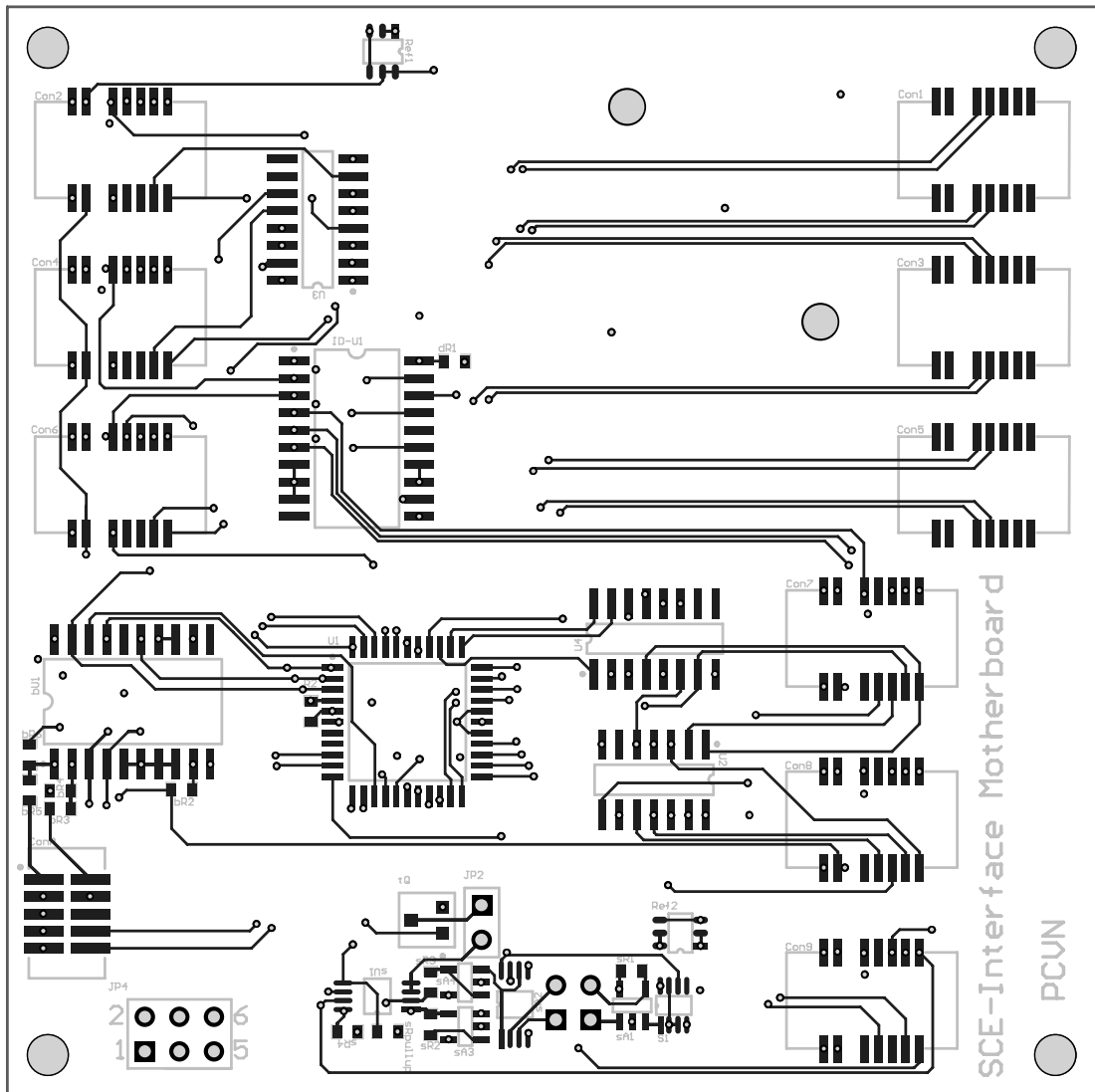


Figure A.11: The component side of the *motherboard* PCB layout.

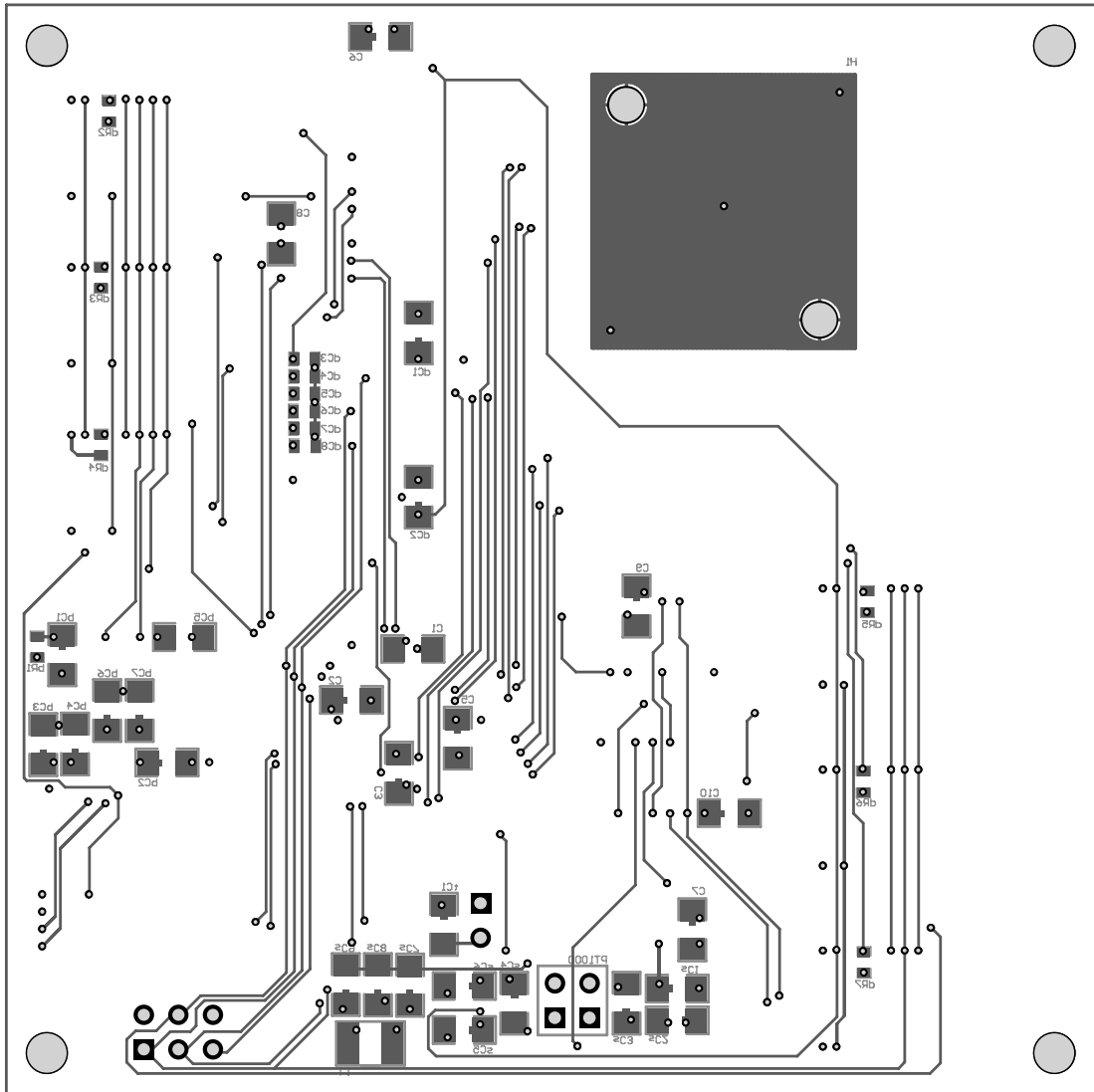
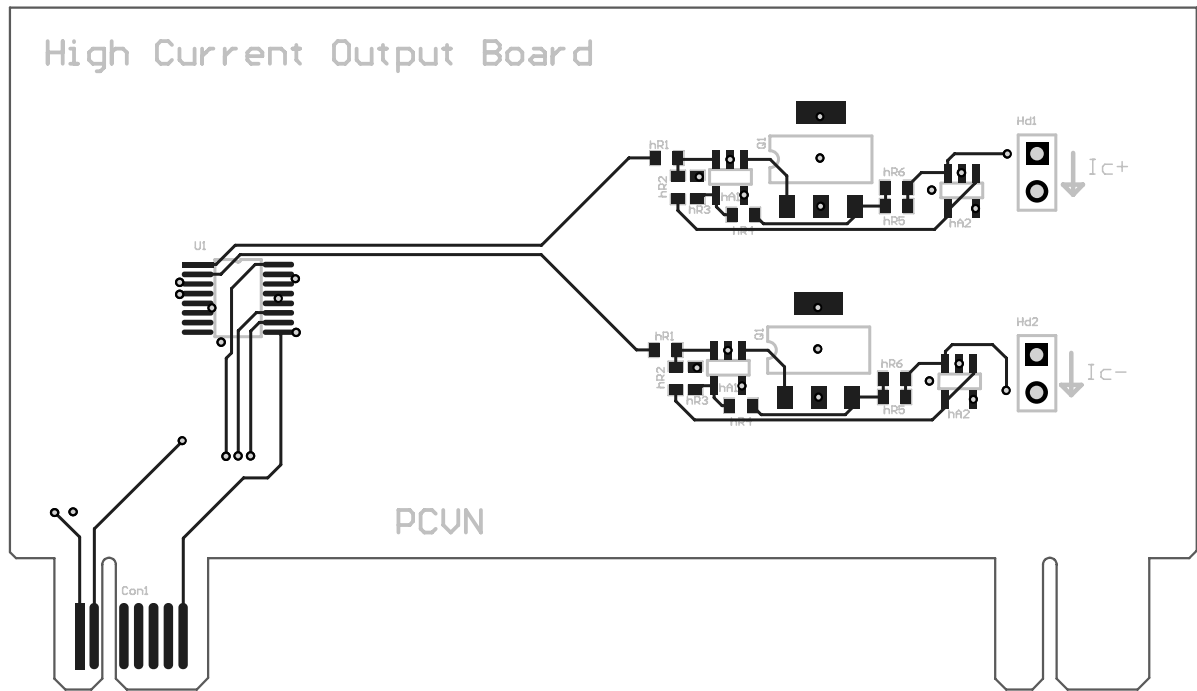
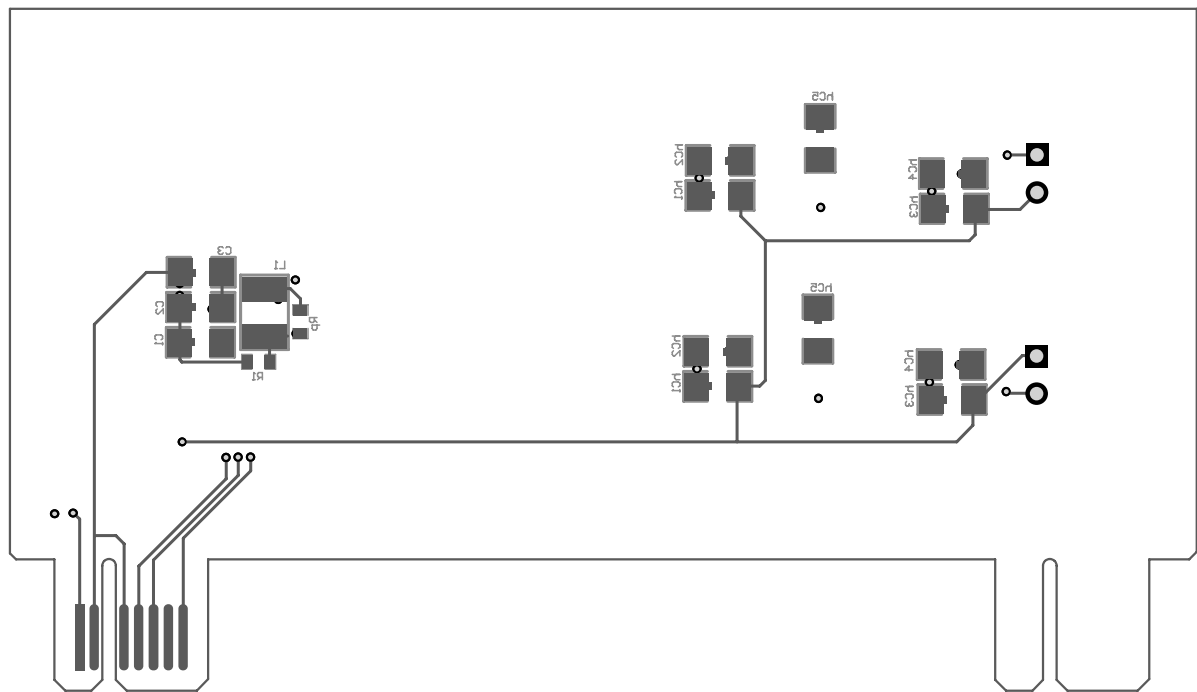


Figure A.12: The bottom side of the *motherboard* PCB layout.

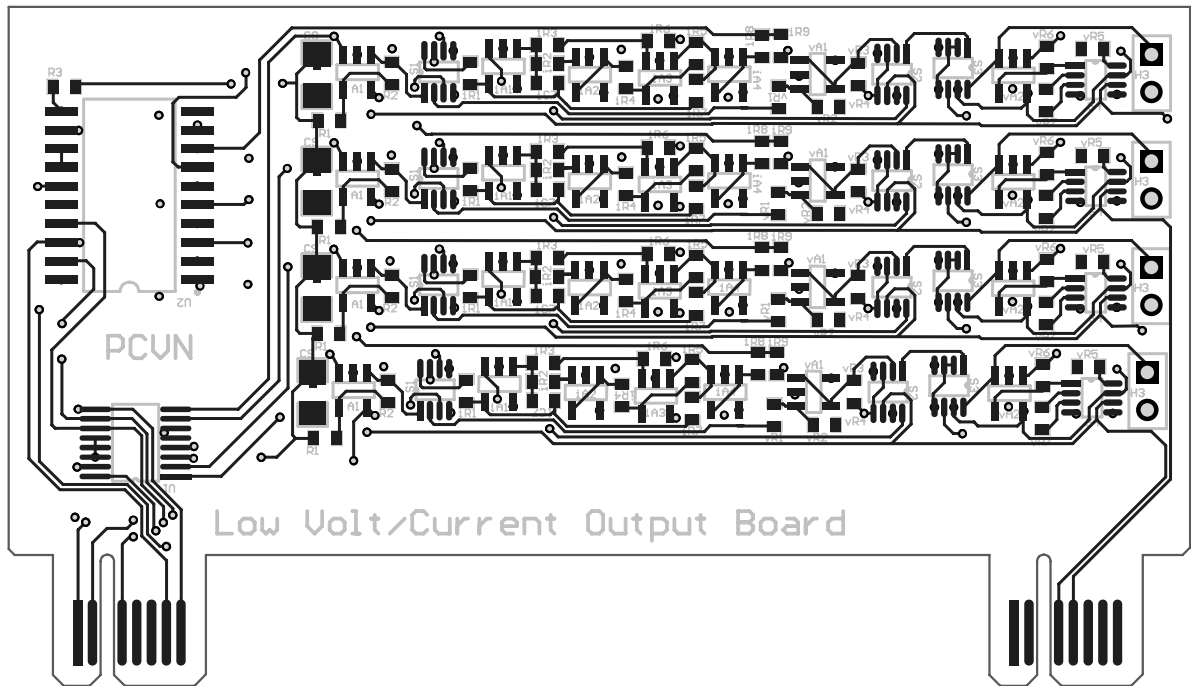


(a) Component side

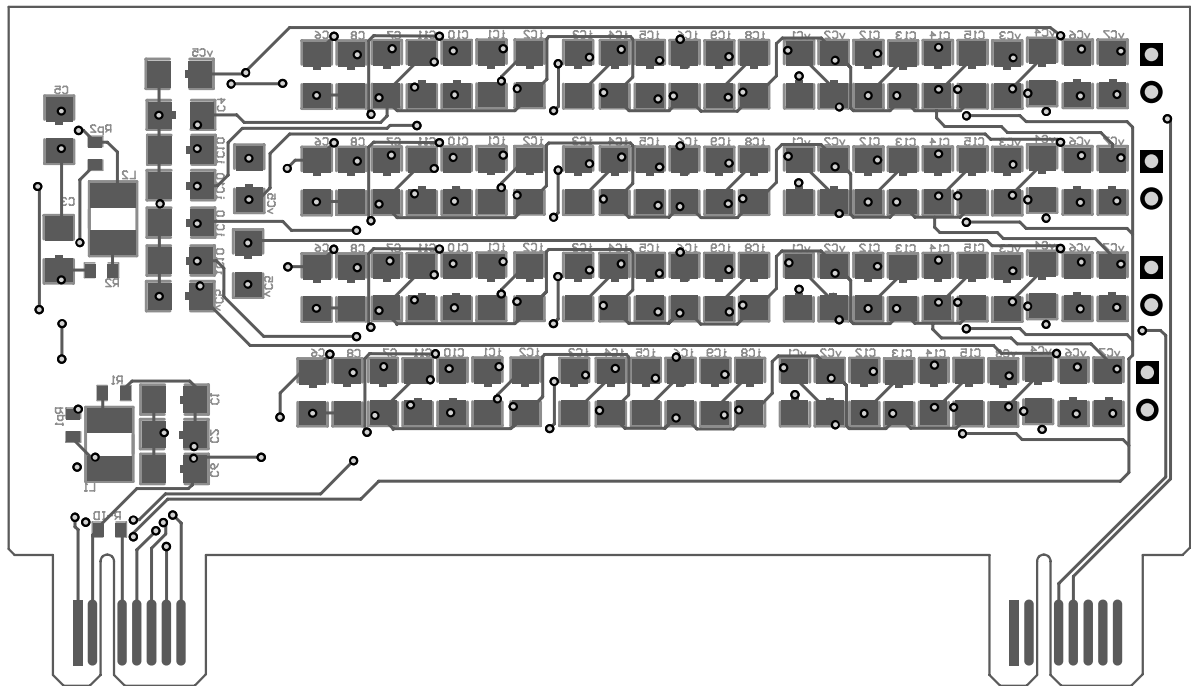


(b) Bottom side

Figure A.13: The (a) component side and (b) bottom side of the *high current daughterboard*.

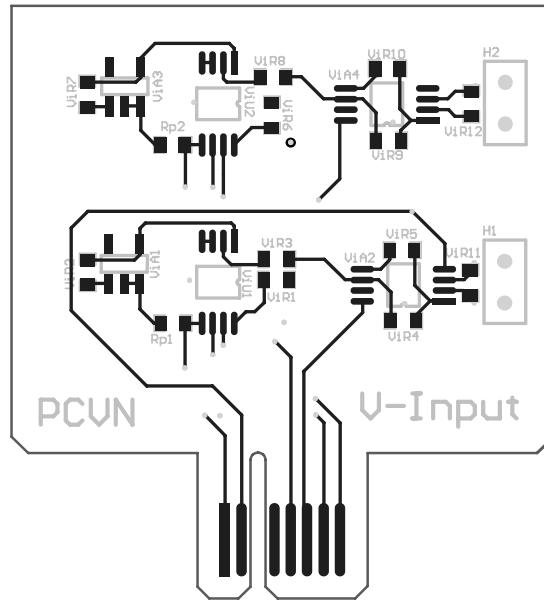


(a) Component side

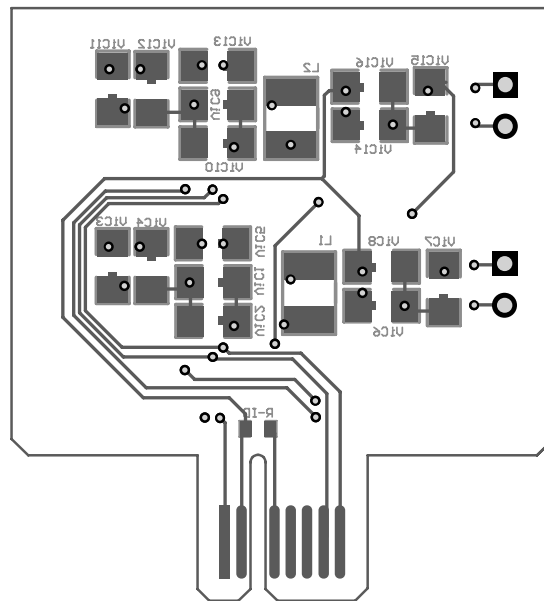


(b) Bottom side

Figure A.14: The (a) component side and (b) bottom side of the *low current and voltage daughterboard*.

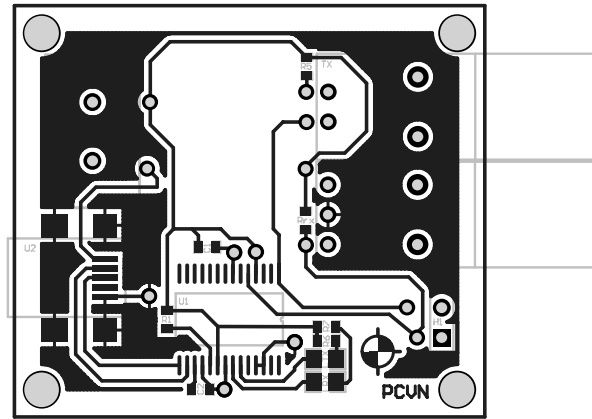


(a) Component side

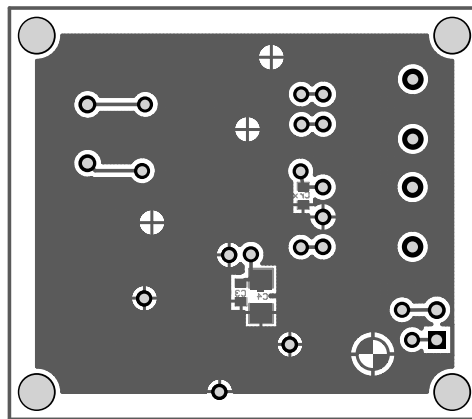


(b) Bottom side

Figure A.15: The (a) component side and (b) bottom side of the *high sensitivity input voltage daughterboard*.



(a) Component side



(b) Bottom side

Figure A.16: The (a) component side and (b) bottom side of the *FTDI USB-RS232* fibre optical converter.

Appendix B

Hardware Designs

Apart from the PCB designs in Appendix A.1, some aluminium cover boxes were also designed. These box designs were done in *Autodesk Inventor Pro 9* to fit, shield and cover the designed PCBs.

The top and the bottom parts of the designed boxes are given separately. They fit together using M3 screws.

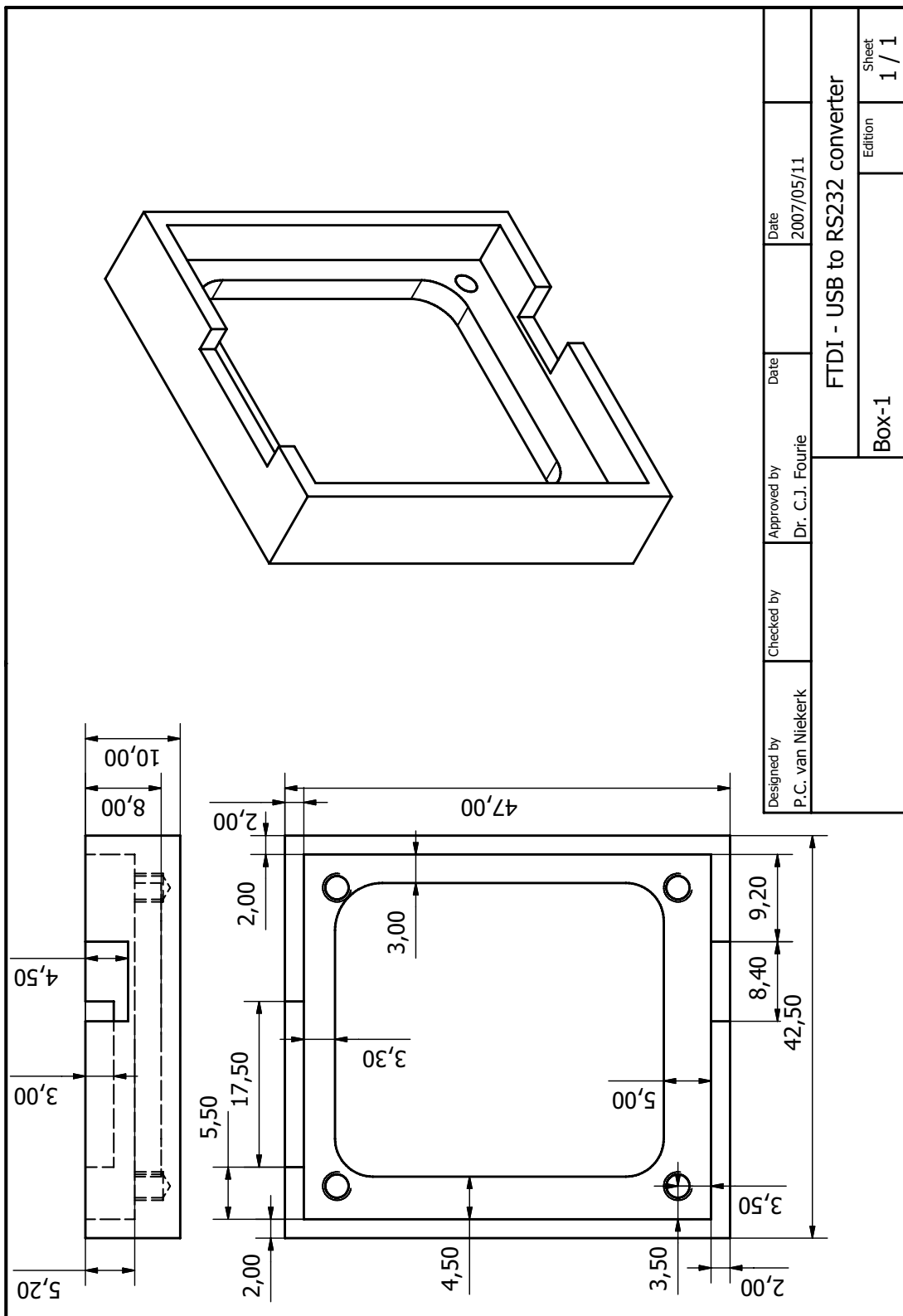


Figure B.1: The bottom part of the *FTDI USB-RS232* fibre optical converter box, containing the PCB in Fig. A.16.

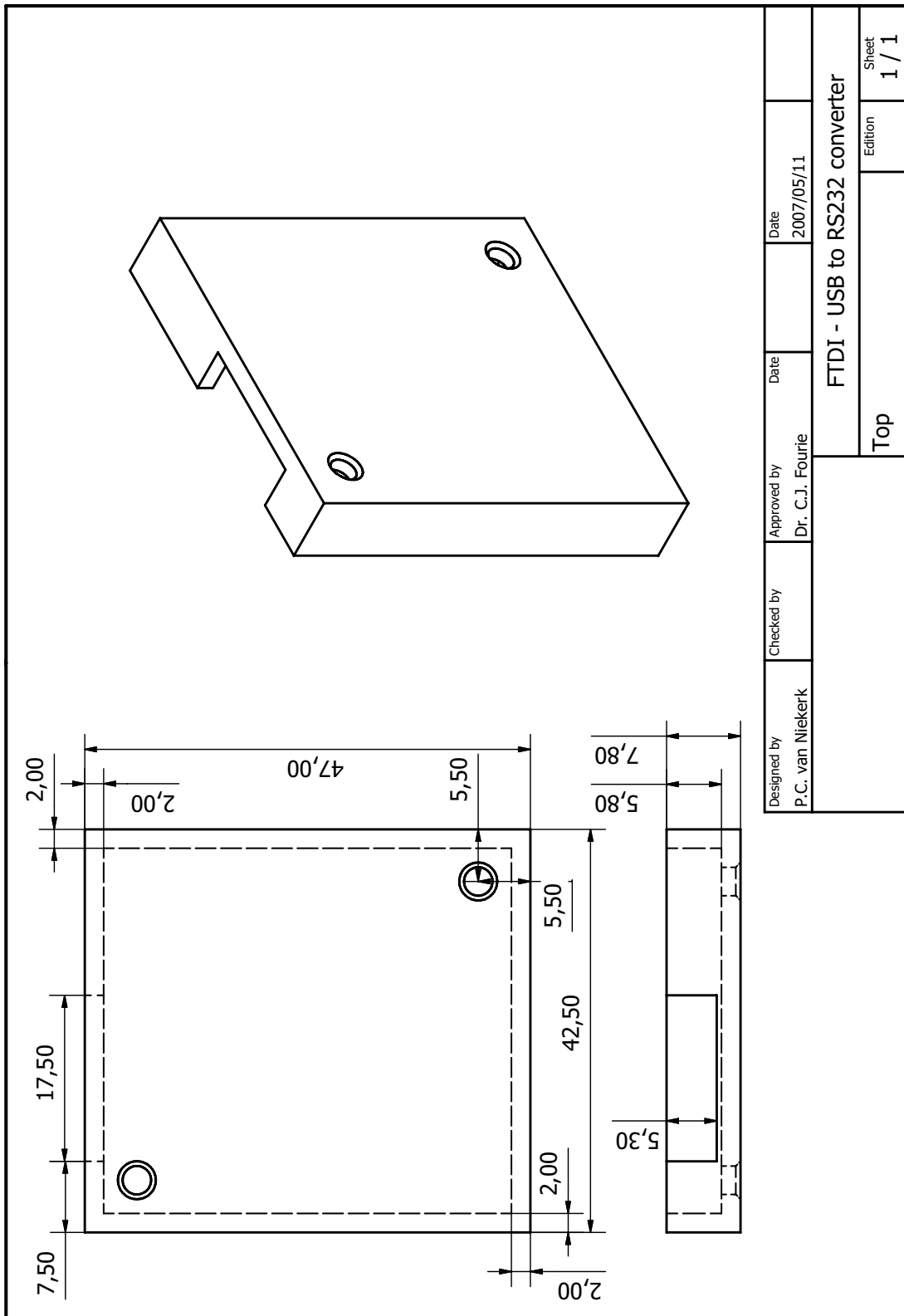


Figure B.2: The top part of the *FTDI USB-RS232* fibre optical converter box.

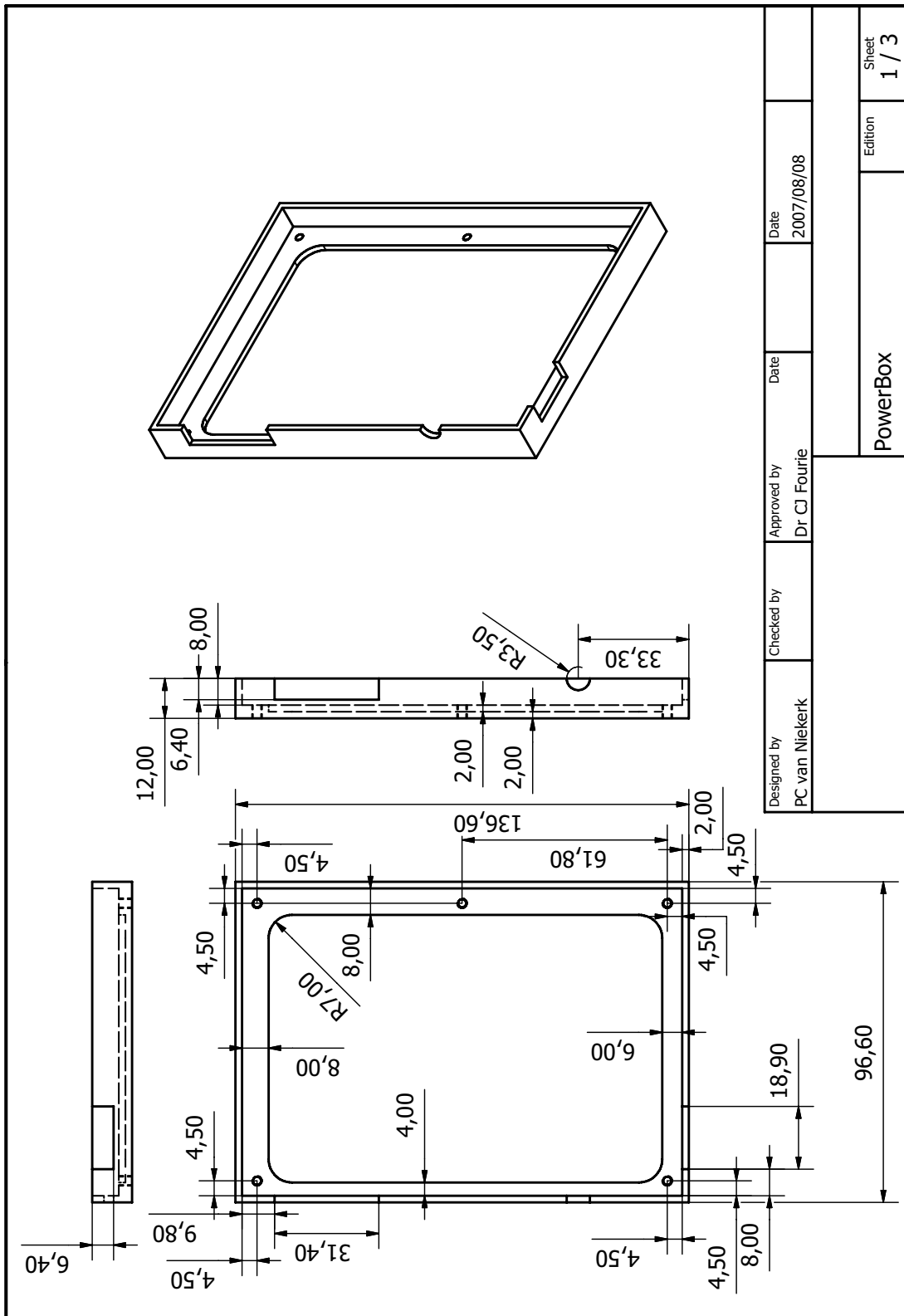


Figure B.3: The bottom part of the power box, containing the power PCB in Fig. A.10.

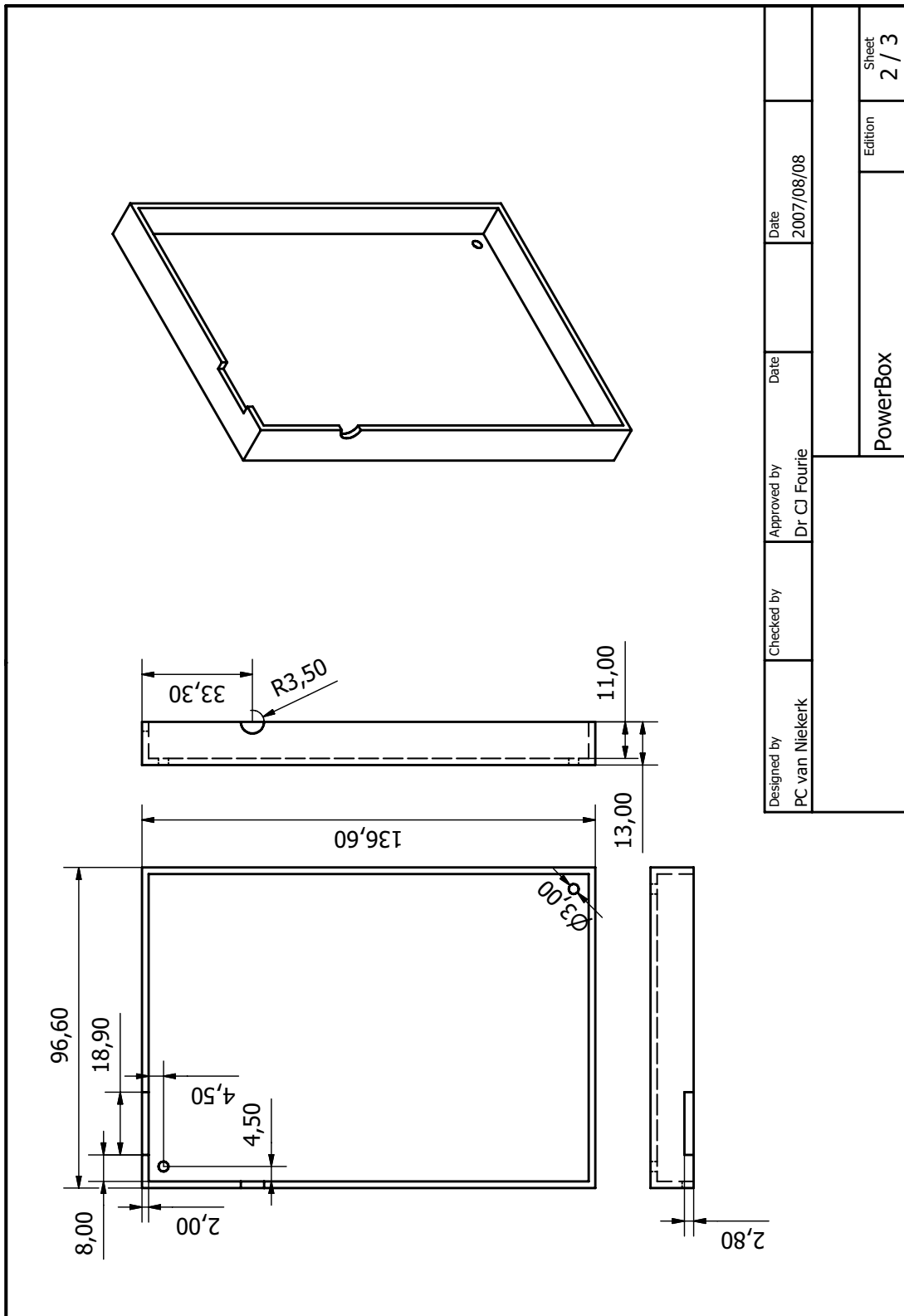


Figure B.4: The top part of the power box, containing the power PCB in Fig. A.10.

Appendix C

Programming Code

Due to the extent of the programming code, an additional CD is included containing all the programming code done for this thesis.

C.1 Assembler Code for PWM

The assembler code can be found on the included CD at: `\Firmware\Assembler\PWMTest.asm`

C.2 Firmware Programming

The implemented firmware code can be found on the included CD at: `\Firmware\C\CCCSV4.c`

C.3 Graphical User Interface

The GUI code can be found on the included CD at: `\GUI Software\CryoTest.pas`

The executable GUI application can also be found on the included CD at: `\GUI Software\CCCS.exe`

Appendix D

PT1000 Calibration Tables

Table D.1: PT1000 Calibration Values

Temperature[K]	PT1000[Ω]	Temperature[K]	PT1000[Ω]	Temperature[K]	PT1000[Ω]
300	1105.103	277.074	1015.897	255.058	929.794
299	1101.225	276.474	1013.356	253.665	924.369
298	1097.347	275.814	1010.795	252.214	918.764
297	1093.467	275.157	1008.154	250.72	912.835
296	1089.585	274.41	1005.512	249.195	906.846
295	1085.703	273.661	1002.548	247.619	900.757
294	1081.820	272.888	999.584	245.995	894.425
293	1077.935	272.108	996.599	244.32	887.771
292	1074.049	271.292	993.474	242.592	881.197
291	1070.162	270.458	990.106	240.815	874.885
290	1066.274	269.652	986.719	238.982	868.412
289	1062.385	268.688	983.049	237.125	861.254
288	1058.495	267.755	979.439	235.213	853.813
287	1054.603	266.788	975.931	233.27	846.211
286	1050.710	265.784	971.998	231.283	838.952
285	1046.816	264.71	967.905	229.3	833.225
284	1042.921	263.674	963.751	227.268	827.639
283	1039.025	262.562	959.416	225.22	820.360
282	1035.128	261.415	954.798	223.165	812.758
281	1031.229	260.227	950.140	221.109	805.095
280	1027.330	258.995	945.321	219.057	797.352
279	1023.429	257.73	940.340	217.014	789.629
278	1019.527	256.415	935.279	214.977	781.805

Table D.2: PT1000 Calibration Values (continues)

Temperature[K]	PT1000[Ω]	Temperature[K]	PT1000[Ω]	Temperature[K]	PT1000[Ω]
212.964	774.122	151.402	532.045	76.7152	202.131
210.966	766.419	149.018	522.346	73.9854	189.931
208.984	758.797	146.567	512.445	71.1684	177.590
207.013	751.054	144.115	502.444	68.2764	165.229
205.052	743.371	141.64	492.442	65.2804	152.788
203.098	735.749	139.146	482.239	62.2371	140.407
201.141	728.127	136.628	472.136	59.201	128.167
199.168	720.545	134.084	461.933	56.3302	115.745
197.194	713.044	131.518	451.588	53.6827	104.735
195.2	705.482	128.928	441.244	51.1624	94.673
193.188	697.819	126.322	430.819	48.7934	85.337
191.192	690.096	123.632	420.474	46.5894	76.807
189.153	682.111	120.79	408.093	44.5325	68.963
187.115	674.166	117.897	394.623	42.5684	61.523
185.055	665.979	115.135	381.496	40.7346	54.425
182.968	657.812	112.441	368.530	38.7974	47.508
180.864	649.505	109.82	355.927	36.3738	40.813
178.715	641.076	107.234	343.667	32.9036	34.562
176.551	632.607	104.716	331.810	28.4843	28.654
174.381	624.016	102.198	319.993	24.3367	23.411
172.18	615.386	99.7003	308.358	20.3915	19.015
169.95	606.493	97.1961	296.744	16.6331	15.749
167.694	597.500	94.6988	285.270	14.2407	14.256
165.434	587.861	92.197	273.796	11.276	12.805
163.159	578.585	89.6562	262.101	9.1796	12.038
160.838	569.753	87.1207	250.264	7.7736	11.575
158.5	560.498	84.5656	238.367	6.2846	11.312
156.143	551.242	81.9961	226.429		
153.78	541.805	79.3706	214.331		

These values are also provided in digital format on the included CD at:

\Temperature\CalibratedPT1000values.tpr

Appendix E

Cryocooler Time Cycles

The cool-down and natural heat-up time measurements for the *Cryomech PT405* cryocooler are displayed in Fig. E.1 and Fig. E.2 respectively.

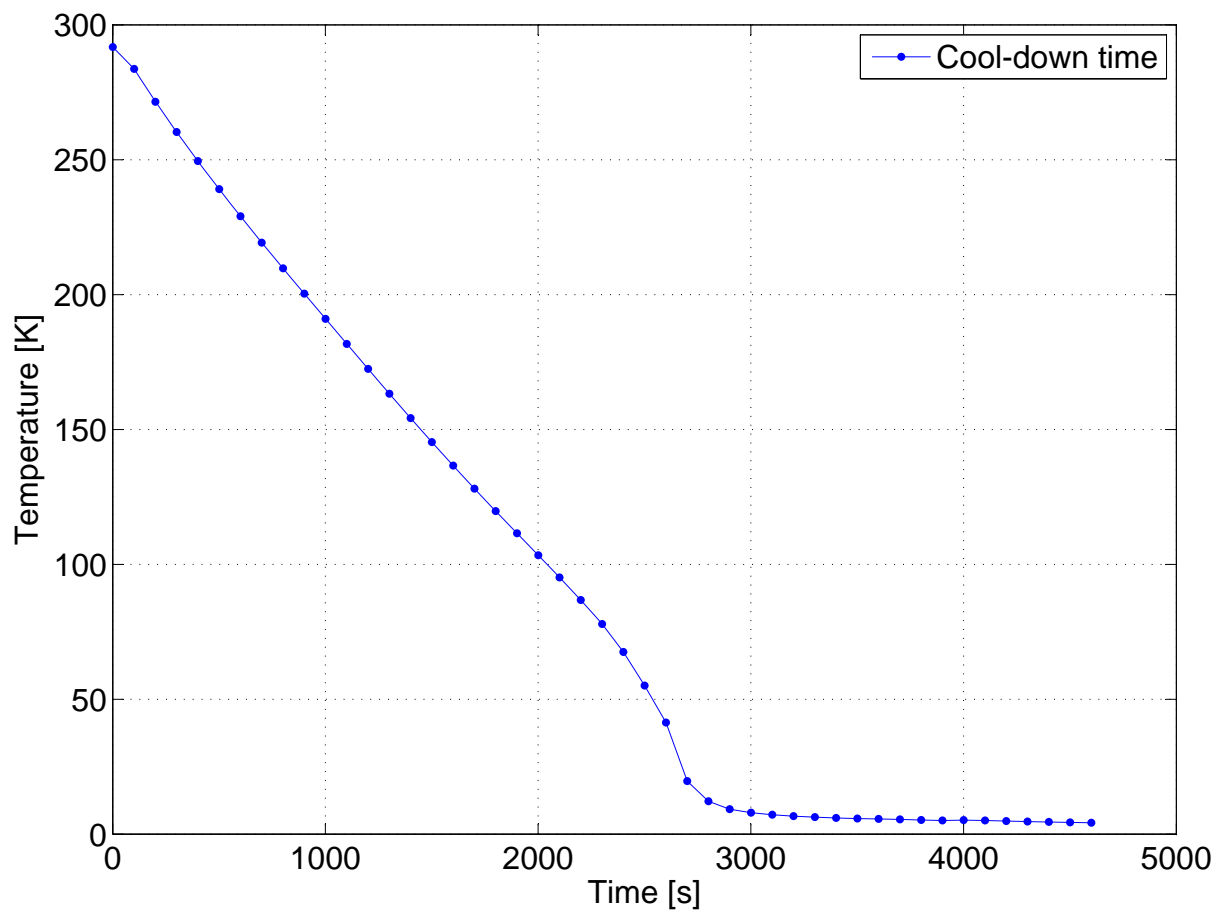


Figure E.1: Cool-down time for the *Cryomech PT405*.

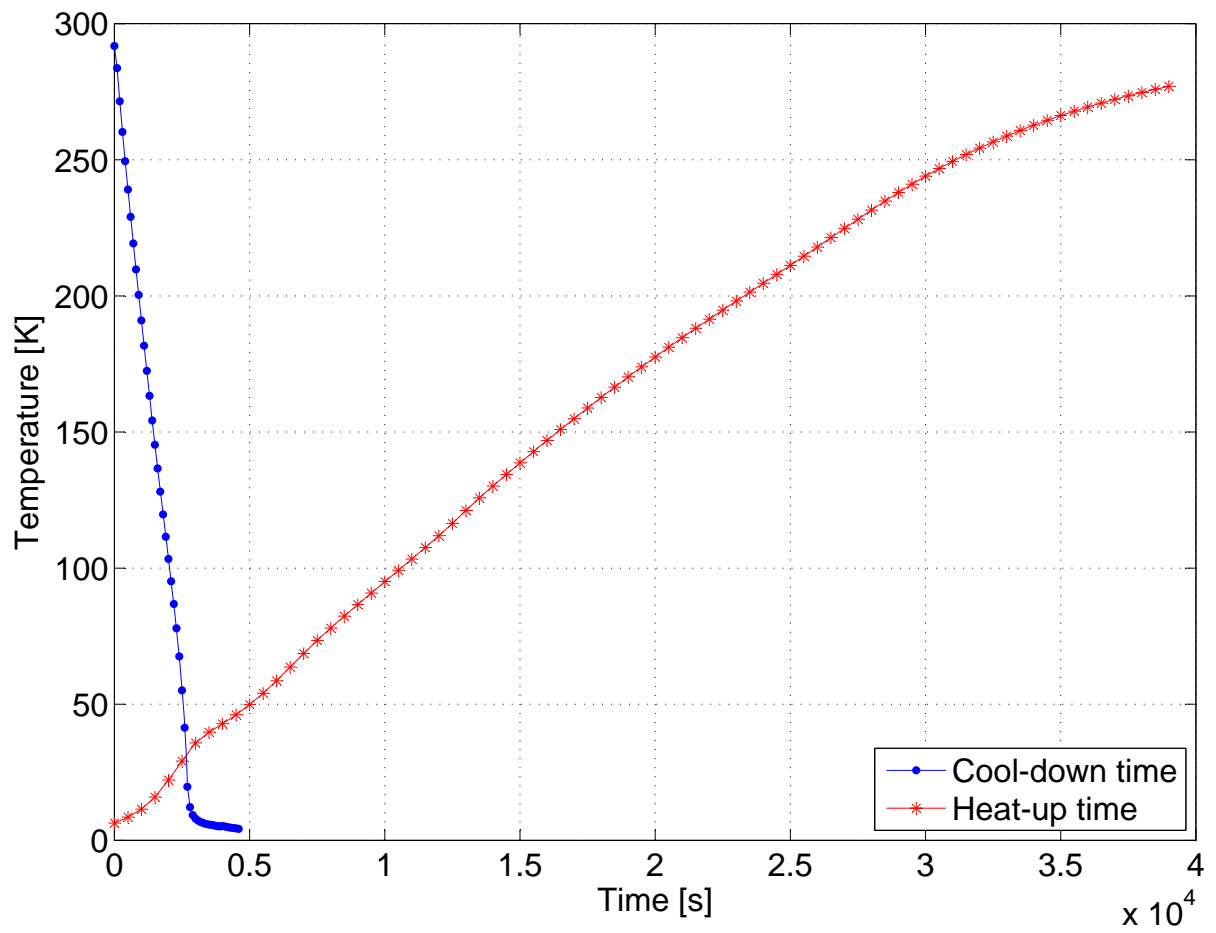


Figure E.2: Cool-down and natural heat-up time for the *Cryomech PT405*.

Appendix F

Datasheets

Table F.1 gives a list of the datasheets that were used in designing the *cryogenic CMOS-based control system*.

Table F.1: Datasheets

Device	Datasheet	Name; Package Used	Manufacturer
Microprocessor	ATMEL AT-mega16/ATmega16L	ATmega16; TQFP44	ATMEL Corporation
Microprocessor	ATMEL AT-tiny26/ATtiny26L	ATtiny26; SOIC-20	ATMEL Corporation
Microprocessor	PIC16F87X	PIC16F876; PDIP-40	Microchip
USB-RS232	FT232R USB UART	FT232R; SSOP-28	FTDI Ltd.
Fibre Optic Transmitter	SFH756/SFH756V	SFH756V	Infineon Technologies
Fibre Optic Receiver	SFH551/1-1(V)	SFH551/1-1V	Infineon Technologies
Multiplexer	MAX398/MAX399	MAX398ESE; SO-G16	MAXIM
Positive Regulator	LP3872/LP3875	LP3872 ES-5.0; TO263-5	National Semiconductors
Negative Regulator	LM2990	LM2990S-5.0; TO263	National Semiconductors
Negative Regulator	UCC284-5	UCC284-5; SOIC8	Texas Instruments
Voltage Reference	REF3212/REF3225	REF3212/REF3225; SOT23-6	Texas Instruments
P-channel MOSFET	IRLML5103	IRLML5103; SOT-23	International Rectifier
NPN-Transistor	PN2222A	PZT2222A; SOT-223	Fairchild Semiconductor
Digital Switch	ADG619/ADG620	ADG619BRTZ; MSOP-8	Analog Devices
Instrumentation Amplifier	INA322/INA2322	INA322; MSOP-8	Texas Instruments
Operational Amplifier	LMC7101	LMC7101AIM5; SOT23-5	National Semiconductors
12-bit ADC	MAX186/MAX188	MAX186AEWP; SO-G20	MAXIM
16-bit ADC	ADS8325	ADS8325I; MSOP-8	Texas Instruments
16-bit DAC	DAC8555	DAC8555; TSSOP-16	Texas Instruments
Digital Potentiometer	AD5262	AD5262BRU200; TSSOP-16	Analog Devices