UNIVERSITEIT•STELLENBOSCH•UNIVERSITY
jou kennisvennoot • your knowledge partner

The Evaluation of Doherty Amplifier Implementations

by

Roelof Jansen

Department of Electrical and Electronic Engineering
University of Stellenbosch
Private Bag X1, 7602 Matieland, South Africa

Supervisor: Prof. C. van Niekerk

March 2008

Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

Signature: .....
R.A. Jansen

Date: 20 February 2008

Abstract

Modern communication systems demand efficient, linear power amplifiers. The amplifiers are often operated in the backed-off power levels at which linear amplifiers such as class B amplifier are particularly inefficient. The Doherty amplifier provides an improvement as it increases efficiency at backed of power levels. Doherty amplifiers consists of two amplifiers, a carrier amplifier and a peaking amplifier, of which the output is combined in a novel way. Implementation of the Doherty amplifier with transistors is not ideal. One of the main problems is the insufficient current production of the peaking amplifier at peak envelope power (PEP) if it is implemented as a class C amplifier. A suggested solution to this problem is a bias adaption system that controls the peaking amplifier gate voltage dynamically depending on the input power levels. The design and evaluation of such a adaptive Doherty amplifier is the main goal of this thesis. A classical Doherty amplifier with and an uneven Doherty amplifier with unequal power division between the carrier and peaking amplifiers are also evaluated and compared with the adaptive Doherty amplifier.

The amplifiers are designed using a 10 W LDMOS FET device, the MRF282. The adaptive Doherty amplifier and the uneven Doherty amplifier show significant improvements in efficiency and output power over the even Doherty amplifier. At PEP the adaptive Doherty delivers 42.4 dBm at 39.75 % power added efficiency (PAE), the uneven Doherty amplifier 41.9 dBm at 40.75 % PAE and the even Doherty amplifier 40.8 dBm at 38.6 % PAE. At 3dB backed-off input power the adaptive Doherty amplifier has an efficiency of 34.3%, compared to 34.9 5% for the uneven Doherty amplifier and 29.75 % for the even Doherty amplifier.

Samevatting

Moderne kommunikasie stelsels vereis effektiewe, linieêre drywing versterkers. Die versterkers word dikwels in laer drywings vlakke bedryf waar linieêre versterkers soos 'n klas B versterker besondere lae effektiwiteit het. Die Doherty versterker bied 'n uitweg omdat dit verbeterde effektiwiteit by lae drywings vlakke bied. 'n Doherty versterker bestaan uit twee versterkers, die hoof versterker en die aanvullende versterker, waarvan die uittrees met 'n spesiale kombinasie netwerk bymekaar gevoeg word. Die implementasie van Doherty versterkers met transistors is nie ideaal nie. Een van die hoof probleme is die onvoldoende stroom wat deur die aanvullings versterker gebied word by piek omhulsel drywing (POD). 'n Oplossing vir die probleem is om 'n aanpassings sisteem te gebruik wat die aanvullende versterker se hekspanning dinamies beheer afhangende van die intree drywings vlakke. Die ontwerp en evaluasie van so 'n aanpassings Doherty versterker is die hoof doel van hierdie tesis. 'n Klassieke Doherty versterke met gelyke drywings verdeling en 'n ongelyke Doherty versterker wat gebruik maak van ongelyke drywings verdeling tussen die hoof-en aanvullende versterkers is ook gevalueer en vergelyk met die aanpassings Doherty versterker.

Die versterkers was ontwerp met 'n 10 W LDMOS FET, die MRF282. Die aanpassings Doherty versterker en die ongelyke Doherty versterker het aanmerklike verbeteringe in effektiwiteit en uittree drywing gebring in vergelyking met die ewe Doherty versterker. By POD het die aanpassings versterker 42.4 dBm teen 39.75 % drywing toegevoegde effektiwiteit (DTE) gelewer, die ongelyke Doherty versterker 41.9 dBm teen 40.75 % DTE, en die ewe Doherty versterker 40.8 dBm teen 38.6 DTE. By 'n intree drywingsvlak 3 dB laer as POD het die aanpassings Doherty versterker 'n effektiwiteit van 34.3 % getoon, in vergelyking met die onewe Doherty versterker se 34.9 % en die ewe Doherty versterker se 29.75 % DTE.

Acknowledgements

The Lord for his grace in allowing me to write this thesis

Prof Cornell van Niekerk for his invaluable guidance and patience

Wessel Croukamp and Lincoln Saunders for all their work and advice on the hardware

Ashley Cupido for his work in manufacturing the PCB boards

Martin Siebers for his assistance in the high frequency lab

My parents for all their support and love

My friends who had to listen to my excuses for all this time

List of Abbreviations

SMD	Surface Mount Device
PEP	Peak Envelope Output
BW	Bandwidth
DC	Direct Current
DUT	Device Under Test
FET	Field Effect Transistor
GPIB	General Purpose Interface Bus
PAE	Power Added Efficiency
PCB	Printed Circuit Board
PEP	Peak Envelope Output
RF	Radio Frequency
SMA	SubMiniature version A
SMD	Surface Mount Device
SOLT	Short-Open-Load-Through

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Overview of Doherty Amplifiers

Modern microwave and radio frequency communications systems have raised the demand for highly efficient base station power amplifiers. Modulation schemes such as CDMA-2000, WCDMA and ISA-95 make efficient use of the frequency spectrum but have a large peak-to-average power ratio. Linear amplification is therefore required over a wide range of power levels. However, linear amplifiers typically have greatly reduced efficiency levels when operating in backed-off power regions. The Doherty amplifier offers a technique to improve the linear range of the power amplifier and provide greater efficiency at backed off power levels [11].

The Doherty amplifier involves the use of two amplifiers of which the outputs are combined in a novel way. The first amplifier, the carrier amplifier, is designed via a load-line technique to reach saturation at a backed-off power level. This backed-off design increases its efficiency at low power levels. A second amplifier, the peaking amplifier, is then only used at power levels near saturation. It provides a load-pulling effect on the carrier amplifier, changing its load line so that it reaches saturation at the classic load-line design point.

The implementation of the Doherty amplifier with modern transistors provides some problems. A classic approach is to use class AB and class C amplifiers to provide the required behaviour for the carrier and peaking amplifiers [10]. However, the class C amplifier used to implement the peaking amplifier provides insufficient current at PEP (peak envelope output) for the load-pulling effect to occur fully. One suggested solution to this problem is to use uneven power division for the two amplifiers, increasing the peaking amplifier drain current at PEP by giving it more input power than the carrier amplifier. A second solution is to increase the peaking amplifier drain current at PEP by using a bias adaption scheme to raise the gate voltage of the peaking amplifier at power levels near saturation.

1.2 The Scope and Layout of this Study

An adaptive Doherty amplifier varies the peaking amplifier gate voltage according to input power levels. This study proposes to evaluate such an adaptive Doherty amplifier and compare it with two other Doherty amplifier schemes. The first of these is a classical Doherty amplifier described in literature using an even power division scheme, while second is an uneven Doherty

amplifier using unequal input power distribution between the carrier and peaking amplifiers. This thesis will describe the design, manufacture, measurement and evaluation of the three Doherty amplifier schemes.

The theoretical background and a more detailed explanation of how Doherty amplifiers work is provided in chapter 2. The insufficient current production of the peaking amplifier and the suggested solutions are also investigated in more detail in this chapter.

In chapter 3 the design of the carrier and peaking amplifiers are presented. This chapter describes the load-line design, the choice of bias points, the models used for the design, the design of stabilisation network and the design of input and output matching networks. A new study is presented on the effect of the intermediary impedance R_0 on length and performance of offset lines suggested by Kim [9] to improve the Doherty performance.

The more practical aspects of power amplifier design is described in Chapter 3. For passive component modeling a novel external network is proposed for capacitors that is used in conjunction with provided models to improve the match between simulation and measured performance. The modular design method used to design the various Doherty schemes is also described in this chapter, along with the measurement setups used to measure amplifier performance and to test for amplifier oscillations. The measured performance of the peaking and carrier amplifiers is discussed, and a shift from the specified permittivity of the substrate is investigated.

In chapter 4 the optimal bias points for the even and uneven Doherty amplifiers is determined experimentally. This experimental procedure provides gate bias points that deviate from the points designed in chapter 3 in order to compensate for the non-ideal phase behaviour of the amplifiers and the incorrect design assumption that the class C amplifier provides sufficient current at PEP. The criteria for the optimisation and the process itself is described.

A bias adaption system is presented in Chapter 5. This system includes the design of a coupler, envelope detector, bias shaper circuit and delay line. An experimental method to determine the required length of the delay line is introduced. The performance of the adaptive Doherty amplifier is then optimised using the adaption shaper circuit.

In chapter 7 the even, uneven and adaptive Dohery amplifier performances are discussed and compared. Comparisons are also made with relevant results from literature.

Chapter 8 provides the conclusions and recommendations of this study.

Chapter 2

Doherty Amplifiers and Bias Adaption

2.1 Introduction

The Doherty amplifier was first presented in 1936 [11] as a scheme designed to improve the efficiency of linear amplifiers. It comprises two amplifiers, a carrier amplifier and a peaking amplifier, of which the outputs are combined in a special way. In order to understand the Doherty amplifier we must first look at the load-line design technique (section 2.2) for power amplifiers, as well as understand the concept of load-pulling (section 2.3). In section 2.4 the operation of the Doherty amplifier is explained. Practical implementation of a Doherty amplifier brings new problems. Section 2.5 discusses one of the main problems, while section 2.6 suggests two possible solutions.

2.2 Load-line Amplifier Design

Transistor amplifiers are designed using a conjugate match at the input and output of the transistor provide the maximum amount of gain possible for that transistor [16]. A conjugate match is made by setting the real part of the load impedance equal to that of the real part of the generator impedance, while setting the imaginary part of the load resistance equal but negative to the imaginary part of the generator impedance. At first glance this solution to the matching problem seems ideal for power amplifiers - surely achieving the highest gain possible is desirable? However, as Cripps [10] shows, the conjugate match technique is hampered by the physical limitations of the source, in this case the transistor. Transistors have a finite maximum current (I_{max}) and a limited sustainable voltage (V_{max}) across their output terminals. To utilise the maximum available current and voltage swing of the transistor the optimum load needs to be chosen according to the formula [10]

$$Ropt = \frac{V_{dc}}{I_1} \tag{2.1}$$

where V_{dc} is the drain biasing voltage and I_1 is the fundamental current flowing through the load. This load is referred to as the load-line match. Figure 2.1 demonstrates a transistor used in

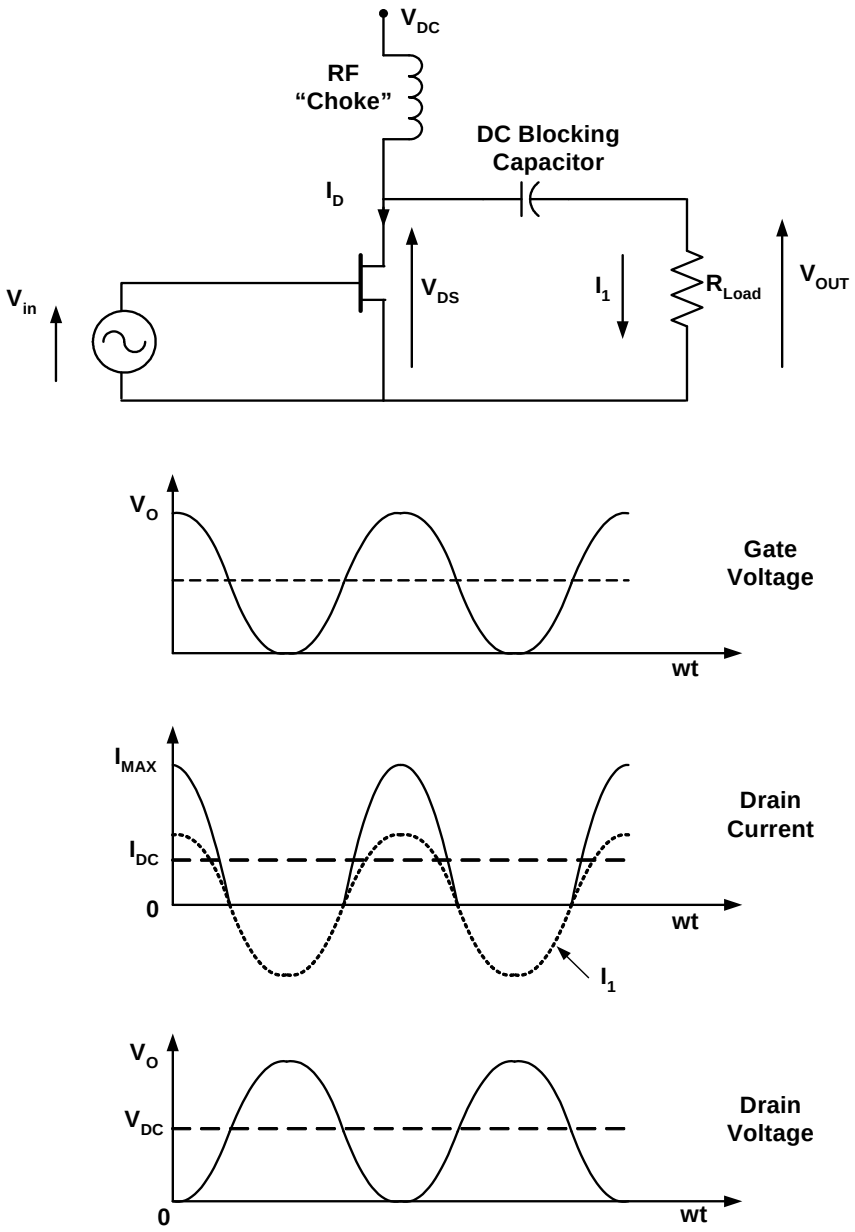


Figure 2.1: A load-line matched Class B amplifier with waveforms [10]

a Class B amplifier load-line design. The resulting load-line graphs for such a load-line match, as well as a possible outcome for a conjugate match , can be seen in figure 2.2 [10]. The conjugate match in this example has resulted in the generator reaching V_{max} well before I_{max}. This will limit the current to a value lower than its maximum and therefore also limits the available power from the transistor. The load-line match graph reaches both V_{max} and I_{max} and so utilises the full potential of the transistor.

Figure 2.3 compares the gain for the same load-line and conjugate match examples [10]. At low power the conjugate match exhibits more gain, but the load-line match demonstrates a higher 1 dB compression point than the conjugate match. Because we are designing power amplifiers and are primarily interested in obtaining a high output power we therefore use the load-line match when determining the load for the transistor.

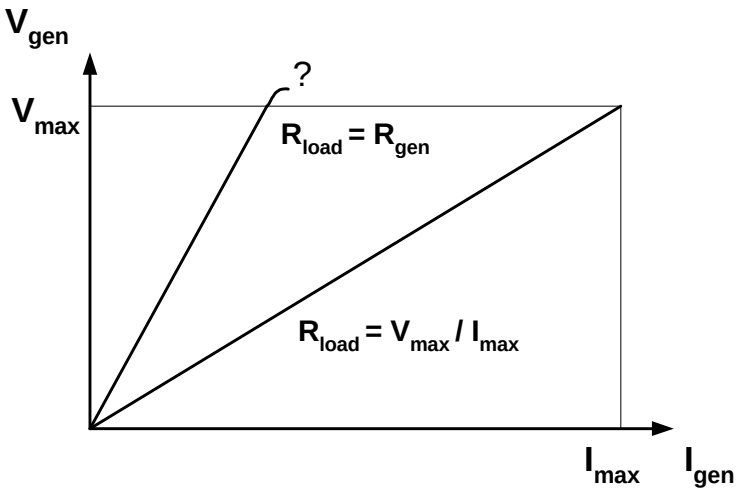


Figure 2.2: The load-line graph for a load-line and a conjugate match. The load-line match makes full use of the capabilities of the transistor.[10]

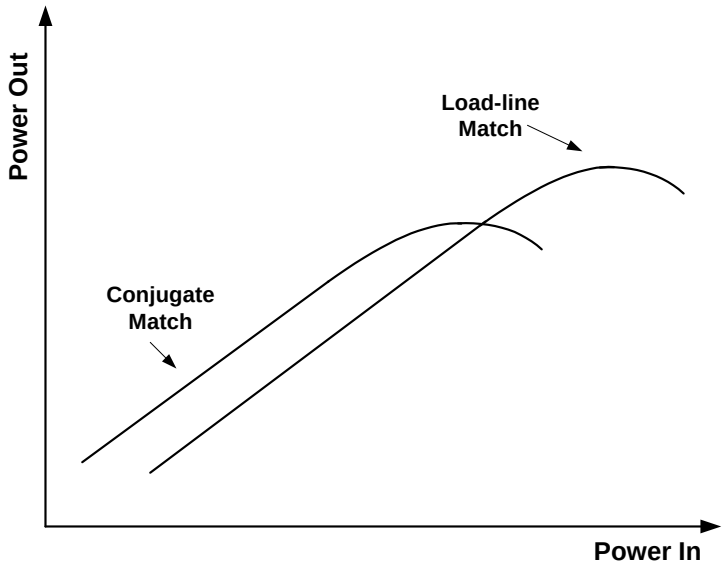


Figure 2.3: The gain against input power for a load-line and conjugate match. The conjugate match shows a higher gain than the load-line match, but reaches its compression point at lower power levels. [10]

2.3 Active Load-pulling

Active load-pulling refers to a technique by which the impedance seen by a generator is controlled by the phase and magnitude of the current provided by a second generator. Figure 2.4 demonstrates the concept [10]. The voltage appearing across the load resistance is

$$V_L = R_L \times (I_1 + I_2) \tag{2.2}$$

It can further be shown that the complex impedance seen by generator 1 is [10]

$$\mathbf{Z}_1 = R_L \times (1 + \frac{\mathbf{I}_2}{\mathbf{I}_1}) \tag{2.3}$$

It is therefore possible to change the impedance $\mathbf{Z}_1$ by controlling the current and phase of $\mathbf{I}_2$. For example, if the currents from the two generators are in in phase, $\mathbf{Z}_1$ can be load-pulled to higher resistive values. If the currents are out of phase, $\mathbf{Z}_1$ can be pulled to lower resistive values [10].

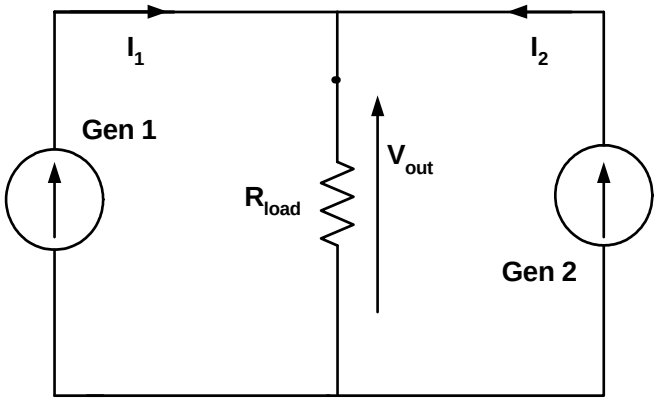


Figure 2.4: Schematic showing an active load-pull system. [10]

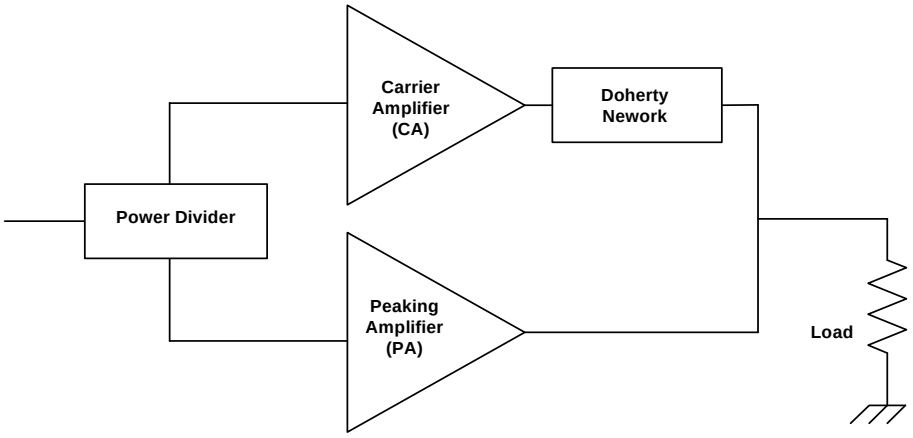


Figure 2.5: Schematic representation of a Doherty Amplifier [10]

2.4 How Doherty Amplifiers Work

2.4.1 The Carrier Amplifier

The Doherty amplifier makes use of both the load-line matching and the load-pulling techniques discussed in the previous sections. Figure 2.5 shows a schematic representation of a Doherty amplifier. The term "Doherty amplifier" is misleading - it does not in fact refer to a single amplifier but rather to a method of combining the output from two amplifiers. The first of these amplifiers is the carrier amplifier. As discussed in section 2.2 an amplifier with a load-line

match can provide the highest possible power without saturation for a particular transistor. The efficiency for an amplifier with a load-line match is given by [10]

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{V_{RF} I_1}{2 V_{DC} I_{DC}} \tag{2.4}$$

Refer to figure 2.1 for a representation of a Class B amplifier with waveforms at full power. The fundamental current $I_1 = \frac{1}{2} I_{MAX}$, and $V_{RF} = V_{DC}$ [10]. The DC current level is given by $I_{DC} = \frac{I_{MAX}}{pi}$. Inserting these values into equation 2.4 results in an impressive efficiency of 78.5%. However, at lower power levels the efficiency falls rapidly. If the input power is backed off by 6dB from the PEP (Peak Envelope Power), then $V_{RF} = \frac{1}{2} V_{DC}$, $I_1 = \frac{1}{4} I_{MAX}$ and $I_{DC} = \frac{I_{MAX}}{2pi}$. This results in an efficiency of 39%. Figure 2.6 shows the load-line graph of a Class B load-line matched amplifier with waveforms for a full-power signal and a signal backed off by 6 dB. To combat this loss of efficiency at lower power levels the Carrier amplifier does not use a load-line match, but instead presents the transistor with a value twice as much as that expected of a load-line match

$$R_{carrier} = \frac{2 V_{max}}{I_1} \tag{2.5}$$

Now if the same 6dB backed off signal is applied then $V_{RF} = V_{DC}$ and the efficiency is again 78.5%. Of course a problem now occurs if the power is increased - the value of the output voltage will exceed V_{DC} and result in signal distortion. The solution to this problem is the key to the Doherty amplifier. The load-pulling technique is used to change the load seen by the carrier amplifier from $R_{carrier} = 2R_{opt}$ at 6dBs backed off to R_{opt} at full power. Figure 2.7 shows this required change in the load-line of the carrier amplifier.

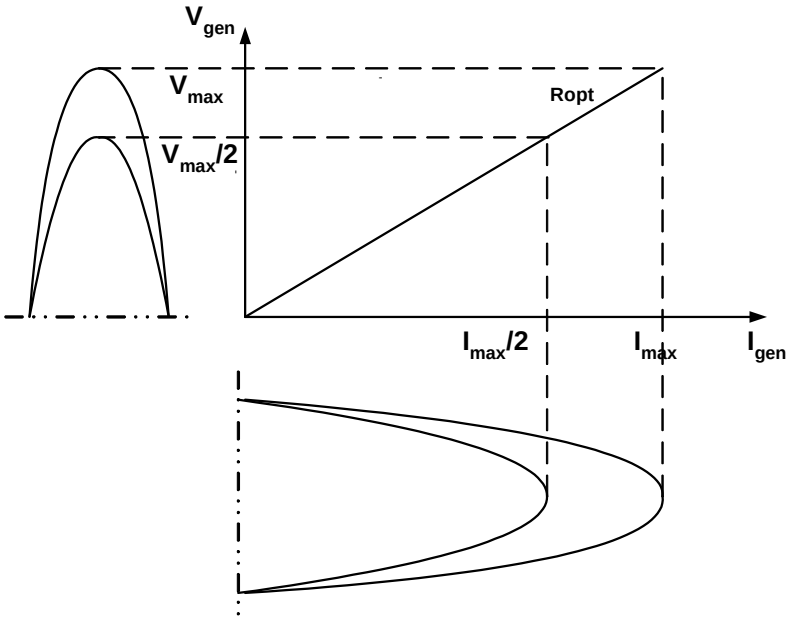


Figure 2.6: The load-line graph for a class B load-line matched amplifier. When the output voltage is at its maximum level the output current is also at its maximum (a result of the load line match). As the output voltage drops the output current also reduces by the same factor.

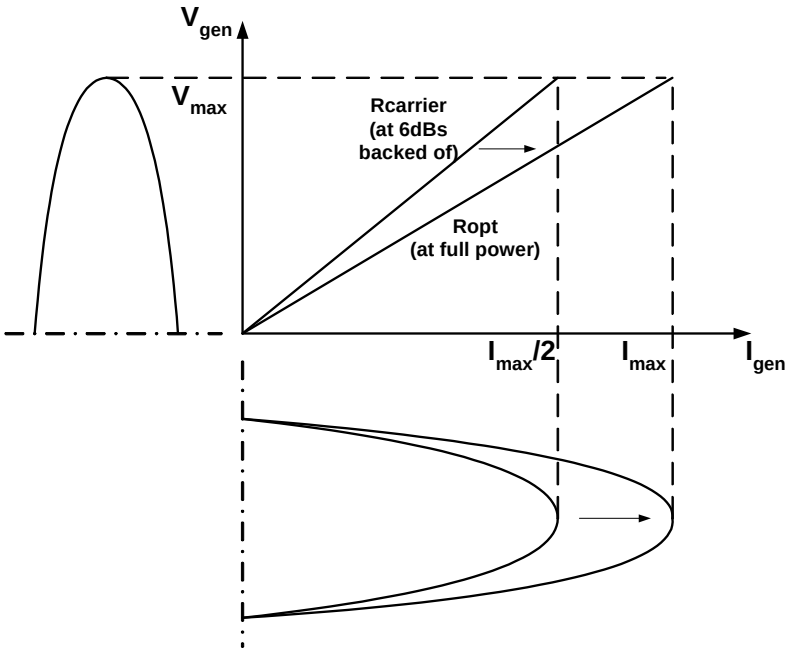


Figure 2.7: This figure demonstrates the required load-line change for the Doherty amplifier. When the carrier amplifier reaches half its maximum current the output voltage is already at its maximum as a result of the choice of $R_{carrier}$. As the power increases further the load-pulling technique is used to change the load-line of the carrier amlifier and prevent the output voltage from saturating.

2.4.2 The Peaking Amplifier and Doherty Network

The amplifier used to provide the current for the load-pulling is called the peaking amplifier. In section 2.3 the load-pulling technique was explained. However, if the carrier amplifier and peaking amplifier are connected in the same way as in figure 2.4 a problem arises. As can be seen from Equation 2.2 when the current from generator 2 (in this case the peaking amplifier) increases the load seen by the carrier amplifier also increases. This is the opposite effect to what is required. As was explained in section 2.4.1 the load seen by the carrier amplifier needs to decrease as the input power increases. To solve this problem a quarter wave transformer is added between the carrier amplifier and the load. This quarter wave transformer acts as an impedance inverter - as the effective load increases (because of the load-pulling action by the peaking amplifier), the load seen by the carrier amplifier decreases. This impedance inverter is the "Doherty network" that can be seen in figure 2.5. In order for the load seen by the carrier amplifier to change from $2R_{opt}$ at 6dBs backed of to R_{opt} at full power, the peaking amplifier must provide no current at 6dBs backed of and a current equal to that of the carrier amplifier at full input power.

2.4.3 Regions of Operation for a Doherty Amplifier

The Doherty operation can be divided into two sections divided according to input power. The first section, the low-power section, is valid at input powers of less than 6dB below PEP. In section 2.4.1 it was explained that with the impedance seen by the carrier amplifier chosen by equation 2.5, the carrier amplifier will reach saturation at 6dB below PEP. In this low-power section the carrier amplifier is not in saturation and no current from the peaking amplifier is

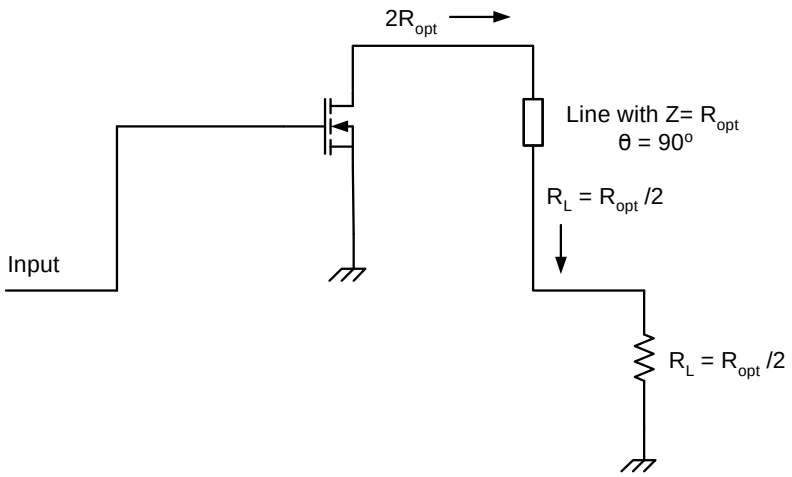


Figure 2.8: Equivalent Doherty amplifier in the low power area of operation. The peaking amplifier is inactive in this area. No load-pulling takes place and the $R_{opt}/2$ load is transformed to the $2R_{opt}$ that is required by the carrier amplifier for this area of operation.

needed for load-pulling purposes. The peaking amplifier is designed so that it is not active during this stage, and is therefore not drawing current. Figure 2.8 shows a representation of the Doherty amplifier in the low-power section. The impedance transformer transforms the $\frac{1}{2}R_{opt}$ load to the $2R_{opt}$ that should be seen by the carrier amplifier according to the design in section 2.4.1.

At input levels higher than 6dBs below the PEP the Doherty amplifier enters a second area of operation. The peaking amplifier now delivers current and load-pulling takes place. Figure 2.9 shows a representation of the Doherty amplifier at full power with the input power level at PEP. For the ideal case the peaking amplifier and carrier amplifier are now delivering equal currents at full power. Due to the load-pull effect the impedance seen by the transformer is R_{opt}. Since the transformer also has an impedance of R_{opt} no transformation takes place and the carrier amplifier sees R_{opt} as required.

2.4.4 Efficiency of a Doherty Amplifier

The Doherty amplifier as described above brings an improvement in efficiency over a classic balanced amplifier design. The carrier amplifier is designed to reach its maximum RF voltage swing at 6 dB before the PEP, and therefore also reaches its maximum efficiency at this point. Only the carrier amplifier is active when the input is more than 6 dB below PEP, with the peaking amplifier inactive and not drawing current. This is the low power area of operation as described in the previous section. The efficiency for this area of operation is given by [10]

$$\eta_{low-power} = \frac{2 * v_{in}}{V_{max}}(\frac{\pi}{4}), 0 < v_{in} < \frac{V_{max}}{2}$$

where v_{in} is the input voltage and V_{max} the maximum output voltage for the transistor. At power input power levels higher than 6 dB before PEP the peaking amplifier becomes active and starts providing current. The efficiency for the high power area of operation is given by [10]

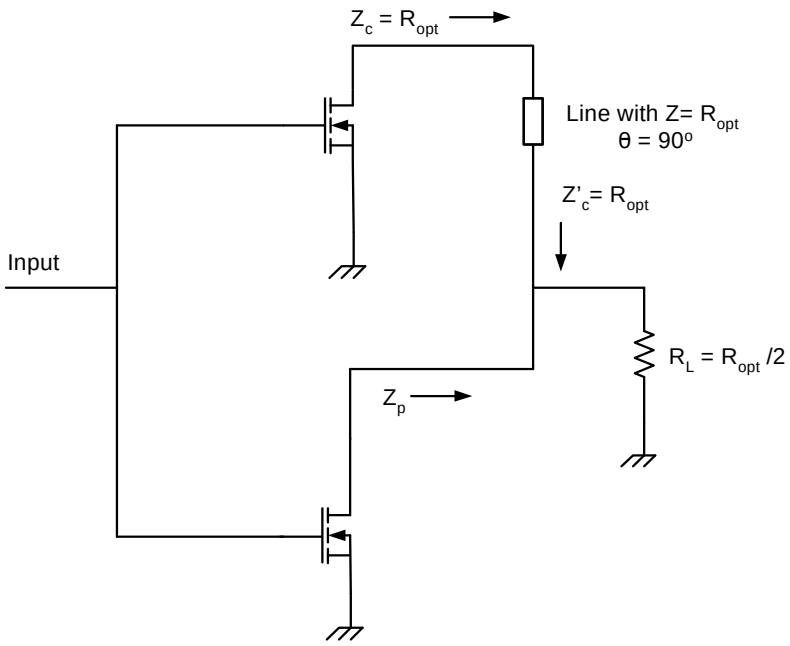


Figure 2.9: Equivalent Doherty amplifier at full power with input power at PEP level. With the load-pulling action provided by the peaking amplifier the quaterwave transformer sees an impedance of R_{opt}. Since the quarterwave transformer also has an impedance of R_{opt} no transformation takes place and the carrier amplifier see R_{opt} as required at PEP.

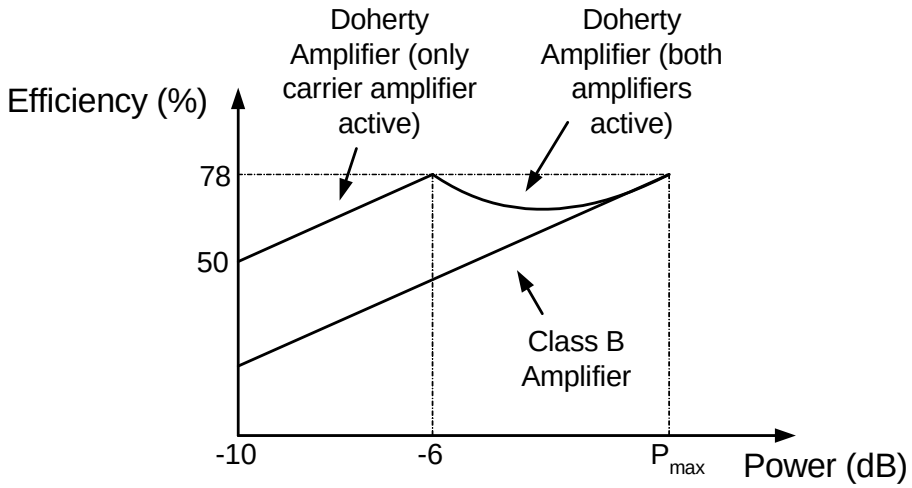


Figure 2.10: Efficiency agianst backed-off input power for a Doherty amplifier and a class B amplifier. At input power levels less more than 6 dB below PEP only the carrier amplifier is active.

$$\eta_{high-power} = \frac{\frac{\pi}{2}(\frac{v_{in}}{Vmax})^2}{3(\frac{v_{in}}{V_{max}})^2 - 1}, \frac{V_{max}}{2} < V_{in} < V_{max}$$

Figure 2.10 shows a graph comparing the efficiency of a Doherty amplifier and a comparable balanced class B amplifier. At PEP the efficiencies are equal, but at backed-off power levels the Doherty amplifier shows an improvement over the balanced amplifier.

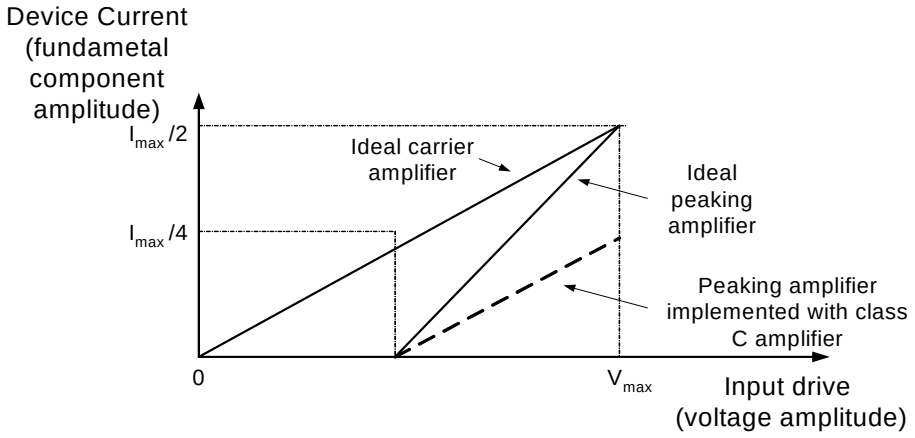


Figure 2.11: The output currents for the carrier and peaking amplifiers in an ideal Doherty amplifier. If the peaking amplifier is implemented using a class C amplifier, however, it won't reach the same output current as the carrier amplifier. This current is indictated on the figure with a dotted line.

2.5 Doherty Amplifier Implementation Problems

The problem in designing a practical Doherty amplifier is achieving the correct behaviour for the two amplifiers, the carrier amplifier and peaking amplifier. Figure 2.11 shows the required currents from the amplifiers for ideal Doherty operation [10]. For the implementation and discussion of the Doherty amplifier in this thesis two identical transistors are used for the amplifier design. A class B amplifier will satisfy the requirements for the carrier amplifier - the challenge arises in controlling the behaviour of the peaking amplifier. The delayed switch-on of the peaking amplifier can be accomplished by making use of a class C amplifier. The main drawback to this approach is that the class C amplifier will not provide enough current at PEP to provide full load-modulation for the carrier amplifier. A further problem is that the phase of the class B amplifier used for the carrier amplifier and the class C amplifier used for the peaking amplifier could differ. The phase has an effect on the load-pulling action as discussed in section 2.3.

2.6 Solutions to the Peaking Amplifier Current problem

The current given at full power by the peaking amplifier must be increased to equal that of the carrier amplifier at PEP, while still keeping its characteristic of only becoming active at an input power of 6 dB below PEP. Two options are investigated, unequal power division and bias adaption.

2.6.1 Uneven Power Division

The RF input power to the Doherty amplifier has to be divided between the carrier amplifier and peaking amplifier. Up to this point it has been assumed that equal power division is used. Using an unequal division could, however, provide a solution to the peaking amplifier current problem. Choosing the division ratio so that the peaking amplifier receives a greater amount of power than the carrier amplifier will result in the current from the peaking amplifier increasing at a faster rate with respect to input power than the current from the carrier amplifier. This is

exactly what is needed to achieve a current closer to that of the ideal current for the peaking amplifier as showed in figure 2.11. A class C configuration can still be used as before to allow the peaking amplifier to only start producing current at 6 dB before PEP. With the current of the peaking amplifier increasing at a faster rate than the carrier amplifier because of unequal power division, equal currents at saturation can be achieved. The design of an unequal power division system is investigated in section 3.11.

2.6.2 Bias Adaption of Doherty Amplifiers

To better emulate the ideal current for the peaking amplifier (as seen in figure 2.11) it would be advantageous to have the peaking amplifier biased as a class C amplifier at low power to control the input power level at which it becomes active. At full power, however, the ideal biasing point for the peaking amplifier is as a class B amplifier in order to provide the same current as the carrier amplifier. This is exactly what bias adaption aims to do by controlling the gate bias voltage of the peaking amplifier dynamically depending on the level of input power to the Doherty amplifier. Figure 2.12 shows a suggested transfer function for such a bias adaption system [10]. In order to create such an adapted bias signal it is neccessary to continously monitor

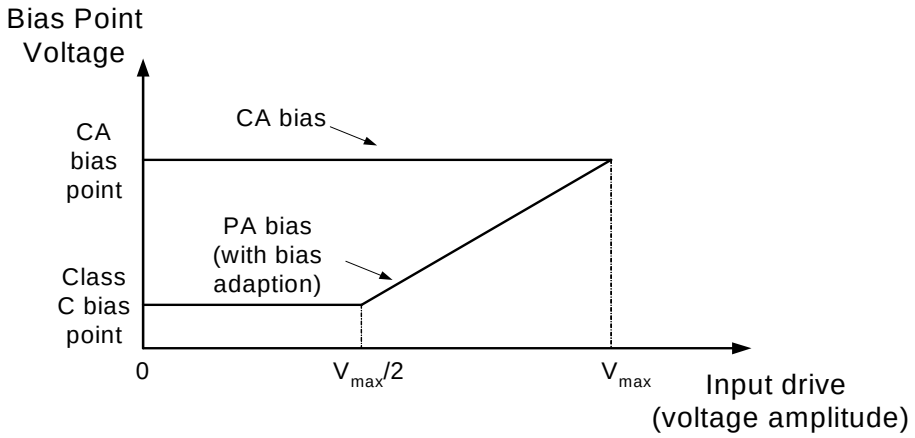


Figure 2.12: Suggested bias adapted scheme for peaking amplifier

the input power level. Because the base-band signal is not available a coupler is added before the Doherty amplifier to sense the input voltage. Figure 2.13 presents a schematic for a bias control system. The bias signal has to change depending on the amplitude of the input signal, but actual RF information is not required for the bias adaption. An envelope detector is therefore used to provide a voltage that is proportional to the input power level. This signal is then manipulated by the bias control circuitry to provide the final bias signal to control the peaking amplifier. A complication of the system is the need to synchronise the changing bias voltage with the input, as the time taken for the signal from the coupler to travel through the envelope detector and through the bias control circuitry must be taken into account. For this reason a delay line is added between the coupler and the Doherty amplifier, to delay the RF input signal so that it arrives at the carrier and peaking amplifiers at the same moment as the changing bias voltage. In Chapter 6 a practical bias adaption system is designed.

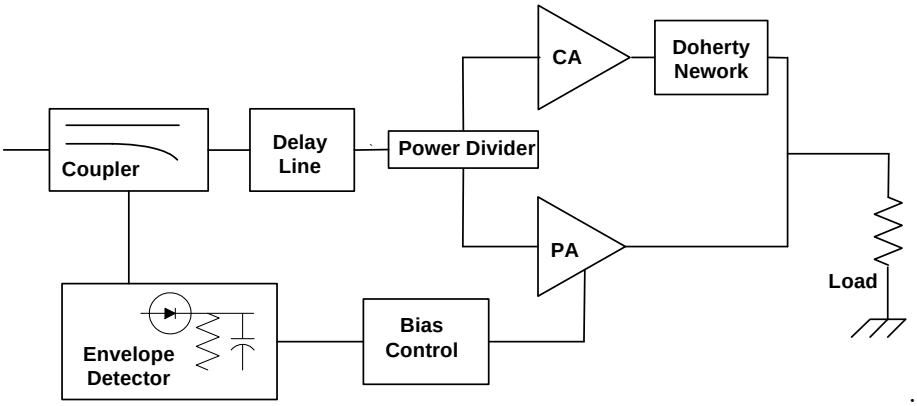


Figure 2.13: Schematic representation of Doherty amplifier with a bias adaption network. The adaption system consists of a coupler to sense the input signal, an envelope detector to extract the envelope from the RF signal and a bias control component to manipulate the voltage to the desired gate voltage values for the peaking amplifier. A delay line is added to synchronise the RF power and the adaption voltage.

2.7 Conclusion

In this chapter the Doherty amplifier was introduced. Load-line matching and load-pulling techniques were discussed in sections 2.2 and 2.3 respectively, while in section 2.4 the operation of the Doherty amplifier is explained. In section 2.4.4 that the improved efficiency of the Doherty amplifier over a balanced amplifier is shown. Finally a problem with the implementation of the Doherty amplifier was pointed out (section 2.5), and solutions to the problem suggested in the form of bias adaption and uneven power division (section 2.6). In the next chapter the design of a Doherty amplifier will be discussed.

Chapter 3

Doherty Amplifier Design

3.1 Introduction

In Chapter 2 the concepts involved in the operation of a Doherty amplifier were discussed. The explanations assumed ideal models for the separate components. In this chapter the design of a practical Doherty amplifier is presented. The Doherty amplifier is to be designed at a centre frequency of 1.6 GHz, using the MRF282 LDMOS transistor for both the carrier amplifier and peaking amplifier. The Rogers 4003 [4] substrate was used for the printed circuit board (PCB) design.

3.2 The MRF282 Transistor

The MRF282 is a 10 W MOSFET transistor. According to its datasheet the MRF282 is capable of handling a maximum DC drain voltage of 26 V. However the available DC sources supply 20 V and are therefore the limiting factor in deciding which drain voltage to use for the design. The transistor was measured at different biasing voltages [8]. Figure 3.1 plots the I_{DS} against V_{DS} curves for the MRF282. From these measurements it can be seen that V_{knee} for the transistor is 6 V . Figure 3.2 plots the I_{DS} against V_{GS} curve for the chosen V_{DC} of 20 V. It can be determined from this graph that the threshold voltage for the transistor is 4 V when it is biased at 20 V. When the voltage at the gate is raised above the threshold voltage the transistor starts producing current. From the same graph the saturation point can also be determined as being equal to 9 V.

3.3 Choosing the Bias Points for the Doherty Amplifier

The ideal behaviour of the Doherty amplifier was described in section 2.4. The two amplifiers involved, the peaking amplifier and carrier amplifier, were assumed to have ideal behaviour for the requirements of the Doherty amplifier. By carefully choosing the different bias points for the peaking amplifier and carrier amplifier the transistor amplifiers can approximate this ideal behaviour. In the next sections the requirements for each amplifier and the subsequent choice of bias points will be discussed.

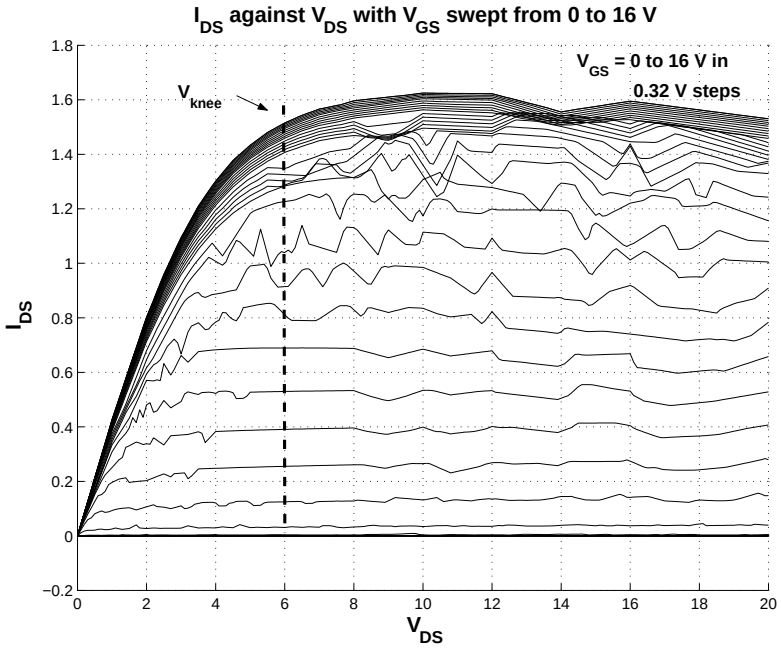


Figure 3.1: I_{DS} against V_{DS} measurements for various V_{GS} demonstrating the V_{knee} voltage for the MRF282 transistor. [8]

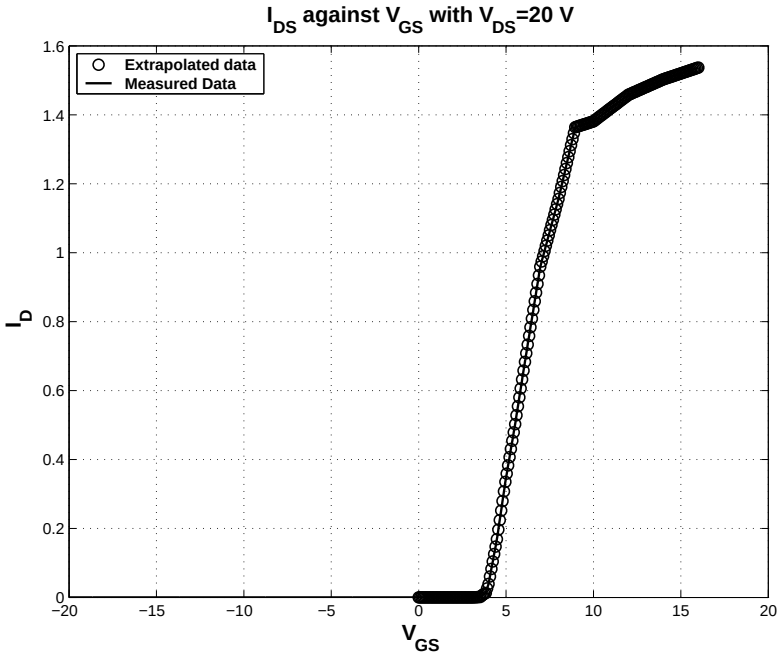


Figure 3.2: Measured and extrapolated I_{DS} vs. V_{GS} curves for the MRF282 transistor with V_{DS} equal to 20 V [8]

3.3.1 Bias Point for the Carrier Amplifier

As explained in section 2.4.3 only the carrier amplifier is active in the low power region of operation. It is therefore required to have a linear gain throughout this region. The low power region was defined as the area of operation with input powers less than 6dB below the peak envelope power (PEP). In chapter 2 the use of a class B amplifier was assumed for all explanations. How-

ever, from figure 3.2 it can be seen that the behaviour for the MRF282 around the threshold area is not completely linear. A class AB design will therefore be more linear than a class B design as the amplifier will operate in the linear region away from the threshold area even for very small signals. The MRF282 datasheet also suggests using the transistor in a class AB or class A configuration. According to Cripps [10] the bias point for a "mid"-class AB amplifier is given by

$$V_G = 0.25 * V_s + V_{threshold} \tag{3.1}$$

where V_S is the maximum allowed voltage swing for the transistor. This maximum voltage swing can be determined as 5 V given the values for threshold voltage (4 V) and saturation voltage (9 V) as determined in section 3.2. Equation 3.1 results in a V_G biasing voltage of 5.25V for the carrier amplifier.

3.3.2 Bias point for the peaking amplifier

The ideal operation for the peaking amplifier was detailed in section 2.4.2. For ideal operation the peaking amplifier has to be inactive in the low-power region, only becoming active when an input power level of 6dB before PEP is reached. To achieve this characteristic of only being active in the high-power region, the transistor is biased in class C mode. This means that the gate biasing voltage is below the threshold of the transistor at low power. When the input voltage reaches a certain level the voltage becomes higher than the threshold voltage and the transistor enters its active area. According to Cripps [10] the bias point for a "mid"-class C amplifier is given by

$$V_G = -0.5 * V_s + V_{threshold} \tag{3.2}$$

resulting in a V_G voltage of 2.5V for the peaking amplifier. The actual gate voltage used for the peaking amplifier was 2 V, a slightly deeper class C configuration. As was discussed in section 2.5, the problem with using a class C configuration is that although the peaking amplifier becomes active at the input power level, it does not deliver enough current at full power.

3.4 Determining the Optimum Load-Line Resistance

The design of a load-line amplifier was discussed in section 2.2, with a formula to determine the ideal load-line match given in equation 2.1. However, this equation was based on an ideal transistor model. For a transistor with a non-negligible knee voltage the equation must change to take the knee voltage into account [10]

$$R_{opt} = \frac{V_{dc} - V_{knee}}{I_1} \tag{3.3}$$

With V_{DC} and V_{knee} determined in section 3.2 as 20V and 6V respectively the only unknown is the fundamental current I_1. The maximum voltage amplitude for a sine wave at the gate terminal can be determined by

$$V_{sinemax} = V_{sat} - V_G \tag{3.4}$$

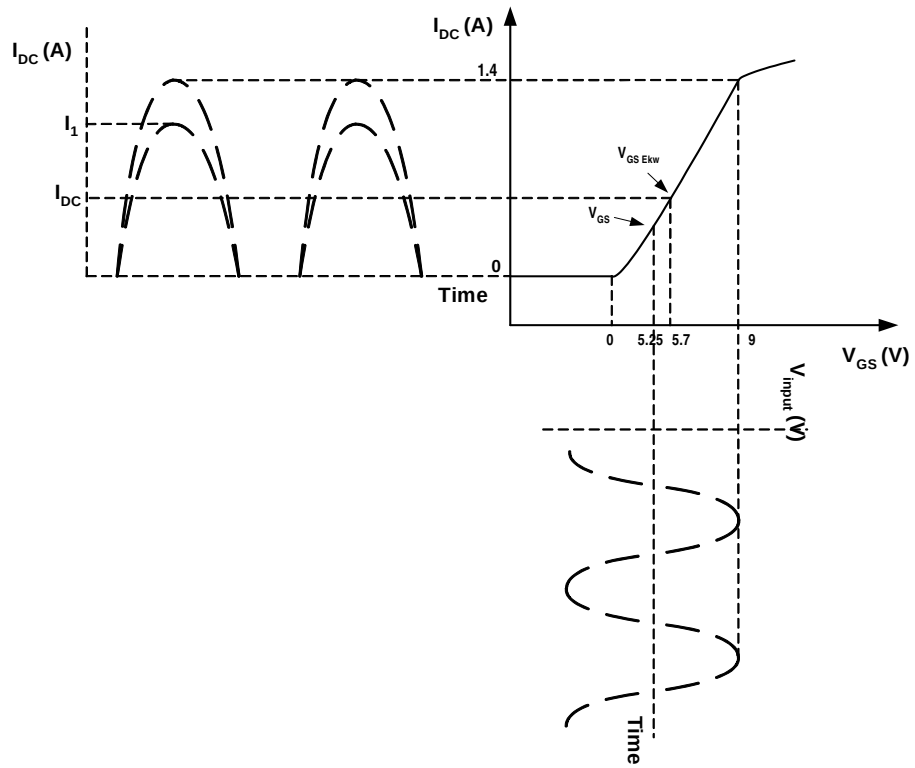


Figure 3.3: The I_{DS} vs. V_{GS} curve for the MRF282 transistor with V_{DS} equal to 20 V is used as a transfer function to calculate the resulting drain current at PEP. Fourier analysis can then be done to determine the fundamental current I_1. The figure also shows the dc component of the drain current and the equivalent gate bias point for the class AB configuration used in the design of the carrier amplifier.

For the carrier amplifier this results in a maximum input amplitude of 3.75 V and a maximum of 7 V for the peaking amplifier. Matlab software is now used to determine the fundamental currents at full power for the peaking amplifier and carrier amplifier [8]. The software uses the measured V_G against I_D curve as a transfer function to determine the drain currents given a sine wave input with the maximum amplitude. A Fourier analysis can then be done to determine the fundamental currents. Figure 3.3 illustrates the method with the help of a diagram. The resulting fundamental currents is used to determine the R_{opt} for the amplifiers by applying Equation 3.3. The R_{opt} is found to be 18.53 Ω for the carrier amplifier and 21.56 Ω for the peaking amplifier.

3.5 Taking the Extrinsic Transistor Parameters into Account

The ideal load-line resistance, R_{opt}, has been determined. This is the impedance that should be seen when looking from the drain terminal of the transistor. The transistor is a packaged device however, and at the design frequency the package parasitics and line lengths are not negligible. The extrinsic network in figure 3.4 represents the package parasitics. The values for these extrinsic parameters are extracted using a multi-bias direct extraction method [20]. The series extrinsic parameters are determined by using cold S-parameter data with the gate biased below pinch-off. The question is what impedance is needed at the output of the package so that the drain terminal still sees R_{opt}? This impedance is indicated in figure 3.4 as Z_{opt}. It seems a simple way to calculate this would be to determine the impedance looking back at the transistor

package and use a conjugate match to determine Z_{opt}. This is in fact not correct because of the series resistance contained in the extrinsic network. A numerical technique is used in Matlab to determine Z_{opt}. [8]

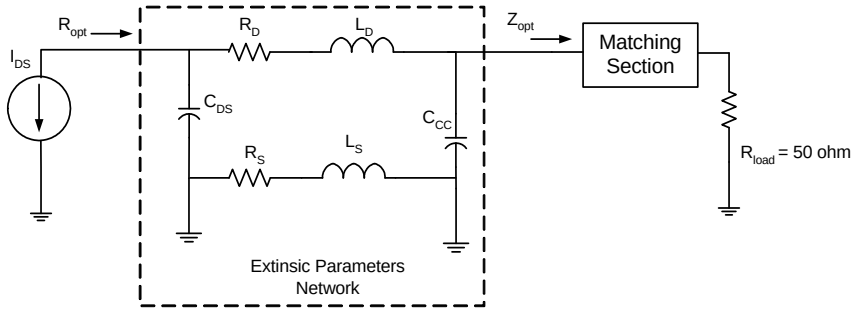


Figure 3.4: A numerical technique is used to determine Z_{opt}, the impedance that needs to be presented at the output of the transistor terminal so that the generator I_{DS} sees the optimal load-line impedance R_{opt}.

3.6 Small Signal Model for Design

A large-signal model that is accurate for all areas of operation was not available for the design. Therefore a small-signal model of the transistor was used. This model is calculated from the measured data for the MRF282 [20]. In order to make a better approximation of the large signal behaviour, the small-signal model was not based on measurements at the bias point of the transistor. Instead the equivalent bias point at full power is calculated and the measurement data for the MRF282 at this bias point is used in the extraction of the small-signal model. In section 3.4 the fundamental current at full power was calculated for the peaking amplifier and carrier amplifier. The DC component of the drain current can also be determined by calculating the average of the drain current over time. Once the DC component is known the V_G against I_D curve can be used to determine the equivalent gate bias voltage of the amplifier. The determining of the dc component is demonstrated in figure 3.3 for the case of the carrier amplifier. Figure 3.5 presents the small signal model for the class AB configuration used in the carrier amplifier design. The small signal model for the class C configuration is extracted in the same way.

3.7 Stabilisation

Stabilisation is an important part of power amplifier design. Not only could oscillations from an unstable transistor result in incorrect working of an amplifier, but these oscillations could reach high power levels and could be potentially damaging for equipment connected to the amplifier. One way to test for unconditional stability is by using Rollet's stability factors [16]

$$K = \frac{1 - \mid S_{11} \mid^2 - \mid S_{22} \mid^2 + \mid \Delta \mid^2}{2 \mid S_{12} S_{21} \mid} \tag{3.5}$$

$$\Delta = \mid S_{11} S_{22} - S_{12} S_{21} \mid \tag{3.6}$$

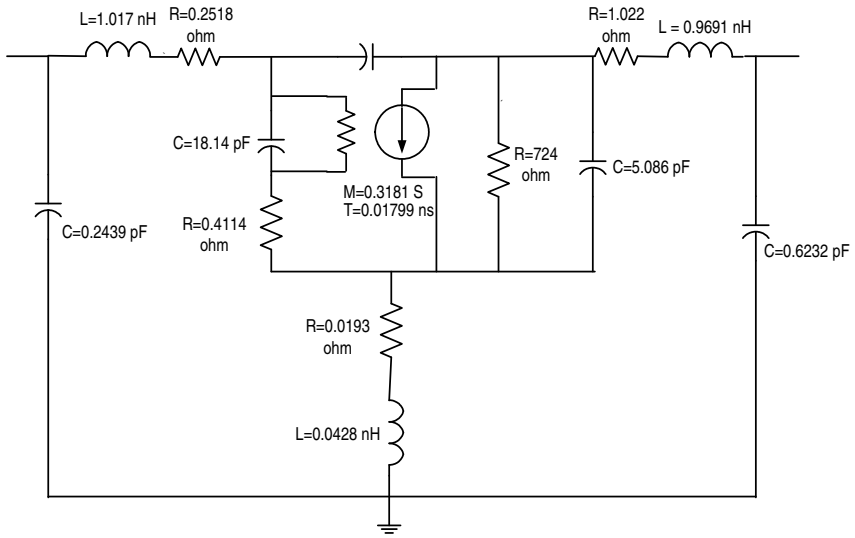


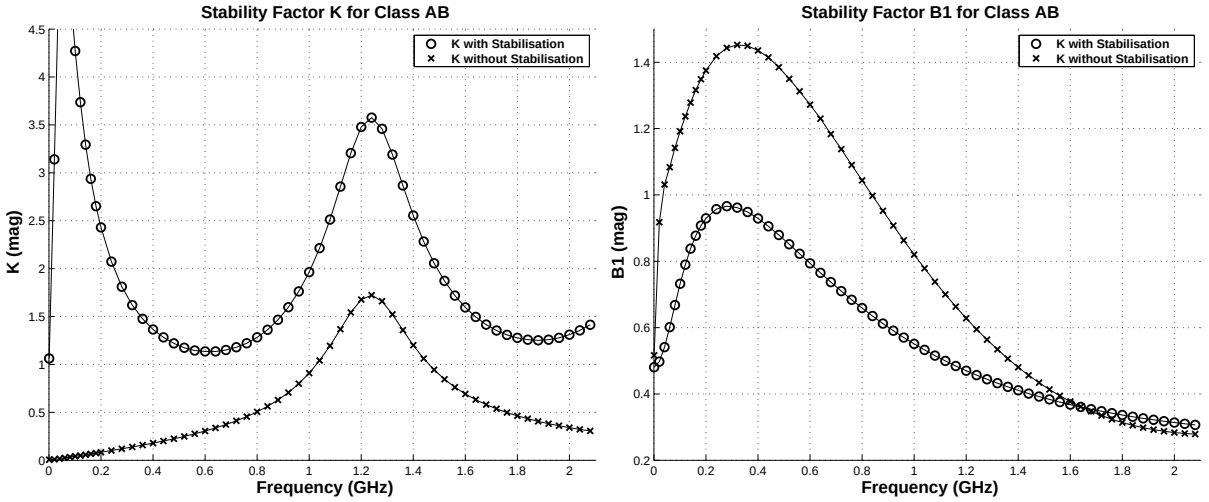
Figure 3.5: The small-signal model for the Class AB amplifier used in the carrier amplifier. The model is based on the measured characteristic of the MRF282 at a voltage equal to the sum of the bias voltage and the dc component of the input signal at full power.

B_1 is an auxiliary stability factor defined as

$$B1 = 1 + \mid S_{11} \mid^2 - \mid S_{22} \mid^2 - \mid \Delta \mid^2 \tag{3.7}$$

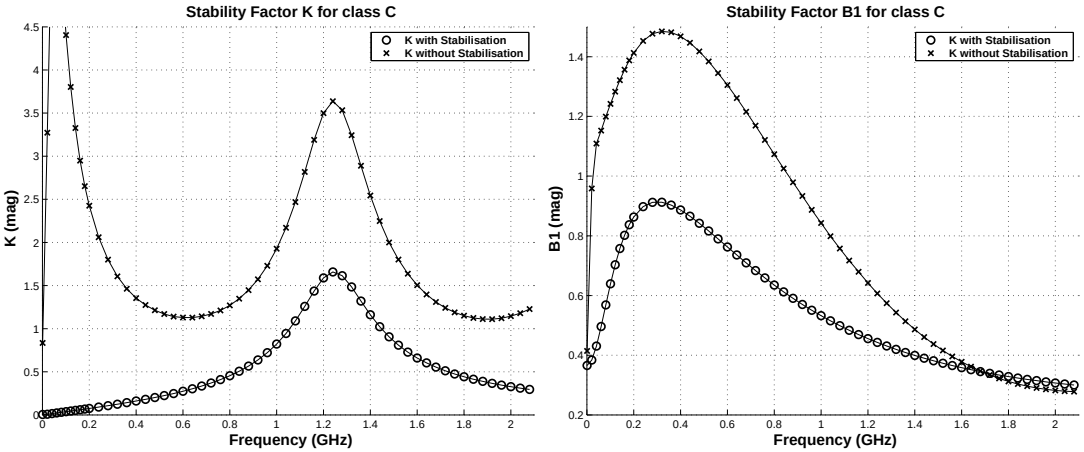
Unconditional stability for the amplifier is assured if $K > 1$ and $B_1 > 1$. The stability must be investigated over a wide frequency range as the amplifier can oscillate at frequencies different to the design frequency. At lower frequencies the transistor is especially vulnerable because the available gain is higher in this area. At high frequencies when the gain drops to less than 1 stability is less of a problem. The frequency range considered for the analysis stretches from 1 MHz to 2 GHz. The small-signal networks extracted in section 3.6 for the peaking amplifier and carrier amplifier are used to test the stability for the amplifiers. This small-signal model is used to extrapolate data down to the 1 Mhz frequency, since the lowest frequency at which the device was characterised was 400 Mhz.

In figures 3.6 and 3.7 it can be seen that the K and B_1 calculated by equations 3.5 and 3.7 for the unstabilised amplifiers is less than 1 for both amplifiers over a large area of the frequency domain. This means that the amplifiers are not unconditionally stable. To ensure stability a stabilisation network is added (see figure 3.10 for the stabilisation networks used). The idea is to add loads in parallel at the input and output of the amplifier. Some of the energy will flow into these loads reducing the gain in the system and therefore its tendency to be unstable. However, only the available gain at the design frequency is of importance. Using reactive elements in the network allows us to change the stability loads as a function of frequency. The network can therefore be optimised to ensure stability at all frequencies while attempting to minimize the impact on gain at the design frequency. In figure 3.8 the layout for the carrier amplifier stabilisation network is shown along with the variables used in the optimisation process. It was discovered that the stability and gain factors are especially sensitive tot the transistor input and output lines (see figure 3.8) Performance increased as the length of these lines were minimised. The lines were therefore made as short as possible while still allowing for the correct footprint



(a) Stability factor K (b) Auxillary stability factor B1

Figure 3.6: The Rollet stability factor K and the auxiliary stability factor B1 for the class AB amplifier (the carrier amplifier) with and without the stability network. The stabilized amplifier has a $K > 0$ and $B_1 > 0$ as can be seen from the graphs, meeting the conditions for unconditional stability of the amplifier.



(a) Stability factor K (b) Auxillary stability factor B1

Figure 3.7: The Rollet stability factor K and the auxiliary stability factor B1 for the class C amplifier (the peaking amplifier) with and without the stability network. The stabilized amplifier has a $K > 0$ and $B_1 > 0$ as can be seen from the graphs, meeting the conditions for unconditional stability of the amplifier.

size for the MRF282 transistor. Figure 3.9 shows the S_{21} for the peaking amplifier and carrier amplifier with and without their stability networks, while the stability factors K and B_1 for the stabilised amplifiers can be seen in figures 3.6 and 3.7. As shown in the figures the stability factors are now above the required conditions for unconditional stability for both amplifiers, without a loss of gain at the design frequency.

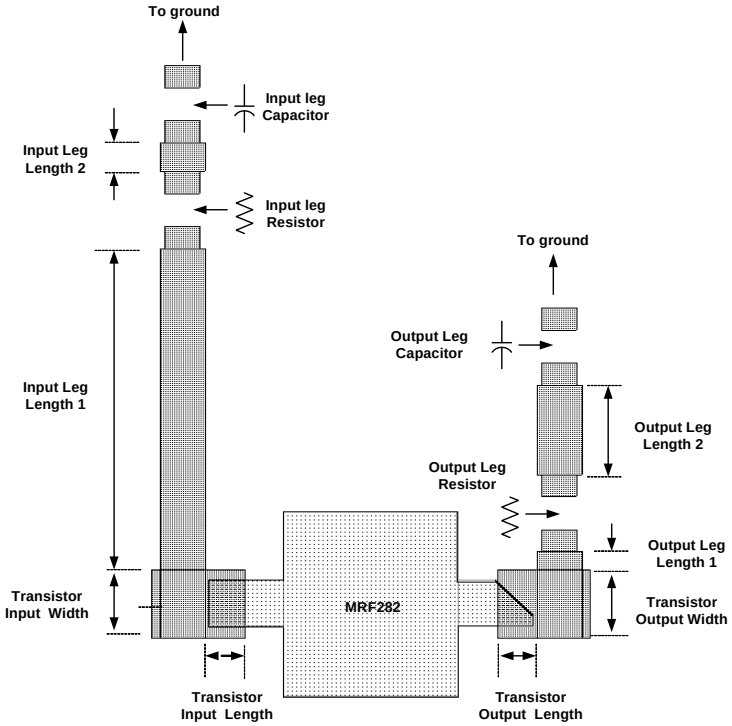
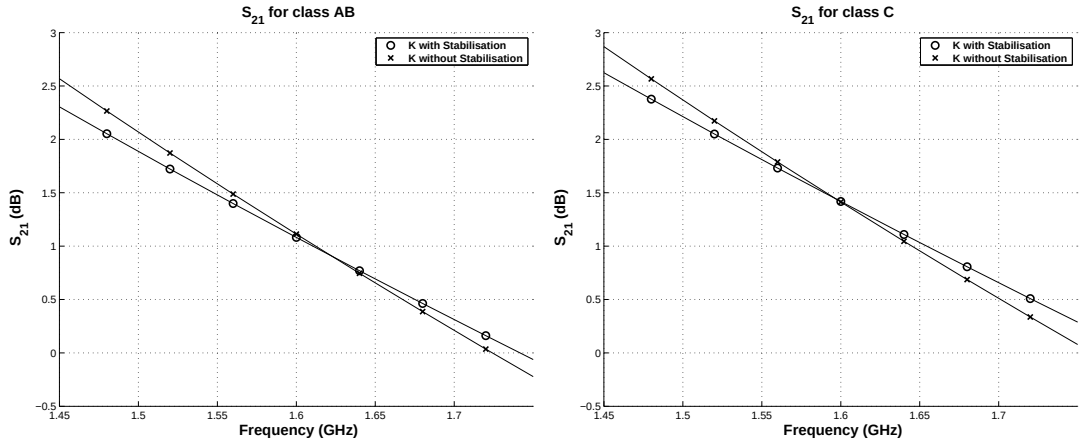


Figure 3.8: The stability network for the carrier amplifier, showing the optimisation variables. These variables where adjusted to achieve unconditional stability while attempting to keep the gain uncompromised at the design frequency. The same variables where used in optimising the network for the peaking amplifier

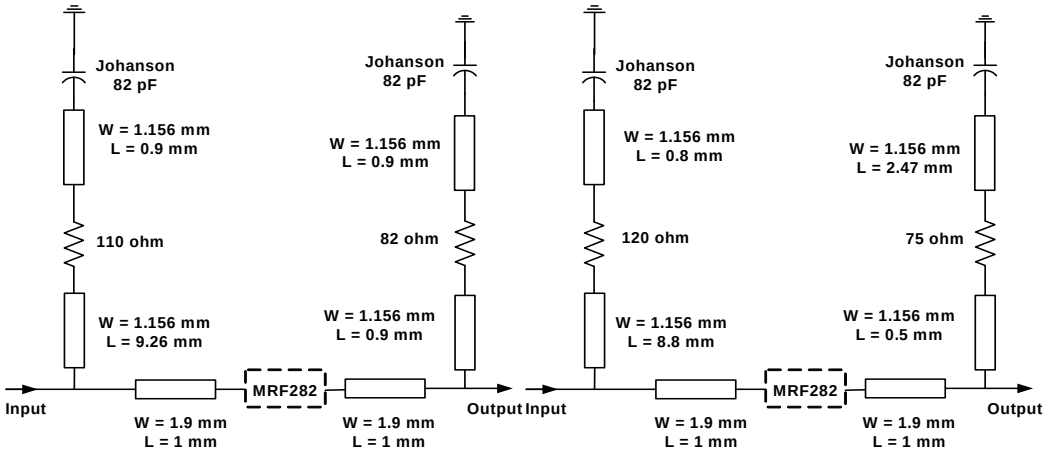


(a) Stability factor K (b) Auxillary stability factor B1

Figure 3.9: These figures demonstrate the S_{21} for the peaking amplifier and carrier amplifier with and without the stability networks. The stability networks were optimised so that no gain is lost at the design frequency.

3.8 Biasing Networks

Biasing networks are used to provide the amplifier with a gate voltage and drain biasing current. They allow the DC current to pass through while isolating the DC supplies from the RF signal. In the next two sections we will look at the design of these networks. The same biasing networks were used in the carrier amplifier and the peaking amplifier.



(a) carrier amplifier stability network (b) peaking amplifier stability network

Figure 3.10: The stability networks for the carrier amplifier and peaking amplifier amplifiers..

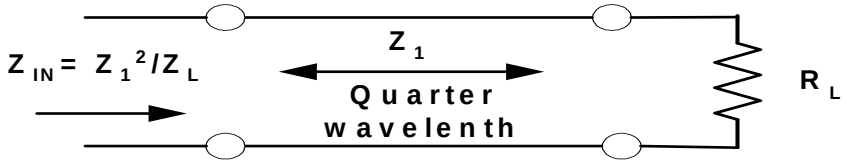


Figure 3.11: A quarterwave transformer with the resulting input impedance impedance Z_{IN} given . [16]

3.8.1 The Drain Bias Network

As discussed in section 3.2 the transistor will be biased with a voltage of 20 V at the drain terminal. The drain bias network serves a dual purpose. The first is isolating the bias source from the RF path at the design frequency. At the same time the bias network contains capacitors which can supply the rapidly changing demand of drain current from the transistor. The DC source is connected to the amplifier with physically long wires with a lot of inductance that make it impossible for the DC source to respond to the fast changing current requirements of the transistor. Figure 3.13 shows the drain bias networks used for the amplifiers. With the drain bias point at 20V the RF swing of the output voltage can alternate between 0 V and 40 V at full power. The large capacitor used must therefore be able to handle in excess of 40V. A electrolytic (63 V, 470 uF) capacitor was used for this purpose. A quarter wave length followed by capacitors to ground is used to achieve the required isolation. The impedance seen when looking into a quarter wave transformer is given by [16] (see figure 3.11)

$$Z_{in} = \frac{Z_1^2}{R_L}$$

In the drain bias circuit of figure 3.13 the resistance R_L approaches zero at high frequency because of the capacitors to ground. The impedance seen into the biasing network from the transistor is therefore very large and looks like an open circuit for the RF signal. The width of the line is kept as small as possible to further increase the impedance seen from transistor. The ideal value for the 2 capacitors to ground was determined by optimisation in Microwave

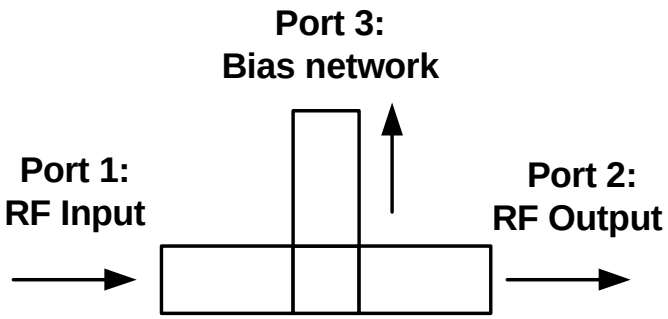


Figure 3.12: A definition of three ports for the optimisation of the biasing networks. [16]

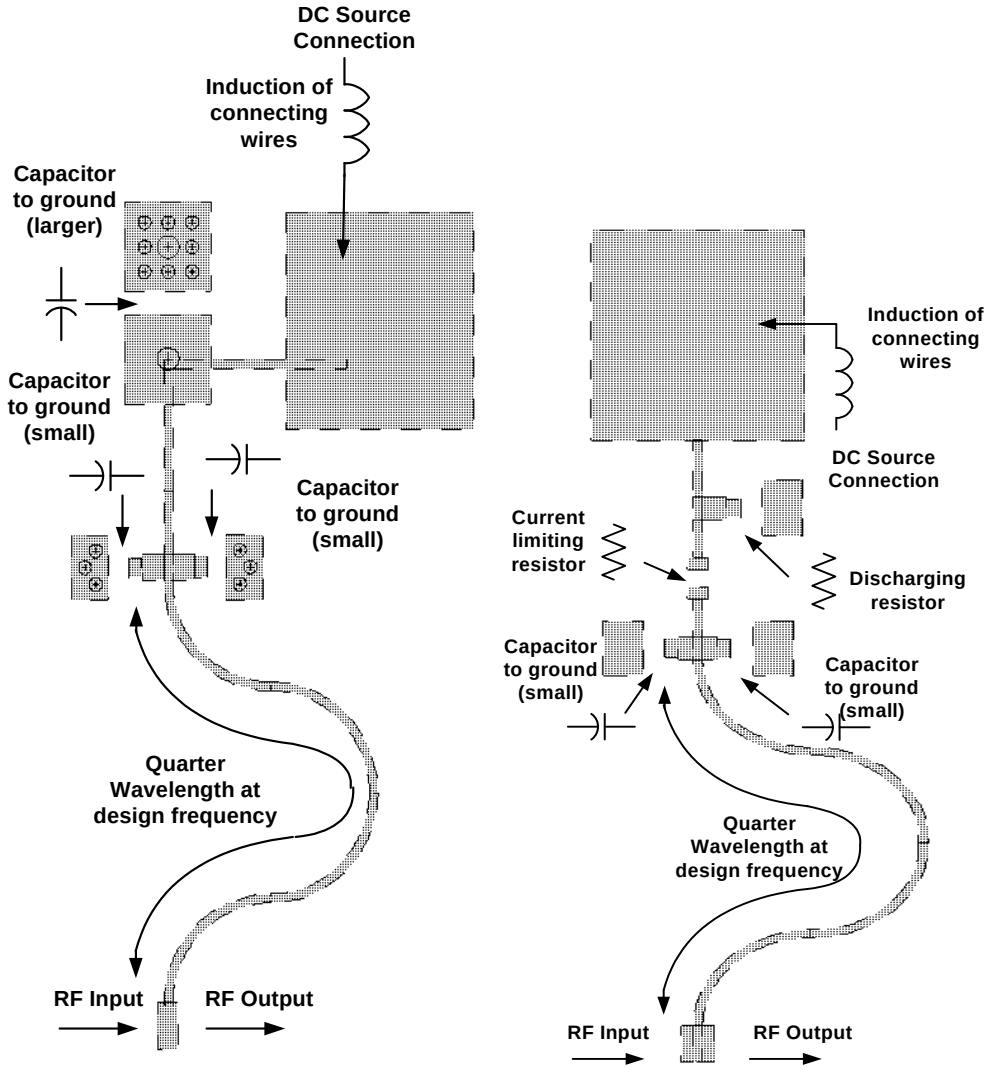
Office (MWO). In figure 3.12 three ports are defined describing the connection between the bias network and the amplifier. The criteria for the optimisation was to keep S_{31} (the RF isolation for the bias network) while ensuring that S_{21} (the RF path) stays as close as possible to unity. An 0603 33 pF Johanson capacitor was used as it was the closest value available to the optimum capacitance. The bias network as designed here resulted in parametric oscillation problems for the amplifier designs. These problems and the solutions there-off are addressed in section 4.7. It should be noted that the parametric oscillations could not be predicted with the stability calculations presented in section 3.7, possibly because the extrapolated data at low frequencies was inaccurate.

3.8.2 The Gate Bias Network

The gate biasing network does not need to deliver any current. Its purpose is only to keep the gate voltage at the required level. The RF isolation requirements as discussed in the previous section for the drain biasing network are also applicable here. The same quarter wave network can be used as in the drain bias network. The gate bias network can be seen in figure 3.13. Because the gate bias network does not have to deliver current the large electrolytic capacitor is not needed. A further difference between the gate and drain bias networks is the addition of 2 resistors. The first of these resistors is added in the bias path as a current limiter to protect the transistor. However as no current flows through the network under normal circumstances there is no voltage drop over the resistor and the gate voltage is not influenced. The second resistor is added to ground too allow for the discharging of electrostatic charges built up over time. A large value resistor in the order of mega ohms is used for this resistor.

3.9 Output Matching Networks

In section 3.4 we determined the optimum loads to be seen by the transistors. Then in section 3.5 we took the extrinsic parameters of the transistor into account and calculated Z_{opt}, the impedance we need to present at the output of the transistor (see figure 3.4). A stabilisation network (section 3.7) and a bias network (section 3.8.1) was added which also influence the output impedance. Figure 3.14 shows a schematic representing the Doherty amplifier at full power. Matching sections have been added in order to match the output impedance of the amplifiers to the intermediary impedance R_O. In the next 2 sections we will look at the design



(a) Drain Biasing Network (b) Gate Biasing Network

Figure 3.13: The drain and gate biasing networks for peaking amplifier and carrier amplifier. RF isolation is provided with a quarterwave transformer grounded with capacitors at high frequency. For the drain network a large electrolytic capacitor allows the provision of fast changes in current demands from the transistor. In the gate network resistors provide current limit protection and a route for the discharge of electrostatic energy.

of these matching sections. R_O was chosen as 80 Ω. In section 3.9.3 the reasons for this choice and implications thereof will be discussed. The load presented (as seen in figure 3.14) to the Doherty amplifier must be equal to $\frac{1}{2}R_0$ (40Ω in this case) for the load-pulling scheme to work correctly.

3.9.1 Carrier amplifier

For the carrier amplifier R_{opt} was determined to be 18.53 Ω. To achieve this impedance at the drain terminal a matching section was designed and optimised in Microwave Office. A LC type matching network was used with a capacitor to ground and a length of line providing the inductive part of the matching circuit. A DC blocking capacitor needs to be added in the output path of the amplifier. This capacitor was included in the opitimisation process. Figure

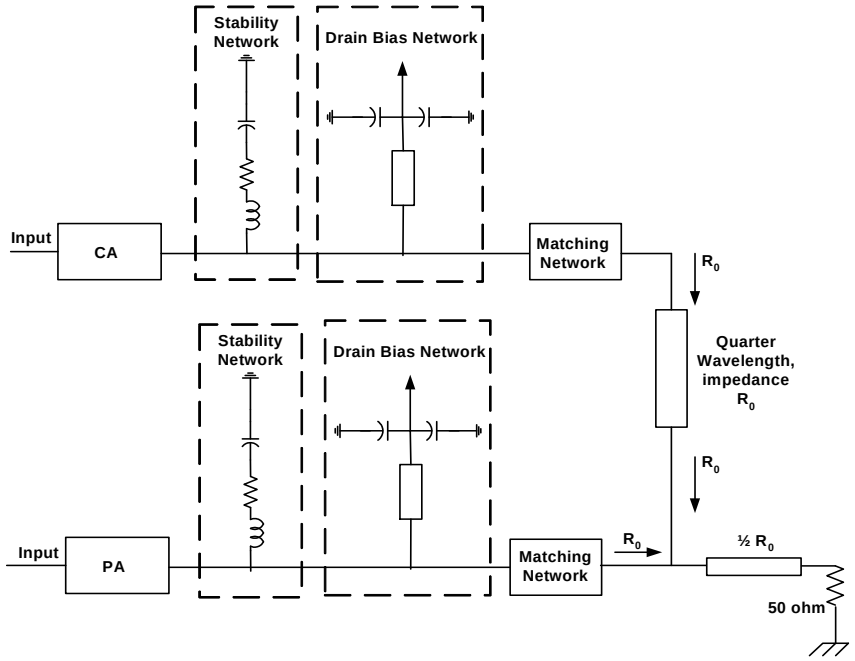


Figure 3.14: The output network of the Doherty amplifier, with matching sections to match the output from the carrier amplifier and peaking amplifier to R_O.

3.15 shows the resultant matching section and the layout used for the optimisation process. The variables optimised where the capacitance values of the DC blocking series capacitor and capacitor to ground, as well as the matching line length and width. The capacitors used where 0603 components from Johanson. For the simulation Johanson's measurement parameters where used in conjunction with a improved model developed in section 4.2.3. The optimisation goal

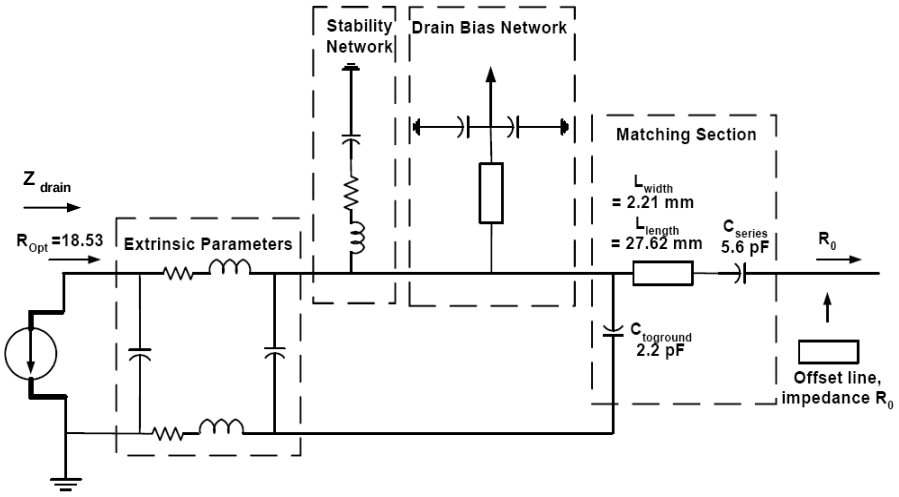


Figure 3.15: The output matching network for the carrier amplifier. The DC blocking capacitor needed is included in the matching network. The location of the offset line added to correct the low power matching characteristics is also indicated.

was to present the drain terminal with the impedance R_{opt} at the design frequency with as large a bandwidth as possible.

At low power Z_{drain}, the impedance seen by the drain terminal of the amplifier, should be

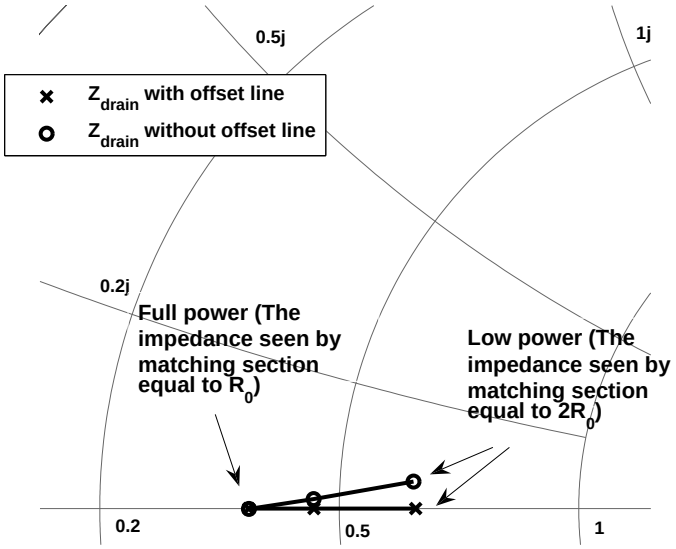


Figure 3.16: The impedance seen by the drain terminal of the carrier amplifier as it changes with different loads. At full power the matching section transforms the R_O impedance to R_{opt}. At low power the matching section sees $2R_O$. It does not transform to $2R_{opt}$, however, and requires an extra offset line with impedance R_O to maximise the real part seen by the drain terminal.

$2R_{opt}$ for correct Doherty operation (see section 2.4). The peaking amplifier is giving no more current and therefore the load seen by the quarterwave transformer is equal to $\frac{1}{2}R_O$. This is then transformed so that the impedance seen by the matching section just designed is $2R_O$. However, Z_{drain} is not equal to $2R_{opt}$ (37.06 Ω) as was expected, but is equal to 31.23 + 2.45j Ω at low power. Figure 3.16 plots the impedance seen from the drain terminal for different load impedances varying from R_o (at full power) to $2R_{opt}$ (at low power) on a Smith chart. The fact that the imaginary value is so small (2.45j Ω) was made possible by the careful choice of the impedance R_O. This choice is discussed further in section 3.9.3. The imaginary component can be moved unto the real axis through the addition of a extra offset line with impedance R_O to the end of the matching network [22] [9]. At high power this offset line will have no influence due to the fact that its impedance R_O is the same as what is being presented to the matching network. At low power however the offset line does have an effect, as can be seen from figure 3.16. The resultant impedance for Z_{drain} at low power is now 31.51 + 0.09i. The offset line has therefore moved Z_{drain} closer to the ideal impedance of $2R_{opt}$ when the amplifier is at low power. In figure 3.18 the real and imaginary parts of Z_{drain} is shown against frequency at full power and at low power.

3.9.2 Peaking amplifier

The matching for the peaking amplifier amplifier was done in a similar manner to the carrier amplifier. At full power the amplifier also sees R_O. Figure 3.17 shows the matching network

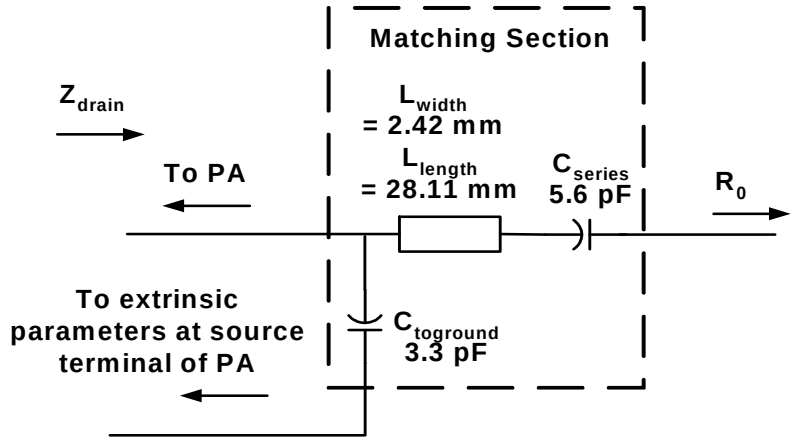


Figure 3.17: The output matching network for the peaking amplifier.

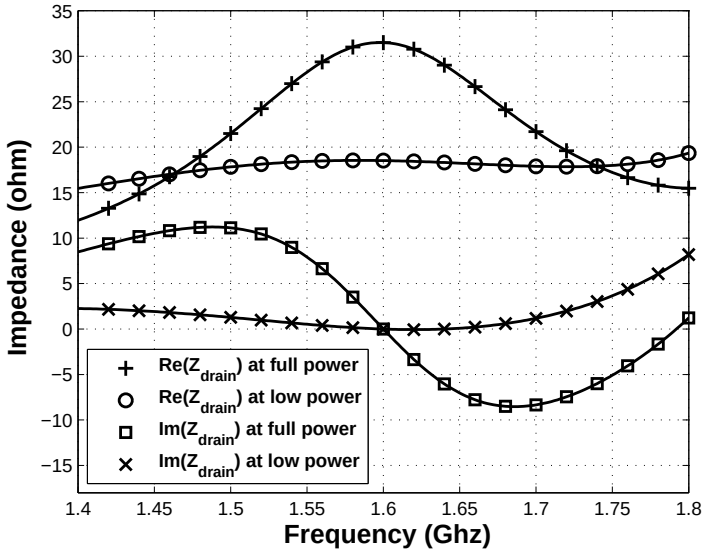


Figure 3.18: The impedance seen from the drain terminal of the carrier amplifier after the matching network and offset line is added. The real an imaginary parts are shown at full power (with R_O presented to the matching network) and low power (with $2R_O$ presented to the matching network)

for the peaking amplifier amplifier, while the resultant Z_{drain} impedance against frequency can be seen in figure 3.19. A potential problem arises with the impedance seen looking back at the peaking amplifier from the load. According to the Doherty design (see section 2.4) the peaking amplifier is supposed to be inactive with the input power at 6dB below PEP. It was assumed that when the amplifier was inactive its output impedance would be infinite. This impedance is seen in parallel to the load by the carrier amplifier, so if it is not infinite some power will be lost. Figure 3.20 shows the output impedance for the amplifier design. The impedance at the design frequency is 470 Ω, which although not infinite is significantly larger than the load impedance. If this were not the case an offset line can be added to shift the phase of the impedance until the maximum of the real part coincides with the design frequency. In this way the imaginary part of Z_{drain} will also be minimised. Figure 3.20 demonstrates the effect of 2 such offset lines, a 6mm line (18.6 degrees of phase offset) and a 55mm line (170.1 degrees of phase offset) on the real part of the impedance. The Smith chart in figure 3.21 can more easily explain what

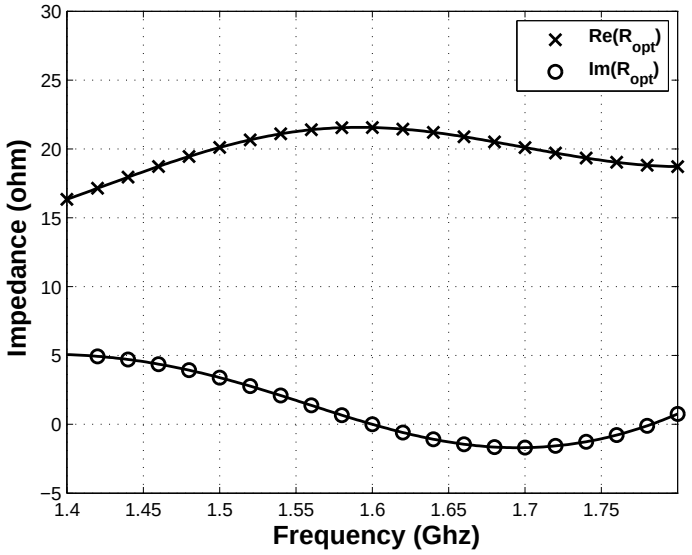


Figure 3.19: The impedance seen from the drain terminal of the matched peaking amplifier against frequency at PEP.

is happening. As the length of the offset line is increased the impedance moves in a clockwise direction on circle centered on the 1.6 Ω point (the normalised impedance of the 80Ω line R_O). In the case of this design the offset line is not needed as the real part of the output impedance is already close to the maximum achievable. This is the result of the choice of R_O and is discussed in the next section.

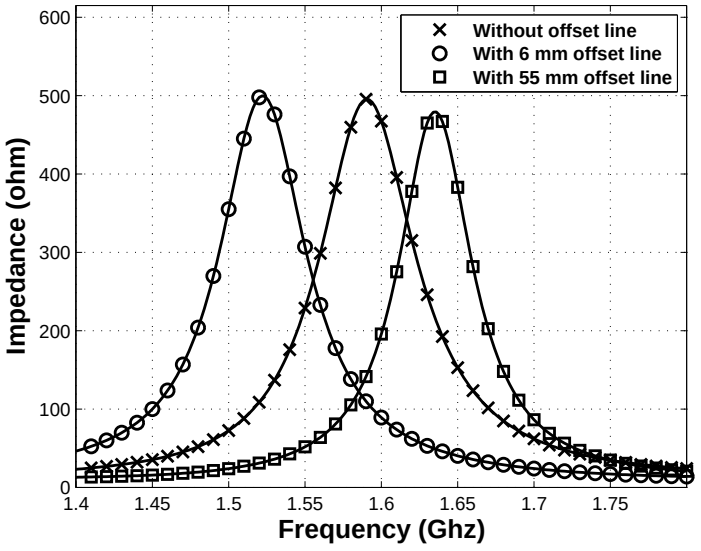


Figure 3.20: The impedance seen looking when looking back to the peaking amplifier from the load after the matching network is added. The effect of adding 6mm and 55 mm offset lines with impedance R_O is shown.

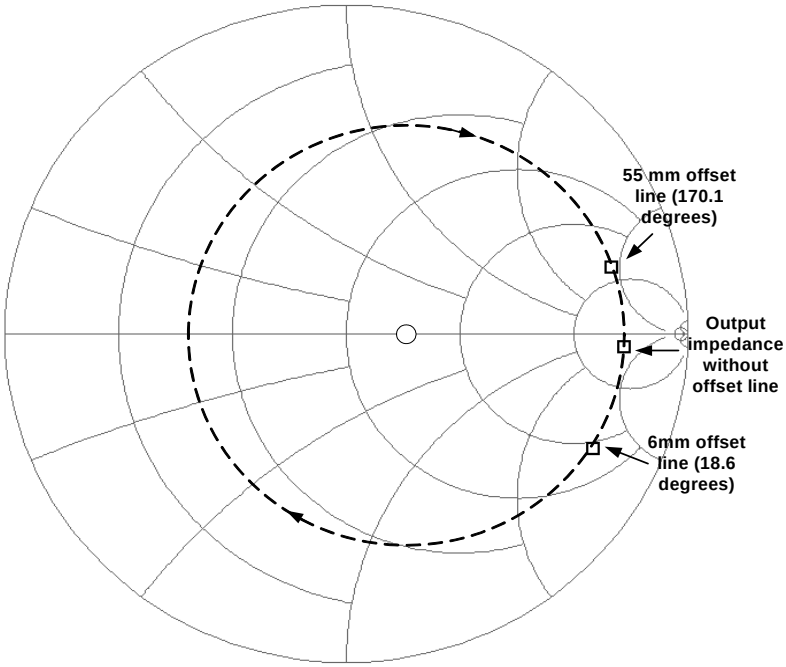


Figure 3.21: The impedance seen looking when looking back to the peaking amplifier from the load after the matching network is added. Adding offset lines of impedance R_O moves the impedance in a clockwise direction around the 1.6 point (R_O normalised on the 50 Ω Smith chart).

3.9.3 Choice of R_0

As mentioned in sections 3.9.1 and 3.9.2, the choice of the intermediate matching impedance R_O has an influence on the matching sections and the length of the required offset lines. In section 3.9.1 it was explained that the Z_{drain} of the carrier amplifier can be tuned at low power through the addition of an offset line with impedance R_0 without impacting the matching at PEP. The effect R_O has on Z_{drain} of the carrier amplifier was investigated by matching the carrier amplifier to various different values of R_O. Values for R_O was chosen between 18.53 Ω (the value of R_{opt} for the carrier amplifier) and 80 Ω. Figure 3.22 demonstrates the resultant Z_{drain} for loads varying from full power (at PEP) to the low power area. It can be seen that the length of the offset line needed to move Z_{drain} to the real axis decreases as R_O is increased from 18.53 Ω to 80 Ω.

A second consideration for the choice of R_0 is the length of the offset line for the peaking amplifier amplifier. This offset line (described in section 3.9.2) maximises the real part of the output impedance seen when looking back at the peaking amplifier from the load. Figure 3.23 demonstrates this impedance for a R_O of 50 Ω, 80 Ω and 120 Ω. Adding an offset line with impedance R_O moves the output impedance clockwise around the smith chart on the constant impedance circle R_O. It can be seen from figure 3.23 that the length of offset line needed decreases as R_O is increased from 50 Ω to 80 Ω. When the impedance is increased beyond 80 Ω (80 Ω is in fact already a small amount past the real axis) the impedance passes the real axis and long offset line is needed to traverse the entire circle around the smith chart.

A limiting factor on the choice of R_O is the physical width of the micro-strip lines. On the Rogers substrate used for this design an 80 Ω line has a width of 426 um. The minimum allowable width for the production of the board is 400 um. A further implication of this is the physical durability

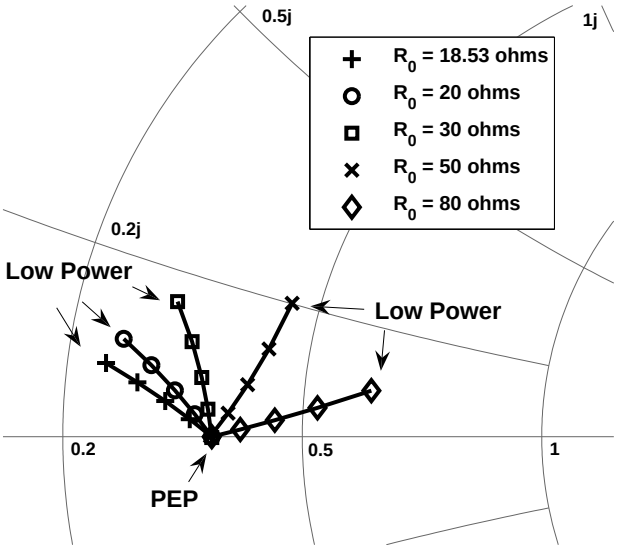


Figure 3.22: Z_{drain} of the carrier amplifier for different choices of R_0 at PEP and at power levels 6dB or more below PEP. By choosing the impedance of R_0 carefully the length of the offset line needed to keep Z_{drain} on the real axis can be minimized.

and loss of such a thin line. This will be discussed in section 4.3.

The investigation into the choice of impedance for R_O has shown that the length of the offset lines can be minimised through a judicious choice of R_O. In this case an impedance of 80 Ω was chosen, resulting in and offset line of 1.33 mm for the carrier amplifier and a zero length offset for the peaking amplifier. In this way the bandwidth can be maximised and conductor losses minimised. The amplifier can also be kept more compact, reducing costs and space needed in larger systems.

3.10 Input Match

A conjugate match is used for the input match of both amplifiers. The input section of the carrier amplifier can be seen in figure 3.24. A stub and a capacitor are used in parallel in order to minimise the effect of any modeling errors. In this way if the model for either the stub of the capacitor is slightly inaccurate the effect on the input match will be reduced. The input matching results can be seen in figure 3.25. The peaking amplifier matching section in figure 3.26 gives very similar results.

3.11 Power Division

A power divider is needed at the input of the Doherty amplifier to divide the input power between the carrier amplifier and peaking amplifier. The classic Doherty amplifier (described

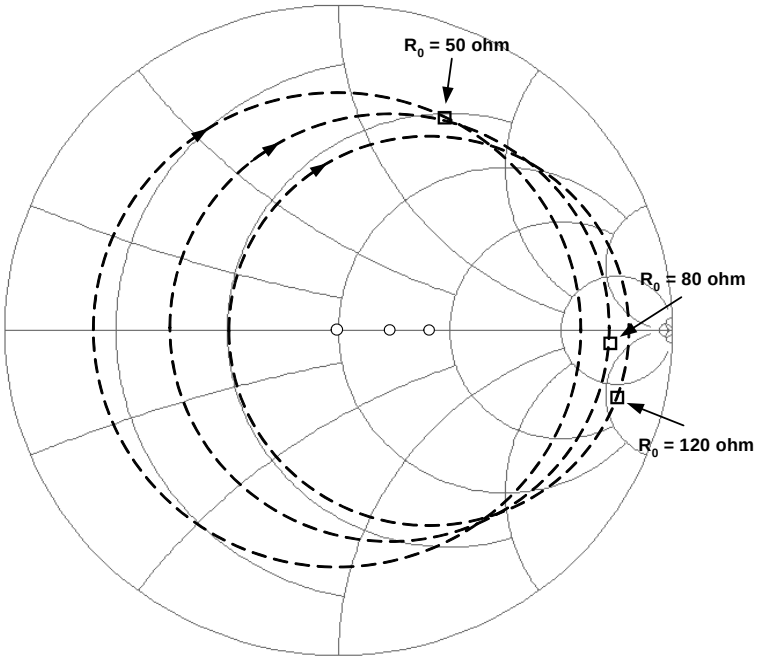


Figure 3.23: The impedance seen looking when looking back to the peaking amplifier from the load after the matching network is added for different choices of R_O. The impedances can be shifted along the circles shown by adding offset lines with impedance R_O.

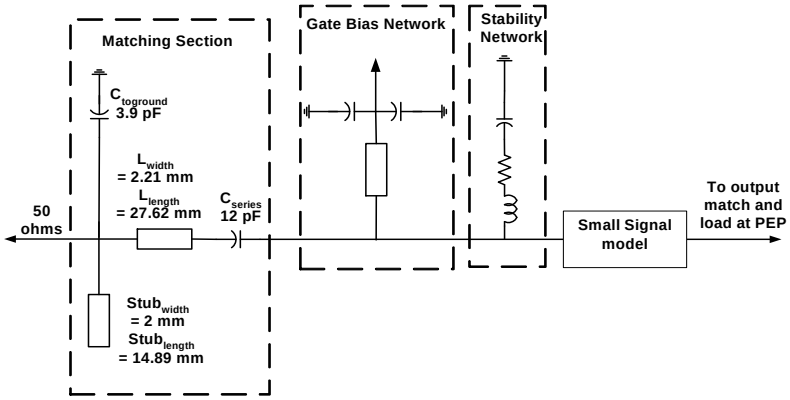


Figure 3.24: The input matching section for the carrier amplifier. The input is matched to 50 Ω using a conjugate match. A stub and a capacitor is used in parallel in order to minimise the effect of incorrect modeling.

in section 2.4) uses even power division. However, as discussed in section 2.6.1, uneven power division offers a possible solution for insufficient current delivery by the peaking amplifier at full power (section 2.5). Such an uneven power divider is designed in section 3.11.2. A quadrature hybrid design was used for both the even and uneven the power dividers [16]. The quadrature hybrid is a directional 3dB coupler providing a difference of 90 degrees between the two output paths. The design of the 3dB quadrature hybrid used for the even power division case is shown in figure 3.27. A 50 Ω load to ground is required at port 4 to absorb any reflections. In a well matched system there should be almost no reflections, however, should something go wrong in the system a lot of power can be sent through this load. If the load fails under high power more power will be reflected into the other ports causing potential damage. Therefore a high power

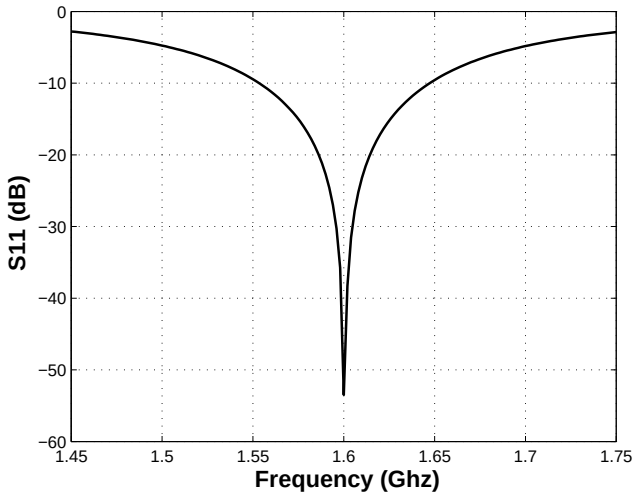


Figure 3.25: The resulting input match for the carrier amplifier.

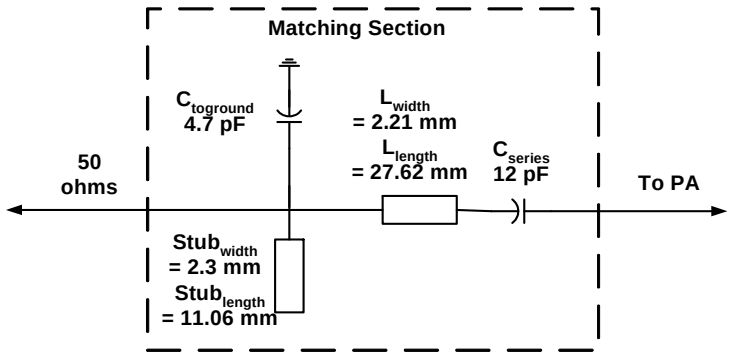


Figure 3.26: The resulting input matching network for the peaking amplifier. A conjugate match is used to match the input of the amplifier to 50 Ω.

50 Ω load (RFP-20-50TP) is used that can absorb up to 20 W of power.

3.11.1 Phase Offset

The Doherty amplifier is designed so that the RF paths through the carrier amplifier and peaking amplifier are of equal phase length in order to avoid destructive interference. The Doherty network (section 2.4.2) adds a quarter wave transformer to the carrier amplifier amplifier output which has the effect adding a 90 degree phase difference. The 90 degrees phase difference between the quadrature hybrid outputs can be used to compensate for the quarter wave transformer, resulting in equal phase paths for the carrier amplifier and peaking amplifier. However equal phase paths are still not assured. The length of the matching sections and also the phase difference between the carrier amplifier and peaking amplifier themselves at full power must also be take into account. The phase for the carrier amplifier and peaking amplifier at full power was simulated in Microwave Office and a small offset line of 1.06 mm added to the peaking amplifier to correct the difference. This offset will be added at the output of the quadrature hybrid. Figure 3.28 demonstrates the phase after corrections, while the positioning of the offset line can be seen in figure 3.27.

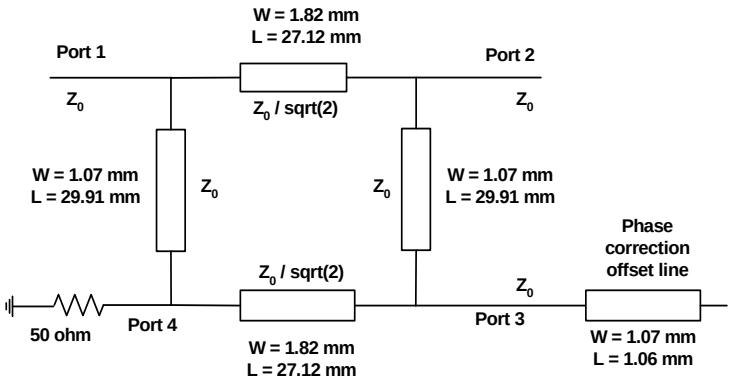


Figure 3.27: The 3db quadrature hybrid. The figure shows the theoretical impedance values and the real widths and lengths of the lines used in the design. The lengths do not include the T-junction used to join the lines. The positioning of the offset line designed in section 3.11.1 is also indicated.

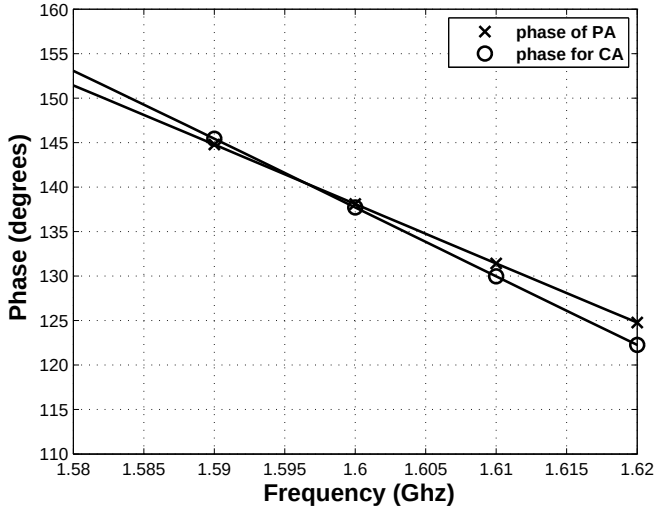


Figure 3.28: The phase of the carrier amplifier and peaking amplifier at full power determined by a Microwave Office simulation. A offset line of 1.06 mm has been added to match the phase at the design frequency.

3.11.2 Unequal Power Division

The goal of using uneven power division is to increase the peaking amplifier current at full power. Ideally both the peaking amplifier and the carrier amplifier provide their maximum current at full power. In section 3.3 the bias points for the amplifiers was chosen. The input voltage at the gate terminal to determine the maximum linear current was determined with equation 3.4 as 3.75 V for the carrier amplifier and 7 V for the peaking amplifier. This is the the maximum voltage at the gate terminal however, not at the input of the amplifier. Microwave Office was used to determine the input voltage needed to provide these voltages at the gate terminals. Figure 3.29 shows a schematic which demonstrates the idea. V_{gen} is increased until V_{in} reaches the required voltage. The harmonic balance simulation results for the carrier amplifier can be seen in figure 3.30. The required input voltages for maximum current determined with this method is 7.873 V for the carrier amplifier and 12.83 V for the peaking amplifier. From these voltages the uneven voltage ratio required by the unequal power divider can be determined as

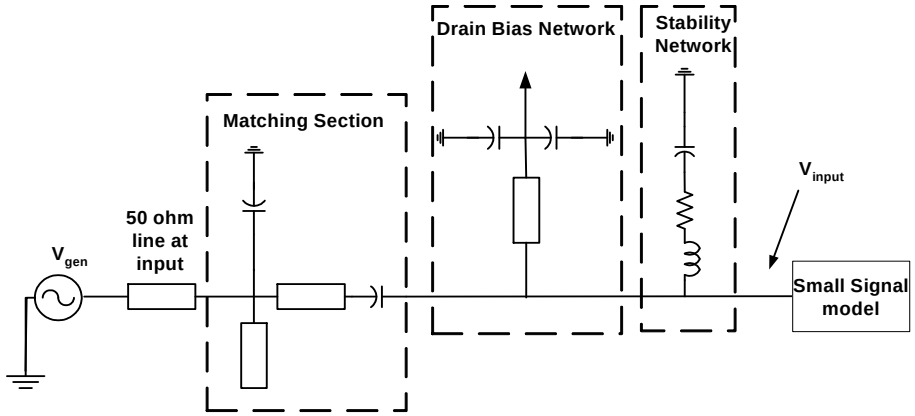


Figure 3.29: A harmonic balance simulation is done to determine the voltage at the gate terminal of the amplifiers for an applied voltage at the input of the amplifier.

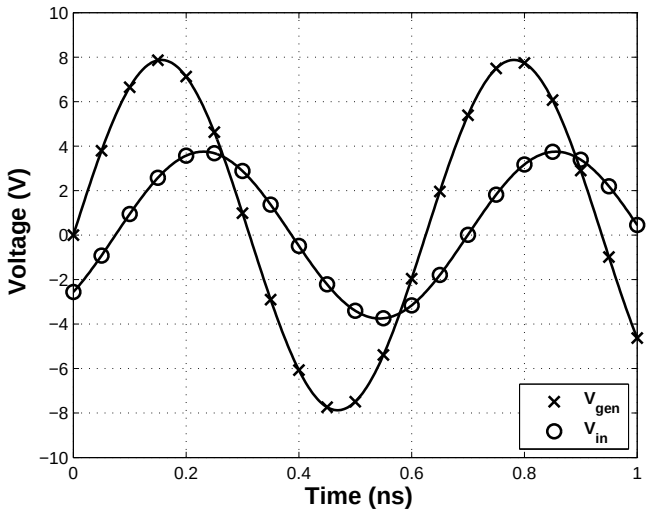


Figure 3.30: The input voltage V_{gen} at the input of the carrier amplifier and the resultant V_{in} at the gate terminal of the carrier amplifier.

$$V_{uneven} = \frac{V_{inputmaxC}}{V_{inputmaxAB}} = 1.635$$

which results in a ratio of 1.635 for this case. The impedance for the quadrature hybrid arms can be calculated as [13]:

$$Z_{Horizontal} = 50/b$$

$$Z_{Vertical} = 50/V_{uneven}$$

where

$$b = \sqrt{1 + {V_{uneven}}^2}$$

The resulting impedances for the uneven hybrid is 26.08 Ω for the horizontal legs and 30.58 Ω. The simulation results can be seen in 3.31. From the simulations it can be determined that the resulting voltage ratio between the 2 output ports is indeed equal to 1.635 when using the

calculated impedances.

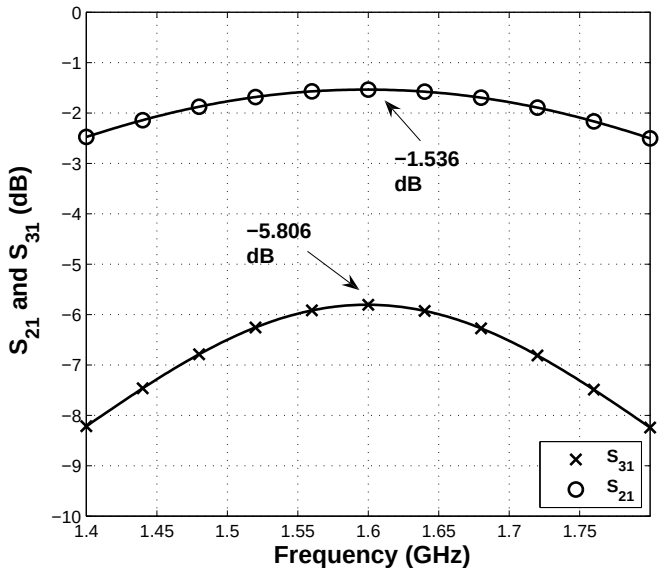


Figure 3.31: The simulation results for the uneven hybrid design.

3.12 Conclusion

In this chapter numerous design issues surrounding the design of a Doherty amplifier have been discussed. A carrier amplifier and peaking amplifier has been designed in class AB and class C configurations respectively. These designs were made using small-signal models calculated from measured results (section 3.6). The amplifiers were stabilised (3.7) and drain and gate biasing networks were added (section 3.8). The amplifiers were matched on the output side so that the optimal impedances for Doherty operation is presented to the drain terminals (section 3.9). However, offset lines with impedance R_0 are required to optimise the Doherty operation. The relevance of this intermediate impedance R_0 was investigated. It was shown that the length of offset lines needed (to optimise Doherty performance) can be minimised through the correct choice of R_0. On the input side a conjugate match was used and quadrature hybrids was designed for even and uneven power division (sections 3.10 and 3.11). In the next chapter some of the more practical design issues such as physical layout are discussed.

Chapter 4

Practical Design Issues

4.1 Introduction

In the previous chapter the design of a Doherty amplifier was discussed in some detail, with the focus mostly residing on the theoretical aspects of the design. In this chapter the practical side of the design will be described. In order to make an accurate RF design one must have good models for the components used in the design. Section 4.2 examines the passive components used in the amplifier design and provides an improved modelling approach for SMD (surface-mount devices) capacitors. The amount of components required for the various Doherty amplifiers evaluated in this thesis can be greatly reduced through a modular design approach. The benefits of the modular design approach and the implementation details are discussed in section 4.3. When the amplifier modules are designed the thermal effects of the power amplifiers must also be considered. Section 4.4 describes the measures taken to control the heat generated by the amplifiers.

The chapter then moves on to describe the electrical aspects of the amplifiers. The effect of a shared ground wire on the drain currents of the amplifiers is shown in section 4.5. Several measurement setups are required to measure different areas of amplifier performance. These measurement setups are describe in section 4.6. Before amplifier measurements can be made however, amplifiers should be tested for stability. The amplifiers designed in this thesis were found to oscillate under certain circumstances. This behaviour and the method used to remove the oscillations is described in section 4.7. Once the stability was assured the amplifiers could be measured, with the performance of the carrier and peaking amplifiers discussed in section 4.8. A frequency shift from simulated values observed in the measurements led to an investigation of the substrate permittivity. In section 4.9 the measured permittivity was found to be different from the specified permittivity, partly explaining this frequency shift.

4.2 Passive Component Characterisation

Passive components are used throughout the amplifier design. Surface mount devices (SMD) such as capacitors are used in the matching sections of the amplifier and also in the biasing networks, and SMD resistors in the stabilisation network. For low frequency designs, designing with passive components is simple as an ideal model of the component can be used for design

and simulation. At higher frequencies more complex models are needed to accurately predict component behaviour. Manufacturers of passive components typically provide such models. These models are created by theoretical predictions and by comparisons to measurements.

It is not always known what substrates are used by manufacturers for their measurements. Passive component behaviour (especially that of SMD capacitors [6, 7]) is influenced by the substrate used. Therefore we cannot know how accurate the vendor supplied models are for components mounted on the substrate used for the amplifier design. It is also not known where the calibration planes are set during manufacturer measurements. This leads to uncertainty in how models should be used, even if it can be assumed that they are accurate.

Accurate models are important for amplifier design. If inaccurate models are used we cannot expect a good correlation between measurements and simulation, which increases the number of iterations needed for a design. As mentioned above, there are uncertainties surrounding the models for the passive components used in the amplifier design. Because of these uncertainties it was decided to measure the components on the same substrate as was used for the amplifier design, compare their behaviour to that of the models provided, and if necessary improve the models to provide better prediction of component behaviour.

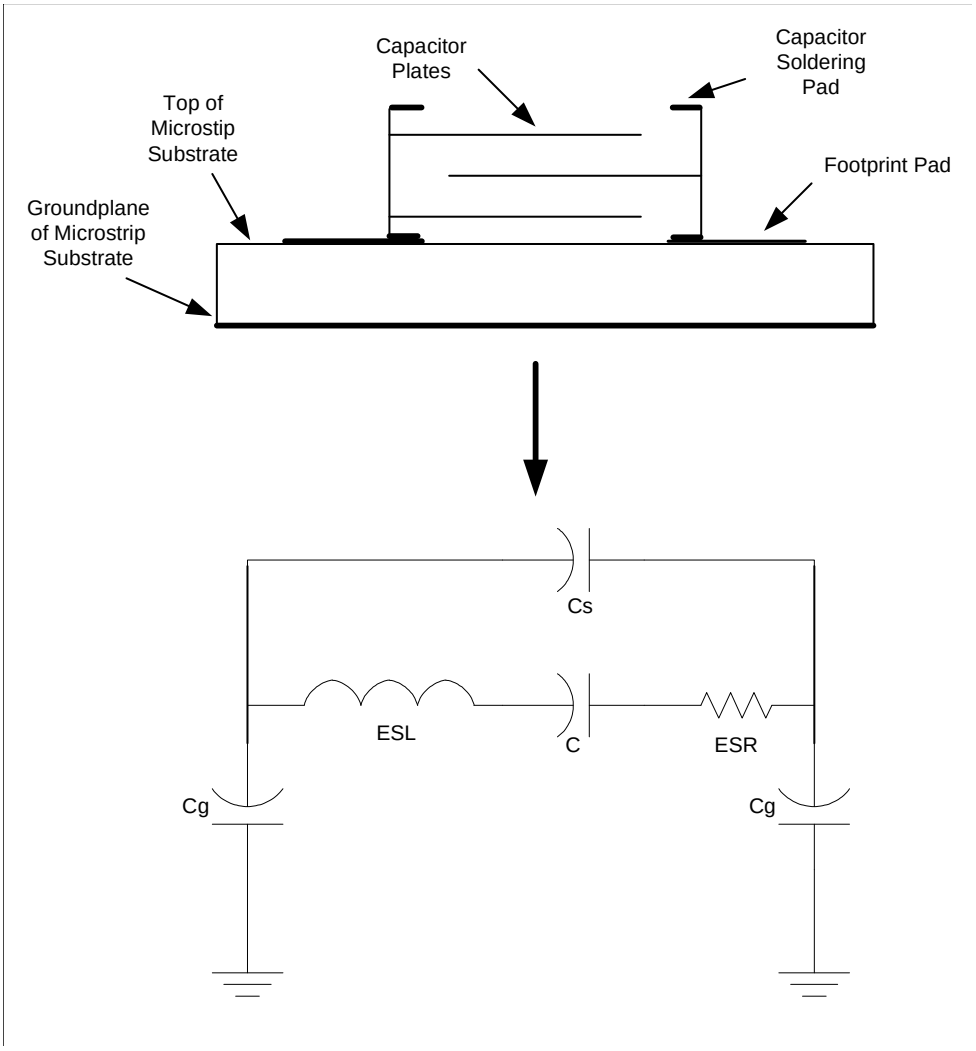


Figure 4.1: Model for multilayer SMD capacitor [6, 7]

4.2.1 A Model for SMD Capacitors

Capacitors are the only passive components used in the matching sections of the amplifier and are also used in the biasing networks. The accuracy of capacitor models are therefore essential to the accurate simulation of the amplifier. The capacitors used in the amplifier design were 0603 multilayer chip capacitors from Dielectric Laboratories [2]. Figure 4.1 presents a model for a chip capacitor [6, 7]. C_s represents a combination of two capacitances:

- The capacitance between the capacitor soldering pads
- The capacitance between the footprint pads

C_g also represents two capacitances:

- The capacitance between the capacitor soldering pads and the top of the micro-strip substrate.
- The capacitance between the footprint pads and the ground plane of the micro-strip substrate.

ESL represents the series inductance and ESR the series resistance of the capacitor, while C represents the capacitance between the capacitor electrodes.

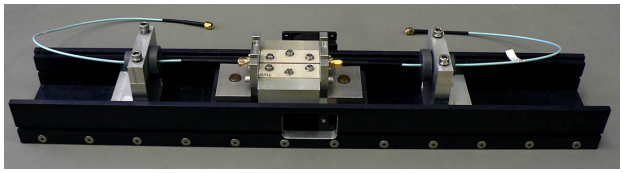


Figure 4.2: The fixture used for TRL measurements. The thru calibration standard is mounted in the fixture.

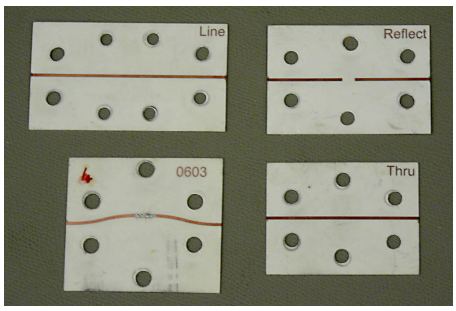


Figure 4.3: The calibration standards used for the TRL calibration and one of the measurement boards that was used for the SMD component characterisation.

4.2.2 Measurement of SMD Capacitors

The effect of the footprint was included when the capacitor behaviour was considered. This was done in order to include the substrate and footprint dependant variables in the comparison between the measurements and models. The same substrate, Rogers 4003 [4], was used as in the amplifier design (see Table 4.1 for the properties of this substrate).

Table 4.1: Properties of Rogers 4003 Substrate

	Height (mm)	Dielectric Constant	Conductor Thickness (mm)
Rogers 4003	0.508	3.38	0.035

A TRL calibration [12] was used and measurements were made on a HP8510 Network Analyser. The TRL fixture used for the measurements can be seen in figure 4.2, while the calibration standards and the measurement board used for the SMD components can be seen in figure 4.3. The footprint used for the capacitors was the same as was used in the amplifier design, with the calibration planes set to the edge of the footprint (see figure 4.4). To provide a basis for comparison eight capacitors were chosen at even intervals from the available capacitor range.

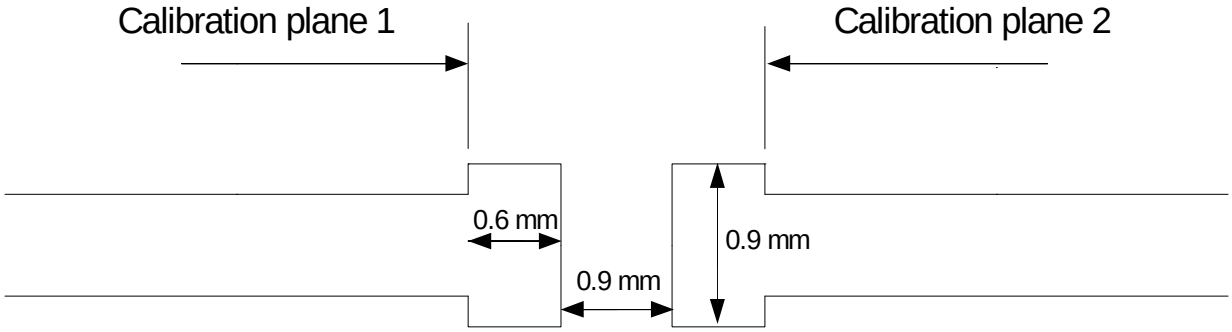
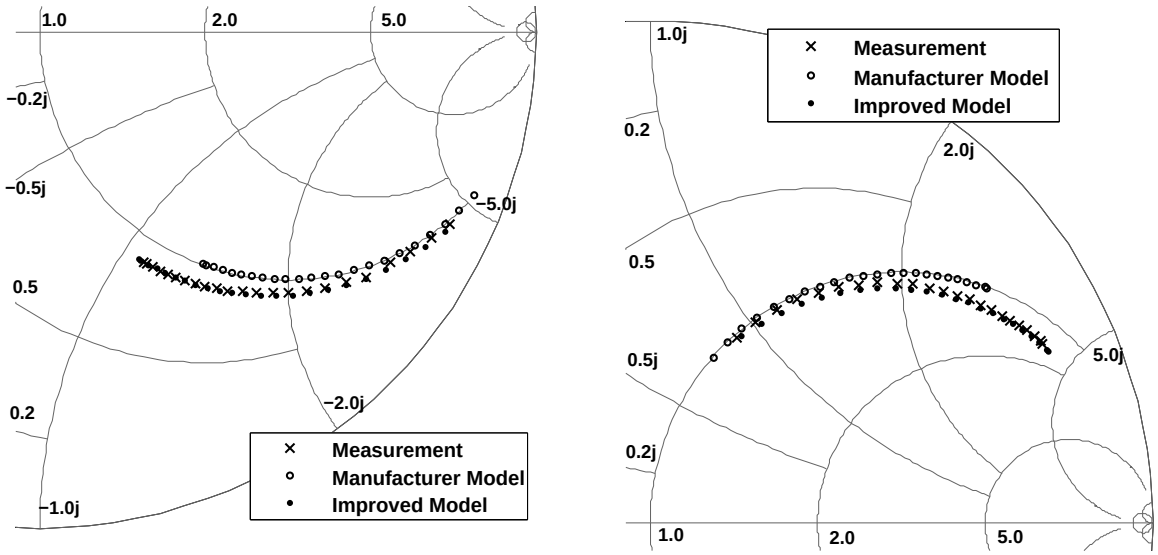


Figure 4.4: Footprint and calibration planes used for the measurement of SMD capacitors.

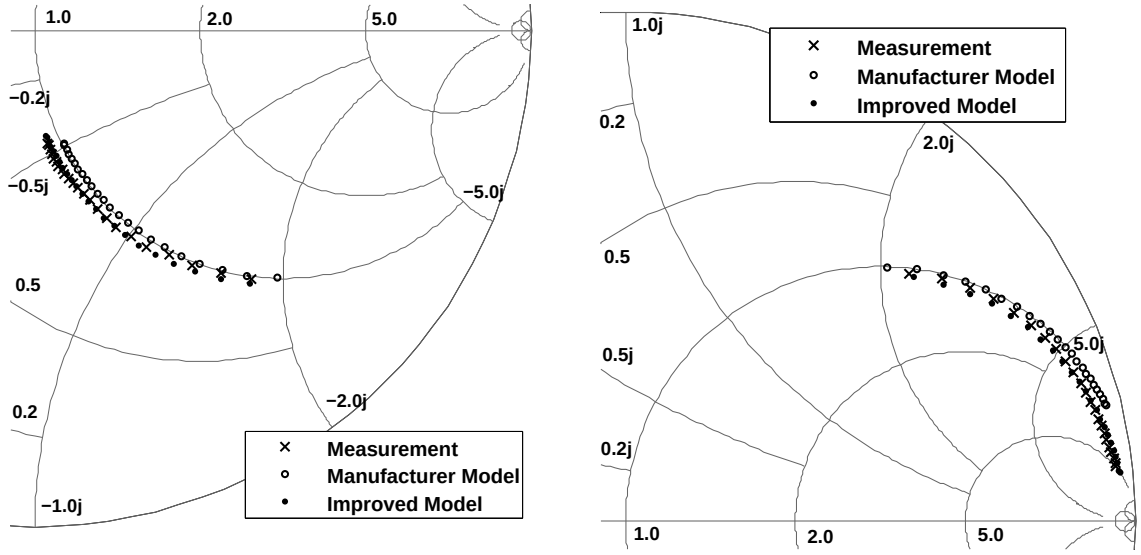
4.2.3 Improvement of Capacitor Model

Comparisons were made between the measurements and the manufacturer models (see figures 4.5-4.8 for selected capacitor values). It can be seen that the models do not accurately predict capacitor behavior. This inaccuracy was attributed to differences between the substrate and footprints used for the measurement and that used by the vendor for modeling [7, 6]. If this assumption is correct the capacitances in the manufacturer model (C_g and C_s(see figure 4.1)) are not correct for our application. To rectify this an external network composing of the elements $C_{g\,footprint}$, $C_{s\,footprint}$ and $ESL_{footprint}$ is proposed (see figure 4.9). $C_{g\,footprint}$ represents the capacitance between the footprint pads and the ground plane, $C_{s\,footprint}$ the capacitance between the two footprint pads, and $ESL_{footprint}$ the inductance of the footprint pads. Although the manufacturer models already contain similar elements (See section 4.2.1), the elements in the external network are intended to account for the difference in the substrate and footprints used in the current design and that in the vendor's.



(a) S_{11} (b) S_{21}

Figure 4.5: Smith chart comparisons for a 1 pF capacitor

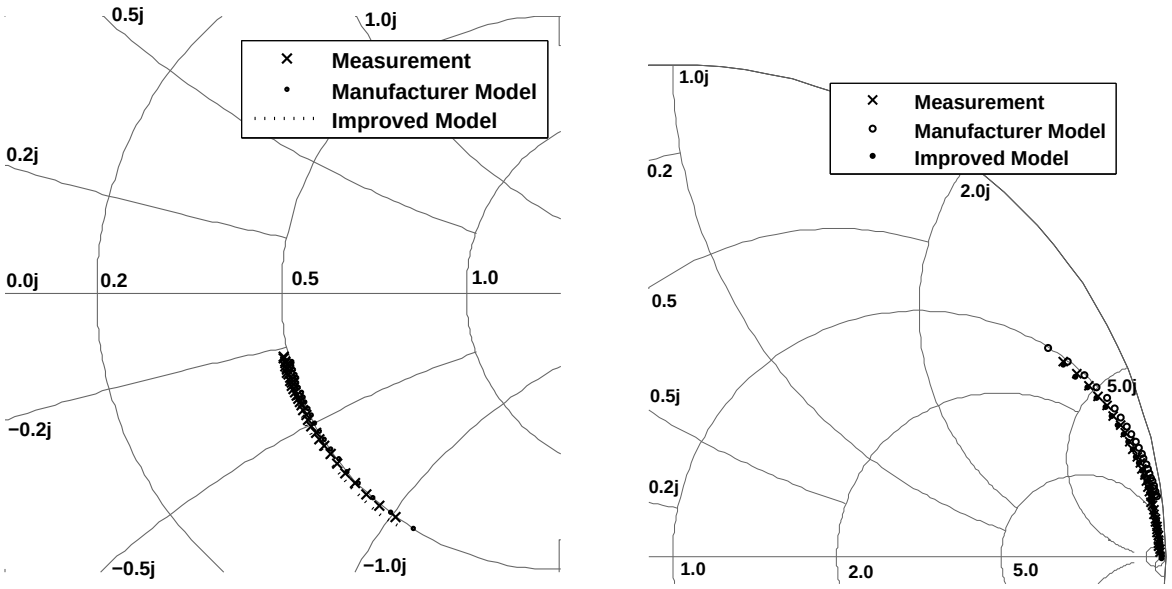


(a) S_{11} (b) S_{21}

Figure 4.6: Smith chart comparisons for a 2.7 pF capacitor

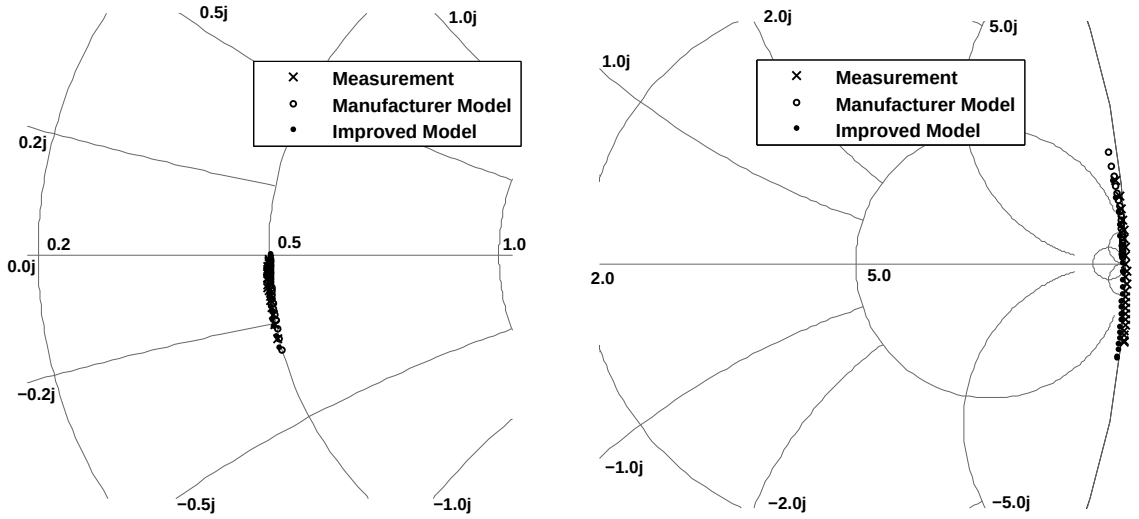
The manufacturer models for the eight capacitors under test were each placed inside this external model. The capacitors all use the same footprint, therefore the same external model is used for all the capacitors. The values of this external model were then optimized by attempting to simultaneously match the modeled and measured response of the eight capacitors. The result of the optimisation is one external model that can be used for any of the capacitors from Dielectric Laboratories used on the same footprint. Table 4.2 gives the values for the elements in the external model.

An improved model can now be formed for a Dielectric Laboratories [2] 0603 multilayer chip capacitor used on Rogers 4003 substrate with the footprint shown in figure 4.4. The improved model is created by placing the model provided by Dielectric Laboratories inside the external



(a) S_{11} (b) S_{21}

Figure 4.7: Smith chart comparisons for a 4.7 pF capacitor



(a) S11 (b) S21

Figure 4.8: Smith chart comparisons for a 18 pF capacitor

Table 4.2: Element Values for Eternal Model

Elements	$C_{g\,footprint}$ (pF)	$C_{s\,footprint}$(pF)	$ESL_{footprint}$ (nH)
Values	0.084	0.2022	0.2328

model (See figure 4.9). The improved model is more accurate than the vendor model on its own. This procedure removes the need to characterise every capacitor individually, as the model that is extracted from a few representative measurements can be used for all capacitors values in the range. Figures 4.5-4.8 show that the improved models closely follow the measured results. These improved models were used in the amplifier design wherever Dielectric Laboratories 0603 capacitors were used.

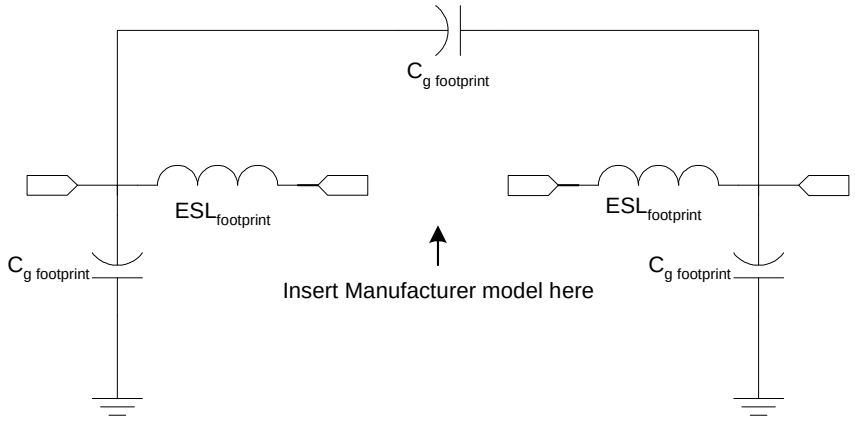


Figure 4.9: The external model for capacitors. It is used in conjuction with the manufacturer model to improve the match between measured and simulated results.

4.2.4 Investigation into Behavior of SMD Resistors

SMD resistors were used in the stabilization network of the amplifier design. There were no models available for the resistors, so an ideal resistor model was used in simulations. It was decided to investigate in order to determine whether the ideal model predicts the behaviour of the resistors accurately enough. For resistors a deviation of 15% between the model and actual behavior was deemed acceptable. This number was chosen because experience showed that deviations of 15% or less in the values of resistors does not have a significant effect on the simulated performance of the stabilisation network.

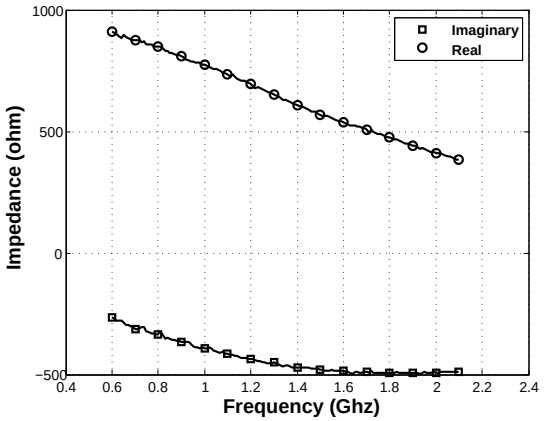
Measurements of three resistors were taken using the same measurement setup as in section 4.2.2 and compared to the behavior of an ideal resistor. The results of the measurements can be seen in figure 4.10. Figure 4.11 shows the percentages by which the measurements differ from the ideal model. It can be seen that the smaller the resistor is, the closer it follows the ideal model. The 51Ω resistor deviates by a maximum of 7% from the ideal model and the 300Ω resistor by a maximum of 44%. By interpolation of these measurements we can predict that a 120Ω resistor is the largest resistor that will not deviate by more than 15% from the ideal resistor model (see figure 4.11). Ideal resistor models could therefore be used in simulations for all resistors of 120Ω and smaller while satisfying the requirement of 15% or less deviation from actual resistor behaviour. No values larger than 120Ω were used in the design of the stabilisation networks.

4.3 Modular Design

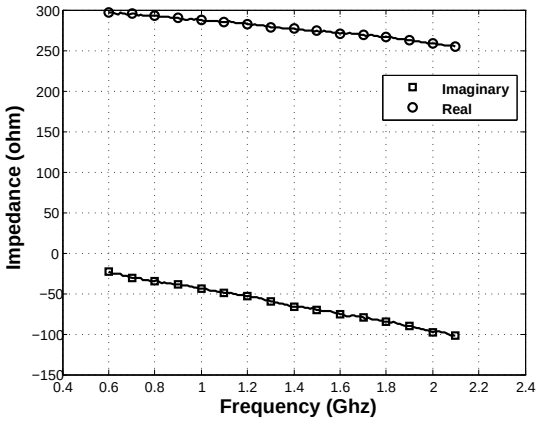
It was decided to use a modular approach for the Doherty amplifier. In this way several different configurations could be compared without the need to manufacture a completely new design.

4.3.1 Input and Output Modules

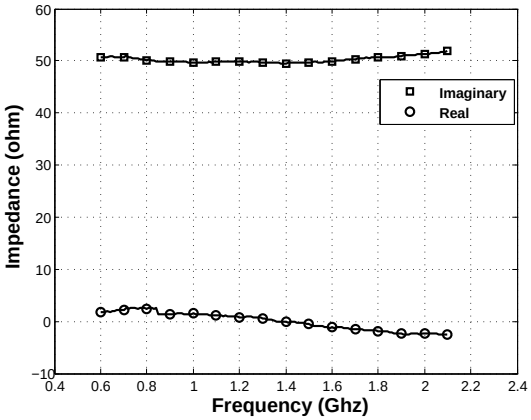
The modular design provides the opportunity to measure the peaking and carrier amplifiers either together in a Doherty configuration or separately. For the Doherty configuration measurements, the input modules consists of the even and uneven power dividers, and the Doherty



(a) Impedance of a 1kΩ resistor



(b) Impedance of a 300Ω resistor



(c) Impedance of a 51Ω resistor

Figure 4.10: The impedance of measured resistors against frequency.

combiner is used as the output module. Figure 4.12 shows the layouts of the uneven power divider and the Doherty combining network, while Figure shows a photo of the completed Doherty configuration using these modules 4.13. Figure 4.14 shows a photo of all the other input and output modules used in the design.

For measuring the peaking and carrier amplifiers on their own, 50 Ω input modules were designed. As the input of the amplifiers are already matched, these simply consist of a 50 Ω line connecting the amplifier modules to the SMA connectors. Different output modules can be designed to present various loads to the amplifiers. The most used output network for single amplifier measurements presents a load of 80 Ω to the amplifiers, which is the same load as the amplifiers would see at full power in the Doherty configuration. (see section 2.4). This design is made using a quarterwave impedance transformer to transform the 50 Ω seen at the measurement port to the required 80 Ω at the output of the amplifier module. Figure 4.15 shows the layouts for the 50 Ω input module for the carrier amplifier and the 80 Ω load output module for the peaking amplifier. All the input and output modules where manufactured on Rogers 4003 substrate using in-house processing capabilities.

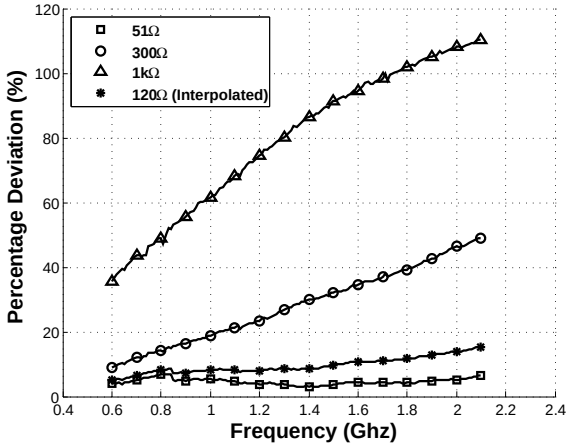
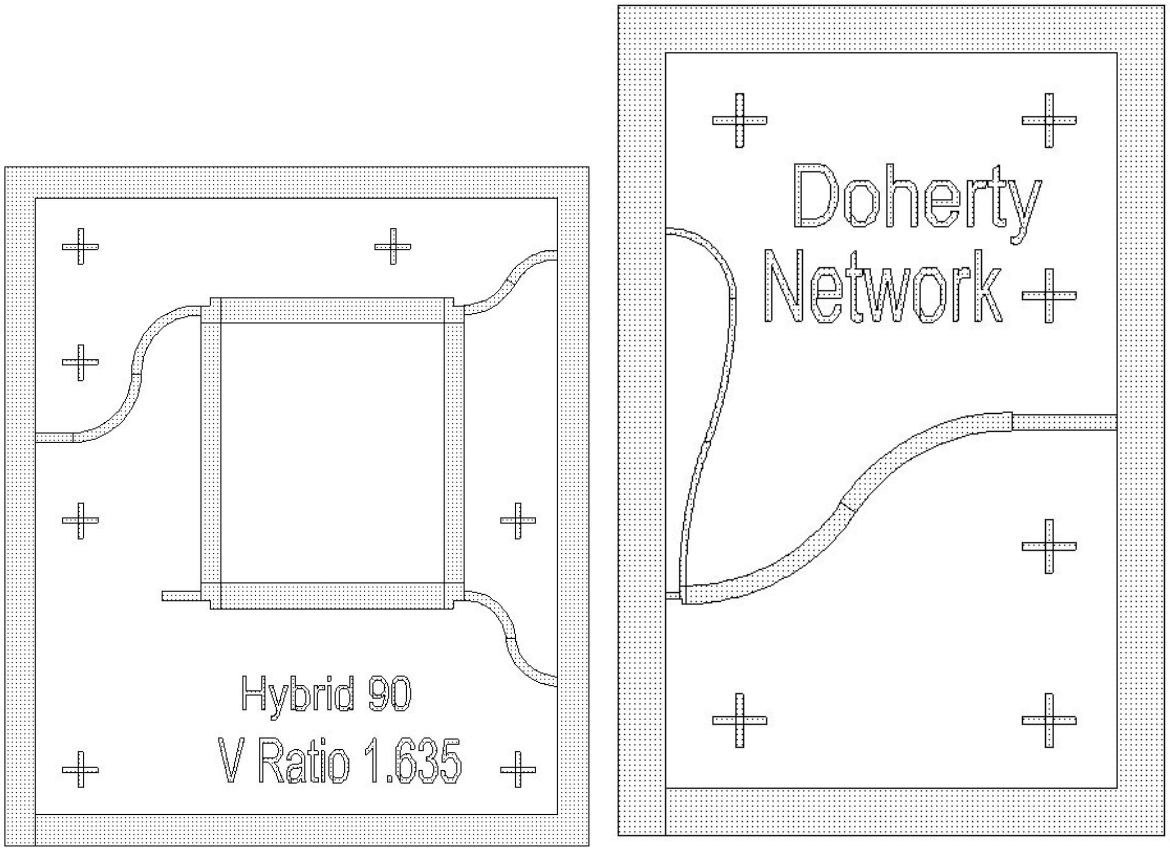


Figure 4.11: The percentage deviation from an ideal resistor model shown by measurements.



(a) Uneven Power Divider (b) Doherty Combining Network

Figure 4.12: The layouts for the uneven power divider and the Doherty combiner network.

4.3.2 Amplifiers

The source terminal of the MRF282 is an exposed terminal underneath the package. Ideally the source would be connected directly to ground as any inductance at the source of the MOSFET will result in a reduced gain. However, because we are using a micro-strip design a connection must be made from the footprint on the top metal layer to the bottom metal layer (the ground plane). The standard way to make such a connection is through the use of vias. Such a via

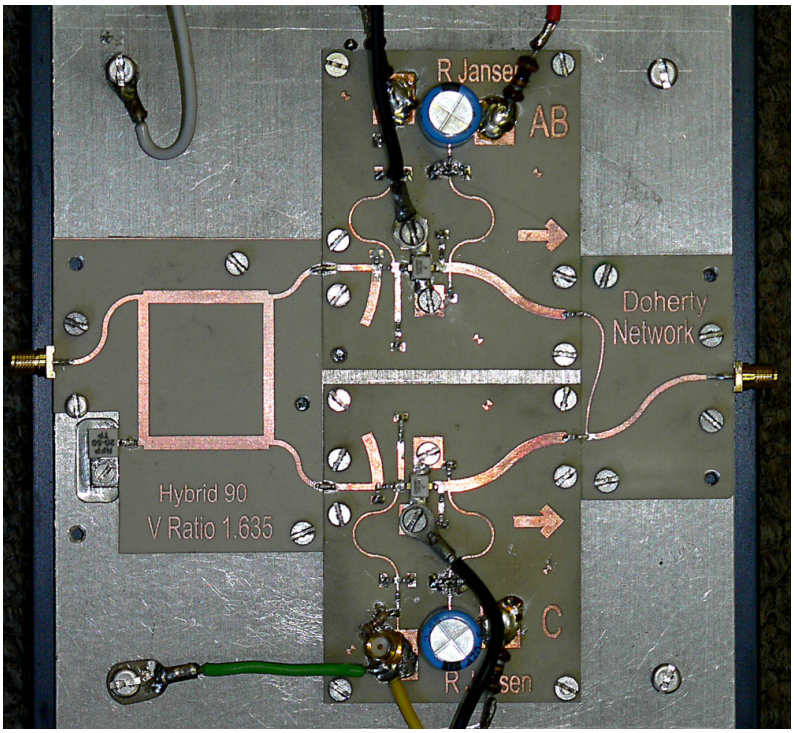


Figure 4.13: The complete Doherty amplifier, in shown with the uneven power divider.

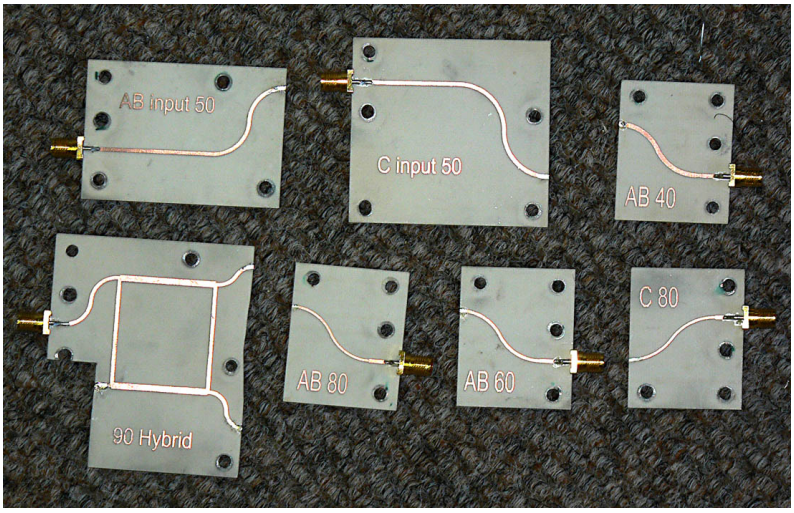
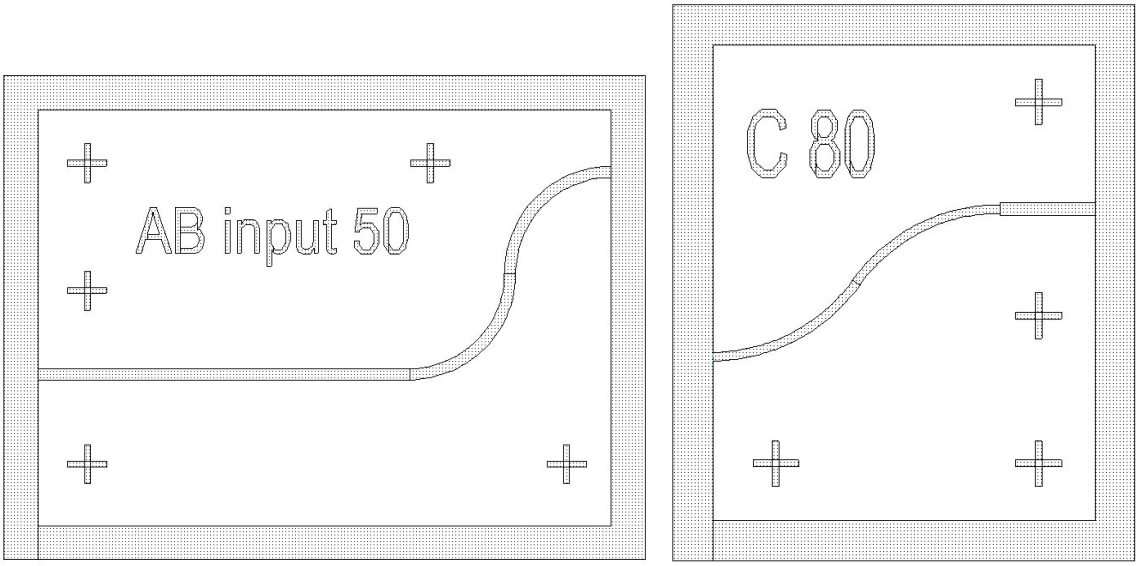


Figure 4.14: Input and output modules used in the modular design.

connection will inevitably have some inductance. The amount of inductance can be reduced through the use of many micro-vias that are used in parallel. This approach was used for this design as can be seen from the transistor footprint in figure 4.16. In order to reduce the inductance further the use of solid vias is desirable. This technique is however not available from commercial board manufacturers in South Africa. Plated through-hole vias filled with solder was used instead. The solder-filled via does not have the good thermal and conduction properties of a solid via, but is an improvement over unfilled plated through-hole vias. The amplifier modules were manufactured by North Tech Services as the capability to manufacture through-hole plated vias was not available using in-house procedures at the time. Besides reducing the inductance at the source the solder filled through-hole vias provide good thermal contact to the ground



(a) Peaking amplifier 50 ohm input module (b) Carrier amplifier 80 ohm output module

Figure 4.15: The layouts for the 50 Ω input module for the carrier amplifier and the 80Ω load output module for the peaking amplifier.

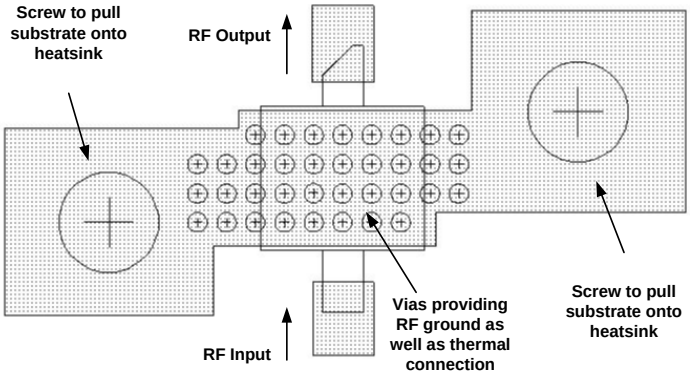
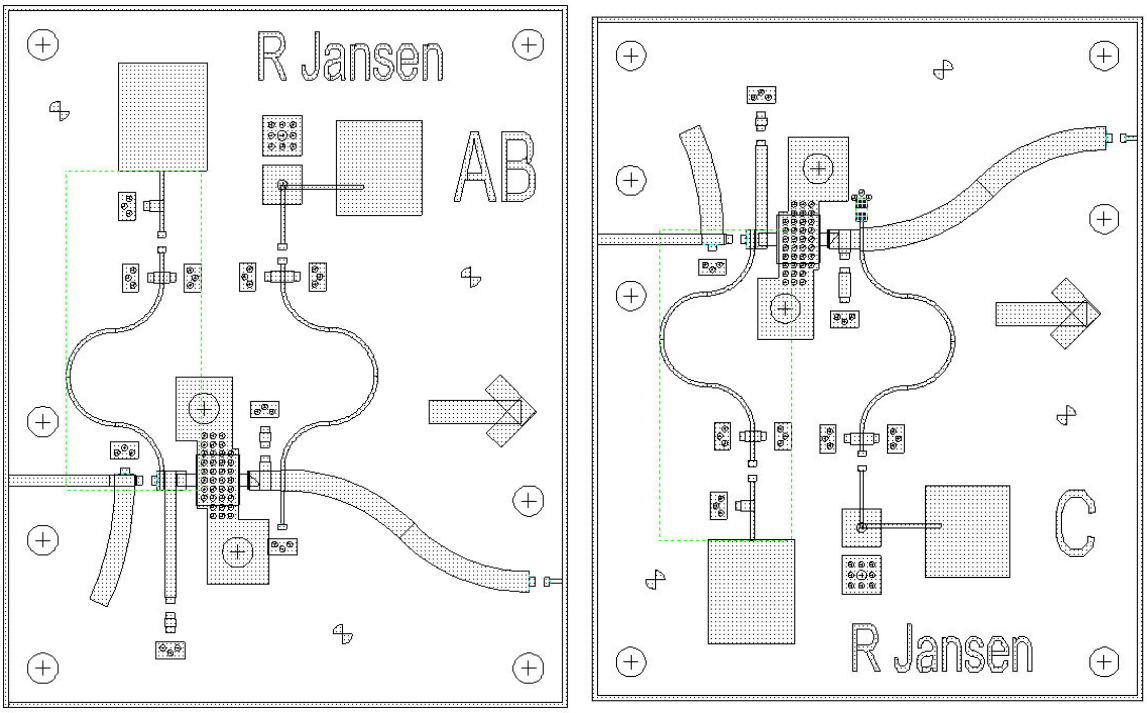


Figure 4.16: The footprint for the MRF282 showing the vias underneath and the screw holes to fasten the pcb tightly to the heat sink.

plane and the heat sink. This is discussed further in section 4.4. The layouts for the carrier and peaking amplifiers can be seen in figure 4.17.

4.3.3 The Joining of the Modules

The modules are joined together on a large aluminium heat sink which serves both as a heat sink and as a solid base on which to connect the modules. In section 4.4 the thermal properties are discussed in more detail. For the RF connections between the modules small metal tabs were used. These where manufactured of copper using in-house processing. Figure 4.18 shows a photograph of the tabs. Tabs of various widths were manufactured to allow the connection of lines with different impedances (and therefore different widths). When the modules are tightened onto the heat sink, the RF lines line up. A tab is simply placed were the two boards meet and soldered into place. In most cases, connections can be made using just solder paste. However,



(a) Carrier amplifier (b) Peaking amplifier

Figure 4.17: The complete layouts for the amplifier modules.

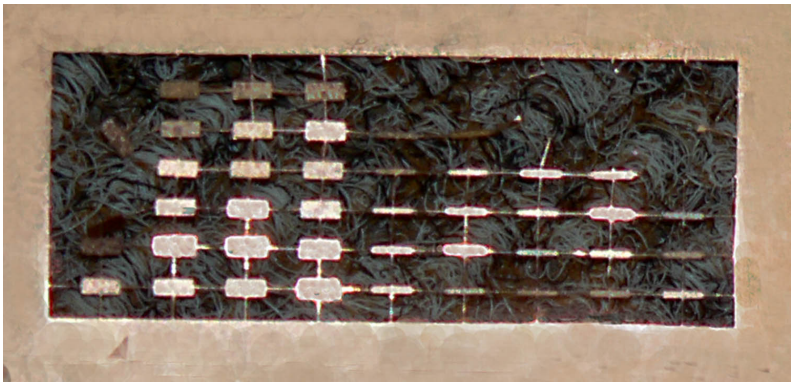


Figure 4.18: The copper tabs used to join the modules together.

the tabs ensure good electrical contact, has less losses compared to a solder only connection, and is physically more robust.

4.3.4 Advantages and Disadvantages of Modular Design

A big advantage to using a modular system is the reduction in costs compared to having several complete designs. The amplifier modules are by far the most expensive. Through the use of the modular design only 1 module each was needed for the peaking and carrier amplifiers for all the different configurations. Depending on which modules are changed, it also allows for a much quicker design time for new designs. For example if a new type of power combiner is designed it can be manufactured using in-house procedures and simply connected to the existing modules. This saves time by not having to manufacture the boards externally, and also because

the population of new components for an entire design is not required.

The disadvantages of the modular system mainly have to do with convenience. Careful attention must be paid to the size of the modules, the location of the holes used for tightening the board unto the heat sink, and the lining up of RF connections. In some cases the design also results in long line lengths which could have been avoided if a non-modular design was used. However, the benefits of the modular design far outweighs the disadvantages in an experimental development process as followed in this thesis.

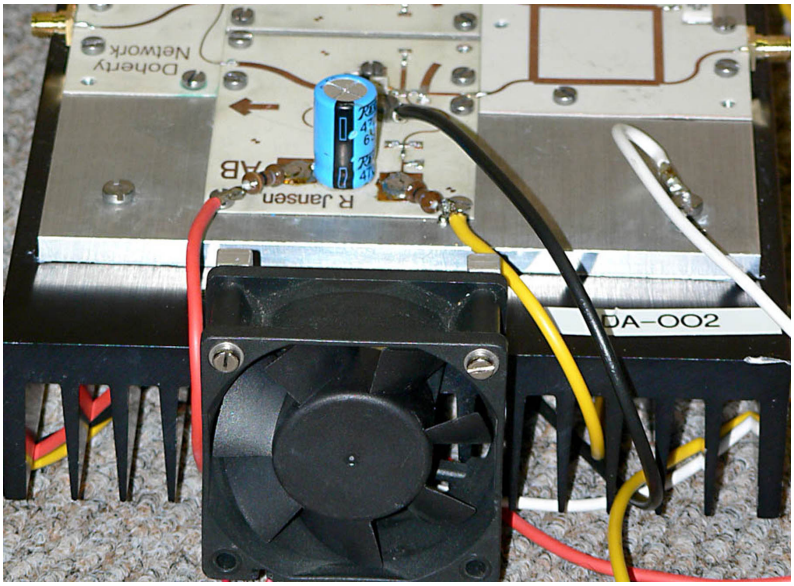


Figure 4.19: A side view of the heat sink and fan used to cool the design.

4.4 Thermal Considerations

The design is made with 10 W power transistors which can overheat easily if temperature is not taken into consideration in the amplifier design. To ensure that the amplifiers are kept at low and non-variable temperature a large heat sink is employed. However, employing a heat sink will not prevent overheating if there is not a good thermal connection between the transistor and the heat sink. The two important factors are the thermal conduction from the transistor through the substrate and the thermal connection between the substrate and the heat sink itself. The transistor is mounted on a metal plane. This plane is filled with solder filled through-hole vias which serve as a low inductance connection to ground, but also provides a good thermal conduction path to the metal ground plane on the bottom of the substrate. The PCB boards are then mounted on the heat sink and fastened securely. Bolts are added close to the transistor to ensure that the section of the PCB where the transistor is mounted is pulled tightly against the metal heat sink. The footprint with the via holes and bolt locations can be seen in figure 4.16. Conductive paste is applied between the substrate and the heat sink, especially in the areas right under the transistors. In this way good thermal coupling is assured. A fan is added to the heat sink directly in line with the transistors to ensure that the air keeps circulating through the heat sink. Figure 4.19 shows a side view of the heat sink with the fan mounted on the side.

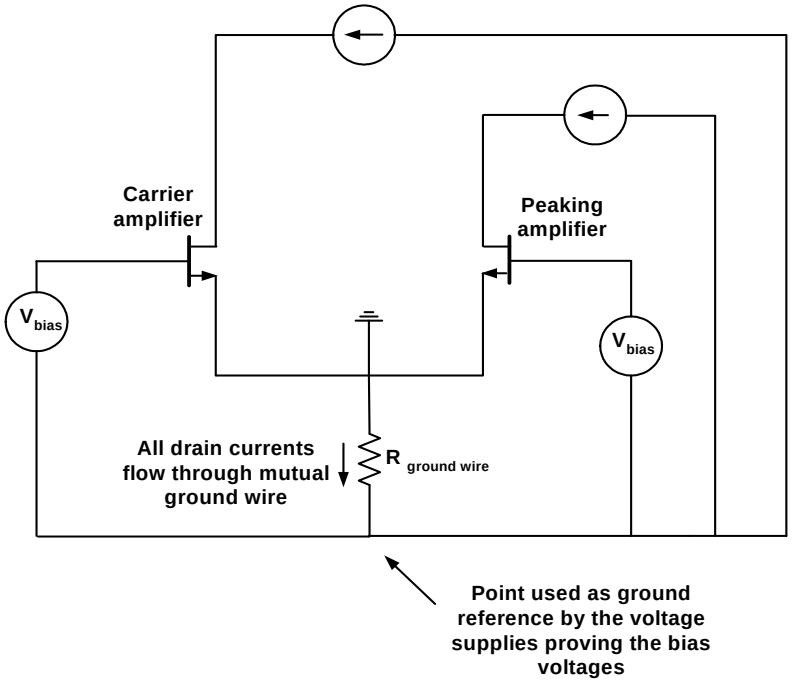


Figure 4.20: A schematic of the Doherty amplifier when a single ground wire is used from the layout to provide a ground for all the power supplies. Changes in the drain current of the one amplifier results in voltage drop across the resistance of this mutual ground wire, which will then lead to a change in the voltage applied across the source and gate terminals of the other amplifier.

4.5 Shared Ground Wire

Tests with the complete Doherty amplifier showed that the carrier amplifier and peaking amplifier influence each other in an unexpected way. The drain current of one amplifier at a certain biasing voltage would change depending on whether the other amplifier was active or not. The cause of this effect was traced back to the wires used to connect the power and voltage supplies to the amplifiers. A single ground wire was connected to the Doherty amplifier and then used as reference for all the gate and drain biasing voltages. The wire has a resistance $R_{groundwire}$ which, although very small, is not zero. The drain currents from the amplifiers flow through this resistance and causes a voltage drop over the resistance. This will cause the bias voltages applied to the amplifiers to change, as the voltage sources are using the wire as a ground reference. Figure 4.20 shows a schematic diagram of the problem. The solution is to provide each amplifier with a its own ground wire connected to the source terminals for use exclusively by the drain power supply. The bolts used to tighten the PCB to the heat sink (see figure 4.16) are convenient for this purpose as they are very close to the source terminals. The use of separate ground wires solved the problem and no more unwanted fluctuations was observed in the drain currents.

4.6 Amplifier Measurement Setup

Measurements were made for the Doherty amplifier with even and uneven power division as well as for the carrier and peaking amplifiers. In this sections the different measurement setups used will be described.

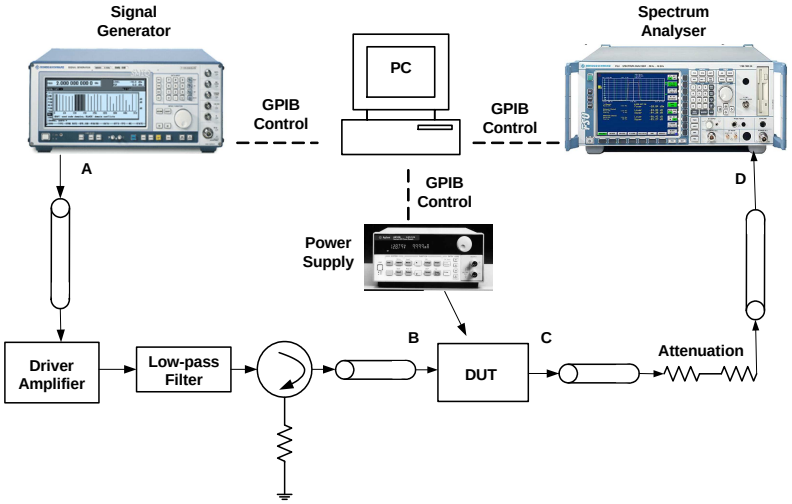


Figure 4.21: The measurement setup for measuring the performance of the amplifiers against input power. The output power is recorded with a spectrum analyser, while the drain currents is measured using power supplies controlled via a GPIB interface with MATLAB.

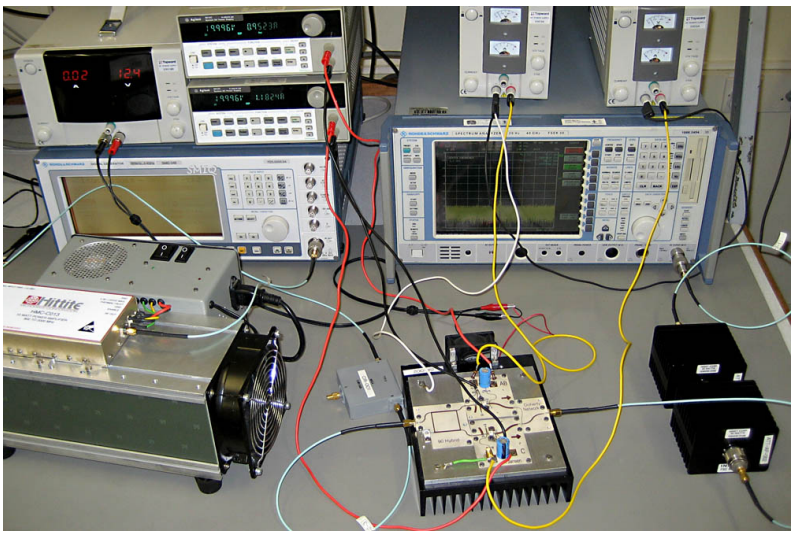


Figure 4.22: A photo of the measurement setup used for measuring the performance of the amplifiers against input power. The low-pass filter used to filter harmonic products from the driver amplifier is not shown in this photo.

4.6.1 Power Measurements

The amplifier performance is measured against input power to calculate performance aspects such as the 1 dB compression point and amplifier efficiency. To measure this information a signal generator was used in conjunction with a spectrum analyser. Figure 4.21 presents a schematic for the setup, while a photo of the measurement setup can be seen in figure 4.22. Both the signal generator and the spectrum analyser were controlled via a GPIB interface from a computer. Measurements were made by doing a power sweep with a single tone at the design frequency from the signal generator. At each point in the power sweep the maximum power is recorded by the spectrum analyser. A programmable DC power source is also controlled via a GPIB interface and records the drain currents of the amplifiers for each measurement. The software for this measurement was written in MATLAB.

The signal generator can not provide enough power to drive the amplifiers into saturation. A driver amplifier was therefore added to provide more input power. A low pass filter is added after the driver amplifier to filter out any unwanted harmonic distortion products. In order to protect the driver amplifier a circulator is added between the DUT (device under test) and the driver amplifier. Attenuators are added at the output of the DUT to keep the measured power levels below the recommended maximum input of the spectrum analyser.

A calibration procedure is required in order to make accurate measurements of the power levels. The accuracy level of the spectrum analyser and signal generator was first confirmed by comparing the reported power levels with a measurement from a power meter. Four calibration points is defined in figure 4.21. The effect of the lines and attenuators between points C and D, E_{CD}, can be measured by connecting point C directly to point A and subtracting the input power level on the signal generator from the spectrum analyser reading. The second step of the calibration is connecting points B and C together and repeating the measurement to measure the sum of networks E_{AB} (the effect of the components between points A and B) and E_{CD}. Since E_{CD} is already known form the first step in the calibration process, E_{AB} can easily be calculated. This concludes the calibration procedure. By adding E_{AB} to the reported input power level form the signal generator the input power at the DUT is known, while the E_{CD} can be added to the reading from the spectrum analyser to provide the true output power.

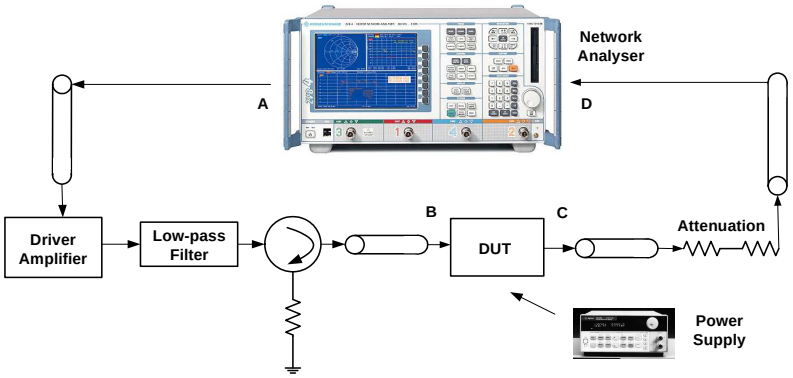


Figure 4.23: The measurement setup for measuring the transmission phase of the amplifiers against input power.

4.6.2 Phase Measurements

The power measurement setup in the previous section measures the amplifier performance against input power. However, the spectrum analyser used for determining the output power can only detect the amplitude of the output signal and not the phase. To determine the transmission phase of the amplifiers a network analyser measurement is needed. The network analyser is set to power sweep mode instead of the usual frequency sweep, with the chosen frequency as 1.5 Ghz. The reason for this choice of frequency is explained in next section 4.8.1. The measurement setup can be seen in figure 4.24. The calibration of the power levels is done in a similar way to that of the power measurement setup. Points A and C (see figure 4.24) are connected to measure E_{CD}, and points B and C connected to measure the combined effect of E_{CD} and E_{AB}. E_{AB} is easily calculated through subtraction of the two measurements. For the phase calibration a

through standard is connected in the place of the DUT in figure 4.24 and a through calibration is done on the network analyser.

The power sweep measurement can now be done on the network analyser. The result is a S_{21} measurement providing us with the phase and amplitude response of the amplifiers against input power. E_{AB} is added to the reported input power from the network analyser to reflect the input power at the input of the DUT.

Since this measurement provides the phase and amplitude response it could be argued that the power measurement setup in the previous section is not needed. However the phase measurement as described in this section does not provide GPIB control over the power supplies used to provide the drain current and is therefore unable to record the drain currents during a power sweep.

4.6.3 Scattering Parameter Measurements

A network analyser was used to measure the scattering parameters for the amplifiers. The measurement setup is shown in figure . Calibration is done using a SOLT (Short-Open-Load-

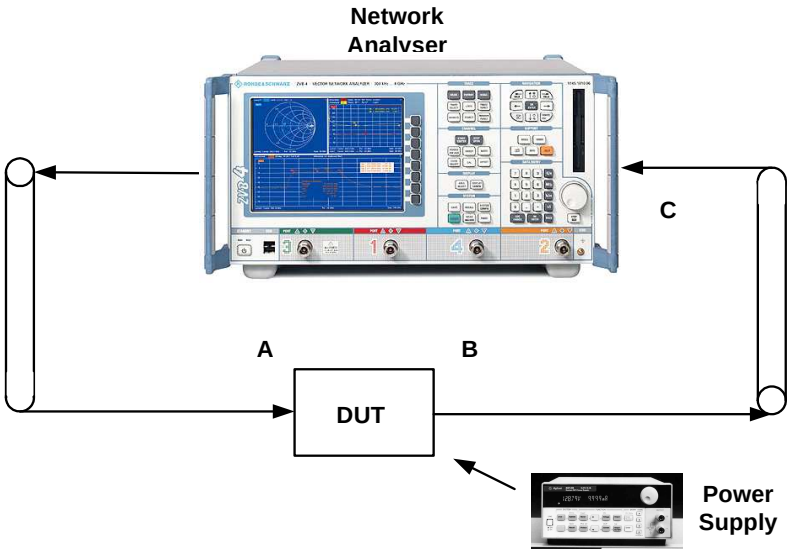


Figure 4.24: The measurement setup for measuring the transmission phase of the amplifiers against input power.

Through) calibration on the network analyser. Care must be taken to lower the power levels at which the measurement is taken to keep the output power well below the recommended levels for the network analyser. The scattering parameters can now be measured for the amplifier with a frequency sweep.

4.7 Amplifier Stability Measurements

Both the peaking amplifier and the carrier amplifier were found to oscillate at certain gate bias voltages and input power combinations. Figure 4.25 shows a typical output measured on a spectrum analyser when one of the amplifiers where oscillating. This type of oscillation was very unexpected, firstly because it only occurs at some bias points (see section 4.7.1 and secondly

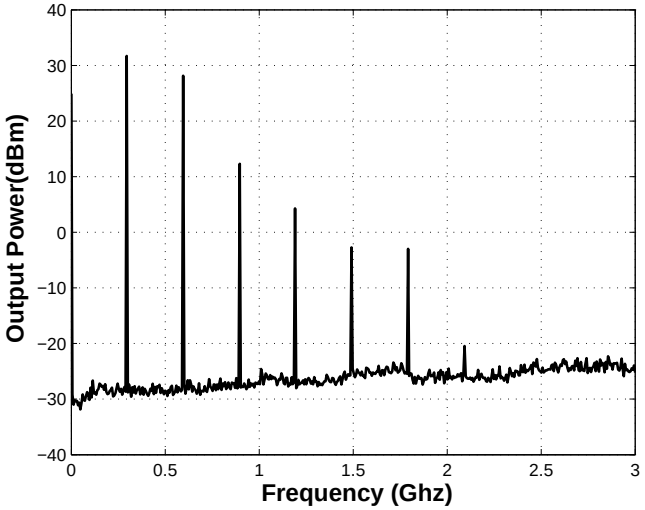


Figure 4.25: Carrier amplifier oscillations measured on a spectrum analyser. These oscillations only appears at certain gate bias voltages and input power combinations. This measurement was taken with no input RF power and a gate biasing voltage of 4.5 V. The peaking amplifier showed similar behaviour.

because the amplifiers where designed to be unconditionally stable (section 3.7). The cause of the oscillation was however traced to the drain biasing network (see section 4.7.1)

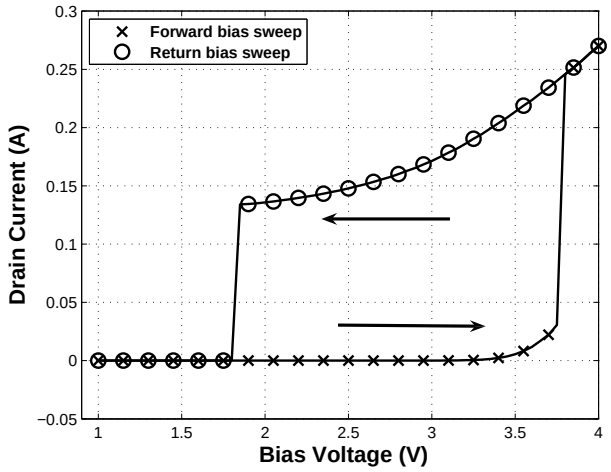


Figure 4.26: A test for parametric oscillations. The biasing voltage is slowly swept from high to low and back while the drain current is being observed. Any sudden jumps in the current means that an oscillation is occurring.The impedance seen looking into the drain biasing network with and without the lossy elements added.

4.7.1 Test for Parametric Oscillations

A parametrically oscillating power amplifier could potentially be dangerous to measurement and other equipment. Because the amplifier only oscillates under certain conditions the oscillation could easily be missed under testing. A simple test is therefore proposed for power amplifiers to check for parametric oscillations. In this test the gate voltage of the power amplifier is swept in steps from well below its threshold voltage to the highest value it will be biased at. Then

without switching the supply voltage off the gate voltage is swept back down to the original voltage. During these two sweeps the drain current is recorded. Figure 4.26 shows the results of this test for the carrier amplifier. It can clearly be seen when the oscillation starts at a biasing voltage of 3.5 V because the current level has a sudden increase. Interestingly it can be seen that the oscillation once started continues oscillating at much lower gate voltages than was originally required to set it off. This can be observed in the return sweep of the bias voltage in figure 4.26. By using this test the chances of a parametrically oscillating power amplifier remaining undetected is reduced.

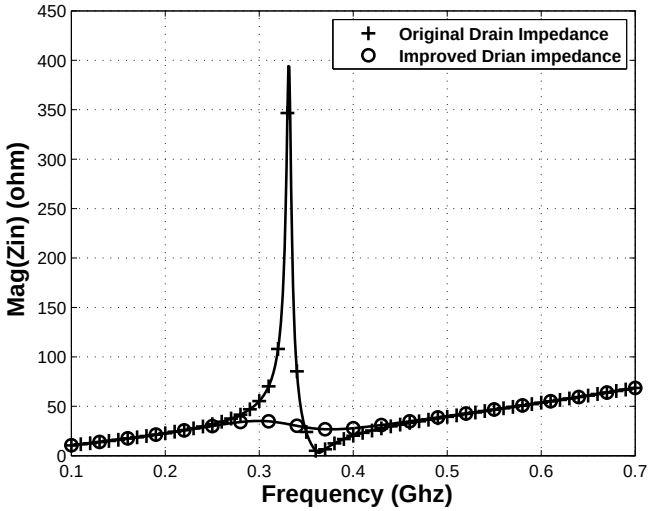


Figure 4.27: The impedance seen looking into the drain biasing network with and without the lossy elements that were added in order to dampen the unwanted resonance at 320 MHz.

4.7.2 Solution to Oscillation Problems

The root of the oscillation problems was found to be the drain bias network designed in section 3.8. A resonance can be observed by simulating the impedance seen when looking into the drain biasing network from the amplifier side with Microwave Office. Figure 4.27 shows that the simulated resonance occurs at around 320 MHz. This can be confirmed as the problem because the resonance frequency is in the same range as the fundamental frequency of the measured oscillation (see figure 4.25). The resonance is occurring due the interaction between the big electrolytic 470 uF capacitor and the smaller 33 pF ceramic capacitors. A snubber network consisting of a 15 Ω resistor in series with a 220 pF is added to ground to provide a lossy network to dampen the resonance (see figure 4.28). From the simulation results in figure 4.27 it can be seen that the resonance is now greatly reduced. The power amplifiers were tested with the spectrum analyser and the test procedure described in the previous section and no more oscillations were found.

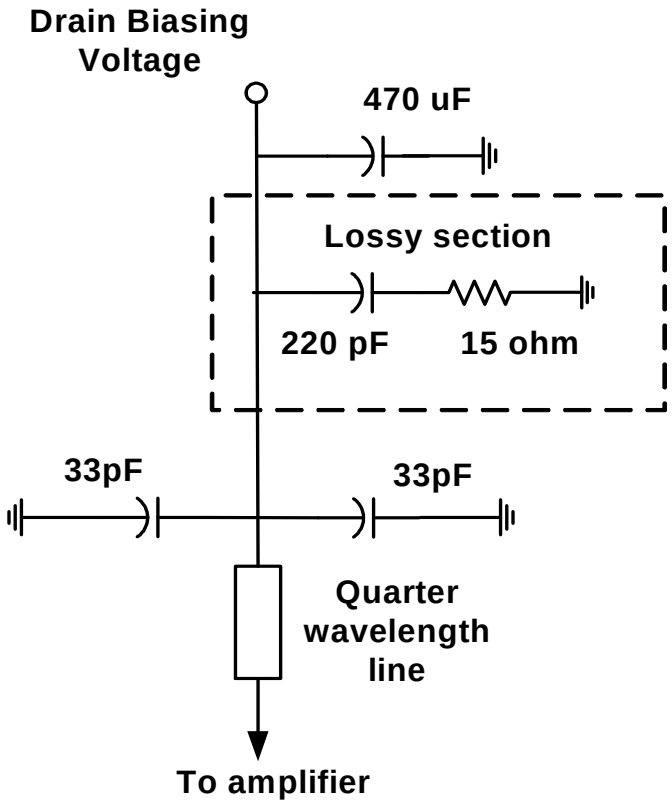


Figure 4.28: This schematic shows drain bias network with the lossy elements needed to dampen the resonance included.

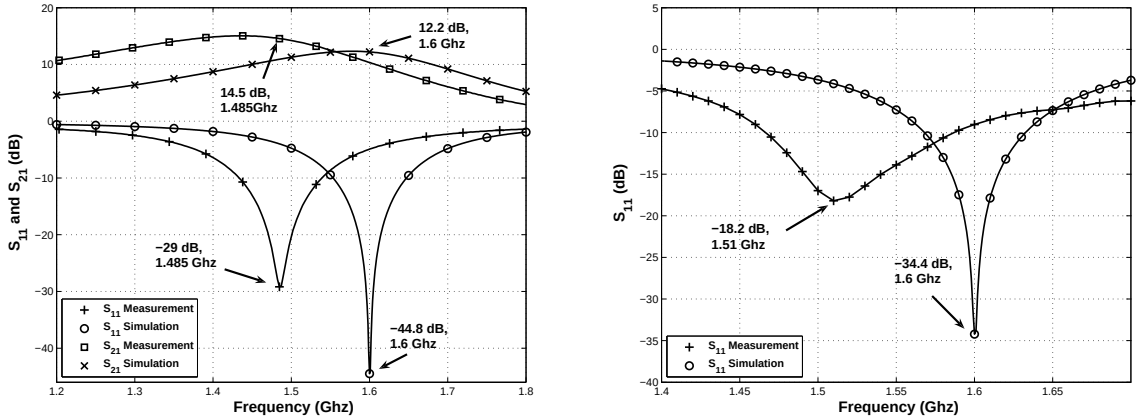
4.8 Amplifier Performance

The carrier and peaking amplifiers designed in Chapter 3 were measured using the techniques described in section 4.6. The results of the measurements will be discussed and compared to simulated values in the next two sections.

4.8.1 Scattering Parameters

Figure 4.29 compares the results of scattering parameter measurements (using the setup described in section 4.6.3) with the simulation results obtained from Microwave Office. The carrier amplifier S_{11} (4.29 a)) shows a shift in frequency to 1.485 GHz from the designed and simulated value of 1.6 GHz. This is reflected in the S_{21} measurement where it can be seen that the maximum gain point has been shifted to a lower frequency. Since the peaking amplifier is biased below its threshold voltage the amplifier is inactive and no S_{21} measurement could be made. However, the S_{11} measurement for the peaking amplifier in figure 4.29 b) also shows a shift to a lower frequency, with the minimum S_{11} appearing at 1.51 GHz instead of the 1.6 GHz designed and simulated frequency. This shift in frequency can be partly attributed to substrate permittivity being different from the specified value. The variation in permittivity and its effect is discussed in section 4.9.

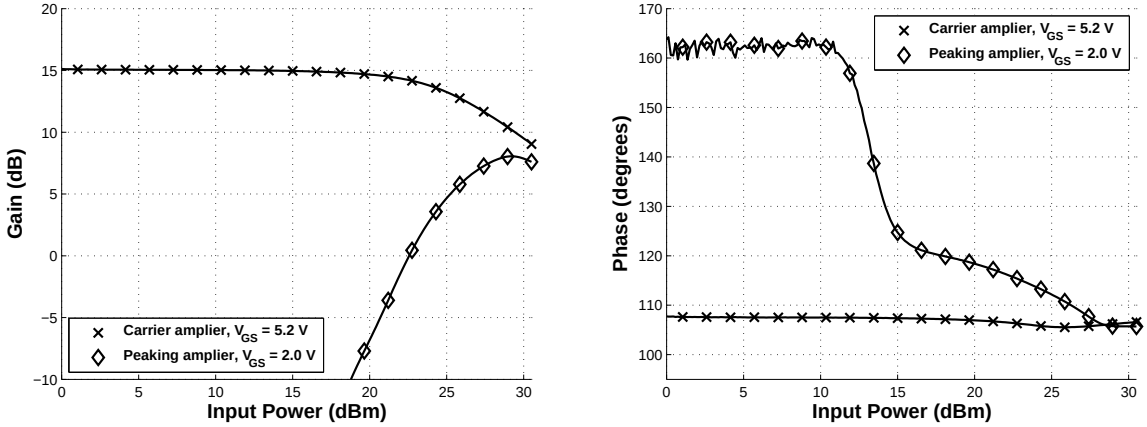
The main goal of this thesis is the evaluation of different types of Doherty amplifiers. This result of this evaluation is independent of the design frequency. It was therefore decided to operate the amplifiers at a center frequency of 1.5 GHz instead of 1.6 GHz for the evaluation to ensure



(a) Carrier amplifier (b) Peaking amplifier

Figure 4.29: The results for the scattering parameter measurements of the carrier and peaking amplifiers. Figure a) shows the measured and simulated values of S_{11} and S_{21} for the carrier amplifier. A frequency shift to 1.485 Ghz can be observed. In figure b) it can be seen that the measured value for S_{11} again deviates from the simulated value and reaches a minimum at 1.51 Ghz.The gain and transmission phase of the carrier and peaking amplifiers. Figure a) shows the typical gain expansion for the class C used by the peaking amplifier. The large variation in the transmission phase as the peaking amplifier becomes active can be seen in figure b).

good input matching and amplifier performance.



(a) Gain (b) The transmission phase

Figure 4.30: The gain and transmission phase of the carrier and peaking amplifiers. Figure a) shows the typical gain expansion for the class C used by the peaking amplifier. The large variation in the transmission phase as the peaking amplifier becomes active can be seen in figure b).

4.8.2 Gain and Phase performance

The measured transmission phase and gain for the two amplifiers can be observed in figure 4.30. The carrier amplifier shows the linear gain expected from a class AB implementation. The gain starts to drop of at higher input power levels with the 1 dB compression point at 23.2 dBm of

input power. The peaking amplifier demonstrates a large amount of gain expansion. This is characteristic of the class C implementation used for the peaking amplifier.

The phase response in figure b) demonstrates a large variation in the peaking amplifier transmission phase, occurring as the peaking amplifier becomes active. The difference in phase difference between the carrier and peaking amplifiers and the variation in peaking amplifier phase plays a large role in the performance of the Doherty amplifier. This is discussed in more detail in Chapter 5.

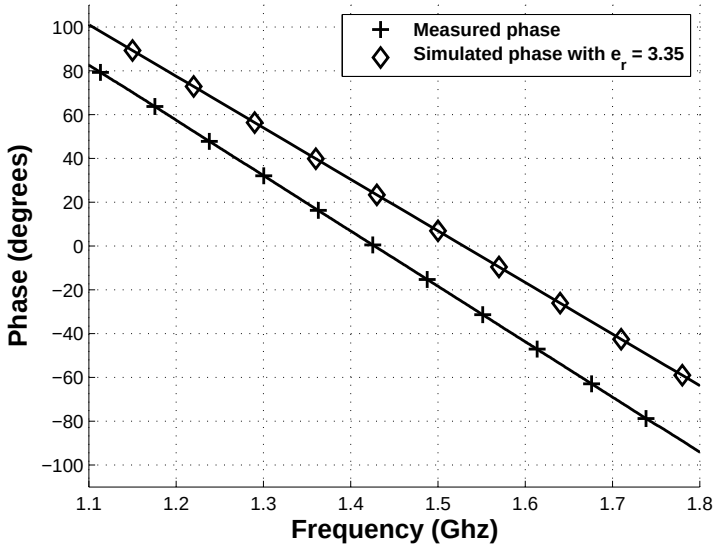


Figure 4.31: The simulated and measured transmission phase for a micro-strip line off 111.7 mm. At 1.5 Ghz the difference between the measurement and simulation is 25.3 degrees. By changing the e_r in the simulation from 3.35 to 3.91 the simulated value can be made to match the measured value very closely.

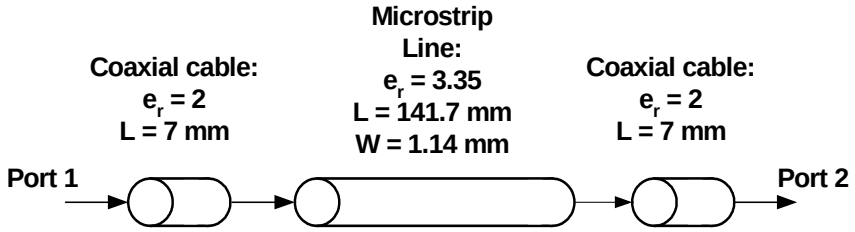


Figure 4.32: A schematic diagram showing how the micro-strip line was simulated. The SMA connectors are presented by two coaxial lines with values obtained from their data sheets.

4.9 Investigation into the Frequency Shift of the Amplifiers

In section 4.8.1 a shift from the design frequency was shown in the measured data for both the carrier and peaking amplifiers. This shift can be partly explained by a variation in the substrate permittivity. The substrate used was Rogers 4003 with a specified e_r of 3.35 at 10 Ghz, with

a variation of less than 1% in the frequency range 1-10 Ghz. However, a test of the substrate showed an e_r of 3.91.

4.9.1 Substrate Test

To test the permittivity of the substrate a single micro-strip line was manufactured on the Rogers 4003 substrate, with SMA connectors added to allow measurement on a network analyser. The length of the line up to the SMA connectors was measured with a vernier as 111.7 mm, while the line width was 1.14 mm. The network analyser was calibrated using a SOLT calibration before measuring the phase response of the micro-strip line. For comparison to measurements a simulation was made in Microwave Office. Figure 4.32 shows a schematic diagram of the simulation. The effect of the SMA connectors were included in the simulation by using a coaxial cable with $e_r = 2$ and length 7 mm. These are values were obtained from the specifications for the SMA connectors. The results of the simulation using $e_r = 3.35$ compared to the measurement is shown in figure 4.31. There is a difference of 25.3 degrees in the measured and simulated values at 1.5 Ghz. Since the physical dimensions of the line where carefully measured and a SOLT calibration performed before measurement, the only explanation for the difference in the simulation and measurement is that the permittivity of the substrate is not 3.35. By tuning the e_r in Microwave Office the simulated value for the phase difference can be made to match the measured phase very closely. The value of e_r at which this occurs is 3.91.

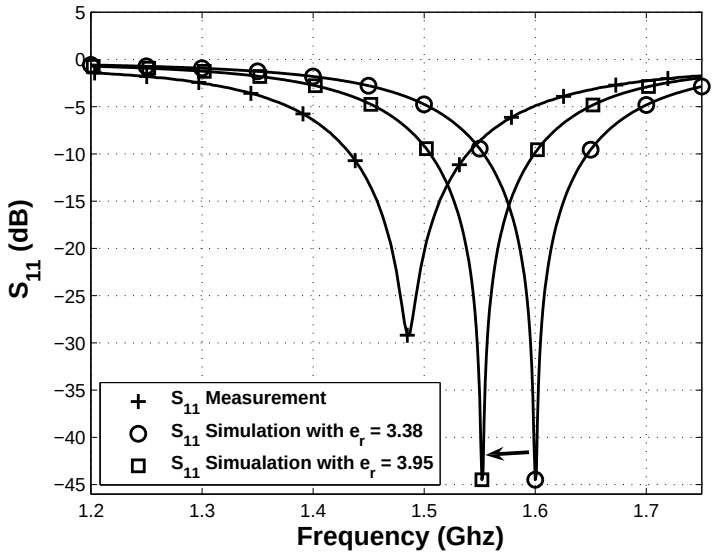


Figure 4.33: The measured values for S_{11} of the carrier amplifier compared to simulation values with the value originally used for the design ,$e_r = 3.35$ and the measured of $e_r = 3.91$. The simulated values with the corrected e_r shows that the variation in e_r is partly responsible for the frequency shift.

4.9.2 Scattering Parameter Simulation with Corrected Permittivity

Figure 4.33 demonstrates the effect of using the correct e_r measured in the previous section for the simulations of the amplifiers. The simulated minimum value for the carrier amplifier S_{11}

changes from 1.6 Ghz with an $e_r = 3.35$ to 1.52 Ghz using $e_r = 3.91$. The difference between the specified e_r and the real e_r is therefore partly responsible for the shift from the design frequency.

4.10 Conclusion

In this chapter many practical aspects of the amplifier design was examined. The modelling of passive components was investigated and an improved model suggested for the SMD capacitors used in the design. Physical design issues discussed included the modular design approach, the thermal considerations involved in the design and the effects of using a single ground wire. The measurement setups used to measure the power amplifiers were also described. The results of the measurements for the carrier and peaking amplifiers showed a shift in the matching of the amplifiers from the design frequency to 1.5 Ghz. This shift can be partly explained by the permittivity of the substrate being different to the specified value. It was decided to continue the evaluation of the Doherty amplifiers at a center frequency of 1.5 Ghz.

Chapter 5

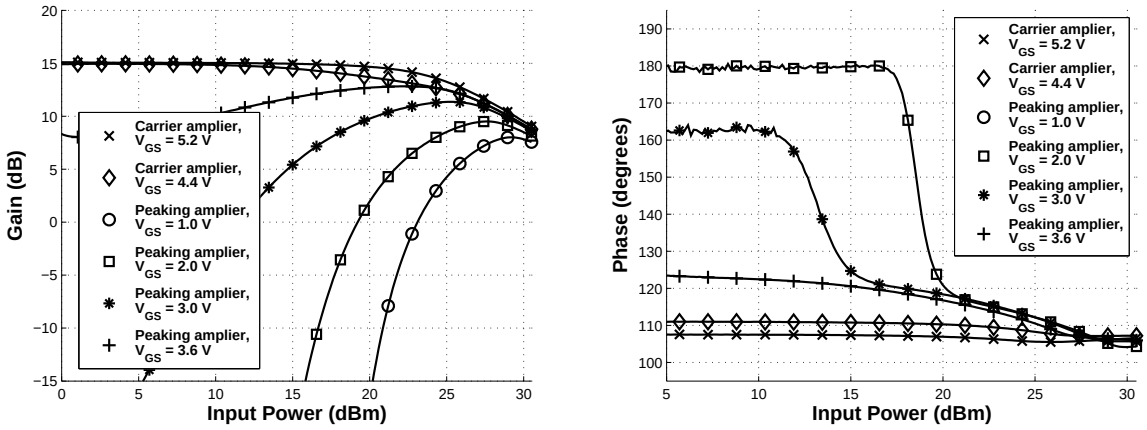
Determining the Best Bias Points for the Doherty Amplifier

5.1 Introduction

In the previous chapters the design and manufacture of a Doherty amplifier was described. However, these designs were based on certain assumptions. The first of these is that the amplifiers provide equal currents at peak envelop power (PEP), allowing the the load-pulling scheme to work successfully. This is however not the case (as discussed in section 2.5). A second problem arises because the phase response of the amplifiers against input power was not considered during the design. This aspect is further investigated in section 5.2. These factors contribute to the Doherty amplifier not working exactly as designed. By choosing the bias voltage carefully we can compensate for some of the non-ideal behaviour of the amplifier. In this chapter the effect of using different bias for the Doherty amplifier will be investigated, with the aim to find the best possible configuration. The criteria for defining what is the best Doherty amplifier will be discussed in section 5.3. Two versions of the Doherty amplifier are investigated, one with equal power division (section 5.5) and one with the unequal power division scheme (section 5.6) designed in section 3.11.2.

5.2 Gain and Phase Performance of the Amplifiers

Ideally the carrier and peaking amplifier should be completely in phase at all input power levels. Unfortunately this is not the case. Figure 5.1 demonstrates the effect of using different bias points for the peaking and carrier amplifiers. In figure 5.1 a) the gain expansion of the class C amplifier used to implement the peaking amplifier can be clearly seen. With increased bias levels the peaking amplifier has less pronounced gain expansion and starts providing output power at lower input levels. By controlling the bias point for the peaking amplifier we can therefore control its contribution to the Doherty Amplifier output to some point. From figure 5.1 b) the variation in the peaking amplifier transmission phase can be seen. For the deep class C peaking amplifiers with V_{bias} at 1 and 2 V the phase difference when the peaking amplifier starts conducting is especially large. As the peaking amplifier bias voltage is increased however, this variation in phase is greatly reduced. The effect of the bias voltage on the carrier amplifier



(a) Gain

(b) The transmission phase

Figure 5.1: The gain and transmission phase of the carrier and peaking amplifiers for various bias voltages. Figure a) shows the typical gain expansion for the class C used by the peaking amplifier. As the peaking amplifier gate bias voltage is increased the gain expansion becomes less pronounced. Figure b) also shows that the variation in phase for the peaking amplifier can be reduced by increasing the gate voltage. The carrier amplifier also shows a slight variation in the transmission phase with varying bias voltage, but remains relatively unchanged over input power.

is less pronounced but still significant. For example a 2.8 degrees phase difference and 0.75 dB gain difference can be observed at 25 dBm input power between a carrier amplifier biased at 5.2 V and one biased at 4.4 V.

5.3 Criteria for Determining the Best Performance

There are several possible criteria by which to evaluate the performance of the power amplifiers and by which to choose the best biasing points. These will be discussed in the following subsections.

5.3.1 Maximum Output Power

The maximum output power refers to the output power level at which gain compression occurs. The 1 dB compression point is the point at which the amplifier gain has dropped 1 dB below its small-signal value. Whenever the term maximum output power is used in this document it refers to the 1 dB compression point. As the main goal of the power amplifier is to provide a high output power, the maximum output power is an important aspect of the results.

5.3.2 Efficiency

The method often used for calculating the efficiency of a power amplifier involves simply calculating the ratio of RF output power to DC input power. However this does not take the input power into consideration. A more useful definition is that of power added efficiency (PAE) [16]:

$$\eta_{PAE} = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{5.1}$$

This is the definition that is referred to as efficiency in this thesis. The DC power can be found by simply multiplying the drain currents of the carrier and peaking amplifiers with the drain biasing voltage. One of the main reasons for using the Doherty amplifier is its improved efficiency compared to the balanced amplifier. Therefore efficiency, along with output power, is one of the main criteria taken into consideration when evaluating performance.

5.3.3 Gain Flatness

The gain flatness of the amplifier refers to the amount of deviation in the amplifier gain as a function of input power. Gain flatness was an important aspect in the evaluation of the amplifiers, but was not a primary design goal. Although better gain flatness was welcomed, a gain flatness of 0.5 dB was considered acceptable for the power amplifiers.

5.3.4 Inter-modulation Distortion

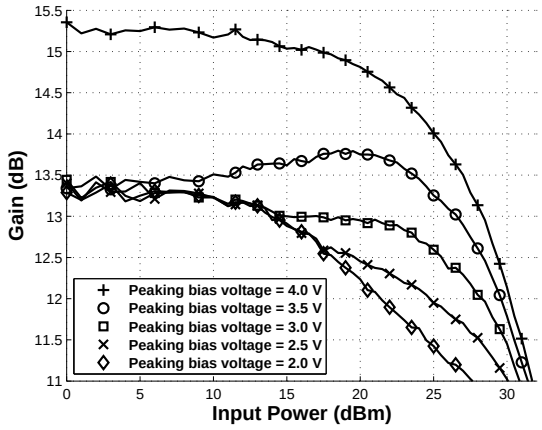
The third order intercept point provides a measure of the level of inter-modulation distortion generated by the amplifiers. Inter-modulation products play a very important role in determining the amplifiers use for real world applications. These products were taken into account for the final comparison of the different Doherty amplifier types, but was not used to determine the best bias points for a particular design.

Table 5.1: The carrier amplifier V_{GS} bias voltages used for the measurements and the resultant drain bias currents.

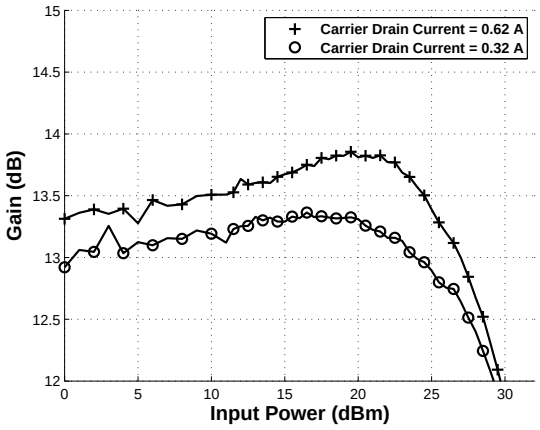
V_{GS} Biasing Voltage (V)	4.5	4.67	4.85	5.02
Drain Bias Current (A)	0.32	0.42	0.52	0.62

5.4 Measurements of Doherty Amplifiers

The measurement setup described in section 4.6.1 was used to measure the performance of the Doherty amplifiers against input power. The two types of Doherty amplifiers (equal and unequal power division) were measured in the same way. The variables in the measurements are the carrier amplifier V_{GS} bias voltage and the peaking amplifier V_{GS} bias voltage. Four different carrier amplifier V_{GS} bias points were used for the measurements. Their values where chosen so that the carrier amplifier drain bias current varies from 0.32 A to 0.62 A in 0.1 A steps. These voltage values can be found in Table 5.1. The peaking amplifier V_{GS} bias voltage was swept from 0 to 5.5 V in 0.5 V steps. All combinations of the the chosen carrier and peaking amplifier V_{GS} bias voltages were measured, creating a matrix of measured data for comparison. For each combination of V_{GS} bias voltages a power sweep was done from 0 to 31 dBm at 1.5 Ghz. The output power for the Doherty amplifier and amplifier drain bias currents of both the carrier and peaking amplifiers were recorded. The results for these measurements will be shown in the next sections when they are used to determine the best bias points for the Doherty Amplifier.

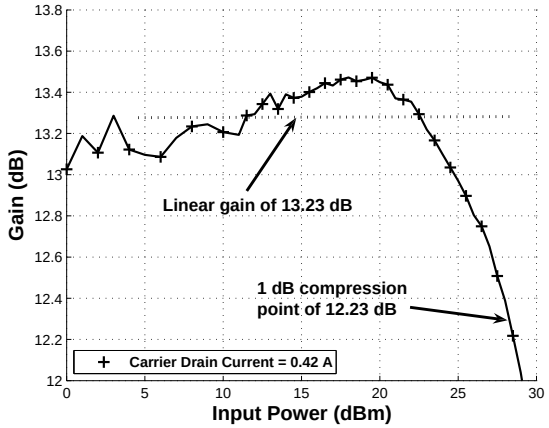


(a) Gain with the carrier amplifier $V_{GS} = 4.85$V

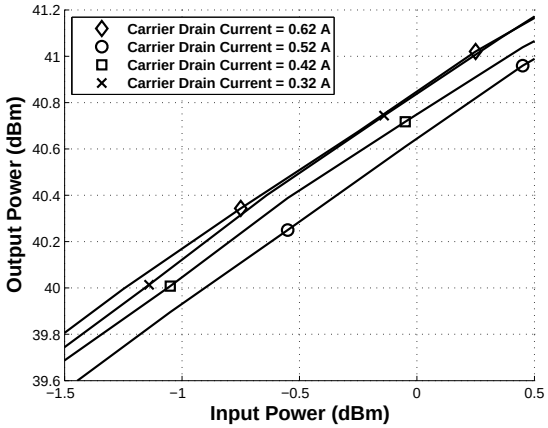


(b) Gain with the peaking amplifier $V_{GS} = 3.5$ V.

Figure 5.2: The gain against input power graph the the even Doherty amplifier with the carrier and peaking amplifiers biased at selected voltages. Figure a) shows the gain graphs obtained if the carrier amplifier is biased with a current of 0.52 A and several different peaking amplifier biasing voltages are selected. Figure b) shows the gain graph with the peaking amplifier biasing voltage fixed to 3.5 V with the carrier amplifier biased at 0.32 and 0.62 A respectively.



(a) Determination of the 1 dB compression point

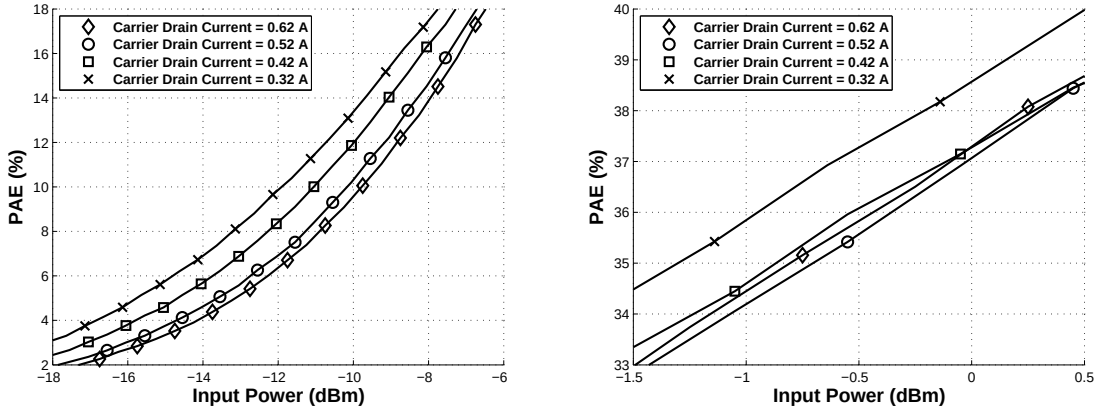


(b) Output power versus backed off input power, with the peaking amplifier $V_{GS} = 3.5V$

Figure 5.3: Figure a) demonstrates how the 1 dB compression point was determined for one of the even Doherty amplifier bias permutations. In figure b) the output power against input power graphs for with the peaking amplifier $V_{GS} = 3.5$ V.

5.5 Equal Power Division Doherty Amplifier

The best biasing voltages for the equal power division Doherty Amplifier will be chosen in this section based on measurements, As discussed in section 5.3, the choice will be based on the output power and efficiency of the amplifier, so long as the gain flatness remains within a acceptable level (section 5.3.3).



(a) PAE against backed off input power at low power levels.

(b) PAE against backed off input power at PEP

Figure 5.4: In a) and b) the power added efficiency against backed off input power can be observed for the even Doherty amplifiers being tested..

5.5.1 Determining the Peaking Amplifier Gate Voltage

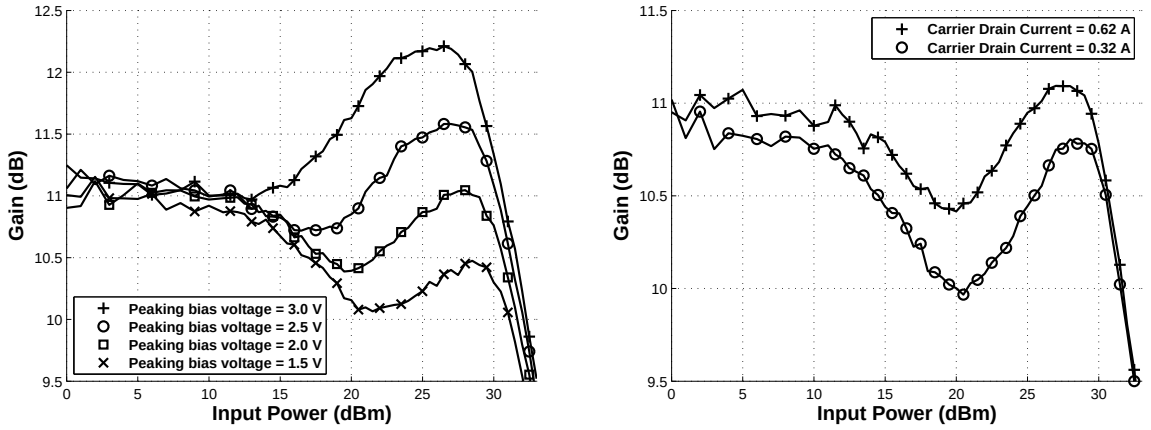
As discussed in section 5.4 a large a matrix of measured data is available for the different biasing points of the carrier and peaking amplifier. To gain a feeling for the issues involved the carrier amplifier V_{GS} was set to 4.85 V (0.52 A drain bias current) and the effect of changing the peaking amplifier V_{GS} voltage investigated. Figure 5.2 a) shows the measurements for selected bias voltages. The first criteria is to find the bias permutations which provide gain flatness. From the figure it can be observed that a peaking amplifier V_{GS} of 4 V results in the peaking amplifier providing current even at low power levels. This is not what we require for the Doherty working. Therefore all peaking amplifier bias voltages from 4 and above was not considered. Figure 5.2 a) also shows that the gain of the peaking amplifier with a V_{GS} of 2 V and lower falls quickly and does not maintain gain flatness at all. The graph shows that although the version with the peaking amplifier $V_{GS} = 3$ V possesses reasonable gain flatness, more gain is obtained with a V_{GS} of 3.5 V at high power.

Changing the carrier amplifier V_{GS} has an effect on the performance, but the general shape of the gain versus input power graphs remain the same. This can be observed in figure 5.2 b) where the gain is plotted for a peaking amplifier V_{GS} fixed at 3.5 V and different carrier amplifier drain currents. Only the measurements with the largest and smallest carrier amplifier V_{GS} measured (with $I_{drain} = 0.32$ or 0.62 A) are depicted for clarity purposes. Because the general shape of the gain graph stays the same the observations about the gain flatness of different peaking amplifier bias points are valid for all four carrier amplifier V_{GS} points measured. The peaking amplifier V_{GS} is therefore fixed at 3.5 V because it provides a reasonable gain flatness across the entire input power range.

5.5.2 Determining the Carrier Amplifier Gate Voltage

The peaking amplifier V_{GS} voltage was already fixed at 3.5 V in the previous section in order to preserve gain flatness. The choice of the carrier amplifier V_{GS} voltage must however still be made. After gain flatness is confirmed, the main criteria for choosing the bias points is maximising the

output power and efficiency of the amplifier (see section 5.3). Figure 5.3 a) shows how the linear gain of an amplifier is chosen as the average gain over the lower input power levels. Using this linear gain and the gain versus input power graph, the point at which the 1 dB compression point occurs can now be determined as 28.3 dBm. Calculating the compression point for each of the four carrier amplifier V_{GS} points allows us to plot the output power against backed off input power (figure 5.3 b)) as well as the efficiency against backed off input power (figures 5.4 a) and b)) graphs. The output power and efficiency performance is now easily compared. It can be seen that the output power at PEP (Peak envelope power, occurring at 0 dBm backed off input power) for all four variations are quite similar and differs only by 0.2 dB. The efficiency graphs show a much clearer difference between the different carrier amplifier V_{GS} points. As is to be expected the lowest bias point for the carrier amplifier allows for the best efficiency, especially at low power levels (see figure 5.4 a)). Because it has been shown that almost no penalty is paid in output power performance, we can choose the carrier amplifier point resulting in the the greatest efficiency, $V_{GS} = 4.5$V. We have now selected the best Doherty amplifier with even power division from the measured data according to our criteria, with the carrier amplifier bias voltage at 4.5 V and the peaking amplifier voltage at 3.5 V. An output power of 40.82 dBm is achieved at PEP with an efficiency 38.6%. The realised efficiency and output power will be discussed further when the different Doherty configurations are compared in chapter 7.



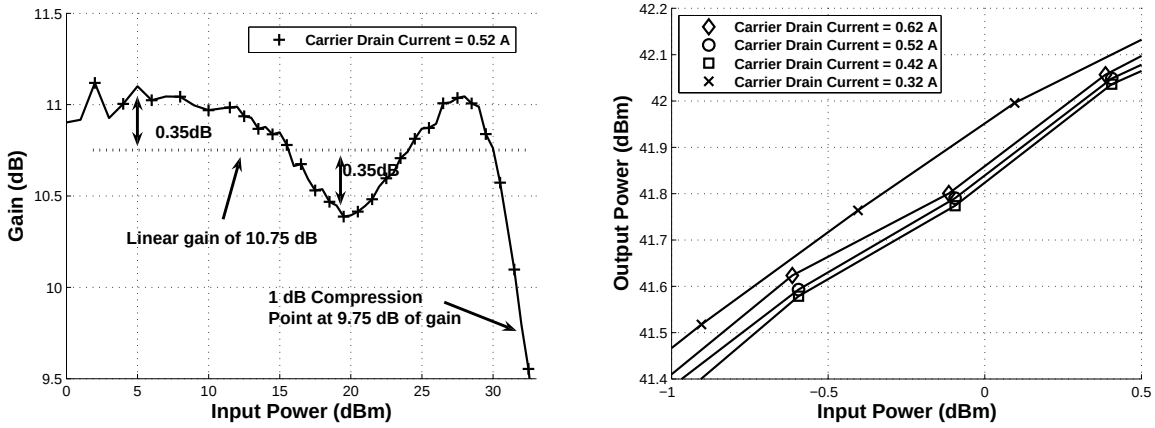
(a) Gain with the carrier amplifier $V_{GS} = 4.85$V

(b) Gain with the peaking amplifier $V_{GS} = 2$ V

Figure 5.5: The gain against input power of the uneven Doherty amplifier with the carrier and peaking amplifiers biased at selected V_{GS} voltages. Figure a) shows the gain obtained if the carrier amplifier is biased with a current of 0.52 A and several different peaking amplifier V_{GS} voltages are selected. Figure b) shows the gain with the peaking amplifier V_{GS} voltage fixed to 2.5 V with the carrier amplifier biased at drain current of 0.32 and 0.62 A respectively.

5.6 Unequal Power Division Doherty Amplifier

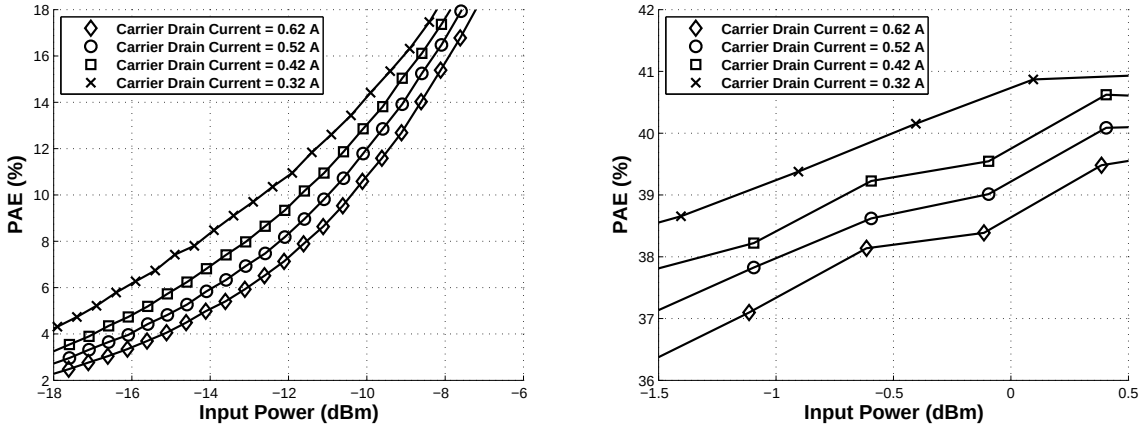
The choice of the bias points for the unequal power division Doherty Amplifier was made in a very similar way to that of the even Doherty amplifier in the previous section. Once again the choice was based on the measurements described in section 5.4, with the main criteria being amplifier efficiency and output power as long as an acceptable gain flatness is achieved.



(a) The determination of the 1 dB compression point

(b) Output power versus backed off input power with the peaking amplifier V_{GS} = 2 V

Figure 5.6: Figure a) demonstrates how the 1 dB compression point was determined for one of the uneven Doherty bias permutations. In figure b) the output power against backed off input power for the uneven Doherty amplifiers are shown with the peaking amplifier V_{GS} = 2.5 V and the four different carrier amplifier bias points. .



(a) PAE against backed off input power at low power levels.

(b) PAE against backed off input power at PEP

Figure 5.7: In a) and b) the power added efficiency against backed off input power can be observed for the uneven Doherty amplifiers being tested with the peaking amplifier V_{GS} = 2.5 V.

5.6.1 Determining Peaking Amplifier Gate Voltage

The effect of the peaking amplifier V_{GS} can be observed in figure 5.5 a). The gain for the unequal Doherty amplifier is shown with the carrier amplifier biased with a drain current of 0.52 A and several different peaking amplifier V_{GS} voltages. It can be seen from the graph that a peaking amplifier V_{GS} of 3.5 V or higher leads to an unacceptable rise in the gain at high input power levels. Similarly the bias combinations with a peaking amplifier V_{GS} of 1.5 V or less are not considered because of the loss of gain flatness. This leaves a peaking amplifier V_{GS} of 2 and 2.5 V as the two remaining possibilities with an acceptable gain flatness. The V_{GS} of 2.5 V is chosen because it results in a higher gain at high power levels as shown in figure 5.5 a).

The carrier amplifier V_{GS} has some effect on the performance, but as can be seen from figure 5.5

b) where the largest and smallest carrier V_{GS} are plotted (with a peaking amplifier V_{GS} of 2.5 V), the general shape of the gain versus input power remains the same. The peaking amplifier V_{GS} is therefore fixed at 2.5 V because it provides a reasonable gain flatness across the entire input power range. In the next section the choice of the carrier amplifier V_{GS} will be discussed.

5.6.2 Determining the Carrier Amplifier Gate Voltage

In the previous section the peaking amplifier V_{GS} was chosen as 2.5 V. The effectively and output power of the unequal Doherty amplifier can now be compared for the four carrier amplifier V_{GS} voltages used and with the peaking amplifier V_{GS} fixed at 2.5 V. The 1 dB compression point calculation for the unequal Doherty amplifier is demonstrated in figure 5.6 a) for a carrier amplifier drain current of 0.52 A (V_{GS} = 4.85 V). The linear gain is taken as the average gain over the lower input power values. In this case the linear gain is 10.75 dB with the 1 dB compression point occurring at a gain of 9.75 dB. The 1 dB compression point is calculated for all four carrier amplifier V_{GS} voltage in order to allow us to compare the output power and efficiency against backed off input power. The output power against backup input power comparison is shown in figure 5.6 a) while the PAE against backed off input power can be seen in figure 5.7 a) (at low input power levels) and figure 5.7 a) (at PEP). For the unequal Doherty amplifier the results are even more clear than the even Doherty amplifier. The lowest carrier amplifier drain bias current, I_{drain}= 0.32 A provides the best efficiency at low input power levels and at PEP, as well as the highest output power. The best points bias points for the unequal Doherty according to the chosen criteria is therfore a peaking amplifier V_{GS} of 2.5 V and a carrier amplifier V_{GS} of 4.5 V. With these values an output power of 41.95 dBm is achieved at PEP with an efficiency 40.75% This result will be discussed further in chapter 7 when performance of the various Doherty amplifiers are compared.

5.7 Conclusion

In chapter 3 a Doherty amplifier was designed. However this design was based on the assumption that the peaking amplifier would provide equal current to the carrier amplifier at PEP. The variations in phase of (especially that of the peaking amplifier) was also not considered in the design. The designed bias points are therfore not necessarily the optimum points of operation. In this chapter the measurement of the even and uneven power division Doherty amplifiers at various bias voltages were described (section 5.4). The criteria upon which the choice would be based was established in section 5.3. In the final two sections the best combinations of the carrier and peaking bias voltages was determined from the measured data for the even power division Doherty amplifier (section 5.5) and the uneven power division Doherty amplifier (5.6).

Chapter 6

Bias Adaption of Doherty Amplifier

6.1 Introduction

The classical Doherty amplifier requires the peaking amplifier to only start contributing current during the last section of input power before PEP (Peak envelope power). A class C implementation is often used to realise this behaviour. However, if the same device is used for the carrier and peaking amplifier, a class C implementation for the peaking amplifier will not provide equal output current to the carrier amplifier at PEP (see section 6.2). Bias adaption is a suggested scheme aimed at solving this problem [10]. The idea is to vary the peaking amplifier gate bias voltage dynamically depending on the input power level of the Doherty amplifier. Bias adaption schemes for single FET amplifiers was suggested by Saleh [18] to increase power added efficiency. Yang [21] demonstrated such a bias adaption system for the Doherty Amplifier. In this chapter a similar bias adaption system is proposed. The design is implemented and experimentally optimised for PAE (power added efficiency) and output power.

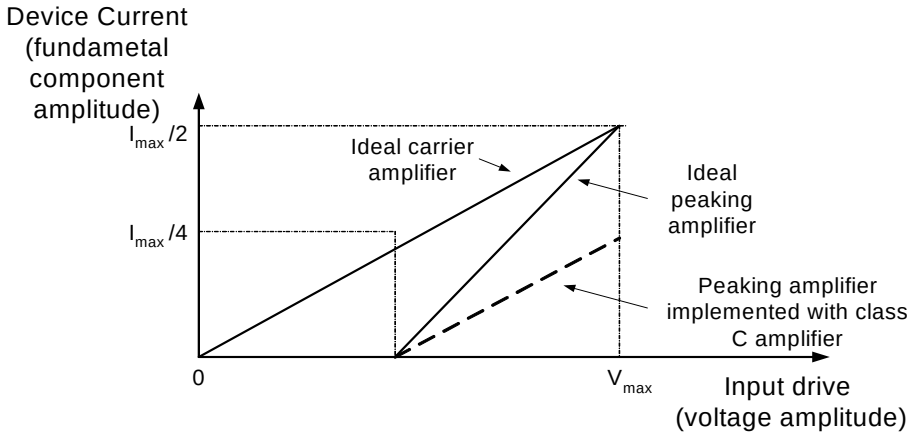


Figure 6.1: The required currents for the carrier amplifier and peaking amplifier to achieve Doherty working. If the peaking amplifier is implemented as a class C amplifier it provides insufficient current at full power for the load-pulling action of the Doherty amplifier.

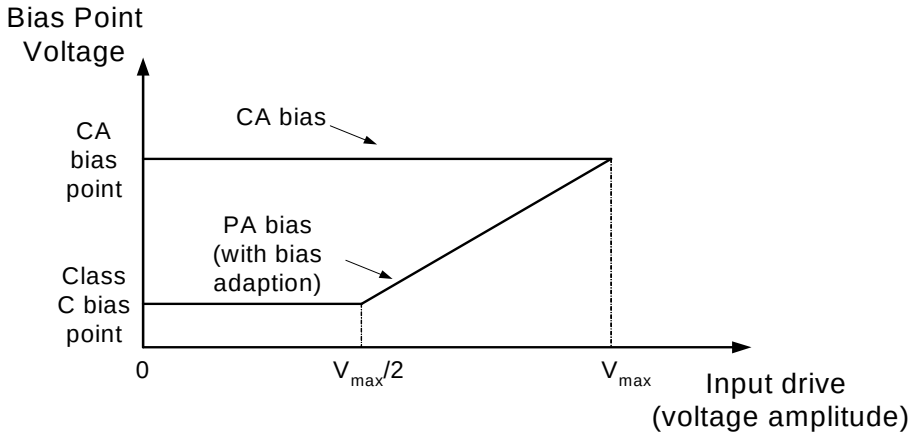


Figure 6.2: A theoretical bias adaption transfer function for the peaking amplifier gate voltage [10].

6.2 Conventional Doherty Amplifier Problem

As mentioned in the introduction of this chapter the peaking amplifier in a classical Doherty amplifier should only start producing current at 6 dB before PEP [10]. At PEP the currents from the peaking and carrier amplifiers should be equal to achieve the full load-pulling effect required by the Doherty amplifier. Figure 6.1 shows the required currents from the amplifiers against input voltage. By implementing the peaking amplifier with a class C amplifier the input power level at which the peaking amplifier starts providing current can be controlled. However, as shown in figure 6.1, the current produced at full power will not be sufficient. A suggested theoretical adaption transfer function is shown in figure 6.2 [10]. At low input levels the gate biasing level is kept at class C level. When the input voltage level reaches half the maximum input level (equal to 6 dB of input power before PEP) the bias voltage of the peaking amplifier starts to increase from its original level, until at the maximum input voltage (PEP) it is equal to the carrier amplifier gate bias voltage. The peaking amplifier current should then be close to the ideal peaking amplifier current shown in figure 6.1.

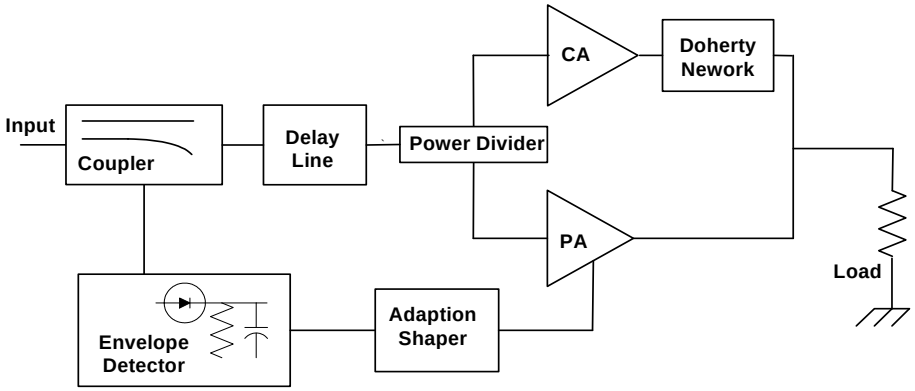


Figure 6.3: Schematic representation of a Doherty amplifier with a bias adaption network

6.3 Suggested Network for Bias Adaption System

Figure 6.3 shows the suggested bias adaption system [21]. The bias voltage of the peaking amplifier must be changed dynamically depending on the amplitude of the input power. Because the base-band signal is unavailable, the input amplitude levels must be sensed in some way. Therefore a coupler is added at the input of the Doherty amplifier. The bias signal has to change depending on the amplitude of the input, but actual RF information is not required for the bias adaption. An envelope detector can thus be used to provide a voltage in relation to the input power level, discarding the RF information. An adaption shaper circuit is then used to manipulate the signal from the envelope detector to provide the final bias signal to control the peaking amplifier. A complication of the system is the need to synchronise the changing bias voltage with the input, as the time taken for the signal from the coupler to travel through the envelope detector and through the bias control circuitry must be taken into account. For this reason a delay line is added between the coupler and the Doherty amplifier, to delay the input so that it arrives at the Doherty amplifier at the same moment as the changing bias voltage.

6.4 Specifications for the Adaption Shaper

The suggested adaption transfer function was demonstrated in figure 6.2. In the next sections the requirements for the adaption network will be investigated in more detail.

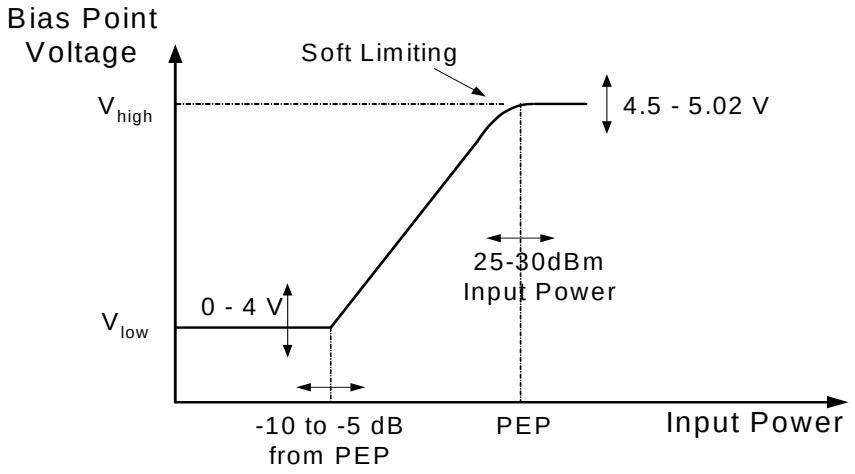


Figure 6.4: The specifications for the bias adaption transfer function

6.4.1 Power Levels

In section 5.5.2 it was shown that the input power for the equal power Doherty amplifier at saturation is 28.3 dBm. This would also then be the suggested input power at which the adaption shaper provides its maximum voltage level to the peaking amplifier. However, the exact saturation point is likely to change with the addition of the bias adaption system. Furthermore the power sampled by the shaper will be different to the input power at the Doherty amplifier because of the losses sustained by the delay line (see section 6.9). It is hard to determine the

exact effect of these two variables prior to the design. The adaption shaper must therefore able to be configurable so that the input power at which the maximum peaking voltage occurs can be changed. An estimation was made that the tuning range should be between 26 and 32 dBm of input power. The classical Doherty amplifier requires the peaking amplifier to begin providing output current at exactly 6 dB below PEP (section 2.4). The design for the Doherty Amplifier was also based on this premise. However as the amplifiers do not display ideal behaviour the optimum point to begin conduction for the peaking amplifier could be slightly different. This is therefore another variable that needs to be configurable. Figure 6.4 shows the required transfer function and the regions that are required to be tuneable.

6.4.2 Maximum Voltage Level

At PEP the peaking and carrier amplifiers should provide the same amount of output current. The adaption shaper should therefore set the gate voltage of the peaking amplifier equal to that of the carrier amplifier PEP. The carrier amplifier was designed with a gate voltage of 5.25 V (section 2.4.1). However in section 5.5.2 it was determined that using a carrier amplifier V_{GS} voltage of 4.5 V results in the best Doherty amplifier performance. From Table 5.1 it can be seen that the largest gate voltage used for the practical optimisation of the carrier amplifier was 5.02 V, and the smallest 4.5 V. This is therefor the range specified for V_{high}, the maximum voltage level to be attained by the adaption shaper.

6.4.3 Minimum Voltage Level

At power levels lower than 6 dB before PEP the peaking amplifier should remain inactive. This is achieved by keeping the effective gate voltage below the threshold voltage of 4 V (see section 3.2). The effective gate voltage is the DC voltage applied by the adaption system added to the DC component of the input voltage. By being able to tune the voltage applied by the adaption system the power level at which the peaking amplifier becomes active can be controlled. This minimum gate voltage level, V_{low}, should be tuneable from 0 V to 4 V for full control of the peaking amplifier bias level.

6.4.4 Soft Limiting

If the suggested theoretical transfer function (figure 6.2) is compared with the specification for the adaption circuit in figure 6.4 it can be seen that a soft transition has been added where the bias adaption attains V_{high}. This is due to linearity concerns as a sharp transition could cause unwanted distortion in the output of the amplifier.

6.5 Coupler

The adaption system must change the peaking amplifier gate bias voltage depending on the amplitude of the input power. As the base band signal is not available the input power level must be sensed in some way. A coupler is used to sense the input power level without interrupting the RF path. A single section coupled line coupler was used for the design [16]. Figure 6.5 shows

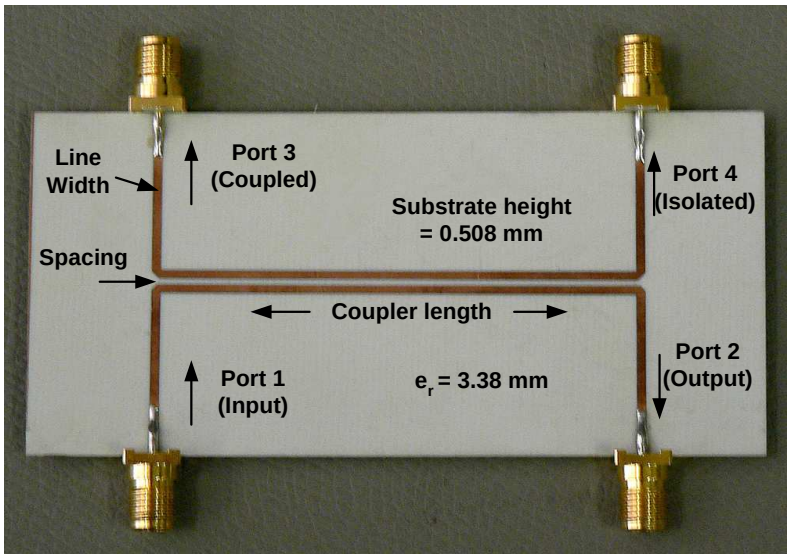


Figure 6.5: The 20 dB single section coupler used for the adaption network. The ports are indicated on the figure.

the manufactured coupler and indicates the port numbers. The coupling factor refers to the power level transmitted to the coupled port (port 3) in relation to the input port (port 1). The coupling factor was chosen as 20 dB. The voltage coupling factor C can now be calculated as

$$C = 10^{-coupler factor/20} = 0.1 \tag{6.1}$$

The output power is given as

$$P_{out} = (1 - C^2)P_{in} \tag{6.2}$$

which for the chosen coupler factor results in a 1% loss of input power. This was deemed an acceptable loss for the coupler. The even and odd mode impedances required to achieve the 20 dB coupling factor can be calculated as [16]

$$Z_{0e} = Z_0\sqrt{\frac{1+C}{1-C}} = 55.28 \tag{6.3}$$

$$Z_{0o} = Z_0\sqrt{\frac{1-C}{1+C}} = 45.23 \tag{6.4}$$

The physical dimensions influencing the even and odd mode impedance of the coupler are shown figure 6.5. They are the substrate height, the permittivity of the substrate, the line width, the coupler length and the spacing between the two lines. The substrate height and permittivity where determined by the use of the Rogers 4003 substrate with a height of 0.508 mm [4]. The line width used was that of a 50 Ω micro-strip line. In order to maximize the coupling to port 3 and minimize the energy coupled to port 2, the length of the coupled line is a quarter wavelength at the design frequency [16]. The spacing between the lines is the only unknown variable left. The method given by Mongia [17] was used to calculate the even and odd mode impedances in MATLAB for spacings varying from 0.1 mm to 4 mm in 0.01 mm steps. Please see Appendix A for the relevant equations used in MATLAB. The impedances were then compared to that of equations 6.3 and 6.4 and the coupler spacing resulting in impedances closest to these was

determined. A coupler spacing of 0.66 mm gives an even mode impedance of 54.78 Ω and an odd mode impedance of 44.82 Ω. By using Mongia's method (code in Appendix 9) the effective characteristic impedance of the coupler lines can be calculated as 49.77 Ω. Manipulating equation 6.3 gives the voltage coupling factor

$$C = ((Z0/Zoe)^2 - 1)/((Z0/Zoe)^2 + 1) \tag{6.5}$$

With Z_0 and Z_{oe} predicted as 49.77 Ω and 54.78 Ω respectively from Mongia's method, equation 6.5 results in a C of 0.096. This is very close to the chosen specification of 0.1 (Equation 6.1). The completed coupler (see figure 6.5) was measured with a network analyser. The measured voltage coupling factor was 0.097, providing a very close concurrence with the theoretical value.

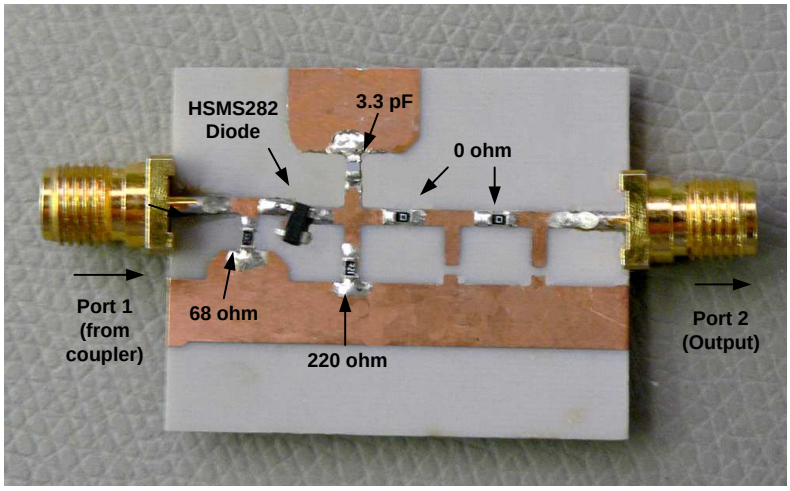


Figure 6.6: The envelope detector used in the design. Space was kept on the design for a higher order low-pass filter. However as this was not needed 0 Ω resistors were used to connect the signal path were interrupted by the unused footprints.

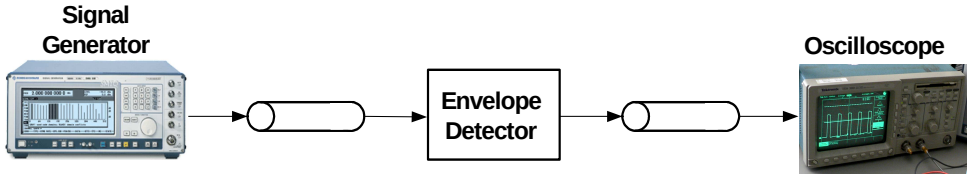


Figure 6.7: A schematic showing the setup used to measure the envelope output against input power.

6.6 Envelope Detector

The adaption system changes the biasing voltage depending on the input RF power level. Only the amplitude of the signal is needed, so a envelope detector was used to determine the input power level. The input signal is an amplitude modulated signal with a carrier frequency of 1.643

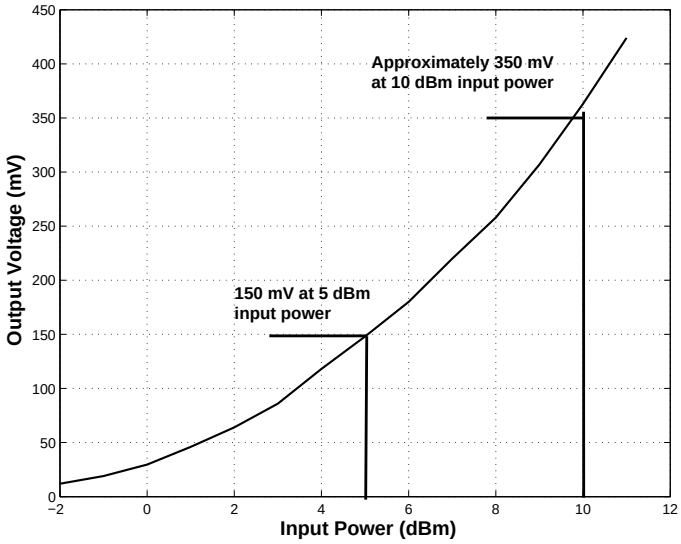


Figure 6.8: The measuring output voltage returned by the envelope detector against input power. The expected input power range and the corresponding output voltage range at which the adaption shaper should reach its maximum output voltage is shown in the figure.

Ghz and a maximum signal bandwidth of 30 MHz. A envelope detector designed with an zero-bias Schottky diode from Agilent was used. Schottky diodes are especially useful for unbiased detectors because their low threshold voltage allows detection of smaller signals. The choice of diode is influenced by the detector input power levels. Agilent recommends using a HSMS282x for unbiased detectors with an input power larger than -20dBm [5]. The input power level for the Doherty amplifier at PEP is 28.3 dBm (see section 6.4). The 20 dB coupler therefore provides a signal of 8.3 dBm to the envelope detector at PEP. Even if the required input power level for the peaking amplifier to start providing current is more than 6 dB below PEP, the input power levels to the envelope detector should remain well above -20 dBm. The HSMS282x is therefore a suitable choice for this design. The HSMS2825 package was chosen. The design is shown in figure 6.6. The 68 Ω resistor is added to ground at the input of the detector. It provides an input match and also provides a DC return path for the output current from the diode [1]. The suppression of the carrier frequency is not critical because the signal has to pass through several operational amplifiers in the adaption shaper part of the circuit. These operational amplifiers have a much lower bandwidth (see section 6.7) than the carrier frequency and will add additional low-pass effect. The values of the low-pass filter were chosen as 3.3 pF and 220 Ω, resulting in 3 dB bandwidth of 219 Mhz. This is much higher than the 30 Mhz bandwidth signal bandwidth, allowing the envelope information to pass through the envelope detector unattenuated.

The measurement setup used to measure the output of the envelope detector is shown in figure 6.7. A signal generator is used to provide input power at the carrier frequency and a oscilloscope is used to measure the output voltage from the envelope detector. The result of the measurements is shown in figure 6.8.

Table 6.1: Comparison of Specifications of Operational Amplifiers

	Slew Rate (V/us)	BW with Gain=1 (MHz)	BW at Higher Gain	Package
AD8007	1000	650	40 (Gain=5)	SOIC 8
AD8036	1500	195	90 (Gain=2)	SOIC 8
OPA690	1800	500	45 (Gain=3)	SOIC 8
OPA843	1000	800	260 (Gain=5)	SOIC 8
AD8003	4300	1650	70 (Gain=5)	LVCSP

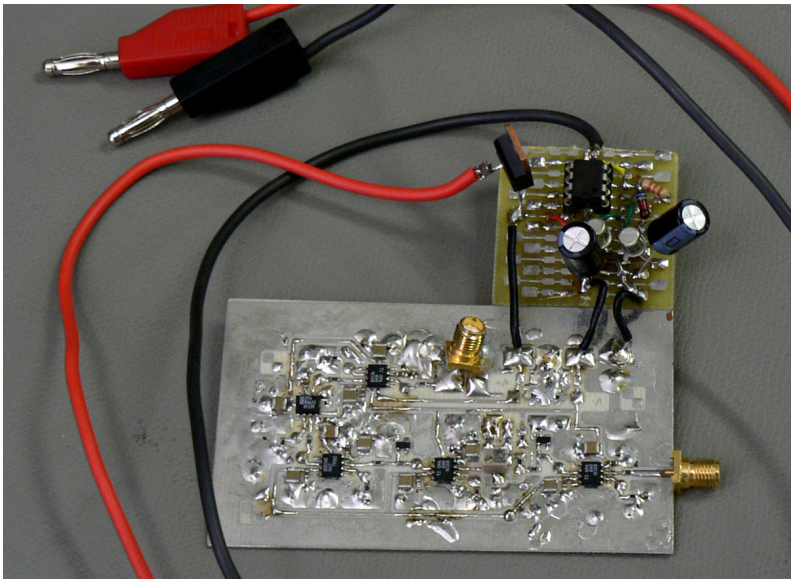


Figure 6.9: The adaption shaper circuit shown with power supply attached. The power supply supplies voltage rails of -3 and 8 V.

6.7 Adaption Shaper

In section 6.4 the specifications for the adaption circuit was discussed, while in sections 6.5 and 6.6 a coupler and envelope detector was designed and measured. This section will show the design of the adaption shaper. The completed adaption shaper can be seen in figure 6.9. The adaption shaper consists of two main stages, namely a soft limiting stage and an amplification stage. From the specifications (section 6.4) the expected power levels from the coupler at saturation will range from 5 to 10 dBm. The measurements of the envelope detector (figure 6.8) can now be used to calculate the input voltage at which the shaper should reach its maximum output voltage. The shaper input voltage range is 150 to 350 mV.

6.7.1 Hardware considerations for the Adaption Shaper

The signal obtained from the coupler and envelope sections of the adaption system is too small to control the biasing voltage of the peaking amplifier directly. An amplification stage is therefore needed to amplify the signal from the envelope detector. It was decided to use voltage-feedback amplifiers to achieve the desired amplification. Several operational amplifiers were considered for the design. The main consideration was the bandwidth of the amplifier, as the signal bandwidth of 30 MHz is quite large compared to the capabilities of many voltage-feedback operational amplifiers. A second important consideration is the slew rate of the operational amplifier.

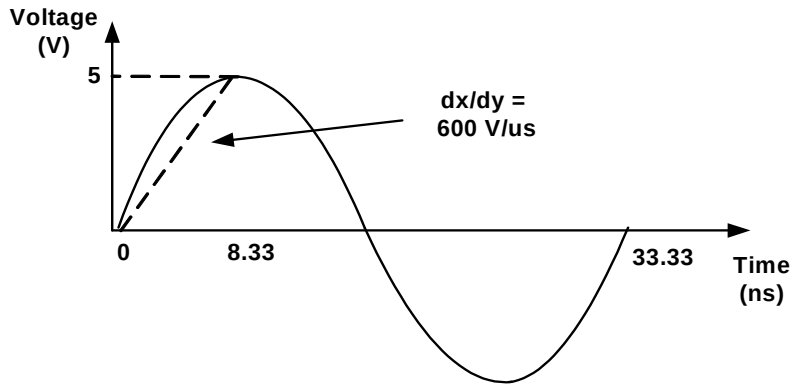


Figure 6.10: An approximation of the required slew rate for a 30 MHz signal with a voltage amplitude of 5 V.

Figure 6.10 shows how an approximation for the required slew rate was calculated. With V_{high} as 5 V and a 30 MHz signal the approximate required slew rate is 600 V/us. Table 6.1 lists the operational amplifiers acquired for the design. The AD8003 has the highest slew rate and also the highest bandwidth. However, it was decided not to use it in the design because it was only available in a LVCSP package. This package has dimensions that are unsuitable for soldering by hand. The other operational amplifiers, although less impressive than the AD8003, nevertheless meets the specifications and are available in SOIC-8 packages which is more suitable for soldering by hand. One type of operational amplifier would have been sufficient for the design. However, as only limited numbers of each type was available, all the types in Table 6.1 were used except the AD8003. The order of the different operational amplifiers in the circuit was determined by their slew rate, with the operational amplifier with the highest slew rate (the OPA690) used in the last amplification stage where the voltage is at its largest. The specifications for the operational amplifiers are based on the use of either a single rail supply voltage of 5 V or a dual rail supply of ±5 V. The maximum output voltage of the OPA690 used in the final stage of amplification is limited to 1.2 V less than the supply voltage. With a positive supply voltage of 5 V it would therefore have maximum output of 3.8 V which is not large enough meet the 5 V requirement for V_{high}. It was therefore decided to use supply voltages of -3 V for the negative rail and 8 V for the positive rail. Using these supply voltages the maximum output voltage is now 6.8 V which meets the requirement for V_{high}.

Decoupling capacitors between the supply voltage and ground is added as close as possible to each operational amplifier. A 100 nF capacitor is used in parallel with a 10 uF capacitor at each supply pin. The decoupling capacitors provide a source of current close to the operational amplifiers and negates the effect of the inductances found in lines leading to the voltage supply. The adaption shaper design was manufactured on a 2 layer FR4 substrate.

6.7.2 Soft Limiter

In section 6.4.4 the need for a smooth transition to V_{high} was explained. The soft limiting effect is obtained by making use of the non-linear behaviour of a diode [19]. The same HSM282 diode was used as in the envelope detector design. Two limiting stages are used to ensure a smooth transition. The stages consist of a operational amplifier used in non-inverting configuration

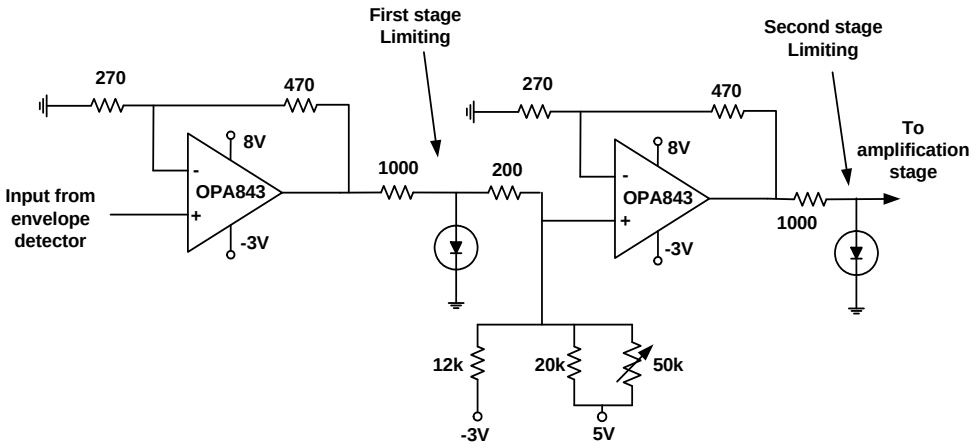


Figure 6.11: The limiting stage of the adaption shaper. This stage uses the non-linear properties of a diode to smooth the transition to V_{high}. The values of the components shown are for the first design iteration of the adaption shaper (see section 6.10.2)

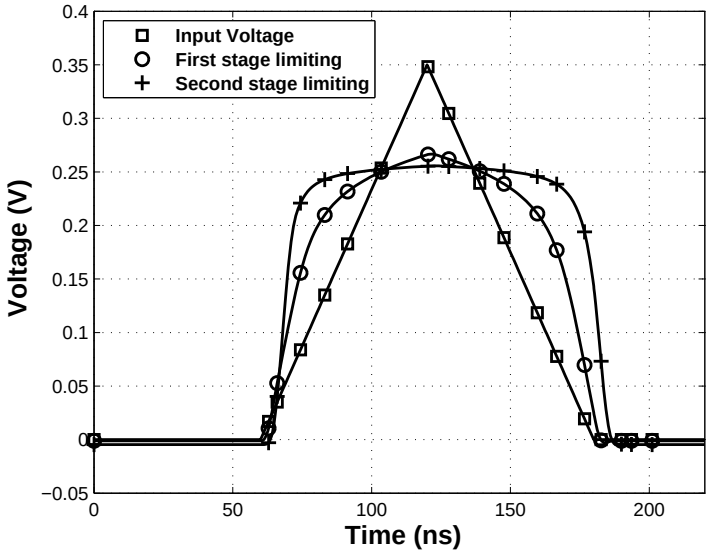


Figure 6.12: The simulated output from the soft limiter stage shown in figure 6.11. A triangle waveform with an amplitude of 350 mV is used as input to test the soft limiting action.

followed by a diode to ground. The diode to ground does not have an effect when the voltage is less than its threshold voltage. However, as the voltage reaches the diode threshold voltage it acts as a voltage limiter. The operational amplifier are used both as a buffer and to amplify the signal. The operational amplifier used in the design is the OPA843. Figure 6.11 shows a schematic of the limiter part of the adaption shaper. The design was simulated using a SPICE package, LTSpice [3]. A triangle waveform with peak voltage of 350 mV was used to test the limiter in LTspice, with the results shown in figure 6.12. As can be seen the required soft limiting action has been achieved, with the output voltage achieving a smooth transition to a limited value of 260 mV. Besides providing the soft limiting effect the limiter also makes controlling V_{high} easier because the input to the next section will always be limited to 260 mV. The gain of the operational amplifiers can be adjusted in the same way as those in the amplification stage to be discussed in section 6.7.3. Although the output voltage will always be limited by the diode

section, the amount of gain effects the gradient of the voltage transfer function.

The limiter part of the adaption shaper also includes the means to adjust the V_{low}. The second limiting stage is also used as a summing amplifier (see figure 6.11). A DC voltage level that is controllable via a potentiometer is summed at the positive terminal of the second operational amplifier in figure 6.11.

6.7.3 Amplification stage

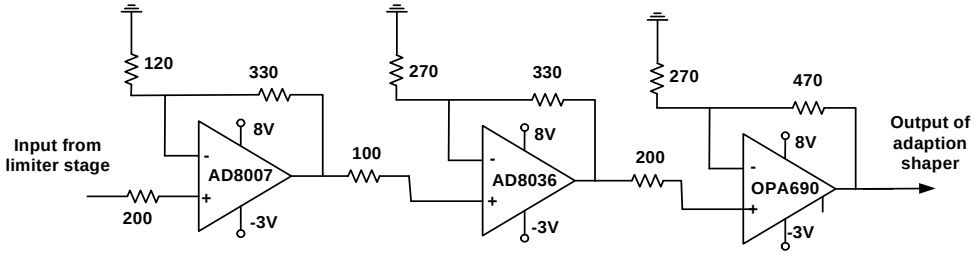


Figure 6.13: The amplification stage of the adaption shaper. The values for the components shown are those used for the first design iteration of the shaper (see section 6.10.2).

The final stage of the adaption shaper is the amplification stage. The input voltage from the envelope detector has been limited to 260 mV using the soft limiter developed in section 6.7.2. According to the specifications from section 6.4 the maximum V_{high} required is 5 V. To amplify the 260 mV to 5 V an amplification ratio of 19 is needed. Table 6.1 shows the specifications for the available operational amplifiers. It can be seen that none have such a high gain at the bandwidths we require, so multiple stages of amplification is needed. Figure 6.13 shows the design for the amplification stage. The operational amplifiers are used in non-inverting configuration where the gain is given by

$$G = 1 + \frac{R_f}{R_g} \tag{6.6}$$

where R_f is the feedback resistor from the output to the negative terminal and R_g is the resistance to ground from the negative terminal. As discussed in section 6.7.1 the sequence in which the different operational amplifiers is used is decided by their slew rates. The amount of gain can be controlled by changing the values of the feedback resistors in the amplification stage. The values shown in figure 6.13 are those used in the first design iteration (see section 6.10.2). For these values the predicted gain is 16.67, resulting in a V_{high} of 4.34 V.

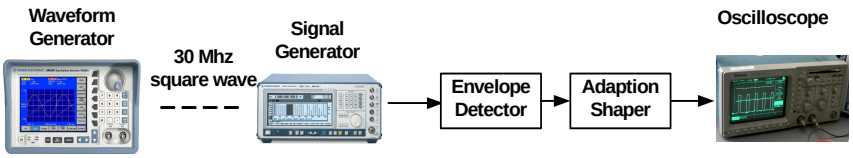


Figure 6.14: The measuring setup used to measure the voltage shaping output against input power. A waveform generator is used to provide a 30 MHz square wave which is used as reference by the signal generator to modulate a 1.5Ghz signal. The output of the circuit is measured on an oscilloscope

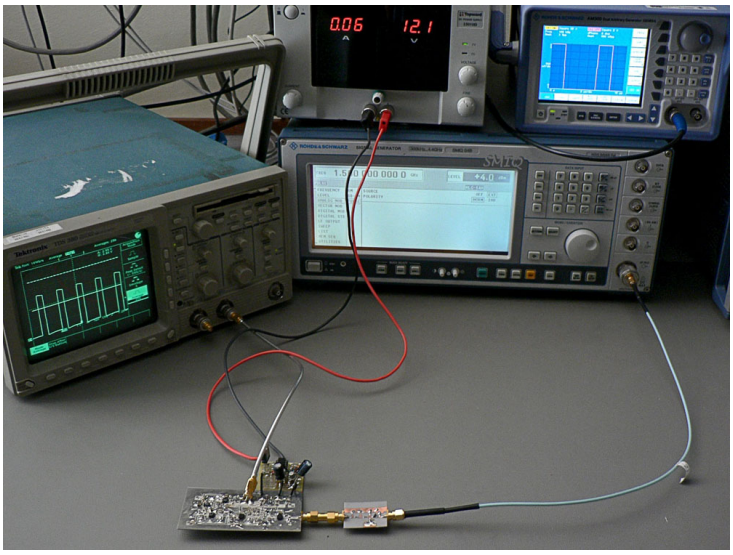


Figure 6.15: The measuring setup used to measure the voltage shaping output against input power. A waveform generator is used to provide a 30 MHz squire wave which is used as reference by the signal generator to modulate a 1.5Ghz signal. The output of the circuit is measured on an oscilloscope

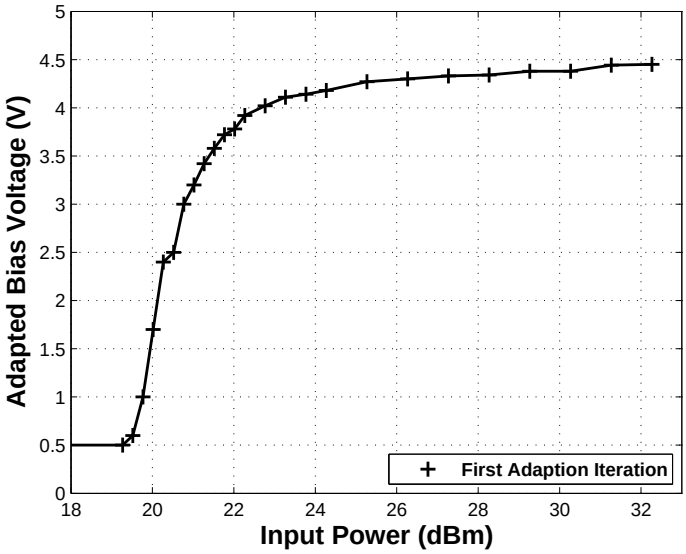


Figure 6.16: The measured response of the first iteration adaption transfer graph. The output voltage (connected to V_{GS} of the peaking amplifier) is plotted against the input power provided to the Doherty amplifier.

6.8 Measuring the Adaption Transfer Function

The adaption transfer function is the function describing the relation between the output voltage of the adaption system and the input power to the Doherty amplifier. A schematic of the setup used to measure this adaption transfer function can be seen in 6.14, and a photo of the setup is shown in figure 6.15. A waveform generator provides a 30 MHz square wave which is used as reference to modulate a microwave signal at 1.5 Ghz. The measurement is made by sweeping the input power from a level of -3 dBm to 11 dBm in steps of 1 dBm. The amplitude of the resulting square wave voltage delivered by the adaption network is measured on the oscilloscope.

The coupler is not included in this setup. However, its effect is easily calculated by adding the coupling factor to the input power set on the signal generator. In this way the output voltage can be plotted against the input power at the Doherty amplifier input. Figure 6.16 shows the result of such a measurement for design iteration 1. The transfer function shows the correct general shape as specified in section 6.4. The output voltage starts increasing at 18 dBm of input power and starts leveling out at 24 dBm, with a maximum voltage of around 4.4 V. Iteration 1 therefore reaches its maximum voltage too fast, since the specifications required the adaption system to reach the maximum voltage in the 25 to 30 dBm input power range. However, the adaption system was designed to be tuneable so that the shape of the transfer function can be changed. By adding attenuators the function can also be shifted to higher input power levels. In sections 6.10.2 to 6.10.5 the adaption transfer function is tuned experimentally to provide the ideal transfer function. The measurement described in this section could also have been accomplished without the square wave modulation. However, by using the modulation we are able to observe V_{high} and V_{low} at the same time.

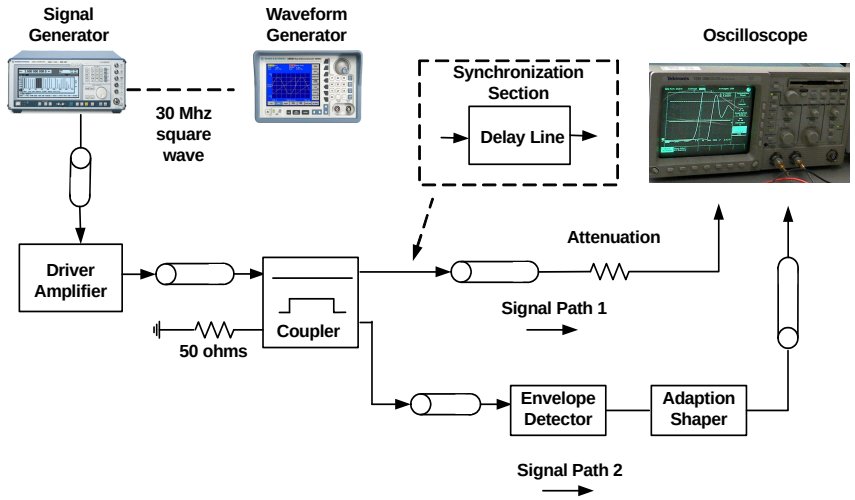


Figure 6.17: The measurement setup used to measure the difference in the time taken for the signal to reach the Doherty amplifier through the RF path and the biasing voltage to reach the peaking amplifier. The figure also shows where the delay line is added to synchronise the two paths. The two inputs on an oscilloscope is used to compare the measurements directly.

6.9 Synchronisation

The adaption system attempts to change the gate bias voltage of the peaking amplifier as a function of the input power levels of the Doherty amplifier. Ideally changes to the bias voltage would occur at exactly the same moment as the corresponding changes in the input voltage. However, a problem arises because of the different signal paths (see figure 6.3). The signal travelling through the adaption system needs to pass through the coupler, envelope detector and the adaption shaper circuit, while the RF signal only needs to travel through the coupler and can then be connected to the Doherty amplifier. The result is that there is a time delay before the bias voltage can react to the change in the input voltage. This unsynchronised behaviour can lead to the generation of unwanted inter-modulation products and non-linear

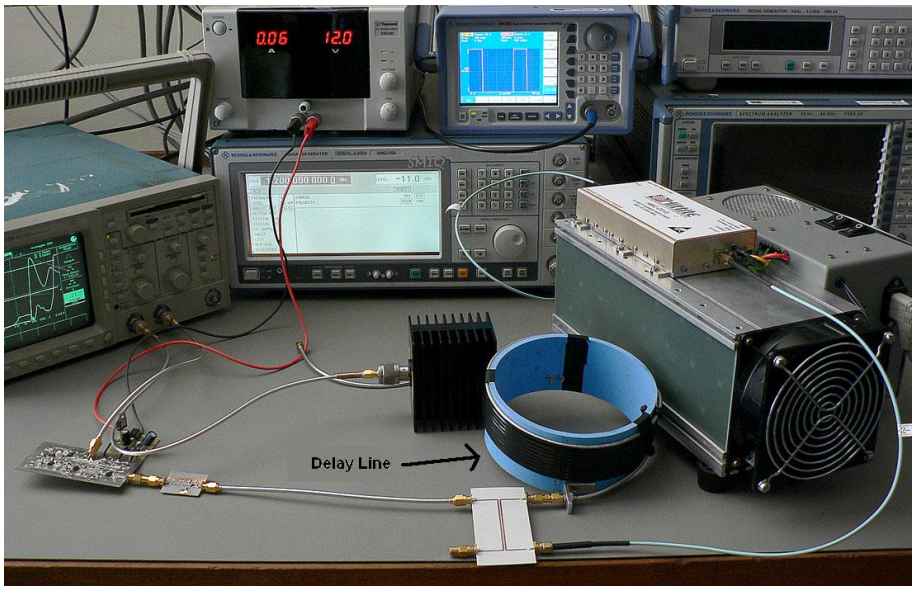
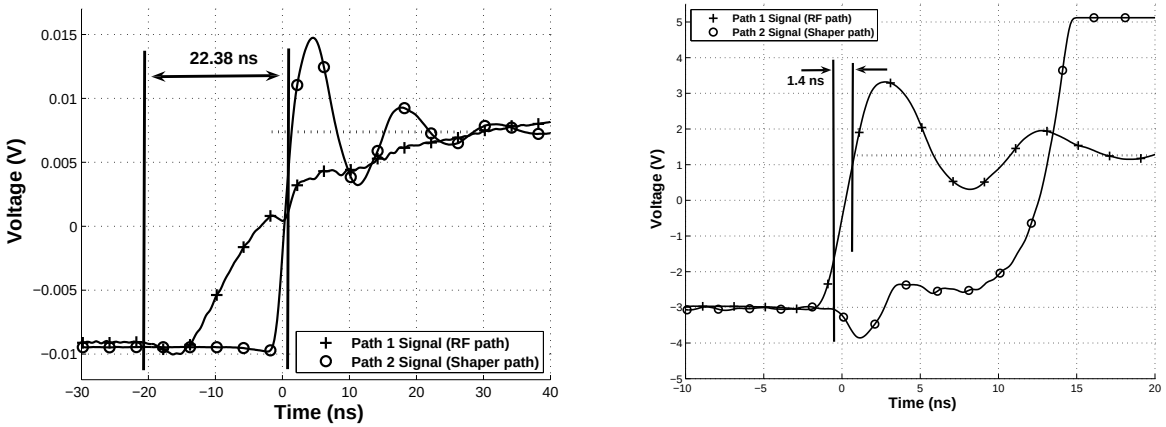


Figure 6.18: The measuring setup used to measure delay time between the 2 signal paths. In the photo the delay line has been added for the synchronised measurement.

behaviour from the entire system. To synchronise the adaption system output to the input signal a delay line is added between the coupler and the Doherty amplifier input. The delay line is implemented with a low loss coaxial cable. Yang [21] reports the use of a 24 ns delay, but does not show how this figure was attained. A measurement system is proposed in the next sections to determine the required length of the delay line.



(a) a) Delay measurements

(b) b) Improved synchronisation measurement

Figure 6.19: These figures show the time delay measurements comparing the 2 signal paths. Figure a shows the measurements of the unsynchronised system. The signal clearly takes a longer time to travel through the adaption shaper path (path 2). Figure b shows the results after the delay line has been added to path 1. The time delay for the 2 signal paths is now equal.

6.9.1 Measuring the Delay Times

The delay times of the two signal paths were measured in real time using an oscilloscope. A schematic of the measurement setup can be seen in figure 6.17, while a photo of the measurement is provided in figure 6.18. In figure 6.18 the delay line added in the next section is already included. A waveform generator is used to give a square wave as reference for the signal generator to generate a pulse modulated 1.5 Ghz signal. This signal is then amplified by a driver amplifier to achieve the expected input power required for saturation of the Doherty amplifier (see section 6.4). The signal now travels through two paths (see figure 6.17). Path 1 measures the signal that will go to the input of the Doherty amplifier, while path 2 shows the output of the adaption shaping network. The amount of delay time for the two signal paths can now be compared. Figure 6.19 a) shows the measured outputs from the two paths (without the delay line added). The oscilloscope used has a bandwidth of 400 MHz, which is much smaller than the 1.5 Ghz microwave signal in signal path 1. It acts as a low pass filter and only follows the envelope of the pulsed microwave signal. This does not matter however, as only the envelope response is of interest. It can be seen that the first change in the path 1 signal occurs at about 21 ns. The time unit is negative simply because it refers to the trigger time on the oscilloscope. The time for path 2 is not taken where the adaption shaper shows the first response to the square wave, but rather where it reaches its required voltage (1.38 ns). The signal therefore takes 22.38 ns longer to travel through the adaption network (path 2) than through the RF path (path 1). A further observation is the overshoot and settling time needed by the adaption shaper to attain a smooth output. However this effect is mostly due to the use of a square wave as modulation source for the signal as the voltage shaper is unable to cope with the extremely fast rise time of the square wave. The square wave is used as it provides a clear point of comparison for the two paths.

6.9.2 Adding the Delay Line

In order to compensate for the different path lengths a delay line is added in the RF path. The required delay as measured in the previous section is 22.38 ns. A coaxial cable with low losses, the UT141-FORM from Micro Coax. The length needed can be calculated as

$$length = \frac{c}{\sqrt{e_r} time} = 4.7m$$

with c the speed of light and e_r given as 2.041 by the manufacturers. The delay line will also have losses which will influence the RF signal path. According to the manufacturers the losses at 1 Ghz amounts to 0.41 dB/m. The total loss for the delay line at 1 Ghz is therefore 1.927 dB. Exact losses where not specified for our operating frequency of 1.5 Ghz, but the losses expected will be higher than at 1 Ghz. The loss for the delay line measured at 1.5 Ghz as 2.72 dB. The delays for the two signal paths were again compared, this time with the delay line added. Figure 6.19 b) shows the results. The graph shows that there is now a only a small delay of 1.4 ns from the time the RF signal path (path 1) shows its first movement to the time the adaption system (path 2) attains its required voltage.

6.10 Optimising the Adaption Circuit

An adaption system has been designed comprising of a coupler, envelope detector, delay line and and an adaption shaper. The adaption shaper provides the means to adjust the voltage transfer function. The V_{high} voltage can be tuned by changing the gain in the amplification stage (section 6.7.3) while the V_{low} can be adjusted using the potentiometer in the limiter stage of the design. The shape of the transfer function can be controlled by changing the gain in the limiter stage. Finally the entire transfer function can be shifted to higher power levels by adding attenuators before the envelope detection stage. In the next sections these tools are used to optimise the output of the bias adaptive Doherty amplifier. The optimisation goal is to increase the region with acceptable gain flatness. This will improve the output power and should have a positive effect on the efficiency of the amplifier at PEP.

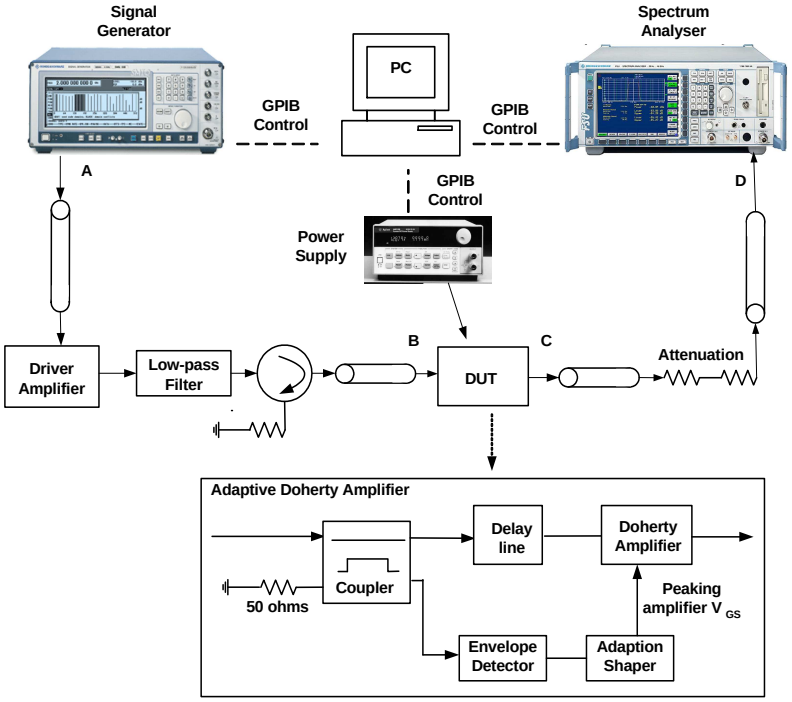


Figure 6.20: The measurement setup for measuring the adaptive Doherty amplifier performance. 6.10.2).

6.10.1 Measuring the Adaptive Doherty Amplifier Performance

The adaptive Doherty amplifier performance is measured against input power to calculate performance aspects such as the 1 dB compression point and amplifier efficiency. To measure this information a signal generator was used in conjunction with a spectrum analyser. Figure 6.20 presents a schematic for the setup, while a photo of the measurement setup can be seen in figure 6.21. Both the signal generator and the spectrum analyser were controlled via a GPIB interface from a computer. Measurements were made by doing a power sweep with a single tone at the 1.5 Ghz. At each point in the power sweep the output power is recorded by the spectrum analyser. A programmable DC power source is also controlled via a GPIB interface and records

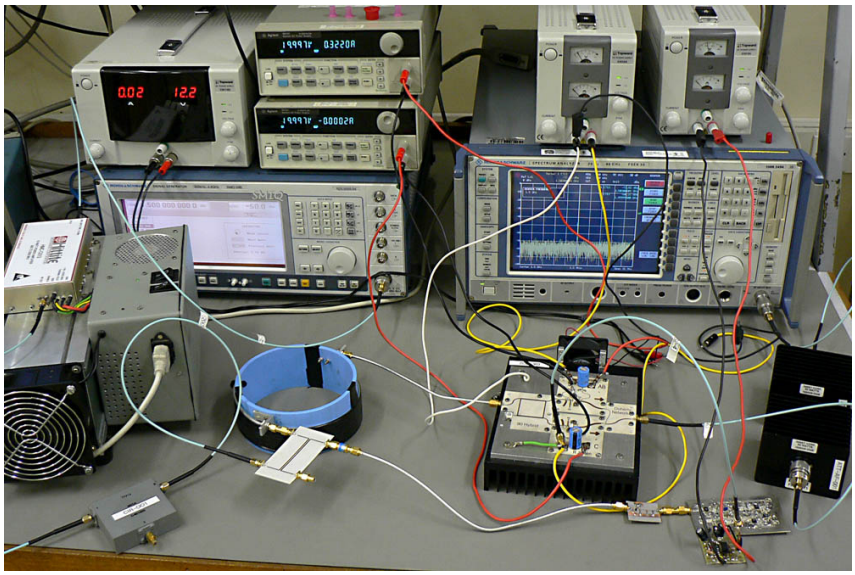


Figure 6.21: A photo of the measurement setup used for measuring the adaptive Doherty amplifier performance. 6.10.2).

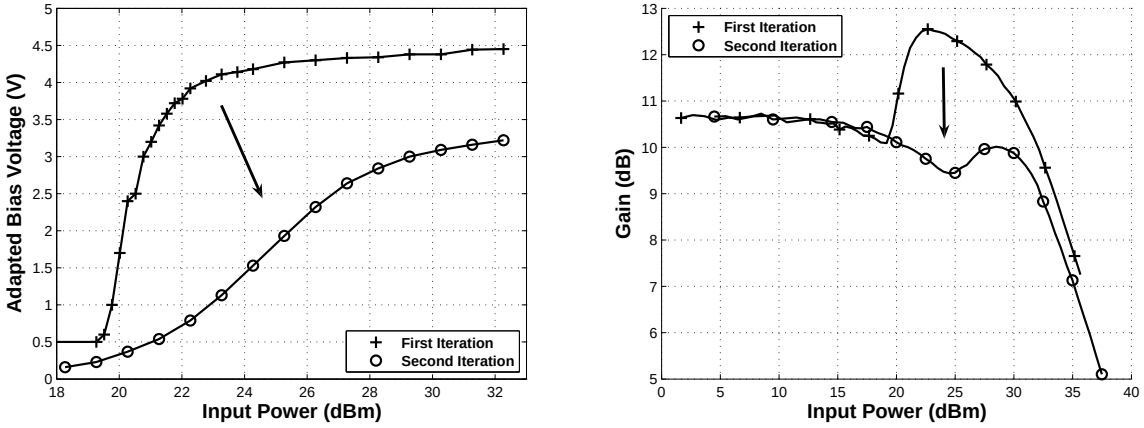
the drain currents of the carrier and peaking amplifiers for each measurement. The software for this measurement was written in MATLAB.

The signal generator can not provide enough power to drive the adaptive Doherty amplifier into saturation. A driver amplifier is therefore added to provide more input power. A low pass filter is added after the driver amplifier to filter out any unwanted harmonic distortion products. In order to protect the driver amplifier a circulator is added between the DUT (device under test) and the driver amplifier. Attenuators are added at the output of the DUT to keep the measured power levels below the recommended maximum input of the spectrum analyser.

A calibration procedure is required in order to make accurate measurements of the power levels. The accuracy level of the spectrum analyser and signal generator was first confirmed by comparing the reported power levels with a measurement from a power meter. Four calibration points are defined in figure 6.20. The effect of the lines and attenuators between points C and D, E_{CD}, can be measured by connecting point C directly to point A and subtracting the input power level on the signal generator from the spectrum analyser reading. The second step of the calibration is connecting points B and C together and repeating the measurement to measures the sum of networks E_{AB} (the effect of the components between points A and B) and E_{CD}. Since E_{CD} is already known form the first step in the calibration process, E_{AB} can easily be calculated. This concludes the calibration procedure. By adding E_{AB} to the reported input power level form the signal generator the input power at the DUT is known, while the E_{CD} can be added to the reading from the spectrum analyser to provide the true output power.

6.10.2 First and Second Iterations

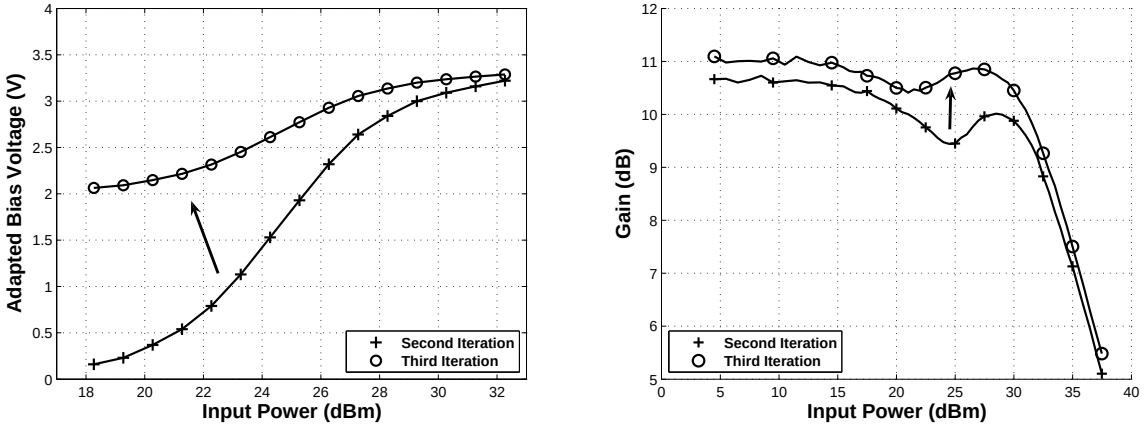
Figure 6.22 presents the measurement results of the first and second iteration attempts. In figure 6.22a the measured voltage transfer function is shown and in figure 6.22 b the gain of the adapted Doherty amplifier is presented. The first iteration uses the component values seen in figures 6.11 and 6.13. As can be seen from the graphs the very steep gradient in voltage transfer



(a) Adaption transfer function (b) Adaptive Doherty amplifier gain

Figure 6.22: Measurement results for iterations 1 and 2. Iteration 2 lowers the gain in the limiter stage compared to iteration 1. Figure a) shows the adaption transfer function and figure b the gain of the adaptive Doherty amplifier.

function resulted in a sharp increase in the gain of the complete amplifier. This is because the peaking amplifier is switched on too fast. For the second iteration an attempt was made to reduce the gradient of the voltage transfer function. This was accomplished by lowering the gain of the operational amplifier stages. The feedback resistor (value 470 Ω, see figure 6.11) was replaced with a 47 Ω in both non-inverting amplifiers. The cumulative gain in the limiter changes from 7.51 to 1.38 (this can be calculated using equation 6.6). From 6.22 it can be seen that the attempt to remove the sharp increase in gain from iteration 1 has been successful.



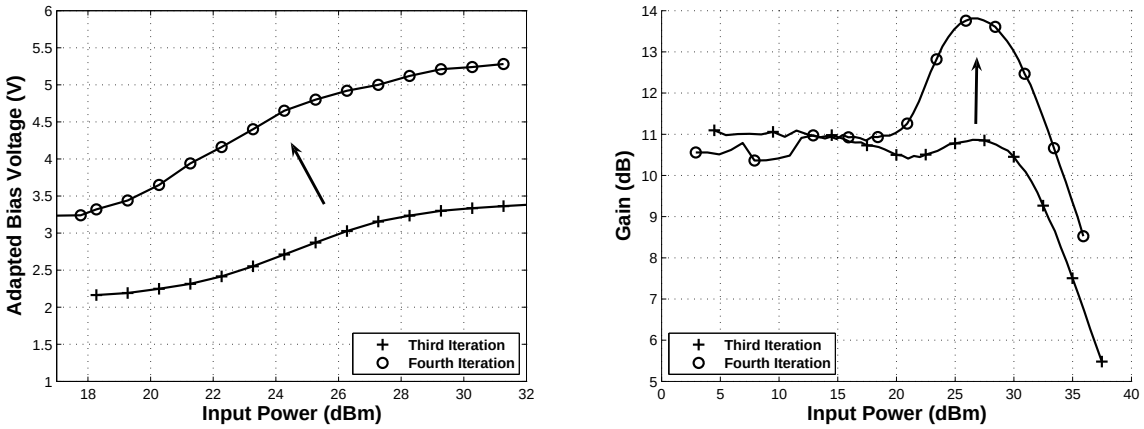
(a) Adaption transfer function (b) Adaptive Doherty amplifier gain

Figure 6.23: Measurement results for iterations 2 and 3. Iteration 3 increases V_{low} compared to iteration 2. Figure a shows the adaption transfer function and figure b the gain of the adaptive Doherty amplifier.

6.10.3 Third Iteration

The third iteration attempted to remove the dip in the gain that can be seen in iteration 2 around 25 dBm input level. Figure 6.23 shows the adaption transfer function and gain for iterations

3 and 4. The goal was to make the peaking amplifier switch on earlier to prevent the dip in gain. By raising the V_{low} voltage the amount of input power needed for the peaking amplifier to start producing current is reduced. For iteration 3 V_{low} was raised to 2 V by adjusting the potentiometer in the limiter section of the adaption shaper (see section 6.7.2). The results are favourable and can be seen in figure 6.23. The dip in the gain of the adapted Doherty amplifier is reduced from 1.1dB to 0.5 dB.



(a) Adaption transfer function

(b) Adaptive Doherty amplifier gain

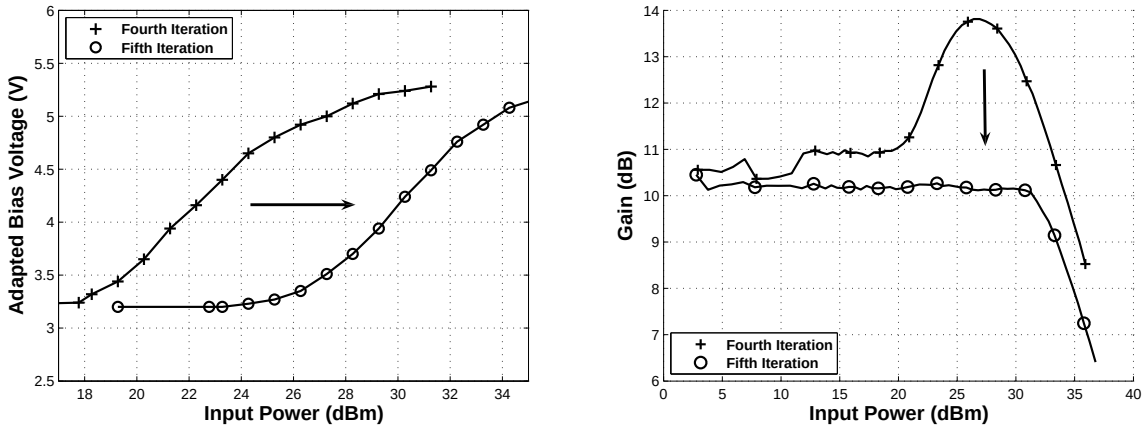
Figure 6.24: Measurement results for iterations 3 and 4. Iteration 4 increases V_{high} compared to iteration 3. Figure a shows the adaption transfer function and figure b the gain of the adaptive Doherty amplifier.

6.10.4 Fourth Iteration

The theoretical ideal for the adaption system is to have the peaking and carrier amplifier voltages equal at PEP in order to provide equal output currents. The carrier amplifier bias voltages used ranges from 4.67 V to 5.02 V (table 5.1). However, in iteration 3, V_{high} was only equal to 3.2 V. The first iteration did in fact have a higher V_{high} of 4.5 V, but this was lowered when the gain in the limiter section was lowered to reduce the gradient of the transfer function (section 6.10.2). In order to increase V_{high} again the gain of the amplification stage is increased (section 6.7.3). This is achieved by changing the feedback resistor for the final stage of amplification (the OPA690 in figure 6.13) from 270 Ω to 470 Ω. V_{low} is also increased to 3.2 V in a further attempt to remove the dip that is still visible in the gain of iteration 3. Figure 6.24 shows the resulting measurements. A higher gain is indeed visible compared to iteration 3 at input levels, and the dip has completely disappeared. Unfortunately a large unwanted rise in the gain has appeared.

6.10.5 Fifth Iteration

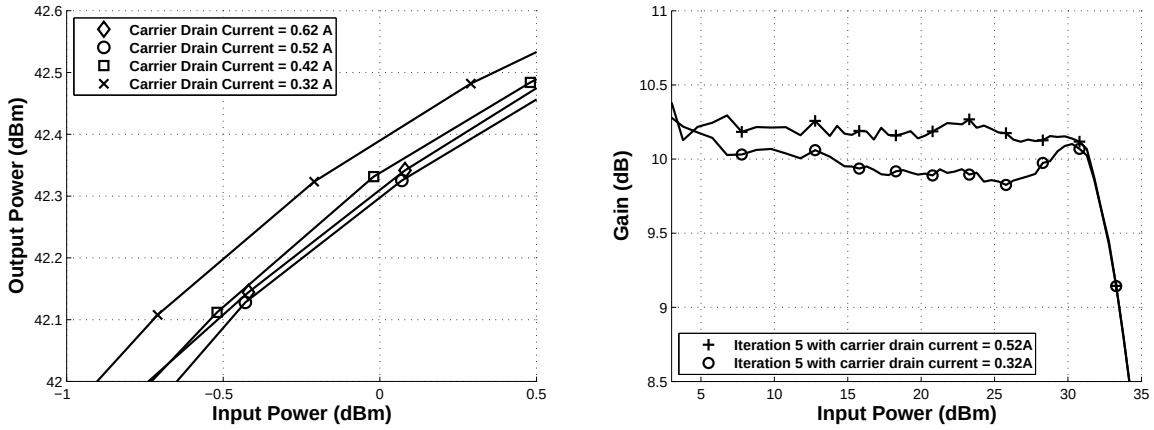
The peaking amplifier seemed to reach its peak current output to early in iteration 4, resulting in an unwanted rise in gain. To alleviate this problem, attenuators were added before the input of the envelope detector for iteration 5. In this way the entire transfer function is simply shifted to a higher power level. Figure 6.25 shows the resulting measurements if 8 dB of attenuation



(a) Adaption transfer function (b) Adaptive Doherty amplifier gain

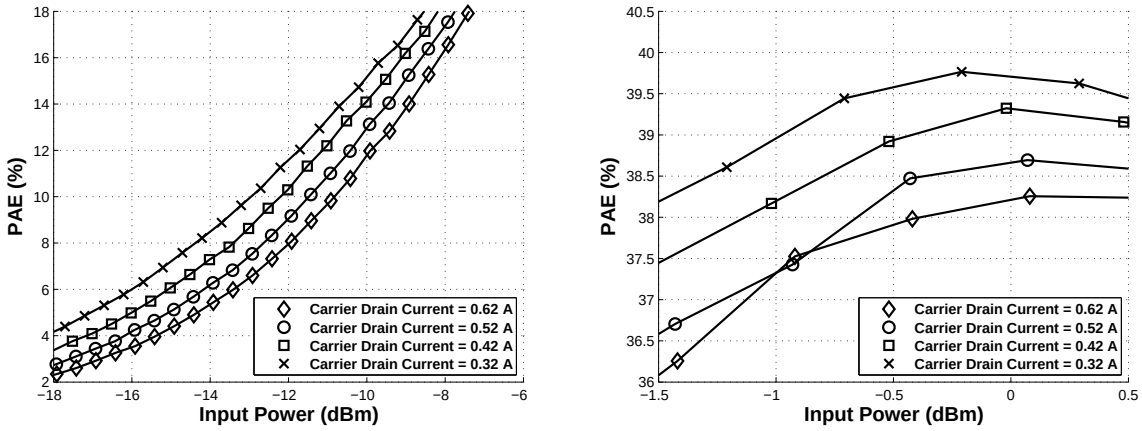
Figure 6.25: Measurement results for iterations 4 and 5. Iteration 5 shifted the entire transfer function to a higher input power level by adding 8 dB of attenuation before the envelope detector. Figure a shows the adaption transfer function and figure b the gain of the adaptive Doherty amplifier.

is used before the envelope detector. From 6.25 a) it can be seen that the addition of the attenuators has successfully shifted the function to the higher power levels. As a result the rise in gain has indeed disappeared as wanted (see 6.25 b)). Iteration 5 now provides a much higher output power because the peaking amplifier is fully switched on. In the next section the output power and efficiency will be examined in more detail.



(a) Adaption transfer function (b) Adaptive Doherty amplifier gain

Figure 6.26: The output power against backed of input power for bias iteration 5 with various carrier amplifier drain currents. Figure a) shows that the adaptive Doherty amplifier has the highest output power when the lowest drain current for the carrier amplifier is chosen. Figure b) shows that the adaptive Doherty amplifier with a carrier drain current of 0.32 A still has acceptable gain flatness, although it is slightly less flat than with a drain current of 0.52 A.



(a) Power added efficiency at low input power levels

(b) Power added efficiency at PEP

Figure 6.27: The power added efficiency against backed of input power for iteration 5 of the adaptive Doherty amplifier with four different drain bias currents used for the carrier amplifier. Biasing the carrier amplifier with a drain current of 0.32 A results in the best efficiency at low power levels and at PEP.

6.11 Efficiency and Output Power of the Adaptive Doherty Amplifier

In the previous sections the bias adaption system was experimentally optimised to obtain an acceptable gain flatness at increased power levels. In chapter 5 the efficiency and output power for the even power division and unequal power division Doherty amplifiers were compared with different bias points for the carrier and peaking amplifiers. Four carrier V_{gs} points were used in the comparison, providing drain bias currents from 0.32 A to 0.62 A in 0.1 steps. The performance of the adaptive Doherty amplifier was also investigated using these four different carrier amplifier biasing points. The output power against backed off input power graph in figure a) shows that the carrier amplifier drain current 0.32 A has an output power of 42.38 dBm, the highest of the four. Figure b) shows that although the gain flatness with a carrier amplifier drain current of 0.32 A is reduced compared to that with a drain current of 0.52 A, it is still within acceptable levels. The efficiency against backed of input power graphs in figure shows that the carrier amplifier drain current of 0.32 A also provides the best efficiency at PEP (39.8%) and at lower input power levels.

6.12 Conclusion

In this chapter an adaptive bias control system has been designed and implemented. The system controls the peaking amplifier gate voltage dynamically depending on the input power levels of the Doherty amplifier. Individual components include a coupler (section 6.5), an envelope detector (section 6.6), a tuneable bias adaption shaper (section 6.7) and a delay line. The required length of delay line needed to synchronise the bias adaption system output voltage with the input power at the amplifier was determined in section 6.9. In section 6.10 the adaption shaper was used to optimise the performance of the adaptive Doherty amplifier. Finally in section 6.11 the efficiency and output power performance for the adaptive Doherty amplifier is

discussed, and the carrier amplifier drain current is chosen to optimise this performance.

Chapter 7

Evaluation of the Doherty Amplifiers

7.1 Introduction

In the previous chapters three Doherty amplifiers were designed, manufactured and measured. They include an even power division Doherty amplifier, an uneven power division Doherty amplifier and a bias adapted Doherty amplifier. In this chapter the results from the amplifiers will be compared and discussed in further detail. In section 7.2 the different amplifiers will be discussed. Different performance aspects for the amplifiers are compared in section 7.3, while in section 7.4 the results obtained is compared to literature.

7.2 The Three Different Doherty Amplifiers

The Doherty amplifier system was designed using a modular approach described in section 4.3. A carrier module and a peaking amplifier module was designed using the MRF282 transistor (see chapter 3). The modular approach allowed construction and testing of three different Doherty amplifiers.

7.2.1 Even Power Division Doherty Amplifier

The even power division Doherty amplifier is the classical Doherty amplifier described in literature [11]. The carrier amplifier is implemented with a class AB amplifier while the peaking amplifier is implemented with a class C amplifier. Although this configuration allows the peaking amplifier to only start producing current at power levels close to PEP (Peak Envelope Power), a problem arises because the class C amplifier is not able to provide the same current as the class AB amplifier at PEP. This effect was explained in section 2.5. Full load modulation is therefore not possible. For this reason it is expected that the even Doherty amplifier would not deliver the full potential available from the Doherty configuration.

7.2.2 Uneven Power Division Doherty Amplifier

The uneven power division Doherty amplifier is very similar to the even Doherty amplifier described in the previous section. The difference is that an uneven power divider is used so

that the peaking amplifier receives a larger ratio of input power than the carrier amplifier. The goal of this setup is to increase the rate at which the peaking amplifier current grows with input power compared to that of the carrier amplifier. In this way the two amplifiers can provide equal current at PEP, even though the peaking amplifier only started producing current at a much higher input power level than the carrier amplifier. The uneven power divider was designed in section 3.11.2.

7.2.3 Adaptive Doherty Amplifier

The adaptive Doherty amplifier attempts to solve the same problem as the uneven Doherty amplifier but uses a different approach. The adaptive bias control system was designed in chapter 6. The gate voltage of the peaking amplifier is adjusted dynamically depending on the input power level, and is increased as the input power nears PEP. In this way the current levels delivered by the peaking amplifier can be controlled to equal that of the carrier amplifier at PEP. At low power levels the adaption shaper lowers the gate bias voltage of the peaking amplifier so that it produces no current. A drawback of the adaptive Doherty amplifier is a loss of gain. This is due to the losses incurred in the delay line needed at the input of the Doherty amplifier to synchronise the adaption voltage at the gate of the peaking amplifier and the input power at the Doherty amplifier. The loss of the delay line was measured as 2.72 dB (section 6.9).

Table 7.1: Gate voltages for the three Doherty amplifiers used in the comparison

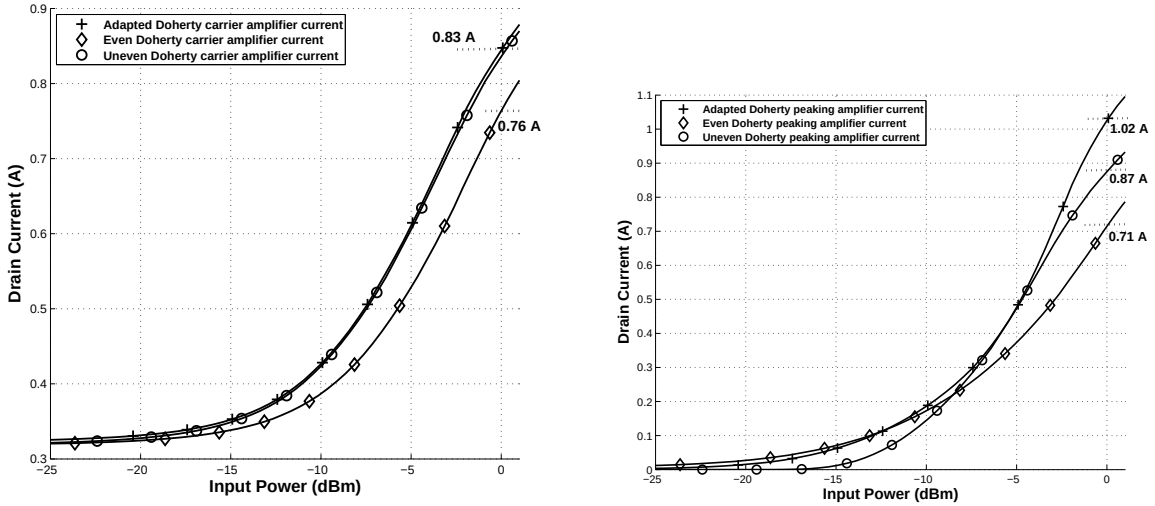
	Carrier Amplifier V_{GS}	Peaking Amplifier V_{GS}
Even Doherty amplifier	4.5 V	3.5 V
Uneven Doherty Amplifier	4.5 V	2.5 V
Adaptive Doherty	4.5 V	Adaptive biasing, Iteration 5

7.3 Comparing the Doherty Amplifiers

The Doherty amplifiers were experimentally optimised to obtain the best output power and efficiency while maintaining an acceptable gain flatness of 0.5 dB. The values for the optimised gate voltages can be found in table 7.1. In this section different aspects of amplifier performance will be compared.

7.3.1 Carrier and Peaking Amplifier Drain Currents

As explained in section 7.2 one of the main goals of the uneven and adaptive versions of the Doherty amplifiers was to increase the peaking amplifier current at PEP. Figure 7.1 a) shows the carrier amplifier currents against backed of input power and figure 7.1 b) the peaking amplifier currents. The uneven and adaptive Doherty carrier amplifier currents are higher than the even Doherty amplifier carrier amplifier current. This is due to the fact the PEP for these two amplifiers occurs at a higher power level (see next section) than the even Doherty amplifier because of the improved load-pulling effect provided by their increased peaking amplifier currents.



(a) Carrier amplifier drain current

(b) Peaking amplifier drain current

Figure 7.1: The drain currents of the carrier and peaking amplifiers against backed of input power for the even power division, uneven power division and adaptive Doherty amplifiers.

For the even Doherty amplifier the carrier amplifier drain current at PEP is 0.76 A and the peaking amplifier drain current 0.71 A. The peaking amplifier current is less than carrier amplifier current as predicted, although the two currents are closer together as might have been expected. It must be remembered, however, that these results are for the experimentally optimised even Doherty amplifier (see section 5.5). The peaking amplifier V_{GS} that resulted from this experimental optimisation was 3.5 V, a much larger voltage than the V_{GS} of 2 V that was originally used for the design of the peaking amplifier in chapter 3. The peaking amplifier V_{GS} voltage cannot simply be increased until the currents are equal at PEP, however, because the peaking amplifier gate voltage has to remain below the transistor threshold voltage to retain its class C characteristics.

The uneven Doherty amplifier peaking amplifier current at PEP is 0.87 A, while the carrier amplifier current is 0.83 A. The uneven power division has therefore succeeded in increasing the peaking amplifier current levels. For the experimental optimisation the measurements of amplifier performance was made using 0.5 V steps for the gate voltage. By using smaller steps it should be possible to find a V_{GS} peaking amplifier voltage which provides equal current to the carrier amplifier at PEP.

The adaptive Doherty amplifier also manage to increase the peaking amplifier current at PEP. In fact, with a carrier amplifier current of 0.83 A and a peaking amplifier current of 1.02 A, it seems as if it has increased too much. This peaking amplifier current at PEP could be reduced by lowering V_{high}, the maximum output voltage from the adaption shaper described in chapter 6. In the next section it can be seen that this high peaking amplifier current does not have a negative effect on the output power of the adaptive Doherty amplifier. However it could have an influence on the efficiency. This is discussed further in section 7.3.4.

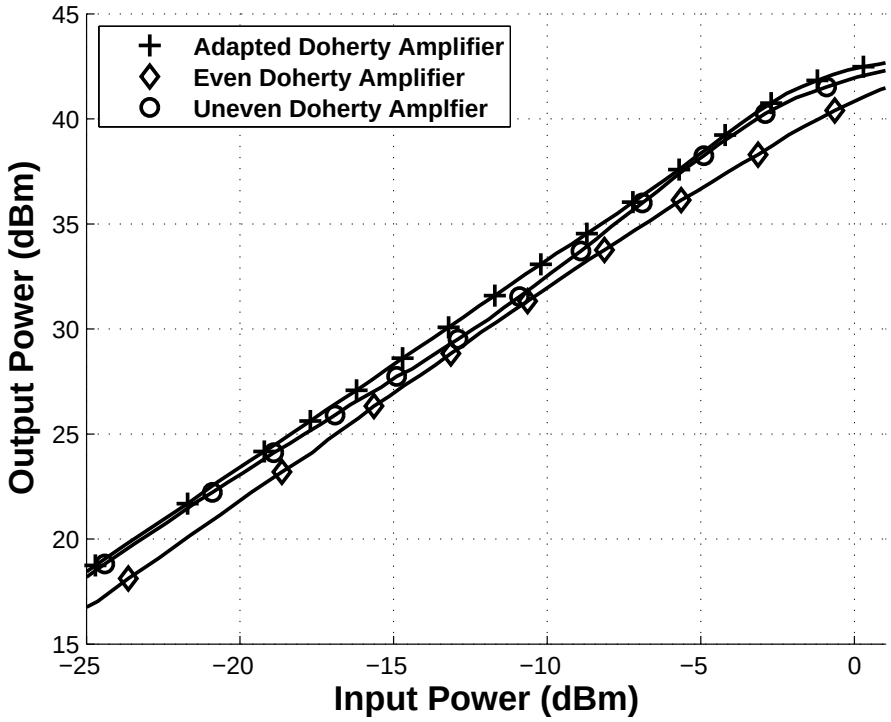


Figure 7.2: The output power against backed off input power for the even power division, uneven power division and adaptive Doherty amplifiers..

7.3.2 Output Power

The output power against backed of input power for the compared amplifiers is shown in figure 7.2, with the PEP value taken at the 1 dB compression point. The adaptive Doherty amplifier at 42.4 dBm (17.4 W) provides the highest output power at PEP. For the Doherty configuration two 10 W MRF282 transistors is used. Achieving 17.4 W is a therefore a very good result, especially considering that the drain bias voltage used was 20 V instead of the 26 V maximum specified for the MRF282.

The uneven Doherty amplifier also presents an improvement over the even Doherty amplifier, with a output power of 41.9 dBm at PEP compared to 40.8 dBm for the even Doherty amplifier. The higher power levels for the adaptive and uneven Doherty amplifiers can be attributed to the larger peaking amplifier current provided as discussed in the previous section.

7.3.3 Gain

The gain of the amplifiers is the one area where the even Doherty amplifier shows better performance than the adaptive or uneven Doherty amplifiers. Figure 7.3 shows the gain against backed of input power for the three amplifiers. The adaptive Doherty amplifier shows reduced gain compared to the even Doherty because of the addition of the delay line as discussed in section 7.2. The delay line loss of 2.72 dB has the same effect on the gain as adding an attenuator with the same loss value would have. The loss of gain in the uneven Doherty amplifier is due to the uneven power division. The peaking amplifier has a lower gain than the carrier amplifier (see section 4.8), so the total gain for the Doherty amplifier is lowered if more of the input power

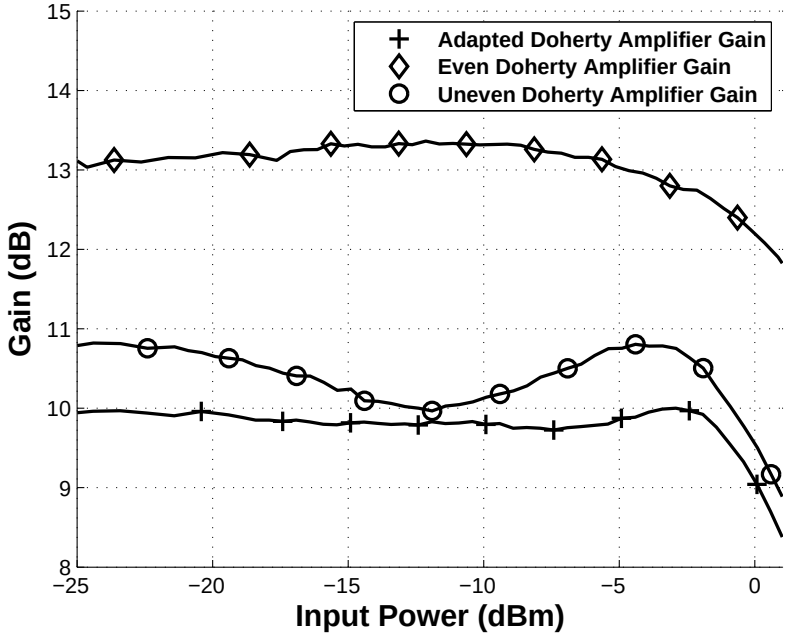


Figure 7.3: The gain against backed off input power for the even power division, uneven power division and adaptive Doherty amplifiers.

is distributed to the peaking amplifier.

7.3.4 Efficiency

Since improved efficiency over balanced amplifiers is one of the main reasons for using a Doherty amplifier, efficiency is a important aspect of the comparison. PAE (power-added efficiency) against backed off input power for the three different Doherty amplifiers is shown in figure 7.4. At PEP the uneven Doherty shows a PAE of 40.75 %, the highest of the three amplifier variations, providing an improvement of 1.05 % over the adaptive Doherty amplifier (39.7 % at PEP) and 2.15 % over the even Doherty amplifier (38.6 % at PEP).

At 3dB backed off from PEP the uneven and adaptive Doherty amplifiers offer even larger improvements over the even Doherty amplifier design, with 34.9% and 34.3 % PAE respectively compared to 29.75 % for the even Doherty amplifier. At 10 dB backed off from PEP the adaptive Doherty amplifier shows the best performance with 15.2% compared to 14.2 % and 13.4 % for the uneven and even Doherty amplifiers respectively.

A significant difference can also be seen at 15 dB backed of input power. The uneven and adaptive Doherty amplifiers provide similar efficiencies of 7.25 %, while the even Doherty amplifier has an efficiency of 5.75 %.

7.3.5 Complexity of Design

The even and uneven Doherty amplifiers share a very similar design. The only difference is the use of different power divider for the input network and different V_{GS} gate voltages for the peaking and carrier amplifiers. The adaptive Doherty amplifier is a lot more complex. The modules used for the amplifier itself is the same as for the even Doherty amplifier, but the

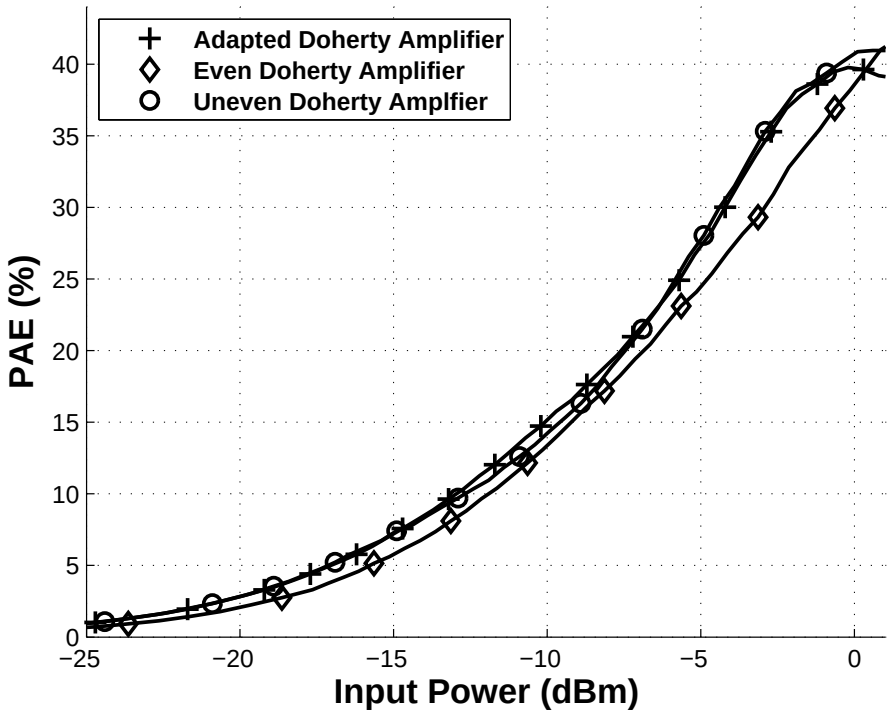


Figure 7.4: The power added efficiency against backed off input power for the even power division, uneven power division and adaptive Doherty amplifiers..

bias adaption system is added to control the peaking amplifier gate voltage. In chapter 6 this bias adaption system was designed, including a coupler, envelope detector, adaption shaper and delay line.

Table 7.2: Comparison of amplifiers designed in this thesis to literature. The efficiency and output power figures are quoted at PEP.

	PAE	Drain efficiency	Output power	Transistor	Frequency
Even Doherty	38.6 %	41 %	40.82 (dBm)	MRF282 (10W)	1.5 Ghz
Uneven Doherty	40.8 %	45.8 %	41.95 (dBm)	MRF282 (10W)	1.5 Ghz
Adaptive Doherty	39.8 %	45.6 %	42.38 (dBm)	MRF282 (10W)	1.5 Ghz
Brand [8] (Even)	27 %	31 %	37.4 (dBm)	MRF282 (10W)	1.643 Ghz
Cha [15] (Even)	NA	40 %	46 (dBm)	MRF21180 (38W)	2.14 Ghz
Kim [14] (Uneven)	NA	40 %	33 (dBm)	MRF281 (4W)	2.14 Ghz
Yang [21] (Adaptive)	39.4 %	NA	32.7 (dBm)	MRF281 (4W)	2.14 Ghz

7.4 Comparison to Literature

The even, uneven and adaptive Doherty amplifier results are summarised in table 7.2 along with comparative results from literature using LDMOS technology. Brand [8] demonstrates a Doherty amplifier with 27 % power added efficiency at PEP and an output power of 37.4 dBm. The even Doherty amplifier presented in this thesis shows an efficiency improvement of 11.6 % and output power improvement of 3.4 dBm over these results. Cha [15] also presents an

even Doherty amplifier with a drain efficiency of 40 %, which is comparable with the 41% drain efficiency achieved in this thesis.

The uneven Doherty amplifier presented in this thesis has a drain efficiency of 45.81 %. This can be compared to an uneven Doherty amplifier presented by Kim [14] which has an drain efficiency of 40 %.

Yang [21] demonstrated and an adaptive Doherty amplifier with a PAE of 39.4 %, which shows close agreement with the 39.8 % achieved for the adaptive Doherty amplifier in this thesis.

7.5 Conclusion

In this chapter the performance of the even, uneven and adaptive Doherty amplifiers has been compared to each other and to relevant results from literature. The uneven and adaptive Doherty amplifiers have both shown a significant improvement over the even Doherty amplifier in efficiency and output power. The reason for the improvements can be attributed to the increased peaking amplifier current at PEP. These improvements come at a loss of gain compared to the even Doherty amplifier. The uneven amplifier demonstrated the highest efficiency figures at PEP, while the adaptive Doherty amplifier showed the largest output power at PEP. The improvements achieved by the uneven Doherty amplifier over the even Doherty amplifier are especially noteworthy considering that the complexity of the system remains the same. The adaptive Doherty amplifier adds considerable complexity to the design, but provides the possibility to be optimised further through the control of the transfer function.

Chapter 8

Conclusion

The objective of this thesis is the evaluation of an adaptive Doherty and comparison with two other Doherty schemes, an even Doherty amplifier and an uneven Doherty amplifier. To this end the three Doherty amplifiers to be evaluated were designed, manufactured and measured.

In chapter 3 the design of the carrier and peaking amplifier using a load-line design approach is described. This design includes a stabilisation network, biasing networks and input and output matching networks. A new investigation is presented into the effect of the intermediate impedance R_0 on the offset lines used to optimise Doherty performance, showing that the length of these offset lines can be minimised through the correct choice of R_0. The design of an uneven power divider is presented for use in the uneven Doherty amplifier, with the power division ratio calculated to allow the peaking amplifier to produce equal current to the carrier amplifier at PEP (peak envelope power).

In chapter 4 the more practical issues surrounding the amplifier designs where discussed. A novel method is presented to increase the match between simulated and measured results for the capacitors used in the design. This is accomplished by using an external model extracted from measurements in conjunction with provided manufacturer modules. The peaking and carrier amplifiers where found to oscillate under certain circumstances. A test is proposed to detect such unstable oscillations and the addition of a snubber network to remove the oscillations is described. The chapter also includes the description of the measurement setups used to measure the scattering parameters, transmission phase, output power and drain currents of the amplifiers against input power. The measured carrier and peaking amplifier performance show a frequency shift to 1.5 Ghz from the design value of 1.6 Ghz . It was decided to continue the evaluation of the different Doherty amplifiers at 1.5 Ghz. The shift in frequency is partly explained through an investigation showing that the substrate permittivity is different to the specified value.

The Doherty amplifier design of chapter 3 assumed full load modulation at PEP. However, it was shown that the peaking amplifier does not provide enough current for full load modulation. The variations in phase, especially as the peaking amplifier becomes active, was also not considered in the design. The practical optimum gate voltages does therefore not necessarily agree with the designed values. For this reason the gate voltages of the carrier and peaking amplifier are experimentally optimised for the best performance in chapter 5. The optimum gate voltages for both the even and uneven Doherty amplifiers were determined.

In chapter 6 the design of a bias adaption system is presented. The goal of this system is

to dynamically control the bias voltage of the peaking amplifier depending on the input power level. The system includes a single section coupled line coupler, a envelope detector, an adaption shaper circuit and a delay line. The adaption shaper is designed so that the transfer function of the adaption system can be tuned according to requirements. A measurement setup is developed to measure the required length for the delay line to synchronise the output from the adaption system and the input power to the peaking amplifier. The adaption system was shown to operate successfully. The transfer function was optimised using the tuneable functions of the adaption shaper so that optimum performance is obtained from the adaptive Doherty amplifier.

The results from the adaptive Doherty amplifier, even Doherty and uneven Doherty amplifier was evaluated and compared in chapter 7. The adaptive Doherty amplifier and the uneven Doherty amplifier both provide a significant improvement over the even Doherty amplifier with regards to efficiency and output power. The adaptive Doherty amplifier provides the highest output power of the amplifiers, while the uneven Doherty amplifier has the best efficiency. The uneven Doherty amplifier shows similar results to the adaptive Doherty amplifier, but achieves this with a much less complex design. However, the tuneable transfer function of the adaptive Doherty amplifier offers the possibility to optimise performance for different goals. All three designs show impressive performance when compared to similar results from literature.

Linearity is an important consideration in designing amplifiers for communication systems. The performance of the amplifiers in this aspect is therefore something that should be investigated in future work. A further consideration is the transmission phase of the carrier and peaking amplifiers. The transmission phase of the amplifiers varies with input power, especially that of the peaking amplifier when it starts to become active. Optimisation in this area could lead to further gains in amplifier performance.

Bibliography

[1] Agilent technologies, wireless semiconductor division. *Large Signal Detectors for Cellular Handsets and Base Stations, Design Tip 8.* (Cited on page 74.)

[2] Dielectric laboratories inc. *2777 Rout 20, East Czenovia, New York, 13035-9433.* (Cited on pages 38 and 40.)

[3] Ltspice / swichtercad iii. *Linear Technology Corporation.* (Cited on page 77.)

[4] Rogers corporation. *One Technology Drive, PO Box 188, Rogers, CT 06263-0188.* (Cited on pages 14, 39, and 72.)

[5] Agilent. Design tip 4, detector selection. Technical report, Wireless Semiconductor Division. (Cited on page 74.)

[6] Inder Bahl. *Lumped Elements for RF and Microwave Circuits.* Artech House, Inc., 2003. (Cited on pages xiv, 37, 38, and 39.)

[7] Thomas M Weller Balaji Lakshminarayanan, Horace C Gordon Jr. A substrate-dependent cad model for ceramic multilayer capacitors. *IEEE Transactions on Microwave Theory and Techniques*, Vol. 48:no. 10, 2000. (Cited on pages xiv, 37, 38, and 39.)

[8] Konrad Frederik Brand. Design and characterization of a 10w doherty amplifier. Master's thesis, University of Stellenbosch, 2006. (Cited on pages xii, 14, 15, 17, 18, and 95.)

[9] Aehyok Yi Joongjin Nam Youn Yun Woo Bumman Kim, Youngoo Yang and Jeong Hyeon Cha. Efficiency enhancement of linear power amplifiers using load modulation technique. *Int. Symp. Microwave Optical Technology*, pages pp. 505–508, June 2001. (Cited on pages 2 and 26.)

[10] Steve C. Cripps. *RF Power Amplifiers for Wireless Communications.* Artech House, 1999. (Cited on pages xi, xvii, 1, 3, 4, 5, 6, 7, 9, 11, 12, 16, 68, and 69.)

[11] W.H. Doherty. A new efficiency power amplifier for modulated waves. *Proceedings of the Institute of Radio Engineers*, Volume 24:Number 9, September 1936. (Cited on pages 1, 3, and 90.)

[12] Cletus A. Hoer Glenn F. Engen. "thu-reflect-line": An improved technique for calibrating the dual six-port automatic network analyzer. *IEEE Transactions Microwave Theory and Techniques*, MTT-27:NO 12, 1979. (Cited on page 39.)

[13] G.J. Wheeler J. Reed. A method of analysis for symmetrical four-port networks. *IRE Transactions on Microwave Theory and Techniques.* (Cited on page 34.)

[14] Ildu Kim Bumman Kim Jangheon Kim, Jeonghyeon Cha. Optimum operation of asymmetrical-cells-based linear doherty power amplifiers - uneven pwoer drive and power matching. *IEEE Transactions on Microwave theory and techniques*, 53:1802–1809, 2005. (Cited on pages 95 and 96.)

[15] Bumman Kim Jong Sung Lee Sang Hoon Kim Jeohgheyon Cha, Jangheon Kim. Highly efficient power amplifier for cdma base stations using doherty configuration. *Department of Electronic and Electrical Engineering and Microwave Application Research Center, Pohang University of Science and Technology.* (Cited on page 95.)

[16] David M. Pozar. *Microwave Engineering Third Edition.* Wiley, 2005. (Cited on pages xii, 3, 18, 22, 23, 31, 61, 71, and 72.)

[17] Inder J. Bahl Rajesh Mongia, Prakash Bhartia. *RF And Microwave Coupled-line Circuits.* Artech House Publishers. (Cited on pages 72 and 9–1.)

[18] Adel A. M. Saleh and Donald C. Cox. Improving the power added efficiency of fet amplifiers operating with varying-envelope signals. *IEEE Transactions on Microwave Theory and Techniques*, 31:51–56, 1983. (Cited on page 68.)

[19] Dr W Steyn. (reutech radar systems) the hard and soft of rf limiters. 22-23 March 2005. (Cited on page 76.)

[20] Cornell van Niekerk. Mulit-bias extraction of fet series parasitic elements. *Submitted for publication to IEEE Microwave and Wireless Components Letters.* (Cited on pages 17 and 18.)

[21] Bumjae Shin Youngoo Yang, Jeonghyeon Cha and Bumman Kim. *IEEE Microwave and wireless components letters*, Vol 13:370–372, September 2003. (Cited on pages 68, 70, 81, 95, and 96.)

[22] Young Yun Woo Youngoo Yang, Jaehyok Yi and Bumman Kim. Design for linearity and efficiency of a microwave doherty amplifier using a new load matching technique. *Microwave Journal*, Vol. 44, No. 12:pp. 20–36, 2001. (Cited on page 26.)

Chapter 9

Appendix A: Coupler Dimensions

Here follows the MATLAB code used to calculate the resulting even and odd mode impedances for a single coupled line with coupler spacing S [17].

$h = 0.508$

$W = 1.13994$

$er = 3.38$

$ere = 2.64549$

$t = 0.035$

$dW = ((1 + 1/e_r)/(2 * pi) * log(10.872/sqrt((t/h)^2 + (1/pi/(W/t + 1.1))^2))) * t$

$W = W + dW$

$u = W/h$

$g = S./h$

$f_u = 6 + (2 * pi - 6) * exp(-(30.666/u)^{0.7528})$

$Z_{0=}60/sqrt(e_{re}) * log(f_u/u + sqrt(1 + (2/u)^2))$

$Z_0 = 42.4/sqrt(e_r+1)*log(1+(4*h/W)*(((14+8/e_r)/11)*(4*h/W)+sqrt(((14+8/e_r)/11)^2*(4*h/W)^2 + (1+1/e_r)/2*pi^2)))$

$v = u * (20 + g.^2)/(10 + g.^2) + g. * exp(-g)$

$ae = 1 + log((v.^4 + (v./52).^2)./(v.^4 + 0.432))./49 + log(1 + (v./18.1).^3)./18.7$

$be = 0.564 * ((e_r - 0.9)/(e)r + 3))^{0.053}$

$e_{re-eff} = 0.5 * (e_r + 1) + 0.5 * (e_r - 1). * (1 + 10./v).^{-ae*be}$

$bo = 0.747 * e_r./(0.15 + e_r)$

$co = bo - (bo - 0.207) * exp(-0.414 * u)$

$do = 0.593 + 0.694 * exp(-0.562 * u)$

$ao = 0.7287 * (e_{re} - 0.5 * (e_r + 1)) * (1 - exp(-0.179 * u))$

$e_{ro-eff} = (0.5 * (e_r + 1) + ao - e_r)e). * exp(-co * g.^{do}) + e_{re}$

$Q1 = 0.8695 * u^{0.194}$

$Q2 = 1 + 0.7519. * g + 0.189. * g.^{2.31}$

$Q3 = 0.1975 + (16.6 + (8.4./g).^6).^{-0.387} + log(g.^{10}./(1 + (g./3.4).^{10}))./241$

$$Q4 = (2. * Q1./Q2). * (exp(-g). * u.^{Q3} + (2 - exp(-g)). * u.^{-Q3}).^{-1}$$

$$Q5 = 1.794 + 1.14 * log(1 + 0.638./(g + 0.517. * g.^{2.43}))$$

$$Q6 = 0.2305 + log(g.^{10}./(1 + (g./5.8).^{10}))./281.3 + log(1 + 0.598. * g.^{1.154})./5.1$$

$$Q7 = (10 + 190 * g.^2)./(1 + 82.3. * g.^3)$$

$$Q8 = exp(-6.5 - 0.95. * log(g) - (g./0.15).^5)$$

$$Q9 = log(Q7). * (Q8 + 1./16.5)$$

$$Q10 = Q2.^{-1}. * (Q2. * Q4 - Q5. * exp(log(u). * Q6. * u.^{-Q9}))$$

$$Ze = Z0. * sqrt(e_{re}./e_{reeff})./(1 - (Z00/377). * e_{re}.^{0.5}. * Q4)$$

$$Zo = Z0. * sqrt(e_{re}./e_{ro-eff})./(1 - (Z00/377). * e_{re}.^{0.5}. * Q10)$$