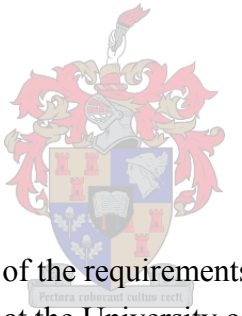
Development and Implementation of a 1.5 MW Inverter and Active Power Filter System for the Injection of Regenerated Energy in a Spoornet Traction Substation

Heinrich Daniël Fuchs



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Supervisor: Prof H. du Toit Mouton

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work , unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

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H. D. Fuchs Date:

Summary

Spoornet is one of South-Africa's largest railway companies. It is very important to operate the railway system as cost effectively as possible. A large portion of the railway operates from 3 kV DC traction supplies. One method of cost saving is to utilise the regenerative braking mechanism of the electric trains. By using this method the train decelerates by using the electric motor of the engine instead of the mechanical braking system. When the electric motor is used for braking, the momentum of the train pushes the motor which then generates electric energy. This regenerated energy flows through the overhead lines back to the nearest substation. Previously this energy was just dumped in large resistor banks and has gone to waste as heat. The aim of this thesis was to implement a system that will inject the regenerated energy back into the Eskom supply network. This will save the cost of the electricity that is supplied back to Eskom as well as the cost saving on the mechanical braking system of the train. Furthermore the system will be an active power filter to eliminate the harmonic pollution on the Eskom network caused by the rectifier in the traction substation.

Opsomming

Spoornet is een van Suid-Afrika se grootste spoorwegmaatskappye. Dit is baie belangrik om die spoorweg so koste effektief as moontlik te bestuur. ‘n Groot gedeelte van die spoorweg werk vanaf ‘n 3 kV GS toevoer. Een metode om koste te bespaar is om die generatorwerking meganisme van die elektriese trein te benut. Hierdie metode gebruik die elektriese enjin van die trein om te rem in plaas van die meganiese remstelsel. Wanneer die elektriese enjine gebruik word om te rem, druk die momentum van die trein die enjine sodat dit elektriese energie genereer. Hierdie hernude energie vloei terug na die naaste substasie via die oorhoofse toevoerlyne. Voorheen is hierdie energie vekwis in weerstandsbanke en het dit dus verlore gegaan as hitte. Die doel van hierdie tesis is om ‘n stelsel te implementeer wat die hernude energie terug sit in die Eskom toevoer netwerk. Dit sal die koste bespaar van die elektrisiteit wat voorsien word aan Eskom sowel as die meganiese remstelsel wat minder gebruik word. Verder sal die stelsel ook optree as ‘n aktiewe filter om die harmonieke, afkomstig van die gelykrigter, te verminder.

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Glossary

ADC	Analog to Digital Converter
APF	Active Power Filtering
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
EMI	Electro Magnetic Interference
EPLD	Erasable Programmable Logic Device
FLC	Flying-Capacitor inverter
FPGA	Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
IMB	Current Measurement Board
NPC	Neutral-Point-Clamped inverter
PEC 33	Power Electronics Controller version 33
PWM	Pulse Width Modulation
Regen	Regenerated energy; the act of producing regenerated energy
SPWM	Sinusoidal Pulse Width Modulation
SS	Series-Stacked inverter
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
VHDL	Very High Speed Hardware Description Language
VMB	Voltage Measurement Board

Chapter 1 - Introduction

Spoornet is one of South-Africa's major railway companies with a large portion of their railway system operating from 3 kV DC. This is provided by a DC traction substation situated every 10 to 15 kilometres along side the railway track. The power for the substations is provided by South-Africa's electrical energy supplier, Eskom. The purpose of the substation is to convert the 3-phase AC supply from Eskom to 3 kV DC. The system implemented for this thesis is installed in the DC traction substation at the town of Wolseley in the Western Cape. The railway track running past this substation is one of the main tracks between Johannesburg and Cape Town. It is host to a few passenger trains but the main occupants are freight trains carrying cargo between these 2 cities. The reason for choosing the substation at Wolseley is due to the occurrence of regenerative braking by the trains in the vicinity of this substation. The concept of regenerative braking is explained further on in this chapter. Under normal conditions all the traction substations operate in parallel to each other. If one substation is to fail, power is supplied by the 2 adjacent substations. Most of the trains operating on these railway tracks uses a 4.5 MW locomotive but depending on the size of the train 2 or even 3 locomotives are used.

1.1. - Regenerative energy / braking

When a train is moving down a descent it will have to brake in order not to exceed the safe speed limit of the track. Two methods of braking can be implemented by the operator of the train; the electrical motor of the locomotive or the mechanical braking system. By using the motor to brake, the momentum of the train down the descent pushes the motor which then acts as a generator. The mechanical energy from the momentum of the train is converted to electrical energy which flows back to the nearest substation. Therefore regenerated energy is defined as the electrical energy created when the train utilises the electrical motor of the locomotive to brake. From here on forward regenerative energy and regenerative braking will be referred to as regen-energy and regen-braking. The amount of regen-energy that can be produced is dependent on the weight of the train and the slope of the descent. If another train is moving upwards during the same time that a train is using regen-braking, the regen-energy will be used by the train moving upwards and the excess regen-energy will flow to the substation.

1.2. – Function of the regen-system

It is both expensive and labour intensive to maintain the mechanical braking system of the train. Therefore regen-braking is a more desirable method of braking. At present the regen-energy is dumped in large resistor banks at the substation. These resistor banks are expensive to maintain and the regen-energy is lost as heat. The purpose of the regen-system is

to inject the regen-energy received from the train back into the Eskom supply, thereby saving the cost of the energy that is supplied back to Eskom. Also the wear on the mechanical braking system is reduced therefore saving the maintenance cost. The need for large regen dump resistors is also eliminated.

The traction rectifier in the substation is a source of harmonic pollution on the Eskom supply network. The 230 V AC and 380 V AC supply in the substation are also affected by this pollution and damage to equipment may occur. The regen-system must minimise this pollution by functioning as an Active Power Filter (APF) during load conditions.

1.3. - Overview of the traction substation

Figure 1.1 provides a diagram of the DC traction supply system of the substation. Power is provided by the 3-phase 66 kV_{LL} Eskom supply. A supply transformer steps the 66 kV down to 6-phase 2 420 V_{LL}. A 6-pulse rectifier is used for the rectifying of the 6-phase secondary of the supply transformer. A filter at the output of the rectifier reduces the ripple in the DC supply. This filter consists of a 1.7 mH inductor in series with the supply and shunt connected capacitors to compensate for the 6^{th}, 12^{th}, 18^{th}, and 24^{th} harmonics. The no-load voltage of the supply varies between 3 150 V and 3.4 kV DC. Under load conditions the voltage may fall to 2.3 kV. The maximum voltage is determined by the over voltage protection that is implemented on the train which limits the DC voltage to 3.9 kV [1]. The positive terminal of the DC traction supply is connected to the overhead lines of the railway. The railway track itself is the negative of the DC supply and is connected to the neutral point of the supply transformer. The “earth” terminal of the substation is isolated from physical earth with the implementation of a spark-gap. The difference in the voltage between the “earth” of the substation and physical earth is limited to approximately 300 V by the spark-gap. The “earth” of the substation is connected to the DC negative of the traction supply therefore all the voltages of the equipment in the substation are relative to DC negative and not physical earth. By isolating the DC negative from earth ensures that the return currents from the railway track will flow in the DC negative cable and not through the earth itself. The substation consists of 2 of the supply units shown in Figure 1.1 working in parallel. Each unit can supply the full load on its own. This allows that one unit can be switched off when maintenance has to be done on that unit.

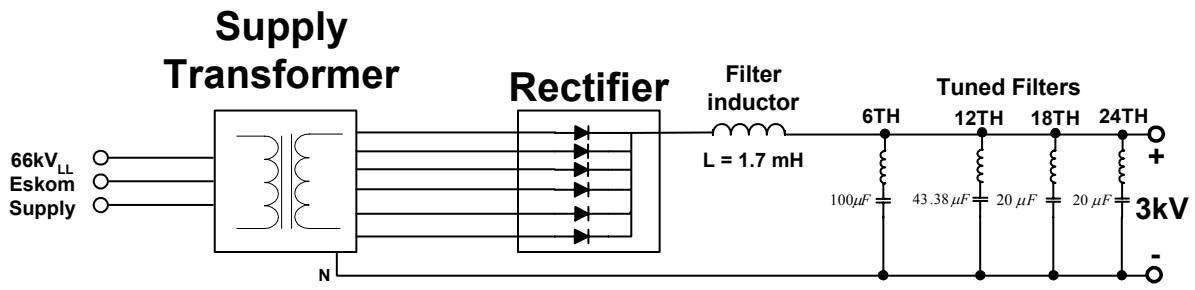

Figure 1.1 – Diagram of the DC traction supply in the substation

1.4. - Overview of the regen-system

Figure 1.2 provides a diagram of the regen-system implemented in the substation. Only 1 of the traction supply units in the substation is used in conjunction with the regen-system. The DC-bus of the regen-system is connected to the 3 kV DC traction supply. The AC side of the regen-system connects to the 6-phase secondary of the supply transformer. The regen-energy that is injected into the Eskom supply flows from the DC supply that is connected to the train through the regen-system into the supply transformer and back into the Eskom grid. The different components of the regen-system are described in later chapters.

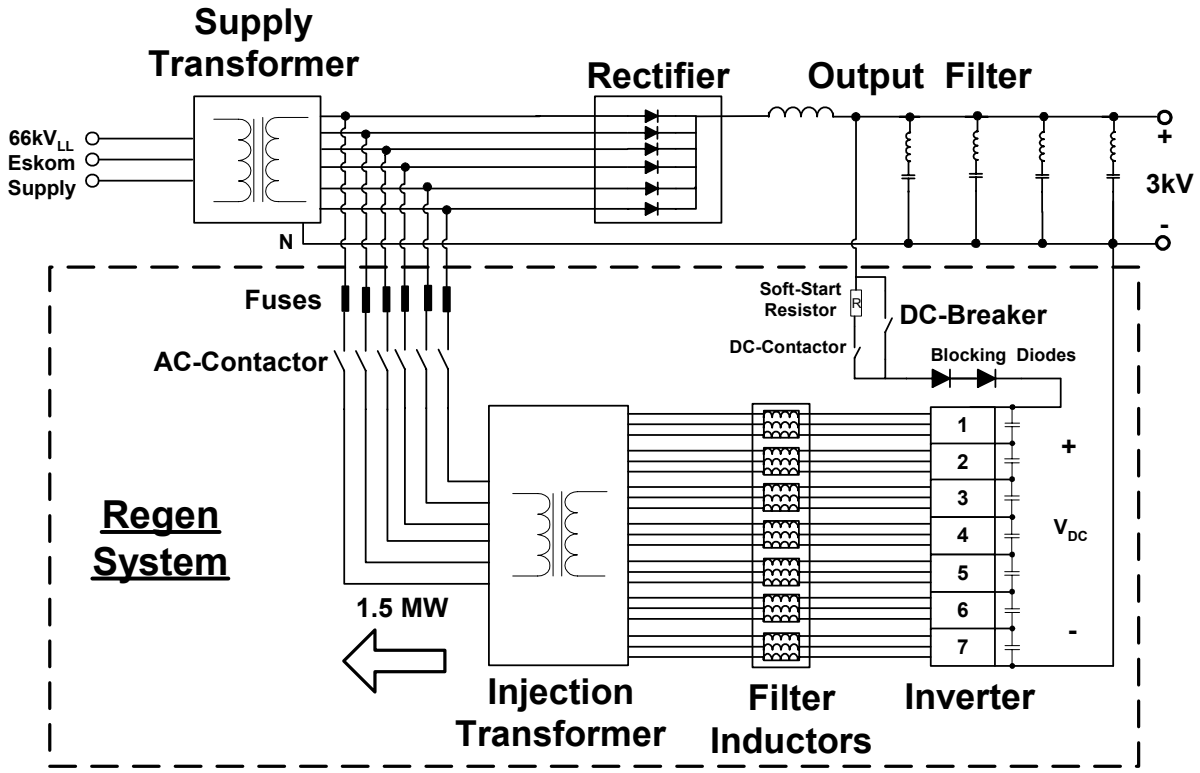

Figure 1.2 – Diagram of the overall system

Figure 1.3 is a photograph of the regen-bay in the substation.

Figure 1.3 – Photograph of the regen-bay

Figure 1.4 provides a photograph of the rectifier bay of the substation. The regen-system connects to the 6-phase secondary of the supply transformer through the fuse cabinet visible in the bottom left of the photograph.

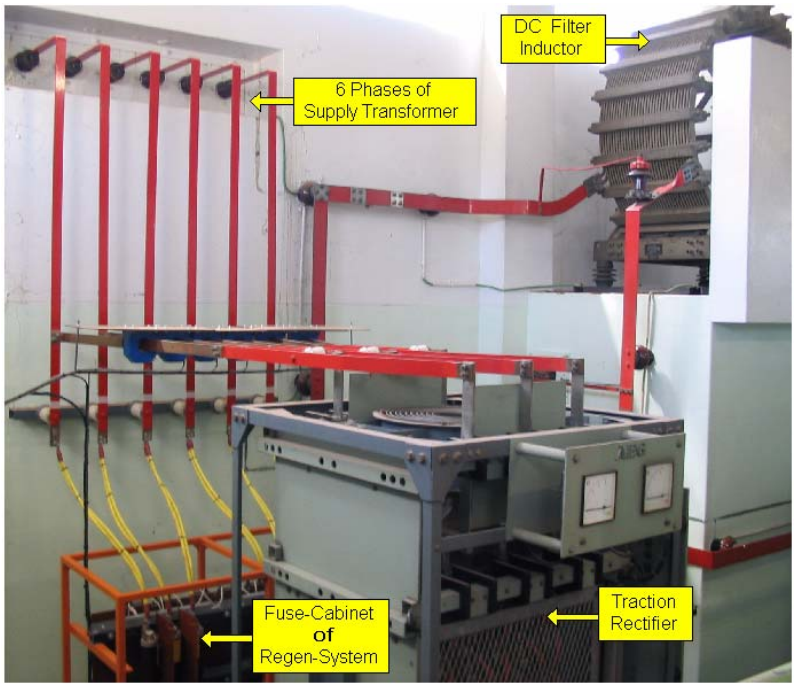

Figure 1.4 – Photograph of the rectifier bay

1.5. – Specifications for the regen-system

The regen-system must be capable of injecting a continuous power rating of 1.5 MW of regen-energy into the Eskom supply. Due to the connection of the regen-system as shown in Figure 1.2 the maximum DC-bus voltage of the regen-system is the same as that for the traction supply. The clearance distance between the high voltage 3 kV equipment and the low voltage equipment is very important for the construction of the system. It is specified that a minimum clearance distance of 150 mm in open air must be maintained around the 3 kV equipment. In an enclosure this distance can be reduced to 75 mm. Everywhere these distances cannot be acquired extra insulation must be installed to achieve the specified 10.5 kV_{rms} insulation. Table 1.1 lists some of the specifications for the regen-system as requested by Spoornet [1].

Table 1.1 – Specifications for the regen-system

Description	**Value**
Power rating	1.5 MW
Maximum DC voltage	3.9 kV
Insulation	10.5 kV_{rms} for 1 min
Ambient temperature	-10 to +50 ^{0}C

All the control and measurement signals connected to the controller must be sent via fibre-optic cables except where isolated Hall-effect current probes are used. The controller and circuitry of the regen-system must operate from the 110 V DC supply from the battery bank of the substation. The full specification for the regen-system is provided in [1] which is also added in Appendix A.

1.6. – Concept of regen-system operation

The regen-mode of the system operates with the implementation of a DC-bus regulator. The DC-bus of the inverter is regulated at 3.5 kV by the regulator implemented in the software of the controller. During load and no-load time periods that the DC voltage of the traction supply is less that 3.5 kV the regen-system draws energy from the AC side of the system to regulate the DC-bus at 3.5 kV. When the train uses regen-braking the diodes of the traction rectifier becomes reversed biased. This causes the DC traction supply voltage to increase. If no regen-system is present the DC voltage will increase until it reaches the maximum of 3.9 kV when the over voltage protection of the train will set in. With the regen-system activated the DC-bus is regulated at 3.5 kV by converting the regen-energy from the train through the

regen-system and injecting it into the Eskom supply. The DC regen-energy is converted to AC by the inverter and injected into the secondary of the supply transformer by means of the injection transformer. Current limiting implemented in the controller limits the energy through the regen-system to 1.5 MW, therefore if more than 1.5 MW regen-energy is received from the train the DC voltage will start to increase. The amount of regen-energy produced by the train depends on how the operator of the train utilises the regen-braking. It is the operator's responsibility to ensure that the DC voltage stays below 3.9 kV

The APF-mode of the regen-system makes use of the current measurements at the input of the traction rectifier. During no-load or regen-conditions there is no current flowing into the rectifier and the APF-mode of the regen-system is dormant. During load conditions the current flow into the rectifier is detected and the APF-mode becomes active [2].

1.7. – Thesis structure

A brief overview of the thesis is provided

Chapter 2 Provides a description of 4 multilevel inverter topologies. The topologies are compared to each other and the topology that is best suited for the regen-system is determined.

Chapter 3 Describes the inverter that is implemented in the regen-system. The different components of the inverter are also discussed.

Chapter 4 The measurement system for the regen-system is described. The different voltage and current measurement hardware as well as the software for the encoding and decoding of the voltage measurements are described.

Chapter 5 The injection transformer that is used for the injection of the regen-energy is discussed. The topology of the transformer is explained as well as the current waveforms for different types of loads on the transformer.

Chapter 6 An overview of the switchgear and protection that is implemented in the regen-system is provided.

Chapter 7 Results for both the APF-mode and regen-mode of operation are presented.

Chapter 8 Concludes the thesis and suggests some improvements to the system.

Chapter 2 – Multilevel Inverter Topologies

The significant increase in the demand for high voltage high power inverter systems has surpassed the abilities of the available semiconductor devices. Readily available semiconductor devices cannot cope with the kilovolt and megawatt ratings that are demanded from them. By simply connecting these devices in parallel or series can over come this problem but with the addition of current sharing and voltage spike problems [4], [13]. This has led to the development of multilevel inverter topologies where semiconductor devices are connected in innovative ways so that the voltage across the device is kept low but the operating voltage and power of the inverter are dramatically increased.

Some features of multilevel inverters are [5]:

- The output waveform has reduced harmonic content and lower dv/dt.
- The input current that is drawn has very low distortion.
- The switching frequency can be low.

The following sections provide an overview of 4 multilevel inverter topologies. The Neutral-Point-Clamped, Flying-Capacitor, Cascaded and Series-Stacked multilevel inverter topologies are discussed. Furthermore the topologies are compared to decide which one will be best suited for the implementation of the inverter in the regen-system.

2.1. – Neutral-Point-Clamped (NPC) Multilevel Inverter Topology

The NPC inverter topology [4], [5], [6], [10], [12], [13] is also referred to as the Diode-Clamped topology due to the diodes that clamp the voltage across the switching element. Applications of the NPC topology include motor drives [7] and active power filters [9].

Figure 2.1 provides a diagram of a 3-level single-phase NPC inverter. The DC-bus voltage is divided by 2 series connected capacitors to produce 3 voltages levels, $V_{DC}/2$, 0, - $V_{DC}/2$, if the output voltage is taken between points a and n. For a DC to DC converter the output is taken between points a and o with the voltage levels being V_{DC}, $V_{DC}/2$ and 0.

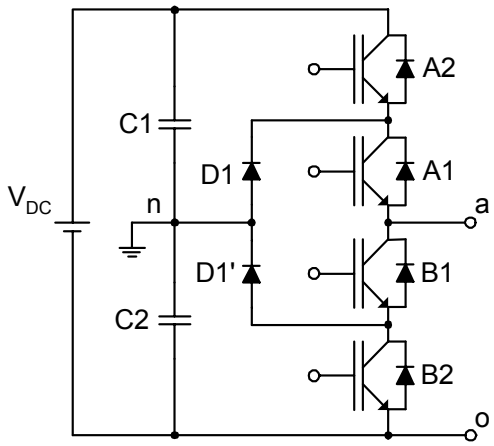

Figure 2.1 – Diagram of a 3-level Neutral Point Clamped inverter

The difference between the NPC topology and a conventional 2-level inverter is the clamping diodes D1 and D1'. The diodes clamp the voltage across the switching element to half of the DC-bus. By turning on the switching elements in a specific sequence the 3-level output is achieved. To realise the voltage $V_{an} = V_{DC}/2$, the top switches, A1 and A2, are closed connecting point a to $V_{DC}/2$. The diode D1' divides the DC-bus voltage across the switches B1 and B2 with B1 blocking the voltage across C1 and B2 blocking the voltage across C2. For the voltage $V_{an} = 0$, the switches A1 and B1 is turned on and for $V_{an} = - V_{DC}/2$, the bottom switches B1 and B2 are turned on. Figure 2.2 provides an illustration of the output voltage of a NPC inverter with the output taken between points a and n.

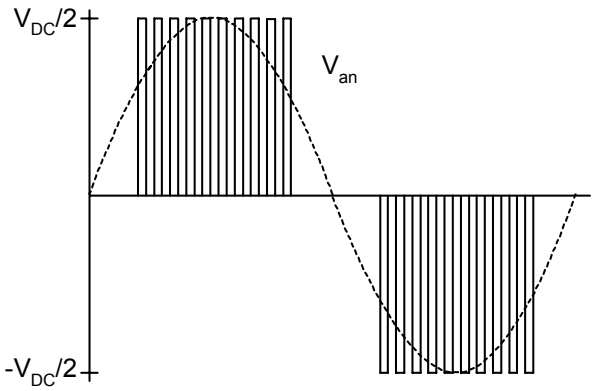

Figure 2.2 – Illustration of output voltage for a 3-level NPC inverter

Figure 2.3 provides a diagram of a 5-level single phase NPC inverter. The DC-bus voltage is divided by 4 series connected capacitors providing the 5 voltage levels for the output. If the

output is taken between points a and n the levels are; $V_{DC}/2$, $V_{DC}/4$, 0, - $V_{DC}/4$, - $V_{DC}/2$. An m-level NPC inverter requires a total of (m-1) DC-bus capacitors connected in series [5] and each phase-arm necessitates the use of (m-1) x 2 switches [4].

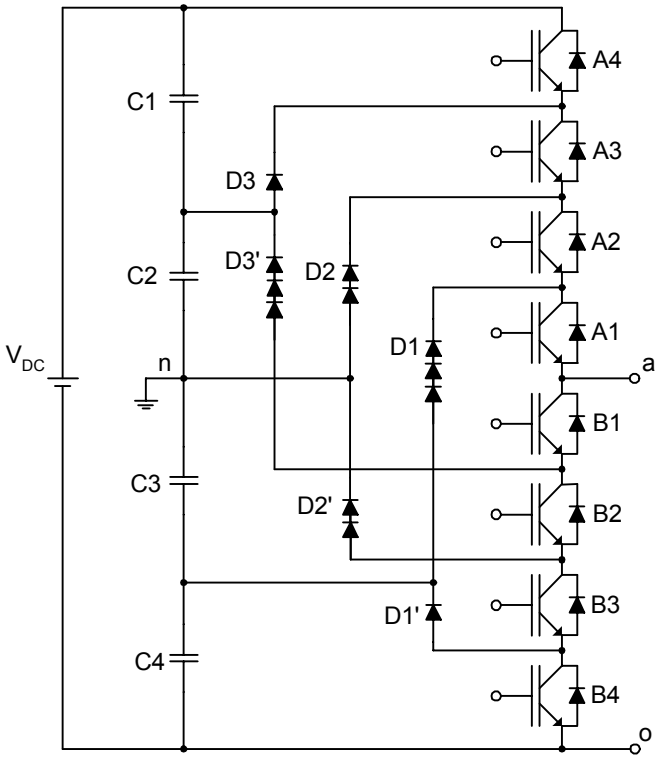

Figure 2.3 – Diagram of a 5-level Neutral Point Clamped inverter

The 5-level staircase output voltage, as shown in Figure 2.4, is synthesized by controlling the switches in a specific sequence.

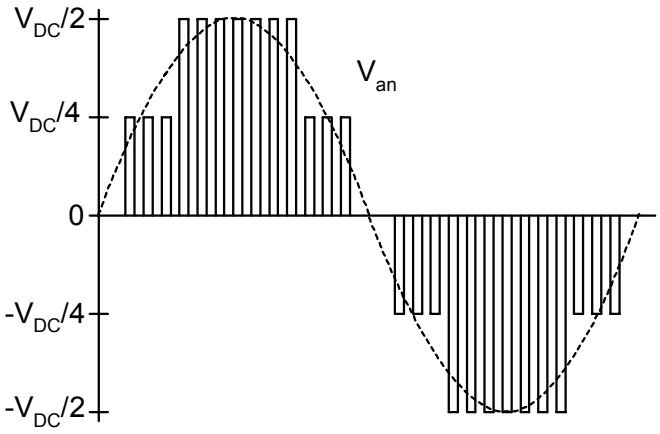

Figure 2.4 – 5-level output waveform of NPC

Table 2.1 lists the switch combinations.

Table 2.1 – Switching sequence for a 5-level NPC inverter

V_{an}	A4	A3	A2	A1	B1	B2	B3	B4
$V_{DC}/2$	***on***	***on***	***on***	***on***	off	off	off	off
$V_{DC}/4$	off	***on***	***on***	***on***	***on***	off	off	off
0	off	off	***on***	***on***	***on***	***on***	off	off
$-V_{DC}/4$	off	off	off	***on***	***on***	***on***	***on***	off
$-V_{DC}/2$	off	off	off	off	***on***	***on***	***on***	***on***

For this 5-level NPC inverter there are 4 complimentary pairs. This means that by turning on one of the switches in the pair, the other one must be off. From Table 2.1 it is seen that these complimentary pairs are (A4, B1), (A3, B2), (A2, B3) and (A1, B4). By means of the clamping diodes each switch only has to block a voltage of $V_{DC}/4$. For a m-level NPC inverter this voltage is $V_{DC}/(m-1)$. The different clamping diodes must block different voltages, for example: if switches B2 to B4 are turned on, diode D3' must block 3 capacitor voltages and D2' must block 2 capacitor voltages. Similarly D1 must block 3 capacitor voltages and D2 must block 2 capacitor voltages. If it is assumed that the diodes have the same voltage blocking rating as the switches a number of diodes must be connected in series to achieve the necessary blocking voltage. This means that for an m-level NPC inverter (m-1)x(m-2) clamping diodes are required for each phase of the inverter. As the number of levels increase the construction of the inverter becomes impractical due to the large number of clamping diodes.

It is difficult to do real power transfer with this topology. This is due to the unidirectional current flow through the capacitors which will cause unbalance in the capacitor voltages [6]. Various control methods and strategies have been devised to address this problem and through the correct selection of the switching combination the current through the capacitors can be controlled and therefore the capacitor voltage can be controlled [7], [8], [9].

The following are some of the advantages and disadvantages of the NPC inverter.

Advantages:

- As the number of levels increases the harmonic content of the output waveform decreases which decreases the filter size.
- Lower switching losses due to the devices being switched at the fundamental frequency without increasing the harmonic content in the output [4], [7].
- Reactive power flow can be controlled as this does not cause unbalance in the capacitor voltages.
- Fast dynamic response.
- Back to back operation is possible [14].

Disadvantages:

- High number of clamping diodes is required as the number of levels increase.
- Active power transfer causes unbalance in the DC-bus capacitors, this complicates the control of the system [4].
- There is no redundancy in the synthesis of the inner voltage levels as with the Flying-Capacitor multilevel inverter. This increases the complexity of the balancing of the DC-bus capacitors [11].

2.2. – Flying-Capacitor (FLC) Multilevel Inverter Topology

The FLC multilevel inverter topology [4], [5], [6], [13], [16] has also been referred to as an imbricated (overlapping) cell topology [13], capacitor-clamped topology and multicell topology [11], [16]. Instead of using diodes as in the case of the NPC inverter the FLC inverter uses flying-capacitors to clamp the voltage across the switching elements. Applications for this topology include voltage-source inverters, high voltage power supplies, active power filters, DC to DC converters and traction systems [13], [15], [16].

Figure 2.5 is a diagram of a 3-level single-phase FLC multilevel inverter. If the output is taken between points a and n the 3 output voltage levels are, $V_{DC}/2$, 0 and $-V_{DC}/2$.

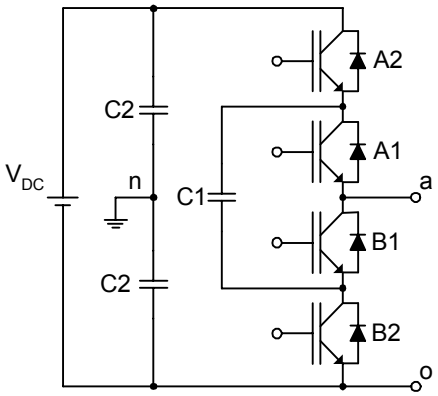

Figure 2.5 – Diagram of a 3-level FLC inverter

The 3-level output voltage V_{an} can be synthesized by the following switch combinations. For $V_{an} = V_{DC}/2$ switches A1 and A2 must be turned on. For $V_{an} = 0$ either A2 and B1 or A1 and B2 must be turned on; and for $V_{an} = -V_{DC}/2$ switches B1 and B2 must be turned on. For the 0 level output there are 2 switching combinations. By choosing the correct sequence the voltage of the clamping capacitor C1 can be controlled. When A2 and B1 are turned on C1 is charged and when A1 and B2 are turned on C1 is discharged.

Figure 2.6 provides a diagram of one phase-leg of a 5-level FLC multilevel inverter. The output voltages between points a and n are: $V_{an} = V_{DC}/2$, $V_{DC}/4$, 0, $- V_{DC}/4$, $- V_{DC}/2$.

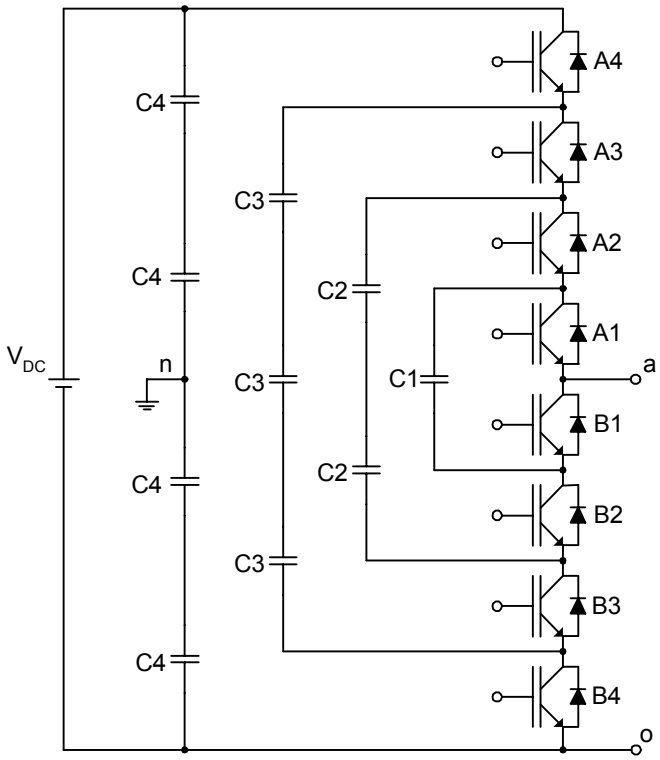

Figure 2.6 – Diagram of a 5-level Flying Capacitor inverter

Figure 2.7 provides an alternative diagram for the 5-level NPC inverter shown in Figure 2.6. The alternative representation helps to clarify the structure of one cell of the FLC inverter topology.

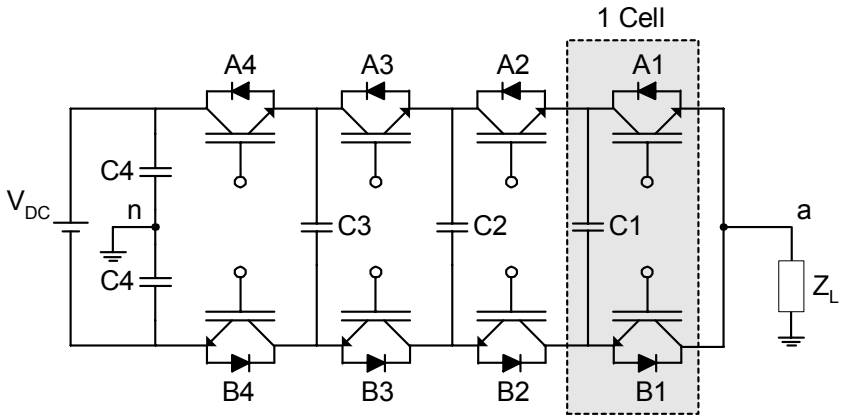

Figure 2.7 – Alternative diagram of a 5-level FLC inverter

One cell of the inverter is the combination of 2 switches and a clamping capacitor as indicated in Figure 2.7. The 5-level FLC inverter consists of 4 cells. The voltage divides across the clamping capacitors so that $V_{C1} = V_{DC}/4$, $V_{C2} = V_{DC}/2$ and $V_{C3} = 3V_{DC}/4$. Therefore the voltage blocking rating of each switch only has to be $V_{DC}/4$ and for an N-cell topology the voltage blocking rating needs to be V_{DC}/N [6].

The synthesis of the 5-level output voltage waveform has more flexibility than that of the NPC inverter. Redundancy in the switch combination for certain voltage levels allows for more freedom in the control of the capacitor voltages. The following provides the switch combinations of how the 5-level staircase output voltage waveform can be achieved [5].

Voltage level 1: $V_{an} = V_{DC}/2$ (1 combination)

1) Turn on switches A1 to A4

Voltage level 2: $V_{an} = V_{DC}/4$ (3 combinations)

Figure 2.8 illustrates the first combination of switches for voltage level 2.

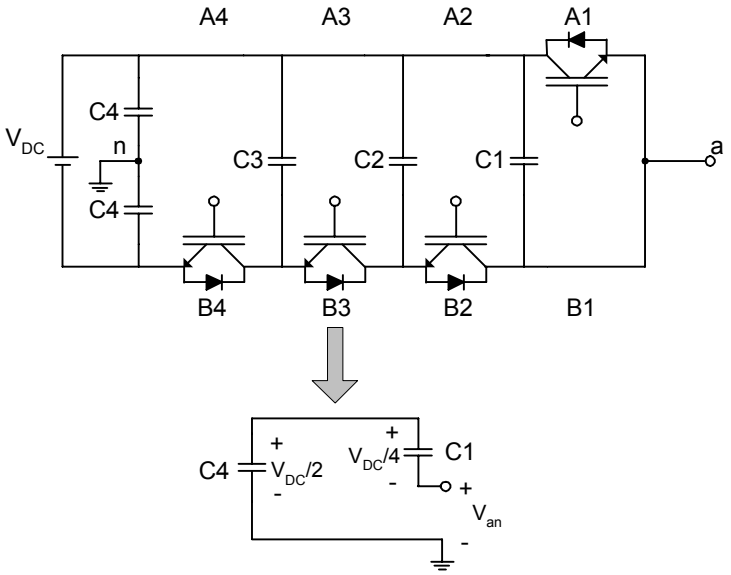

Figure 2.8 – Illustration of a switch combination 1

1) Turn on A4, A3, A2 and B1. $V_{an} = V_{DC}/2 - V_{DC}/4$

2) Turn on A3, A2, A1 and B4. $V_{an} = 3V_{DC}/4 - V_{DC}/2$

3) Turn on A4, A2, A1 and B3. $V_{an} = V_{DC}/2 - 3V_{DC}/4 + V_{DC}/2$

Voltage level 3: $V_{an} = 0$ (6 combinations)

1) Turn on A4, A3, B1 and B2. $V_{an} = V_{DC}/2 - V_{DC}/2$
2) Turn on A2, A1, B3 and B4. $V_{an} = V_{DC}/2 - V_{DC}/2$
3) Turn on A4, A2, B1 and B3. $V_{an} = V_{DC}/2 - 3V_{DC}/4 + V_{DC}/2 - V_{DC}/4$
4) Turn on A4, A1, B2 and B3. $V_{an} = V_{DC}/2 - 3V_{DC}/4 + V_{DC}/4$
5) Turn on A3, A1, B2 and B4. $V_{an} = 3V_{DC}/4 - V_{DC}/2 + V_{DC}/4 - V_{DC}/2$
6) Turn on A3, A2, B1, and B4. $V_{an} = 3V_{DC}/4 - V_{DC}/4 - V_{DC}/2$

Voltage level 4: $V_{an} = -V_{DC}/4$ (3 combinations)

1) Turn on A4, B1, B2 and B3. $V_{an} = V_{DC}/2 - 3V_{DC}/4$
2) Turn on A1, B2, B3 and B4. $V_{an} = V_{DC}/4 - V_{DC}/2$
3) Turn on A2, B1, B3 and B4. $V_{an} = V_{DC}/2 - V_{DC}/4 - V_{DC}/2$

Voltage level 5: $V_{an} = -V_{DC}/2$ (1 combination)

1) Turn on B1 to B4

The 2 switches of a cell must be complimentary pair. This means that if one of the switches is turned on the other one must be turned of. If both switches of a cell are turned on at the same time the clamping capacitor will be shorted.

It is desired that the average current through the clamping capacitors be zero as to keep the voltage level of the cap constant. By applying the correct switching combinations the voltages of the clamping capacitors can be controlled [5], [6], [16]. The redundancy in the switch combinations for certain output voltages leaves more freedom in the control of the system. This makes it possible to do real power transfer with this topology [4].

Assuming that the capacitors has the same voltage rating as that of the switches, the number of capacitors required for the DC-bus in an m-level inverter is (m-1). The number of clamping capacitors required by each phase of the inverter is ((m-1) x (m-2))/2.

The control signals can be interleaved to increase the quality of the output voltage waveform. The ripple of the output voltage has an amplitude of V_{DC}/N and a frequency of N x f_s, the switching frequency. Compared to the normal 2-level inverter topology this reduces the

output filter by approximately N^2. This is due to the simultaneous increase in the apparent switching frequency (N factor) and the smaller voltage steps (N factor) [13], [16].

The following are some of the advantages and disadvantages of the FCL inverter topology.

Advantages

- The large number of capacitors in this topology provides extra ride through during a power outage.
- As the number of levels increase the harmonic content of the output voltage waveform decreases and the size of the filter also decreases.
- Redundancy of switch combinations is provided.
- Fast dynamic response.
- Real and reactive power flow can be controlled.

Disadvantage

- A vast amount of capacitors are required as the levels of the inverter increase. This raises the cost and complicates the construction of the inverter.
- Control is complicated.

2.3. – Cascaded Multilevel Inverter Topology

The Cascaded Multilevel Inverter topology with separate DC sources consists of single-phase full-bridge inverters with their outputs connected in series [4], [5], [12], [14]. Applications of this topology include adjustable speed drives, static var compensation and series sag compensation [14], [17], [18]. The structure of this multilevel inverter is well suited for renewable energy sources such as fuel cell and photovoltaic.

Figure 2.9 provides a diagram of a 9-level single-phase cascaded inverter with separate DC sources.

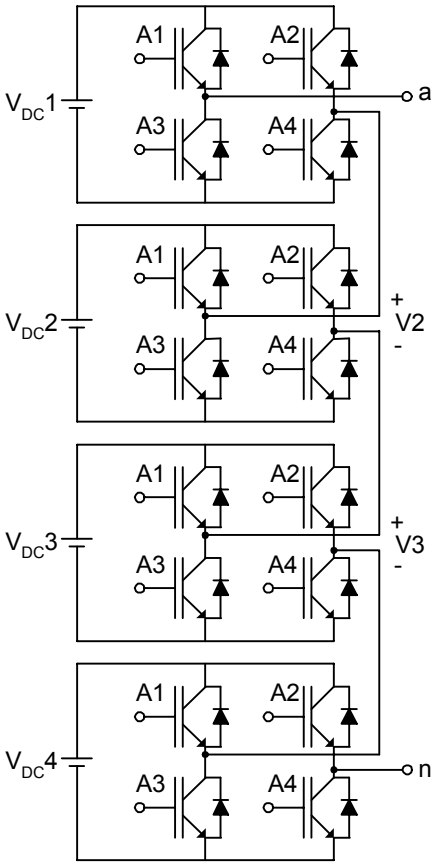

Figure 2.9 – 9-level Cascaded inverter

Each single-phase full-bridge inverter produces a 3-level output waveform with levels at $+V_{DC}$, 0 and $-V_{DC}$. The voltage V_{an} is the sum of the outputs of each full-bridge inverter. The 9-level cascaded inverter shown in Figure 2.9 consists of 4 single-phase full-bridge inverters. The resulting output waveform varies between $4V_{DC}$ and $-4V_{DC}$ as shown in Figure 2.10 and is nearly sinusoidal even without filtering. Each switching element only has to switch once for every cycle of the fundamental output voltage, therefore switching losses are significantly reduced [17].

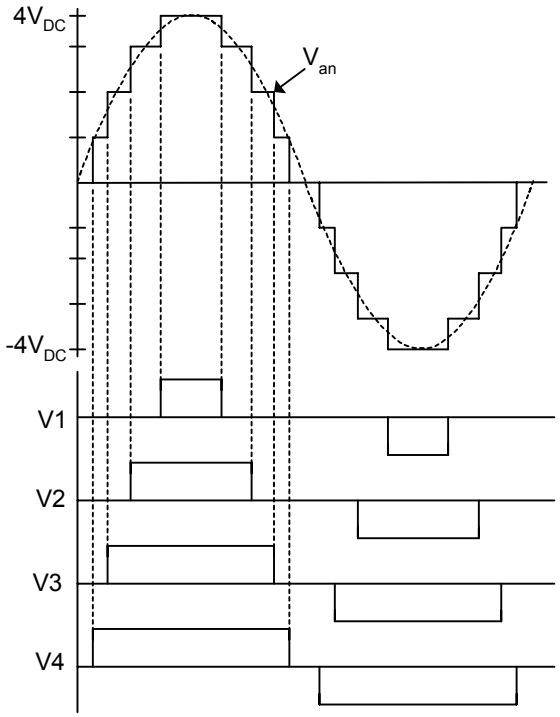

Figure 2.10 – Output waveform for the 9-level cascaded inverter

It is possible to do real and reactive power transfer with this topology. For real power transfer separate DC sources are required for each full-bridge inverter where batteries are typically used as the DC source [14]. To serve as a reactive power compensator the DC sources can be replaced with capacitors so that the cascaded inverter can act as a static var generator [12], [18].

An m-level cascaded inverter requires (m-1)/2 single-phase full-bridge inverters [18]. The number of levels can be related to the number of DC sources as, m = 2s + 1, where m is the number of levels in the output voltage and s is the number of DC sources [4], [14].

The following is a list of some of the advantages and disadvantages of this topology:

Advantages

- For the same number of output voltage levels it has the lowest component count of the multilevel inverters. No extra clamping diodes or capacitors are needed.
- Can easily be extended to a higher level with the addition of more full-bridge inverters in cascade.
- Provides a fast dynamic response [18].
- The circuit layout can be modularised to simplify construction.

Disadvantages

- Requires separate DC sources for each full-bridge inverter used in the topology when real power transfer is needed.
- No back-to-back operation can be performed with this topology due to a possible short circuit between the 2 converters.

2.4. – Series-Stacked (SS) Multilevel Inverter Topology

The series-stacked multilevel inverter topology comprises of standard full-bridge inverters with their DC-busses connected (stacked) in series [3], [12], [19], [21]. Applications of this topology include traction systems, active power filtering and power quality conditioners [2], [20]. Figure 2.11 is a diagram of a 2-level single-phase series-stacked inverter.

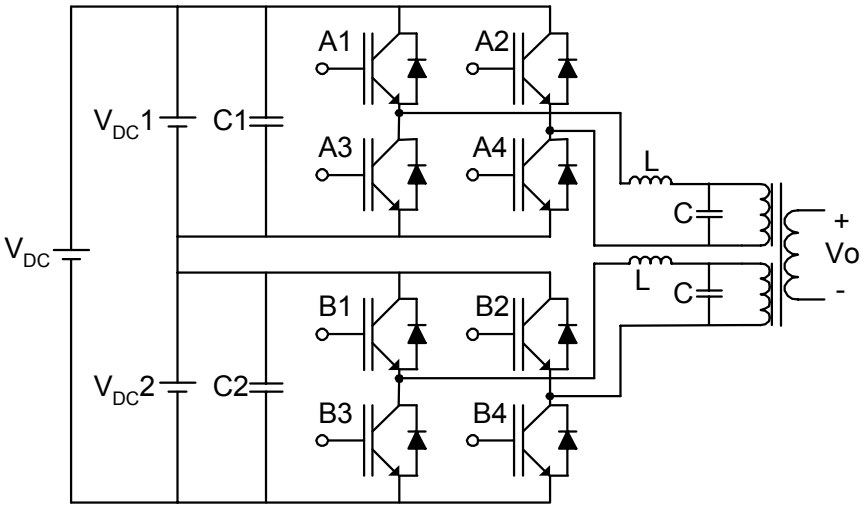

Figure 2.11 – 2-level SS inverter

The "level" in a series-stacked inverter refers to the number of cells that is stacked "on top" of each other. By connecting the DC-busses of the cells in series a high total DC-bus value can be reached with standard inverter modules. The output voltage of each cell is a low voltage output with respect to that cell but is at an offset voltage with respect to the other cells. Each cell's output is connected to the primary of an injection transformer. The primary windings for each cell are identical to each other but are electrically isolated from one another. The output waveforms from each cell are added together by the injection transformer to produce one output waveform on the secondary of the transformer. This output voltage can then be stepped up or down by adjusting the winding ratio of the injection transformer. The power delivered by the secondary is the sum of the power delivered by each cell.

Although there is no need for extra clamping diodes or capacitors, each cell of the SS inverter requires an output filter. The other multilevel inverters that where previously described only requires one output filter per phase of the inverter. The output filter of each cell must also compensate for the high harmonic content produced by the inverter of that cell.

Operation without the injection transformer is not possible. This increases the cost of the inverter due to the non standard transformer that is used. The need for a transformer makes this topology more attractive for applications such as series or shunt compensation where a transformer is already required [19], [20].

Figure 2.12 is a diagram of a 2-level 3-phase SS inverter. The 2 cells consists each of a standard 3-phase inverter. The injection transformer adds the respective phases of each cell together to form a single 3-phase output on the secondary. As with the single-phase topology the primaries are all exactly the same while the primaries associated with each cell must be isolated from each other. This non-standard 3-phase transformer together with the extra output filters increases the cost and component count of the inverter.

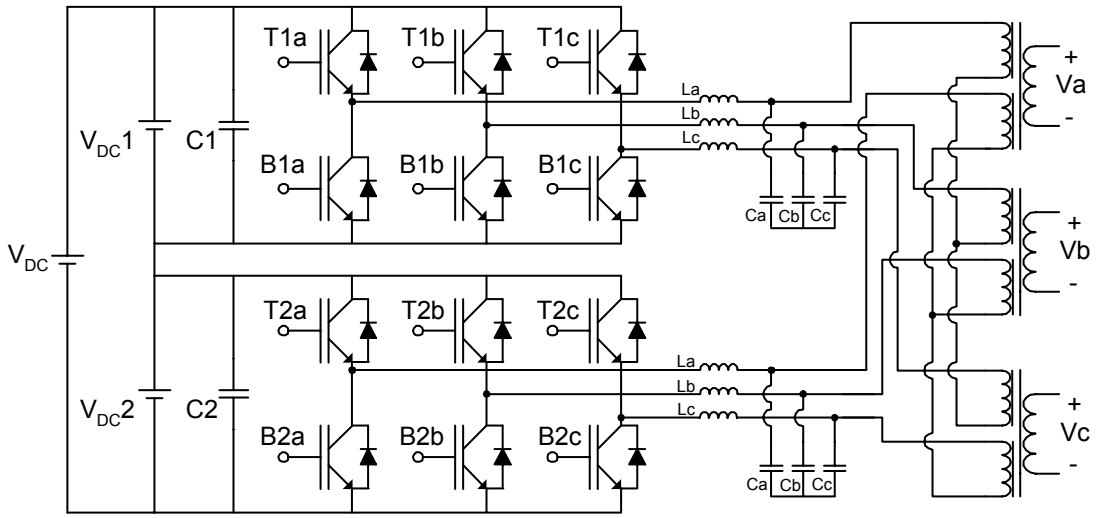

Figure 2.12 – 2-level 3-phase SS inverter

By applying interleaved switching the harmonic content of the output waveform is reduced and the effective switching frequency is increased which reduces filter size and strain on the transformer [3], [20]. As with the other multilevel topologies the balancing of the capacitor voltages is an important aspect of the control of the inverter. It is shown in [21] and [3] that the DC capacitor voltages will balance naturally if the switching frequency is chosen significantly higher than the highest frequency harmonic of its reference signal. This natural balancing mechanism simplifies the control of the inverter significantly and is a large plus point for the implementation of such an inverter. Furthermore the topology is inherently stable

and the DC capacitor voltages return to a balanced state after a perturbation from the stable state.

The total DC-bus voltage is the sum of each cell's DC-bus: $V_{DC\_tot} = V_{DC}1 + V_{DC}2 + V_{DC}3 + \ldots. V_{DC}m$, where m is the number of cells in the series-stack. Each switching element must have a blocking voltage rating of the DC-bus voltage of each cell: $V_{sw} = V_{DC\_tot}/m$. Due to the modularity of the topology it is easy to increase the total DC-bus voltage of the inverter by adding more cells to the series-stack. This does not increase the complexity of the control as it is just an expansion of the previous. This is a significant advantage over the other multilevel topologies due to the increase in the complexity of their control when the total DC-bus voltage is increased [12]. The fact that standard inverter modules are used and that the circuitry is modularised makes this an attractive option for the practical implementation of a high voltage high power inverter.

The following are some of the advantages and disadvantages of the SS multilevel inverter

Advantages

- Natural balancing mechanism and inherent stability of the topology.
- The modularity of the topology simplifies the construction and it is possible to use readily available inverter modules.
- It is easy to increase the total DC-bus voltage by adding another cell to the series-stack.
- Back-to-back operation is possible.
- Control of the system is relatively simple.

Disadvantages

- Non-standard injection transformer is required.
- High number of filter elements is required.

2.5. – Topology selection

The purpose of the following discussion is to determine which one of the 4 previously described topologies will be best suited for the implementation of the inverter in the regen-system in the Spoornet substation.

In order to facilitate the decision for the most apt topology a brief description of some of the specifications for the inverter of the regen-system is provided.

The inverter:

- Must be capable of transferring 1.5 MW of real power from DC to AC.
- Must also operate as an Active Power Filter.
- Must have a DC-bus voltage rating of 3.9 kV and must connect to the DC supply of the substation.
- Must interface with the 6-phase secondary of the supply transformer in the substation.

The full description of the inverter is provided in Chapter 3 .

The DC-bus of the inverter must connect to the DC supply of the substation. The realization of separate DC sources from this single DC supply is both costly and impractical. Therefore the Cascaded multilevel inverter topology will be disregarded in the selection process. The NPC, FLC and SS multilevel inverter topologies are evaluated.

The fact that the AC-side of the inverter must interface with a 6-phase system implies that all the topologies must utilise an injection transformer to convert the 3-phase output from the inverter to a 6-phase output. Therefore the need for an injection transformer in the SS topology will not be considered as a disadvantage at this point. The inverter itself can be extended to produce a 6-phase output but due to the increase in the complexity of the control and construction of the inverter this will not be considered.

Over the past few years IGBTs have been developed that can operate at high voltage levels. The CM600HB-90H IGBT module from Powerex has a Collector-Emitter voltage rating of 4 500 V and a collector current rating of 600 A. This IGBT module can be used to implement a standard 3-phase inverter for the regen-system. Although this will simplify the control of the inverter there are significant drawbacks to the use of high voltage IGBT modules for the implementation of the inverter required by the regen-system. The following is a list of some of the disadvantages.

- High voltage IGBTs has a lower switching frequency capability. For the CM600HB the sum of the rise, fall and delay time is 12 µs compared to the 1.418 µs of the SKIM 400 IGBT module from Semikron. This longer switching times increase the switching losses significantly. Also the APF capabilities of the inverter are reduced.

- The cost of the high voltage IGBT is significantly more than that of a lower voltage rating. Although less IGBT modules will be used in a standard 3-phase inverter the cost of the other components are also increased. Higher voltage capacitors are needed, the isolation of the inverter and output filter must be increased and the construction of the driver circuitry is more complex.

- A large dv/dt will be created by the switching of the high voltage IGBT. This will place the output filter and injection transformer under an increased amount of strain. Furthermore the large dv/dt will create a high amount of EMI that may interfere with the controller and other circuitry.

Therefore a lower voltage IGBT module was chosen for the switching element of the inverter. A SKIM 400 IGBT module from Semikron is used. This module has a maximum blocking voltage of 1 200 V. To ensure performance reliability a safe operating voltage of 800 V is chosen. Therefore the inverter must be designed so that each IGBT will not be subjected to a blocking voltage of greater than 800 V. A full description of the IGBT module is provided in section 3.2.1.

To determine the number of levels that the inverter must have, consider the blocking voltage that each topology subjects the switching elements to. For the NPC and FLC inverter the blocking voltage of each switching element is defined as

$$V_{sw} = \frac{V_{DC}}{(m-1)} \tag{2.1}$$

where V_{sw} is the blocking voltage of the switching element, V_{DC} is the value of the total DC-bus voltage of the inverter and m refers to the number of levels in the output voltage [4].

The maximum DC-bus voltage is given as 3.9 kV but for simplicity a value of 4 kV is used in the calculations. From (2.1) the required number of levels for the NPC and FLC inverter topologies is calculated.

$$\begin{aligned} m &= \frac{V_{DC}}{V_{sw}} + 1 \\ &= \frac{4\times10^3}{800} + 1 \\ &= 6 \end{aligned} \tag{2.2}$$

At least a 6-level NPC or FLC inverter is required to achieve a maximum DC-bus voltage of 4 kV.

For the SS inverter topology the blocking voltage of the switching element can be defined as

$$V_{sw} = \frac{V_{DC}}{m} \tag{2.3}$$

where m refers to the number of cells in the series-stack. The number of cells for a total DC-bus voltage of 4 kV is

$$\begin{aligned} m &= \frac{V_{DC}}{V_{sw}} \\ &= \frac{4\times10^3}{800} \\ &= 5 \end{aligned} \tag{2.4}$$

At least a 5-level SS inverter is required for a DC-bus of 4 kV.

Next the number of switching elements required by each topology is determined.

For the NPC inverter topology the number of switches per phase-arm of the inverter is defined as:

$$(m-1)\times 2 \tag{2.5}$$

Using (2.2) and (2.5) the number of switches per phase is 10, subsequently for a 3-phase inverter the total number of switches is 30.

For the FLC inverter topology there are 2 switches per cell. The number of cells per phase-arm is defined as:

$$N = m-1 \tag{2.6}$$

where N is the number of cells[6]. Using (2.2) and (2.6) the number of cells is 5. Therefore the number of switches per phase-arm is 10 and the total number of switches for a 3-phase inverter is 30.

For the SS inverter topology there are 6 switches for every cell of the series-stack. Using (2.4) the total number of switches is 30.

From the previous calculations it is seen that for all 3 of the topologies a total of 30 switching elements are required. Therefore the number of other components of the topologies plays an important role. Table 2.2 provides a summary of the component requirements per phase of the topologies for an m-level inverter.

Table 2.2 – Summary of component requirement per phase

Components	**NPC**	**FLC**	**SS**
Output filter	1	1	m
DC-bus capacitors	$(m-1)$	$(m-1)$	m
Clamping diodes	$(m-1)\times(m-2)$	0	0
Clamping capacitors	0	$\frac{(m-1)\times(m-2)}{2}$	0

Table 2.3 lists the component count for each topology to implement the 3-phase inverter for the regen-system. It is assumed that all the diodes and capacitors have the same voltage rating as that of the switching element.

Table 2.3 – Component count

Components	**6-level NPC**	**6-level FLC**	**5-level SS**
Main switching element	30	30	30
Output filter	1	1	15
DC-bus capacitors	5	5	5
Clamping diodes	60	0	0
Clamping capacitors	0	30	0

From Table 2.3 it is seen that the SS inverter topology has the least amount of components despite the need for more output filters. The fact that an injection transformer is already required for the implementation of the inverter makes the SS inverter topology the most attractive option. Also the 3-phase inverter modules are readily available on the market.

Furthermore the control of the NPC and FLC topologies becomes significantly complex when the number of levels exceeds 3. The control of a 5-level SS inverter is just an extension of that for a 3-level SS inverter and does not increase the complexity very much. Therefore the SS inverter topology is chosen to implement the inverter for the regen-system in the traction substation. Chapter 3 provides a full description of the SS inverter that is implemented in the regen-system.

Chapter 3 - Inverter

The purpose of the inverter is to convert the DC regenerated energy received from the train, into AC energy that can be injected into the Eskom supply. Furthermore the inverter is an Active Power Filter (APF) that minimizes the harmonics caused by the rectifier when the train is drawing energy from the substation. As concluded in Chapter 2 a Series-Stacked (SS) Multilevel inverter topology is used for the implementation of the inverter of the regen-system.

Chapter 3 commences with an overview of the SS inverter. Subsequently the following components of the inverter are described in more detail

- The individual cells of the inverter
- The IGBT module
- DC-bus capacitor bank
- Heatsink
- Soft-starter
- DC-dump
- DC blocking diodes
- Isolated power supply
- Filter inductor
- Controller

The methods implemented to achieve the required isolation and clearance distance in the construction of the inverter are also discussed.

3.1. - Overview of SS inverter

A 7 level SS inverter is implemented. Seven cells are connected as illustrated in Figure 3.1.

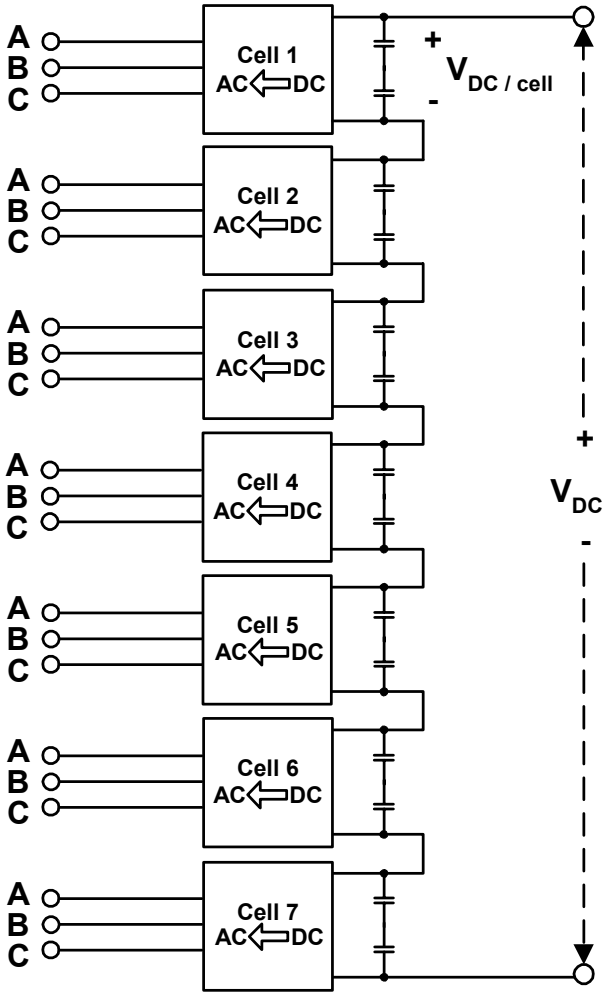

Figure 3.1 – Diagram of the SS inverter

Each of the 7 cells of the inverter is by itself a 3-phase inverter. The DC-busses of the 7 cells are connected in series. Detailed descriptions of the individual cells are provided in section 3.2. The total power of the inverter is divided between the 7 cells. Consequently each cell only has to manage $\left(1.5\times10^{6}\right)/7 = 214\,kW$. The total DC-bus voltage is also divided between the 7 cells. As mentioned in Chapter 1 the maximum DC-bus voltage of the system is 3.9 kV. This means that each cell's DC-bus only has to tolerate $\left(3.9\times10^{3}\right)/7 = 557\,V$. This is a significant reduction in the component rating. With the SS topology it is possible to make use of an interleaved switching scheme. This method of control produces a higher quality output waveform [2], [3]. The higher component count of this topology increases the complexity of the control. Instead of controlling just 3 phases of 1 inverter with this topology 21 phases must be controlled.

Due to the advances in IGBT technology over recent years an IGBT module is used for the switching component of the inverter. An IGBT provides a high power rating combined with a high switching frequency capability. The IGBT module is described in more detail in section 3.2.1.

The inverter is mounted in 4 cabinets. Each cabinet is a steel frame with the following dimensions: W = 1900mm; H = 1900mm; D = 950mm. Figure 3.2 provides a diagram of the top view of the physical layout of the inverter. Each cabinet contains 2 cells of the inverter with Cabinet-A housing cell 1 as well as the blocking diodes described in section 3.2.7.

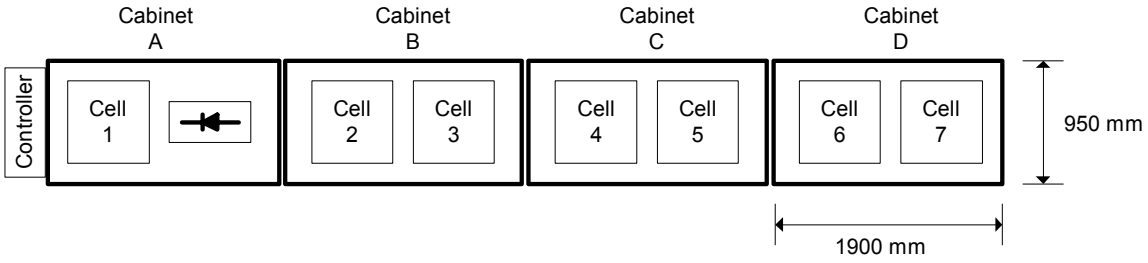

Figure 3.2 – Diagram of the top view of the inverter

Figure 3.3 provides a photograph of the inverter installed in the substation. The inverter is mounted in the top halve of the cabinet and the filter inductors at the bottom.

Figure 3.3 – Photograph of the Series-Stacked Inverter

3.2. - Description of one cell of the inverter

A diagram illustrating the 3-phase inverter of one cell is provided in Figure 3.4.

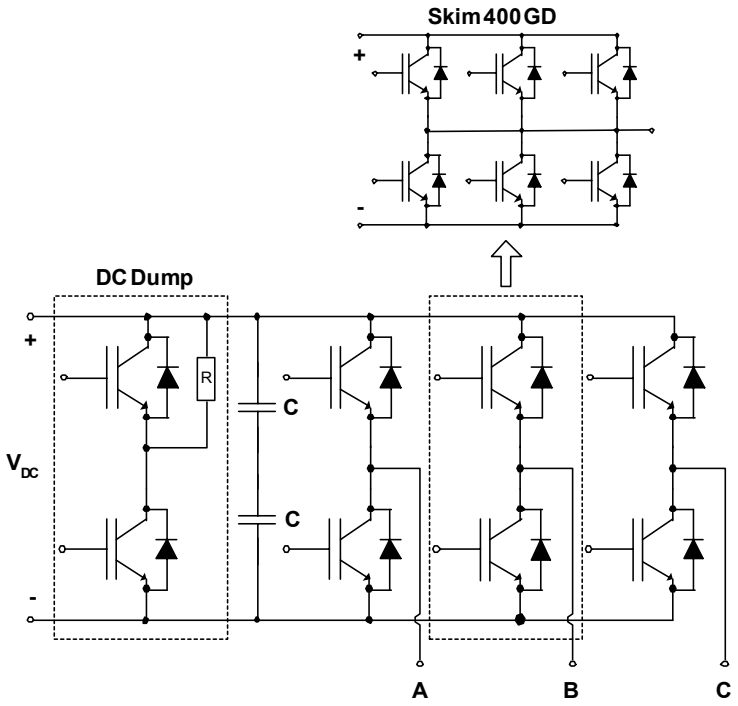

Figure 3.4 – Diagram of one cell of the inverter

Each cell consists of a capacitor bank on the DC input, a DC-dump across the capacitor bank and 3 IGBT phase-arms to produce the 3-phase AC output of the inverter. Each phase-arm consists of a 3-phase IGBT module with the phases connected in parallel. A 3-phase filter inductor is connected at the output of the inverter to reduce the harmonic content of the output waveform.

Calculating the specifications for 1 cell

Due to the natural balancing mechanism of the SS topology the total DC-bus voltage divides equally between the 7 cells [3]. Therefore only the total DC-bus voltage is controlled. As mentioned in section 1.6 the total DC-bus voltage is controlled at a value of 3.5 kV. Therefore the DC-bus voltage of each cell is

$$V_{DC/cell} = \frac{V_{total}}{7} = \frac{3.5\times10^3}{7} = 500\,V \tag{3.1}$$

The input DC current at a DC-bus voltage of 500 V is

$$I_{DC} = \frac{P_{cell}}{V_{DC/cell}} = \frac{214\times10^3}{500} = 428\,A \tag{3.2}$$

Assume the following relationship between the input and the output voltage of the inverter [35], pp.376-386.

$$V_{LL} = m_a\, V_{DC/level} \tag{3.3}$$

where m_a is the modulation index for the inverter. Taking m_a as 0.75 the line-to-line voltage at the output of the inverter for a DC-bus voltage of 500 V is

$$V_{LL} = 0.75\,\frac{V_{DC/cell}}{\sqrt{2}} = 0.75\,\frac{500}{\sqrt{2}} = 265\,V_{rms} \tag{3.4}$$

To determine the current at the output of the inverter it is assumed that the losses in the inverter is small compared to the power through the inverter and can be ignored for these calculations. Therefore the power into the inverter equals the power out of the inverter. The power in 1 phase of the output is

$$P_{\Phi} = \frac{P_{cell}}{3} = \frac{214 \times 10^3}{3} = 71\,kW \tag{3.5}$$

Unity power factor is used for the following calculations therefore the power in 1 phase is defined in terms of the line-to-neutral voltage and phase current as

$$P_{\Phi} = V_{LN}\, I_{\Phi} = \frac{V_{LL}}{\sqrt{3}}\, I_{\Phi} \tag{3.6}$$

Substituting (3.4) and (3.5) into (3.6) the output current in 1 phase is calculated

$$I_{\Phi} = \frac{\sqrt{3}\, P_{\Phi}}{V_{LL}} = \frac{\sqrt{3} \cdot 71 \times 10^3}{265} = 465\ A_{rms} \tag{3.7}$$

As shown in Figure 3.4 each phase consists of another 3 phase-arms that are connected in parallel. The collector current for one IGBT of the module is

$$I_C = \frac{I_{\Phi}}{3} = \frac{465}{3} = 155\ A_{rms} \tag{3.8}$$

Table 3.1 summarises the specifications for one cell of the inverter

Table 3.1 – Specifications for one cell

Description	**Value**
Power [kVA]	214
Nominal DC-bus voltage [kV]	500
Maximum DC-bus voltage [kV]	557
Input DC current [A] (V_{DC} = 500 V)	428
Output current per phase [A_{rms}] (V_{DC} = 500 V)	465
Collector current per IGBT [A_{rms}] (V_{DC} = 500 V)	155

Figure 3.5 is a photograph of one of the cells of the inverter.

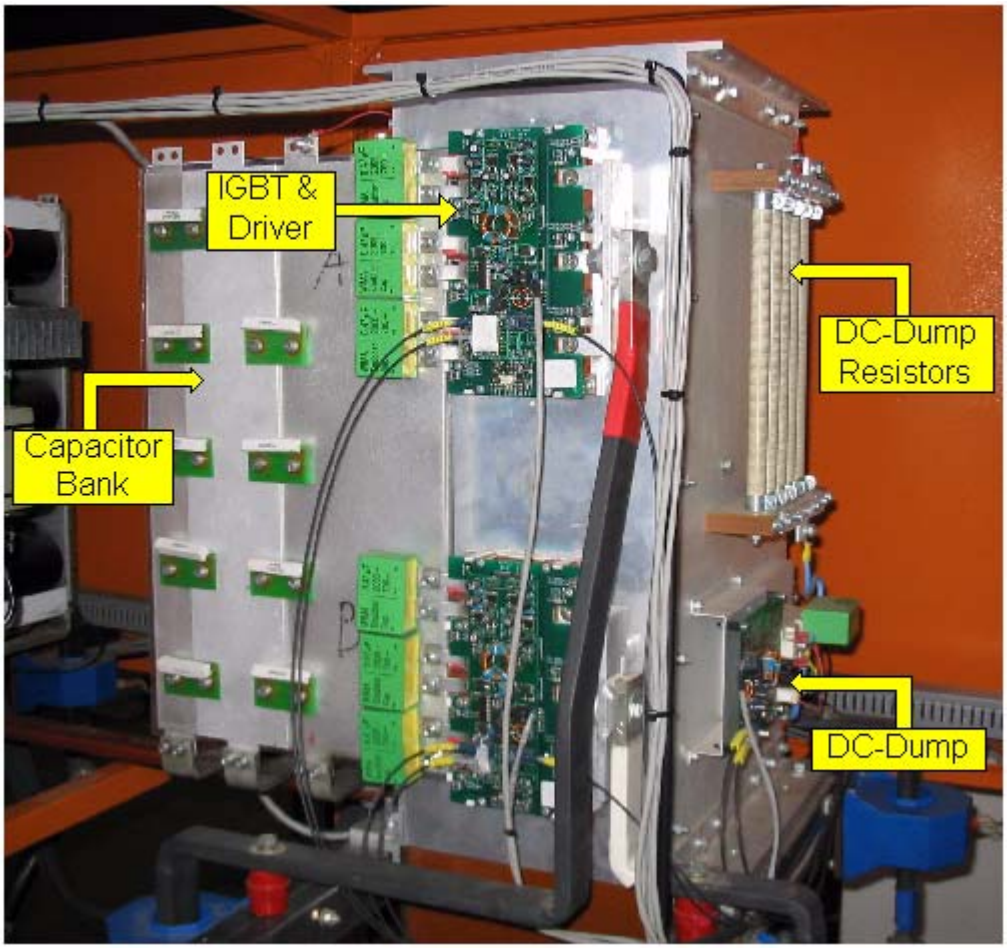

Figure 3.5 – Photograph of one cell of the inverter

3.2.1. - The IGBT module

As shown in Figure 3.4 each phase of the inverter consists of a Skim 400 GD IGBT module from Semikron. Each IGBT module in turn is a 3-phase module. The top 3 IGBTs of the module are connected in parallel to form the top half of the phase-arm and the 3 bottom IGBTs of the module are connected in parallel to form the bottom half of the phase-arm. By doing this the output current is shared by 3 IGBTs which increases the current rating of the phase. As indicated by the datasheet each IGBT of the Skim 400 module has a maximum continuous collector current rating of 270 A. By connecting the IGBTs in parallel the current rating of one phase-arm is increased to 810 A. The maximum collector emitter voltage of the IGBTs in the Skim 400 module is 1 200 V which is sufficient for the maximum DC-bus voltage of 557 V for each cell. A 0.47 μF snubber capacitor is connected between the collector of the top IGBT and the emitter of the bottom IGBT of each phase-arm of the module. This snubber capacitor protects the IGBT against over voltage spikes during the switching of the IGBT.

Driver board

The driver board that is used for the IGBT module was developed by the Power Electronics Group of the University of Stellenbosch for a previous project. The driver board is the link between the controller and the gate driver IC on the driver board. The driver board is mounted on top of the IGBT and uses the spring contact system of the IGBT module to connect to the control terminals. An HCPL-316J from Agilent Technologies is used for the gate driver. The driver board receives the gating signals from the controller via fibre-optic cables. Due to the parallel combination of the phase-arms of the module only 2 gating signals are required for each module, 1 for the top IGBTs and 1 for the bottom IGBTs. In order to protect the gate input of the top IGBT it is essential that the gating signal for the top IGBT be electrically isolated from the gating signal of the bottom IGBT. In order to achieve this isolation the power supplied to the top and bottom driver ICs have to be isolated from each other. A power supply board, which provides the isolated supply, is mounted on top of the driver board. This power supply board utilises a push-pull DC to DC converter to produce the isolated supply.

The 2 foremost causes of damage to IGBTs are over current and over temperature. Therefore 3 fault conditions are monitored by the driver board

- Over current on the top IGBT
- Over current on the bottom IGBT
- Over temperature of the module

The over current fault is implemented by the HCPL-316J driver by measuring the saturation voltage $V_{CE}(sat)$ of the IGBT. When V_{CE} exceeds a predefined voltage an over current fault is indicated and a shutdown sequence is initiated. The over current fault signal from the top and bottom IGBT is combined to form 1 over current fault signal that is transmitted via the fibre-optic cable to the controller.

The temperature sensor included in the IGBT module is used for the monitoring of the temperature of the IGBT. Although the IGBT can tolerate a junction temperature of 150 ^{0}C the over temperature protection is adjusted for a temperature of 85 ^{0}C. This is due to the placement of the sensor in the IGBT module. By the time that the sensor detects a temperature of 150 ^{0}C the junction temperature of the IGBT is much higher and thus the IGBT will be damaged. The over temperature signal is combined with the over current signal, therefore each phase of the inverter has 1 fault signal that is returned to the controller. Figure 3.6 is a photograph of the IGBT module that is mounted on the heatsink. The driver and power supply board is mounted on top of the IGBT module. On the right hand side of the module the parallel connection of the 3 outputs of the module is seen. The schematics of the driver board and isolated power supply board are provided in Appendix C.1 and C.2 respectively.

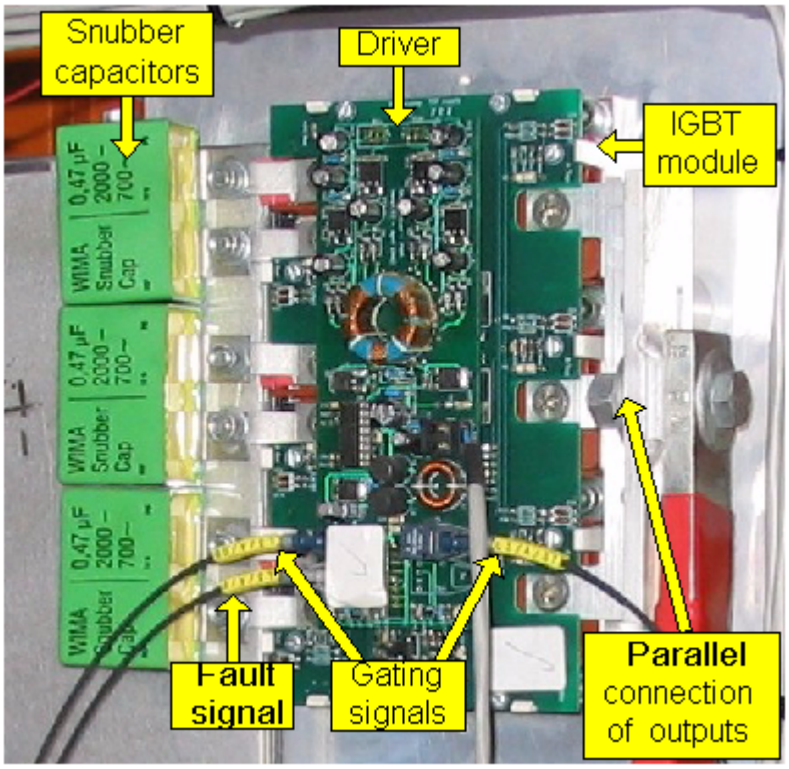

Figure 3.6 – Photograph of IGBT module and driver circuit

3.2.2. – Power loss calculations

To determine the correct heatsink for the inverter, the losses in the IGBT modules have to be determined. The 2 major contributors to the losses of the IGBT are the switching losses and the conduction losses. The total power loss in the IGBT is the sum of the switching losses and the conduction losses.

$$P_{loss} = P_{switch} + P_{cond} \tag{3.9}$$

The conduction losses are considered first.

Conduction losses

As described in [2] the duty cycles for the inverter are not produced by Sinusoidal PWM but Space Vector PWM is used. Space Vector PWM is also referred to as Space Vector Modulation (SVM) [22], [23], [24], [25], [26]. The use of SVM provides a 15% higher bus utilisation and produces less harmonic content on the output waveform [23], [25].

For SPWM a sinusoidal modulation function is compared to the triangular carrier waveform to produce the duty cycles for the inverter. For SVM the implicit modulation function is as shown in Figure 3.7, [22], [24], [25] and can be described as in (3.10). Due to the star connection on the primary of the injection transformer the calculations is done for unity power factor.

$$f(\theta) = \begin{cases} ma\cos(\theta - 30^0) & for\ \theta < 60^0\ and\ 180^0 \le \theta \le 240^0 \\ \sqrt{3}\ ma\cos(\theta) & for\ 60^0 \le \theta \le 120^0\ and\ 240^0 \le \theta \le 300^0 \\ ma\cos(\theta + 30^0) & for\ 120^0 \le \theta \le 180^0\ and\ \theta > 300^0 \end{cases} \tag{3.10}$$

This modulation function is also referred to as an ALT-REV technique [23] due to the null-vector being alternated in each switching sequence and the sequence reversed after each null-vector. This is illustrated in [2] where the switching sequences for the inverter are provided. By using this sequence the transition from one switching state to another is done by switching only one inverter leg therefore minimising the switching frequency of each inverter leg [25]. As seen in Figure 3.7 the modulation function is divided into 6 segments which corresponds to the 6 sectors of the SVM state map [23], [24], [25]. Figure 3.7 is also a representation of the line-to-neutral (phase) voltage waveform of the inverter but the resulting line-to-line voltages of the inverter are sinusoidal [23], [25].

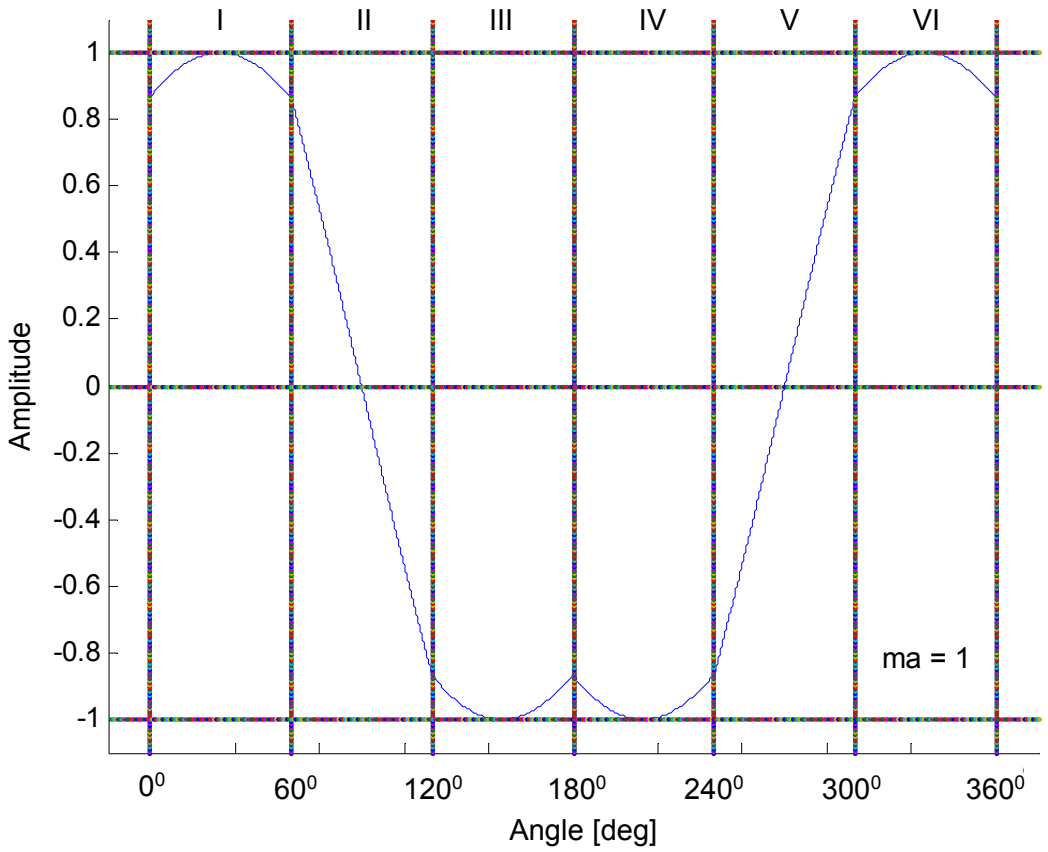

Figure 3.7 – Modulation function for SVM

In order to determine the conduction losses for one cycle of the modulation function the losses for each segment of the modulation function are calculated. Figure 3.8 presents the modulation function used for the calculation of the conduction losses. The frequency of the fundamental of the output voltage of the inverter is 50 Hz. Therefore the frequency of the modulation function is also taken as 50 Hz. The modulation index, ma, is taken as 75% for the calculations.

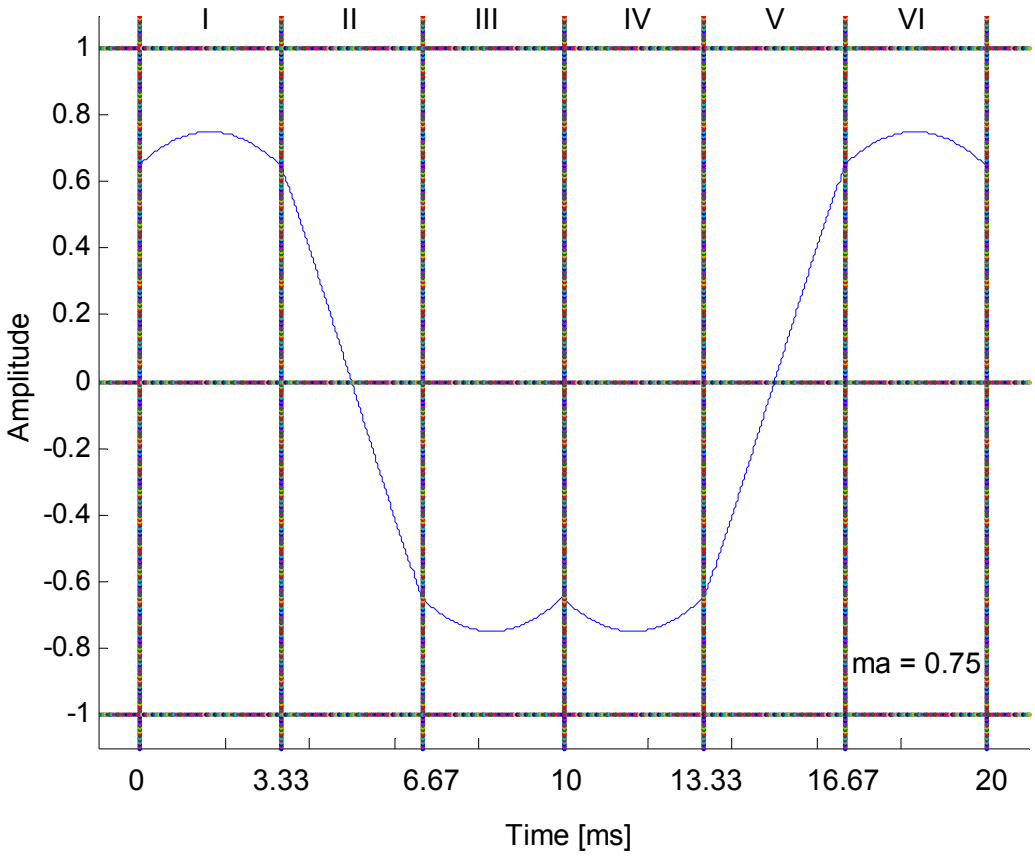

Figure 3.8 – Modulation function for the inverter

Consider one phase-arm of the inverter as shown in Figure 3.9.

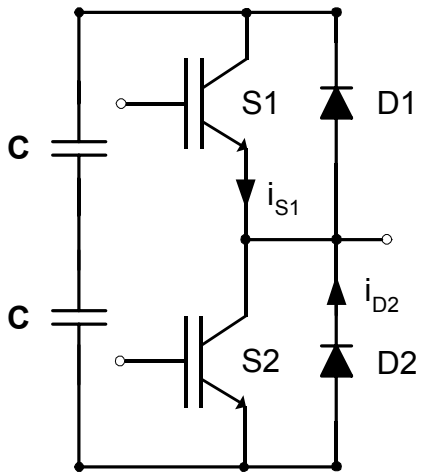

Figure 3.9 – One phase-arm

The duty cycle of the top switch S1 can be expressed as

$$d1 = \frac{1}{2}\left(1 + f\left(\omega t\right)\right) \tag{3.11}$$

where f(ωt) is the modulation function [22]. The derivation of (3.11) is provided in Appendix D.

Assume a sinusoidal output current.

$$i_L = I_O \sin\left(\omega t\right) \tag{3.12}$$

When the output current is positive the current is flowing through S1 and D2. Consider the current through S1 for the positive output current as shown in Figure 3.10. Let $t_i, 1 \le i \le N$ be the centre point of the switching periods.

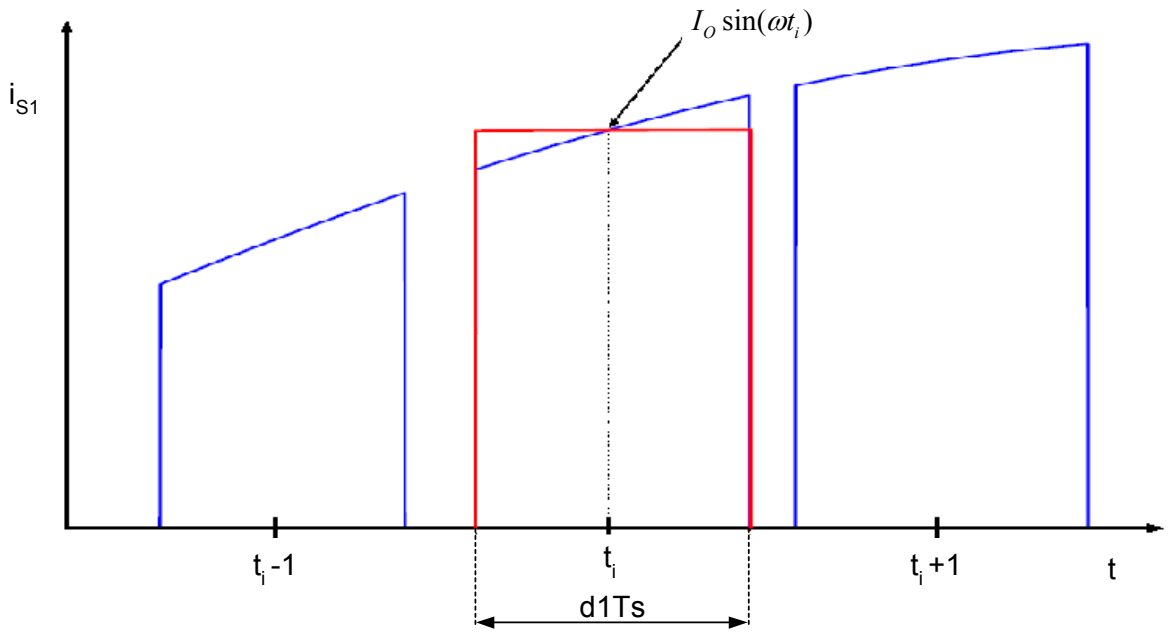

Figure 3.10 – Current through S1 [34]

The energy dissipated during the i-th switching period can be approximated as

$$\begin{aligned} E_i &\approx V_{on\_S} \cdot I_O \sin(\omega t_i) \cdot d1T_s \\ &= V_{on\_S} \cdot I_O \sin(\omega t_i) \cdot \frac{1}{2}\left(1 + f\left(\omega t_i\right)\right) T_s \end{aligned} \tag{3.13}$$

where V_{on_S} is the on state voltage of the IGBT and Ts is the switching period.

The average power dissipated during one period, T, of the fundamental of the output voltage is given by

$$\begin{aligned} P_{cond\_S} &= \frac{1}{T}\sum_{i=1}^{N} E_i \\ &= \frac{1}{T}\sum_{i=1}^{N} \frac{1}{2} V_{on\_S} \cdot I_O \sin(\omega t_i) \cdot \left(1 + f\left(\omega t_i\right)\right) T_s \\ &\approx \frac{1}{T}\int_0^t \frac{1}{2} V_{on\_S} \cdot I_O \sin(\omega t) \cdot \left(1 + f\left(\omega t\right)\right) dt \end{aligned} \tag{3.14}$$

For the losses in S1 only the positive part of the modulation function is required. Due to the symmetry of the modulation function it is only necessary to calculate the losses for half of the modulation function and then multiply the result by 2. Consider the modulation function as indicated in Figure 3.11.

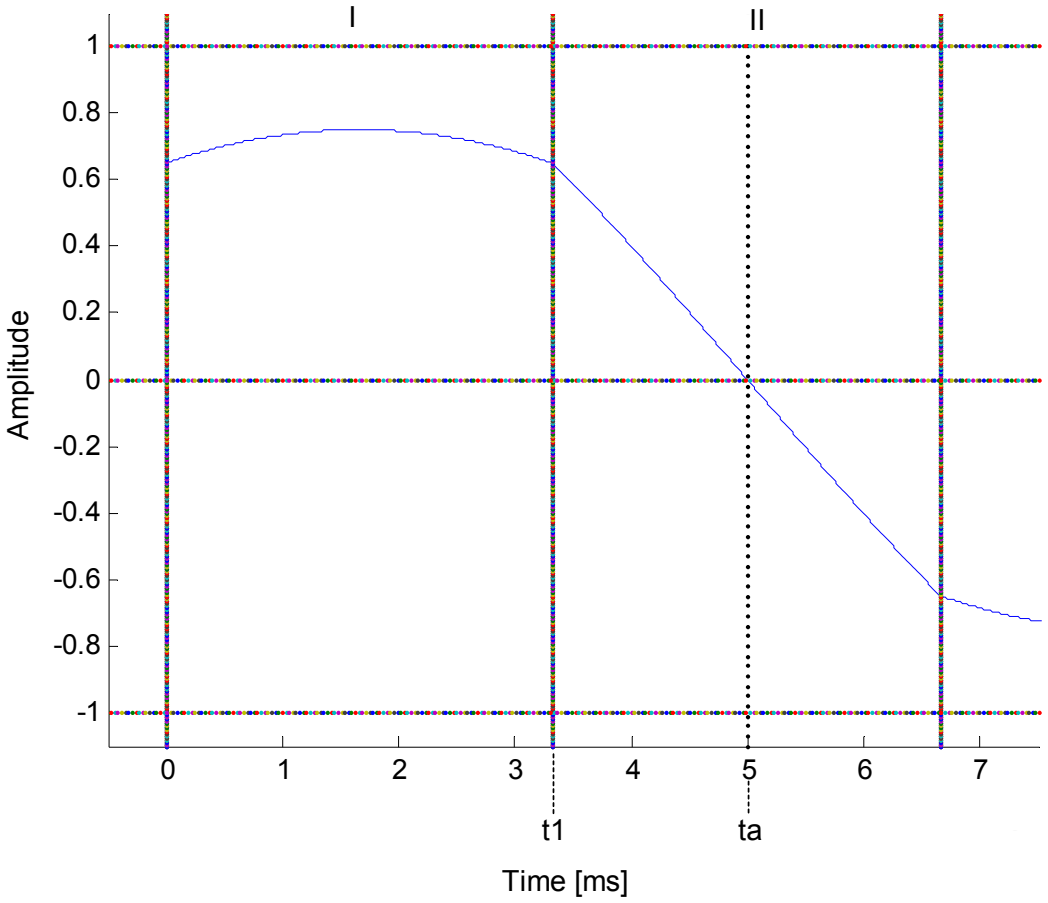

Figure 3.11 – Segment I and II of modulation function

First the conduction loss for segment I is calculated. Substituting the equation for the modulation function for segment I obtained from (3.10) into (3.14) produces

$$P_{cond\_I} = \frac{1}{T}\int_0^{t1}\frac{1}{2}V_{on\_S}\cdot I_O \sin(\omega t)\cdot\left(1+ma\cos\left(\omega\left(t-\beta\right)\right)\right)dt \tag{3.15}$$

$$= \frac{V_{on\_S}}{2T}\left[\underbrace{\int_0^{t1} I_O \sin(\omega t)dt}_{A_I} + \underbrace{\int_0^{t1} I_O ma \sin(\omega t)\cos\left(\omega\left(t-\beta\right)\right)dt}_{B_I}\right]$$

where $\beta = 1.67\ ms \Rightarrow 30^0$ and $t1 = 3.33\ ms \Rightarrow 60^0$.

Consider part A_I of (3.15).

$$\begin{aligned} A_I &\Rightarrow \int_0^{t1} I_O \sin(\omega t)dt \\ &= I_O\left(-\frac{1}{\omega}\cos(\omega t)/_0^{t1}\right) \\ &= \frac{I_O}{\omega}\left(1-\cos(\omega t1)\right) \end{aligned} \tag{3.16}$$

Next consider part B_I of (3.15).

$$\begin{aligned} B_I &\Rightarrow ma\, I_O \int_0^{t1} \sin(\omega t)\left(\cos(\omega t)\cos(\omega\beta)+\sin(\omega t)\sin(\omega\beta)\right)dt \\ &= ma\, I_O\left[\cos(\omega\beta)\int_0^{t1}\sin(\omega t)\cos(\omega t)\,dt+\sin(\omega\beta)\int_0^{t1}\sin^2(\omega t)dt\right] \\ &= ma\, I_O\left[\cos(\omega\beta)\left(\frac{-\cos(2\omega t)}{4\omega}/_0^{t1}\right)+\sin(\omega\beta)\left(\frac{t}{2}-\frac{\sin(2\omega t)}{4\omega}/_0^{t1}\right)\right] \\ &= ma\, I_O\left[\cos(\omega\beta)\left(\frac{1}{4\omega}-\frac{\cos(2\omega t1)}{4\omega}\right)+\sin(\omega\beta)\left(\frac{t1}{2}-\frac{\sin(2\omega t1)}{4\omega}\right)\right] \end{aligned} \tag{3.17}$$

Using (3.16) and (3.17) the conduction loss for segments I is

$$P_{cond\_I} = \frac{V_{on\_S}}{2T}\left(A_I + B_I\right) \tag{3.18}$$

Next the conduction loss for the positive part of segment II is calculated. Using (3.10) and (3.14) gives

$$\begin{aligned} P_{cond\_II} &= \frac{1}{T}\int_{t1}^{ta}\frac{1}{2}V_{on\_S}\cdot I_O\sin(\omega t)\cdot\left(1+\sqrt{3}\,ma\cos(\omega t)\right)dt \\ &= \frac{V_{on\_S}}{2T}\left[\underbrace{\int_{t1}^{ta} I_O\sin(\omega t)dt}_{A_{II}}+\underbrace{\int_{t1}^{ta}\sqrt{3}\,maI_O\sin(\omega t)\cos(\omega t)\,dt}_{B_{II}}\right] \end{aligned} \tag{3.19}$$

where $ta = 5\,ms \Rightarrow 90^0$.

Part A_{II} gives

$$\begin{aligned} A_{II} &\Rightarrow \int_{t1}^{ta} I_O \sin(\omega t)dt \\ &= I_O\left(-\frac{1}{\omega}\cos(\omega t)/_{t1}^{ta}\right) \\ &= \frac{I_O}{\omega}\left(\cos(\omega t1)-\cos(\omega ta)\right) \end{aligned} \tag{3.20}$$

and part B_{II} gives

$$\begin{aligned} B_{II} &\Rightarrow \sqrt{3}\,maI_O\int_{t1}^{ta}\sin(\omega t)\cos(\omega t)\,dt \\ &= \sqrt{3}\,maI_O\left[\frac{-\cos(2\omega t)}{4\omega}/_{t1}^{ta}\right] \\ &= \frac{\sqrt{3}\,maI_O}{4\omega}\left(\cos(2\omega t1)-\cos(2\omega ta)\right) \end{aligned} \tag{3.21}$$

Therefore the conduction loss for the positive part of segment II is

$$P_{cond\_II} = \frac{V_{on\_S}}{2T}\left(A_{II}+B_{II}\right) \tag{3.22}$$

The total average conduction losses for the switch S1 is

$$P_{cond\_S} = 2\left(P_{cond\_I}+P_{cond\_II}\right) \tag{3.23}$$

For that part of the duty cycle when S1 is switched off, the positive output current is flowing through diode D2. The average conduction loss for the diode D2 is as follows

$$P_{cond\_D} = V_{on\_D}\,I_{D2} \tag{3.24}$$

where V_{on_D} is the on state voltage of the diode and I_{D2} is the average current through the diode. The current I_{D2} can be defined as the difference between the average output current and the average current through S1.

$$I_{D2} = I_L - I_{S1} \tag{3.25}$$

The average output current for the positive part of the modulation function is

$$\begin{aligned} I_L &= 2\left(\frac{1}{T}\int_0^{ta} I_O \sin(\omega t)\,dt\right) \\ &= \frac{2I_O}{T}\left(\frac{-\cos(\omega t)}{\omega}\Big/_0^{ta}\right) \\ &= \frac{2I_O}{T\omega}\left(1-\cos(\omega ta)\right) \end{aligned} \tag{3.26}$$

The average current through S1 is the conduction loss divided by V_{on_S}.

$$I_{S1} = \frac{P_{cond\_S}}{V_{on\_S}} \tag{3.27}$$

Therefore the conduction loss for diode D2 is

$$P_{cond\_D} = V_{on\_D}\left(\frac{2I_O}{T\omega}\left(1-\cos(\omega ta)\right) - \frac{P_{cond\_S}}{V_{on\_S}}\right) \tag{3.28}$$

The total conduction loss for the positive part of the modulation function is

$$P_{cond} = P_{cond\_S} + P_{cond\_D} \tag{3.29}$$

From Table 3.1 it is seen that the average current through the IGBT is specified as 155 A_{rms} which has a peak value of $\sqrt{2}\cdot 155 = 220\,A$. From the datasheets of the IGBT module it is seen that the IGBT and the diode has the same on state voltage, V_{on} = 2.3 V. The following values are substituted into (3.29).

$$\begin{aligned} f &= 50\,Hz \\ \omega &= 2\pi f \\ ma &= 0.75 \\ I_O &= 220A \\ V_{on\_S} &= V_{on\_D} = 2.3V \end{aligned} \tag{3.30}$$

The total average conduction losses are

$$\begin{aligned} P_{cond} &= P_{cond\_S} + P_{cond\_D} \\ &= 122.5 + 38.57 \\ &= 161.07\,W \end{aligned} \tag{3.31}$$

The Matlab code for the calculation of the conduction losses and plotting of the modulation function is provided in appendix B.1.

The switching losses are calculated next.

Switching losses

The energy dissipated during the turn-on and turn-off time of the IGBT can be approximated with the following equation [28], p21

$$E_{switch} = \frac{1}{2} V_{CE}\, I_C \left(t_{on} + t_{off}\right) \tag{3.32}$$

where I_C refers to a constant collector current and V_{CE} is the collector emitter voltage of the IGBT.

As mentioned in (3.12) a sinusoidal load current is assumed. Therefore (3.32) must be adjusted to accommodate the sinusoidal current which results in

$$E_{switch} = \frac{1}{2} V_{CE}\, I_O \sin\left(\omega t\right) \left(t_{on} + t_{off}\right) \tag{3.33}$$

Using Figure 3.10, the energy dissipated in switch S1 per switching cycle is defined as

$$E_{switch\_i} = \frac{1}{2} V_{CE}\ I_O \sin(\omega t_i)\left(t_{on} + t_{off}\right) \tag{3.34}$$

Therefore the average switching losses for one period of the fundamental of the output, is defined as [34]

$$\begin{aligned} P_{switch} &= \frac{1}{T}\sum_{i=1}^{N}\frac{1}{2}V_{CE}\cdot I_O \sin(\omega t_i)\cdot\left(t_{on}+t_{off}\right) \\ &= \frac{1}{T\,T_S}\cdot\frac{1}{2}V_{CE}I_O\left(t_{on}+t_{off}\right)\sum_{i=1}^{N}\sin(\omega t_i)T_S \\ &\approx \frac{1}{T\,T_S}\cdot\frac{1}{2}V_{CE}I_O\left(t_{on}+t_{off}\right)\int_0^{\frac{T}{2}}\sin(\omega t)dt \\ &= \frac{1}{T\,T_S}\cdot\frac{1}{2}V_{CE}I_O\left(t_{on}+t_{off}\right)\cdot\frac{T}{\pi} \\ &= \frac{f_S}{\pi}\cdot\frac{1}{2}V_{CE}I_O\left(t_{on}+t_{off}\right) \end{aligned} \tag{3.35}$$

Using (3.32), equation (3.35) is rewritten as

$$P_{switch} = \frac{f_S}{\pi}\cdot\left(E_{on}+E_{off}\right) \tag{3.36}$$

where f_S is the switching frequency of 5 kHz.

The following data is acquired from the data sheets of the Skim 400 IGBT module. The specifications take into account the energy dissipated in the diodes of the module as well.

Table 3.2 – Switching specifications of Skim 400 IGBT

Conditions	**Description**	**Symbol**	**Value**
I_C = 300 A V_{CE} = 600 V	Rise time	t_c(on)	68 ns
	Fall time	t_c(off)	75 ns
	Energy dissipated during turn-on	E_{ON}	32 mJ
	Energy dissipated during turn-off	E_{OFF}	30 mJ
	IGBT on-state voltage	V_{ON}	2.3 V

From (3.32) it is seen that the energy dissipated in the switch is directly proportional to the current and voltage. In Table 3.2 the energy E_{ON} and E_{OFF} is specified for a continuous collector current of 300 A and a collector emitter voltage of 600 V. In Table 3.1 the calculated collector current is specified as $I_C = 155\ A_{rms}$ and the voltage $V_{CE} = V_{DC} = 500\,V$. Therefore the energy dissipation specified on the datasheets, listed inTable 3.2, must be scaled for these values. The current is reduced by a factor

$$\begin{aligned} \alpha &= \frac{\sqrt{2}\cdot 155}{300} \\ &= 0.73 \end{aligned} \tag{3.37}$$

and the voltage by a factor

$$\begin{aligned} \beta &= \frac{500}{600} \\ &= 0.83 \end{aligned} \tag{3.38}$$

Therefore the energy dissipated during switching is

$$\begin{aligned} E_{switch} &= \left(E_{ON} + E_{OFF}\right)\cdot\alpha\cdot\beta \\ &= \left(32\times10^{-3} + 30\times10^{-3}\right)\cdot 0.73\cdot 0.83 \\ &= 37.57\times10^{-3}\ J \end{aligned} \tag{3.39}$$

From (3.36) the switching losses are now calculated

$$\begin{aligned} P_{switch} &= \frac{f_S}{\pi}\cdot E_{switch} \\ &= \frac{5\times10^{3}}{\pi}\cdot 37.57\times10^{-3} \\ &= 60\,W \end{aligned} \tag{3.40}$$

Total losses

From (3.9) the total losses are calculated as

$$\begin{aligned} P_{loss} &= P_{switch} + P_{cond} \\ &= 60 + 161 \\ &= 221\,W \end{aligned} \tag{3.41}$$

The appropriate heatsink for the IGBT module can now be determined.

3.2.3. – Heatsink for the IGBT modules

Consider Figure 3.12 as the equivalent electrical diagram of the thermal resistance of the IGBT module and the heatsink. The junction temperature of the IGBT is defined as

$$T_j = P_{loss}\ R_{thjh} + P_{loss}\ R_{thha} + T_{amb} \tag{3.42}$$

where

T_j = junction temperature of IGBT

R_{thjh} = thermal resistance between the junction and the heatsink

T_h = temperature of the heatsink

R_{thha} = thermal resistance between the heatsink and the ambient

T_{amb} = ambient temperature

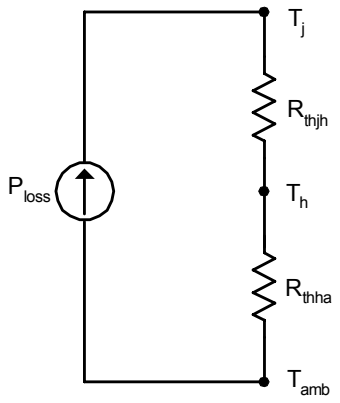

Figure 3.12 – Equivalent electrical diagram of the thermal resistance

The heatsink used for the inverter has the same parameters as the P16 heatsink from Semikron. Each IGBT module consists of 6 IGBT and diode pairs. The losses for the IGBT module were calculated for one IGBT and diode pair. The specifications on the datasheet of the heatsink takes into account that there are 6 pairs therefore it is only necessary to do the calculations for one pair. The thermal resistance between the heatsink and the ambient with forced air cooling is, $R_{thha} = 0.024\ ^0C/W$. For the IGBT the thermal resistance between the junction and the heatsink is $R_{thjh} = 0.13\ ^0C/W$. The maximum ambient temperature is specified as $T_{amb} = 50\ ^0C$ [1]. Substituting these values into (3.42) the junction temperature of the IGBT is calculated for the total average power loss of 221 W as calculated in (3.41).

$$\begin{aligned} T_j &= P_{loss}\left(R_{thjh} + R_{thha}\right) + T_{amb} \\ &= 221\left(0.13 + 0.024\right) + 50 \\ &= 84\ ^0C \end{aligned} \tag{3.43}$$

The maximum junction temperature of the IGBT is specified as 150 ^{0}C. Therefore it is concluded that the heatsink is suitable for the cooling of the IGBT modules.

Figure 3.13 provides a diagram of the heatsink that is used for the inverter. It consists of 4 P16 heatsinks that is connected to form one large heatsink. The IGBT modules are mounted so that each module has the benefit of the area of one P16 segment.

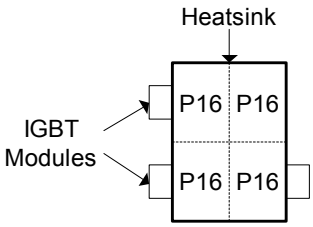

Figure 3.13 – Diagram of the heatsink for the IGBT modules

Mounting of the heatsink

The isolation of the IGBT with respect to the heatsink is given as 2.5 kV_{rms} AC according to the datasheets. The frame of the inverter cabinet is connected to the DC negative terminal of the DC-bus. The offset voltage of the cells is more than the isolation of the IGBT module. Therefore the heatsinks can not be mounted directly onto the frame. To ensure that the heatsink does not float at an arbitrary voltage, each cell's heatsink is connected to that cell's positive DC-bus terminal. Fibre-glass tubing is used for the mounting of the heatsinks in the cabinet. The tubing electrically isolates the heatsink from the frame and also provides the specified 10.5 kV_{rms} AC isolation. Figure 3.14 is a photograph of the heatsink that is mounted on the fibre-glass tubing.

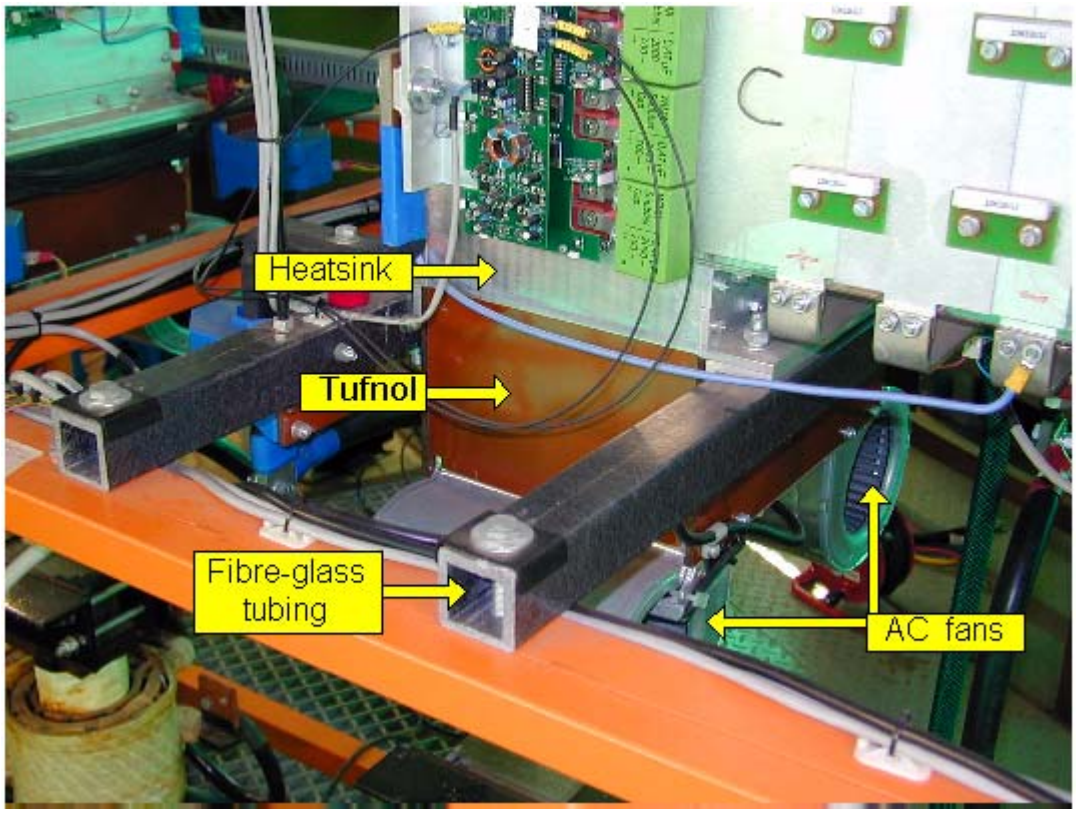

Figure 3.14 – Photograph of the mounting of the heatsinks

The heatsinks are forced air cooled with the aid of 2 AC fans mounted at the bottom of the heatsink. The fans are powered from the 230 V AC supply of the substation therefore the fans must also be electrically isolated from the heatsink. A tufnol section is inserted between the heatsink and the fan as shown in Figure 3.14 to provide the isolation. The heatsink is also mounted in such a manner as to achieve the specified clearance of 75 mm between the high voltage components and the frame of the inverter cabinet.

3.2.4. - Capacitor bank

The capacitor used for the DC-bus is a 450 V, 4.7 mF capacitor from Semikron. The capacitor bank of each cell of the inverter comprises of 20 of these capacitors. Two of the capacitors are connected in series between the positive and negative terminal as shown in Figure 3.4. This series connection yields a capacitor value of $\left(4.7\times10^{-3}\right)/2 = 2.35\,mF$. Ten of these series connected capacitors are connected in parallel as shown in Figure 3.15 producing a total DC-bus capacitance of 23.5 mF for each cell. The DC-busses of the cells are connected in series. This produces a total DC-bus capacitance of $\left(23.5\times10^{-3}\right)/7 = 3.36\,mF$ for the SS inverter.

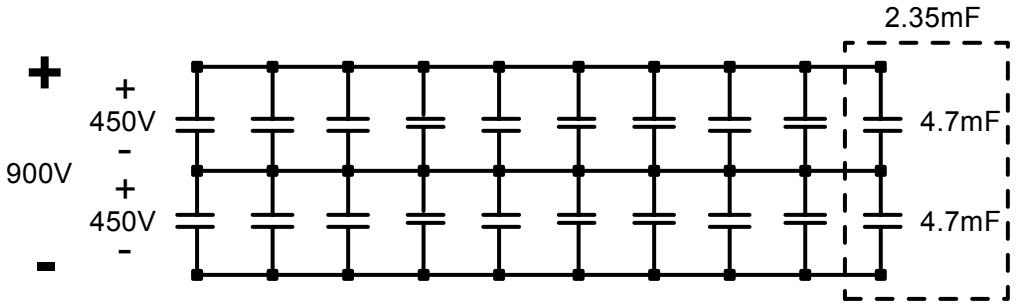

Figure 3.15 – Diagram of the capacitor bank of one cell

The series connection of the capacitors can tolerate a maximum voltage of 900 V. This is sufficient for the maximum DC-bus voltage of 557 V. To ensure that the voltage divides equally between the 2 capacitors connected in series a 10 W, 33 kΩ resistor is connected in parallel with each capacitor. The voltage measurement of each cell's DC-bus is used for the implementation of the over voltage protection. When the controller detects a DC-bus voltage exceeding 600 V the regen-system is shut down. Figure 3.16 provides a photograph of the capacitor bank of one cell of the inverter.

Figure 3.16 – Photograph of the Capacitor bank of one cell

3.2.5. - Soft-Starter

The soft-starter is connected in parallel with the DC-breaker as shown in Figure 3.17.

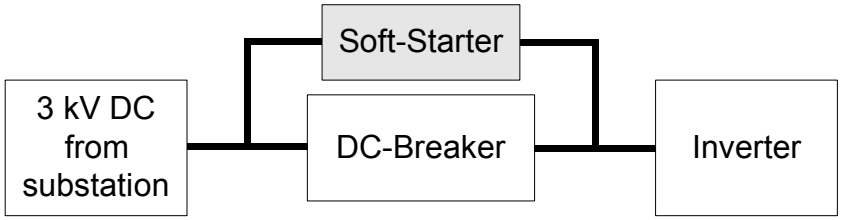

Figure 3.17 – Connection of the Soft-Starter

At the start-up of the regen-system the capacitor bank of the DC-bus is discharged. If the DC-bus of the inverter were to be connected directly to the 3 kV DC supply of the substation the inrush currents will damage the capacitor bank and may cause the DC-breaker to trip. To protect the capacitors at start-up a soft-starter is connected between the DC supply and the inverter. The capacitor bank is slowly charged through the soft-start resistor until it reaches

the same potential as that of the DC supply of the substation. A diagram of the soft-starter is provided in Figure 3.18.

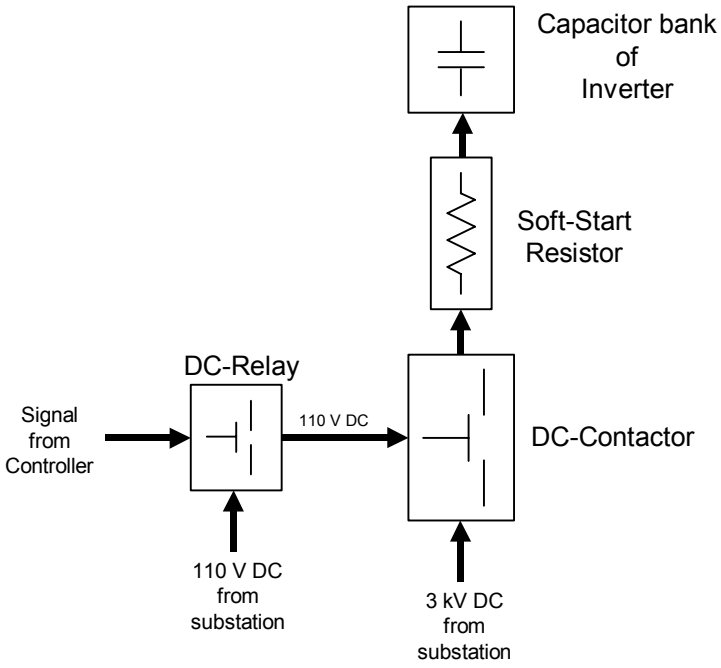

Figure 3.18 – Diagram of the Soft-Starter

A Microelettrica LTHH01001 DC-contactor is connected is series with the soft-start resistor. This DC-contactor has a voltage rating of 4 kV and a current rating of 120 A. When the DC-contactor is closed the capacitor bank is charged through the soft-start resistor. The coil voltage of the DC-contactor is supplied by the 110 V DC supply of the substation. The DC-contactor is controlled with a Kilovac EV200 DC-relay from CII Technologies. A signal from the controller closes the DC-relay which in turn connects the 110 V DC to the coil of the DC-contactor. The contactor then closes and the DC-bus is charged. When the DC-bus voltage equals that of the substation, the DC-breaker closes and the soft-starter is opened. A photograph of the soft-starter is provided in Figure 3.19.

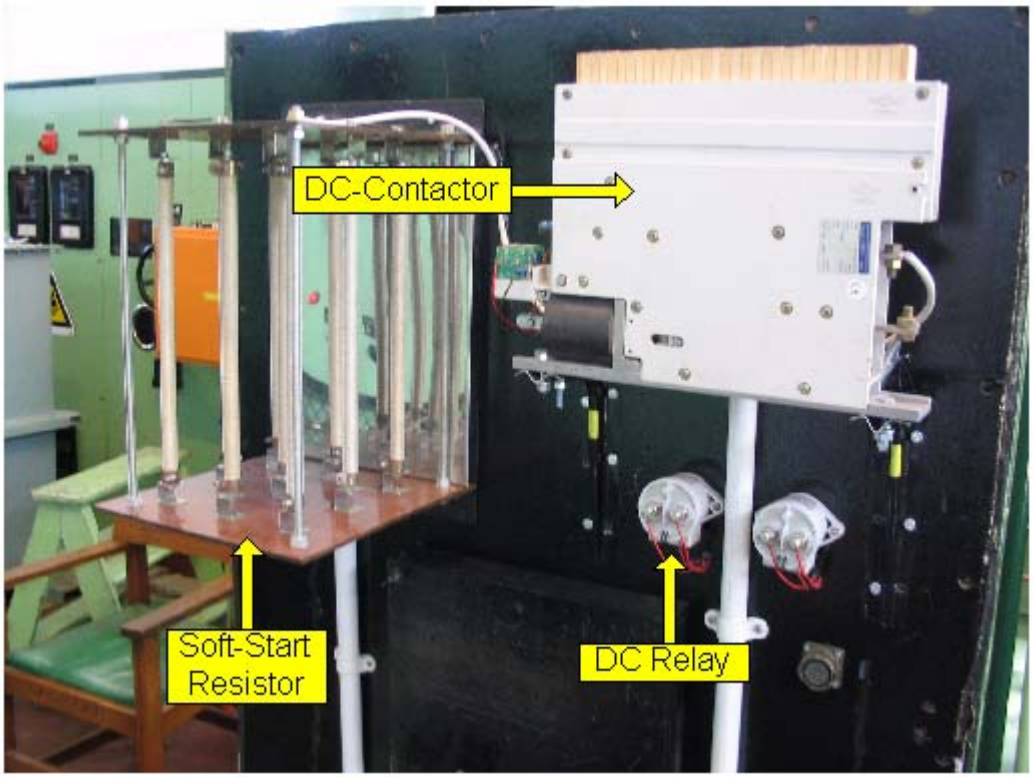

Figure 3.19 – Photograph of the Soft-Starter

The soft-start resistor is comprised of nine 1 kW resistors connected in series producing a 405 Ω soft-start resistor. The initial current through the resistor at start-up is

$$I_{initial} = \frac{V_{DC}}{R} = \frac{3\times10^3}{405} = 7.4\ A \tag{3.44}$$

Therefore the initial power dissipated in the soft-start resistor is

$$P_{initial} = I^2\ R = 7.4^2 \cdot 405 = 22\ kW \tag{3.45}$$

This is much higher than the rating of the resistors, but it is only for a small time period. As mentioned previously the total DC-bus capacitance of the inverter is 3.36 mF.

The time constant for the soft-starter is

$$\begin{aligned}\tau &= R\,C \\ &= 400 \cdot 3.36 \times 10^{-3} \\ &= 1.3\ s\end{aligned} \tag{3.46}$$

For this short time the resistors are able to endure the higher power rating. Assuming that the capacitors will be fully charged after 5 time constants, the soft-start time is estimated as

$$\begin{aligned}5\,\tau &= 5 \cdot 1.3 \\ &= 6.5\ s\end{aligned} \tag{3.47}$$

Figure 3.20 shows an oscillograph of the soft-start sequence.

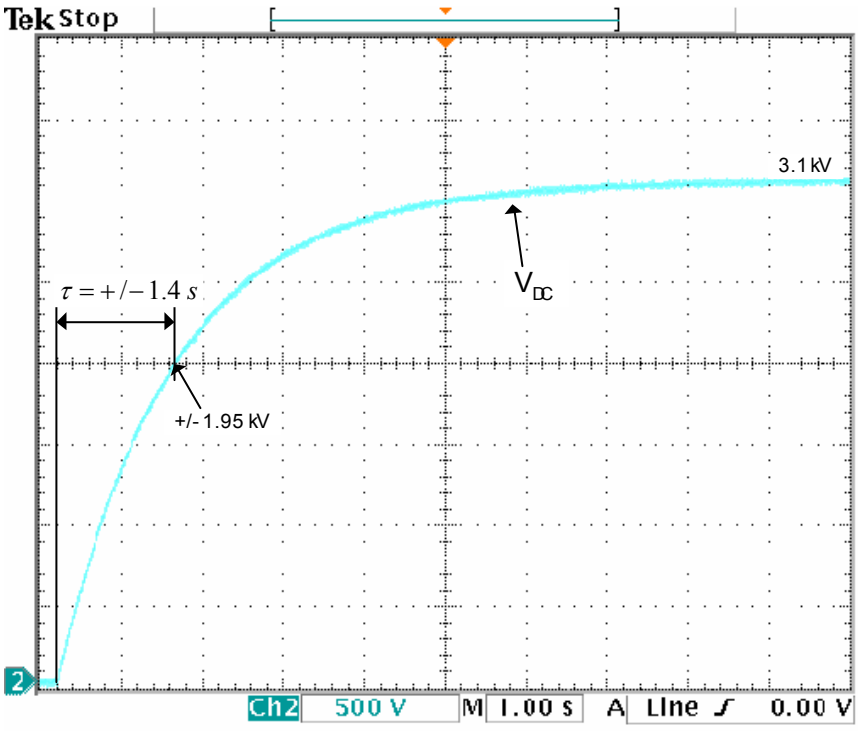

Figure 3.20 – Oscillograph of the soft-start sequence

One time constant is defined as the time that it takes the capacitor to reach 63% of the final value [29], p257. From Figure 3.20 it is seen that 63% of the final value is 1.95 kV. It takes approximately 1.4 s for the capacitor voltage to reach this value which corresponds with the

calculated time constant in (3.46). Figure 3.20 also shows that it takes roughly 6.8s for the voltage to reach its final value. This is near to the estimated time of 6.5s.

3.2.6. - DC-Dump

The DC-dump is necessary to discharge the DC-bus capacitors when the system is switched off. The capacitor has a very slow self discharge rate. This poses a danger when maintenance has to be done on the system. The DC-dump ensures that the capacitors are discharged and safe to work with. Each cell has its own DC-dump components connected across the capacitor bank as shown in Figure 3.21.

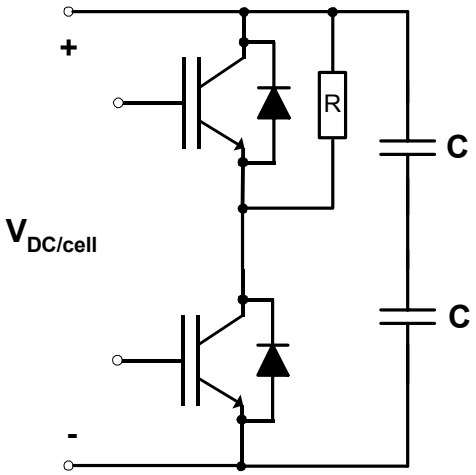

Figure 3.21 – Diagram of the DC-dump of one cell

An SKM 100GB 123D IGBT module from Semikron is used for the switching component of the DC-dump. Only the bottom IGBT of the module is used in the DC-dump. The top IGBT is disabled by shorting the gate terminal to the emitter. Five 53 Ω, 1 kW resistors are connected in parallel to form a 10.6 Ω, 5 kW DC-dump resistor. This resistor is connected between the positive terminal of the DC-bus and the collector of the bottom IGBT as shown in Figure 3.21. When the bottom IGBT is switched on the capacitors are discharged through the resistors. The initial current through the IGBT is calculated as follows

$$\begin{aligned} I_{initial} &= \frac{V_{initial}}{R} \\ &= \frac{500}{10.6} \\ &= 47.2\ A \end{aligned} \tag{3.48}$$

This current is well within the capabilities of the IGBT. The initial power dissipated in the dump resistor is

$$\begin{aligned} P_{initial} &= I^2{}_{initial}\, R \\ &= (47.2)^2 \cdot 10.6 \\ &= 23.6\, kW \end{aligned} \tag{3.49}$$

This is much higher than the rating of the resistors but it is only for a short period of time. The time constant for the DC-dump is

$$\begin{aligned} \tau &= R\, C \\ &= 10.6 \cdot 23.5 \times 10^{-3} \\ &= 249\, ms \end{aligned} \tag{3.50}$$

It is assumed that the capacitor bank will be fully discharged after 5 time constants

$$\begin{aligned} 5\,\tau &= 5 \cdot 249 \times 10^{-3} \\ &= 1.25\, s \end{aligned} \tag{3.51}$$

The dump resistors are capable of enduring the higher power for this short time period. An oscillograph of the DC-dump sequence is provided in Figure 3.22.

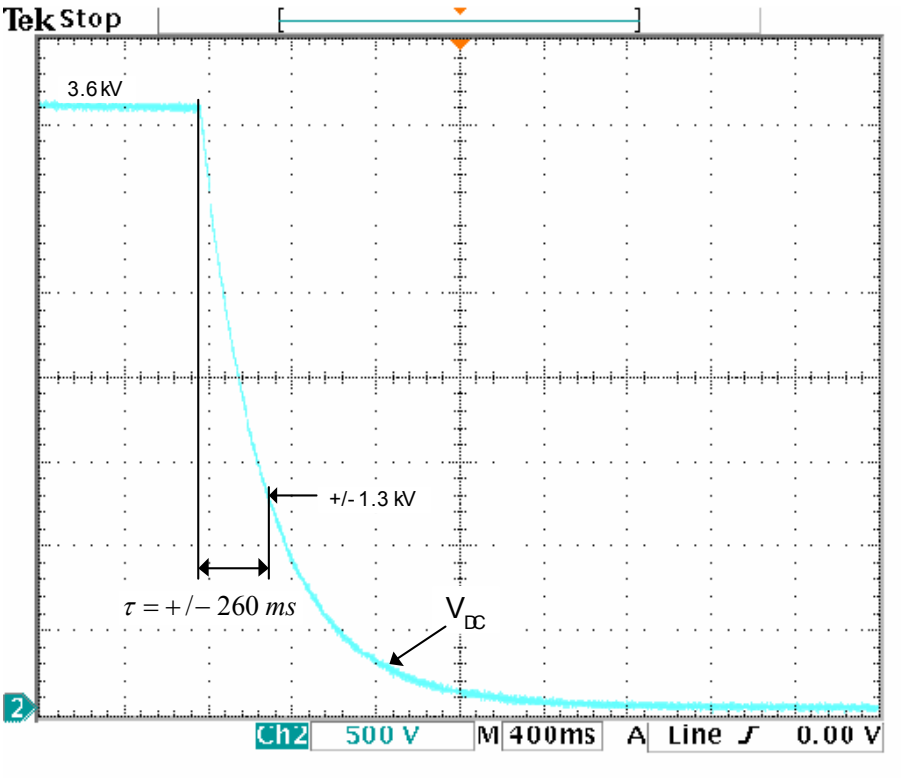

Figure 3.22 – Oscillograph of the DC-dump sequence

The time constant for the voltage decay of a capacitor is defined as the time it takes for the capacitor voltage to reach 37% of the initial value. From Figure 3.22 it is seen that 37% of the initial voltage is 1.3 kV and it takes approximately 260 ms for the voltage to reach this value. The DC-bus is discharged after roughly 1.6 s which is close to the estimated time of 1.25 s. A photograph of the DC-dump of one cell is provided in Figure 3.23.

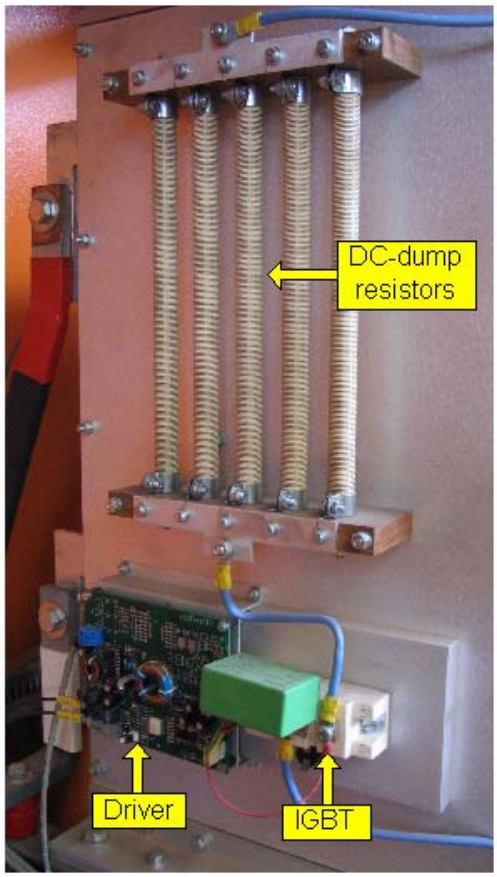

Figure 3.23 – Photograph of the DC-dump of one cell

3.2.7. - DC blocking diodes

Observations have shown that the DC traction supply of the substation varies between 3.3 kV under no-load and 3 kV under load. The DC-bus of the inverter is regulated at a higher voltage of 3.5 kV therefore the DC-bus of the inverter must be prohibited from discharging to the DC supply of the substation. Diodes are connected in series between the DC of the substation and the DC-bus of the inverter as shown in Figure 3.24. These diodes block the flow of energy from the DC-bus of the inverter to the substation. The diodes also protect the capacitor bank from over current damage if a ground fault occurs on the DC input of the inverter.

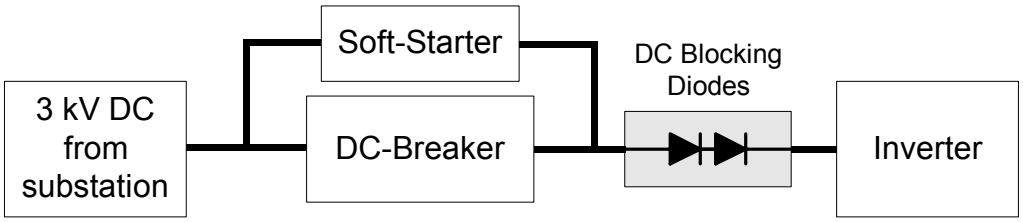

Figure 3.24 – Diagram of the DC blocking diodes

The diodes must be able to withstand a maximum reverse voltage of 3.9 kV and a forward continuous current of 428 A. Two SKKE 600/20 H4 diodes from Semikron are connected in series. Each diode can withstand a peak reverse voltage of 2 kV. Therefore the total blocking voltage of the diodes is 4 kV. The diodes have a sufficient continuous current rating of 930 A_{rms}.

The reverse voltage across the diode is dependant on the reverse resistance of the diode. Each diode has a maximum reverse current of 20 mA. Therefore the maximum reverse resistance of the diode is

$$\begin{aligned} R_r &= \frac{V_r}{I_r} \\ &= \frac{2\times10^3}{20\times10^{-3}} \\ &= 100\ k\Omega \end{aligned} \tag{3.52}$$

The reverse resistance may vary from diode to diode. This will cause the voltage across the diodes not to divide equally and one or both of the diodes may be damaged. To ensure that the reverse voltage divides equally between the 2 diodes a sharing resistor is connected in parallel with each diode. For calculation purposes the reverse resistance of the diodes and the sharing resistors are drawn as shown in Figure 3.25 where R_r1 and R_r2 are the reverse resistance of the diodes and R_a and R_b are the sharing resistors. A reverse voltage of 4 kV is used for the calculation of the values of the sharing resistors.

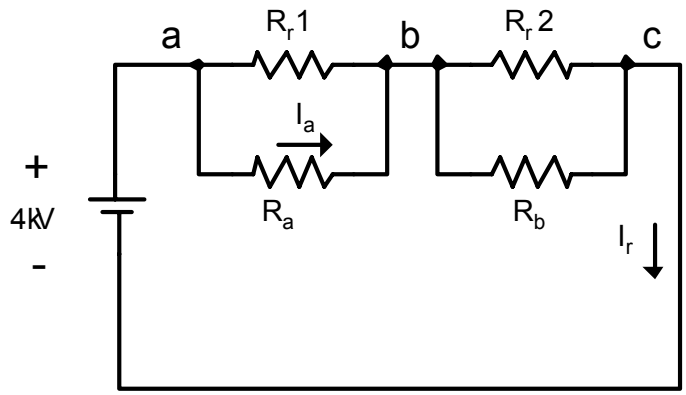

Figure 3.25 – Diagram for the calculation of the voltage sharing resistors

The value of the sharing resistors, R_a and R_b, is known and fixed, therefore it is desired that the voltage sharing between the diodes be dependent on the sharing resistors and not the reverse resistance of the diodes. The sharing resistors must have a significantly smaller value than that of the reverse resistance of the diodes. This will ensure that more current will flow through the sharing resistors and subsequently determine the voltage across the parallel combination of the sharing resistor and the reverse resistance. The parallel resistor combinations R_{ab} and R_{bc} between points **ab** and **bc** shown in Figure 3.25 are defined as

$$R_{ab} = R_a \| R_r 1 = \frac{R_a \, R_r 1}{R_a + R_r 1} \tag{3.53}$$

and R_{bc}

$$R_{bc} = R_b \| R_r 2 = \frac{R_b \, R_r 2}{R_b + R_r 2} \tag{3.54}$$

The reverse voltage across the diodes V_{ab} and V_{bc} is defined as

$$V_{ab} = \frac{R_{ab}}{R_{ab} + R_{bc}} \cdot 4 \times 10^3 \tag{3.55}$$

and V_{bc}

$$V_{bc} = \frac{R_{bc}}{R_{ab} + R_{bc}} \cdot 4 \times 10^3 \tag{3.56}$$

A value of 10 kΩ was chosen for the sharing resistors. Substituting the resistor values into (3.53) and (3.54) and assuming that the reverse resistance is the same for both the diodes, the parallel resistance is

$$R_{ab} = R_{bc} = \frac{10\times10^3 \cdot 100\times10^3}{10\times10^3 + 100\times10^3} \tag{3.57}$$
$$= \frac{1\times10^9}{110\times10^3}$$
$$= 9.09\ k\Omega$$

The total resistance between points **a** and **c** is $2\,R_{ab} = 18.18\ k\Omega$. The reverse current I_r that flows when the diodes are reversed biased is

$$I_r = \frac{4\times10^3}{18.18\times10^3} \tag{3.58}$$
$$= 220\ mA$$

The current through the sharing resistor R_a is

$$I_a = \frac{R_r1}{R_a + R_r1}\,I_r \tag{3.59}$$
$$= \frac{100\times10^3}{110\times10^3} \cdot 220\times10^{-3}$$
$$= 200\ mA$$

Using (3.59) and assuming that the voltage divides equally between the diodes the power rating of the sharing resistors is determined.

$$P_{Ra} = V_{ab}\ I_a \tag{3.60}$$
$$= 2\times10^3 \cdot 200\times10^{-3}$$
$$= 400\ W$$

For the sharing resistors 400 W 10 kΩ wire wound resistors are used.

To check if the sharing resistors are adequate, assume that the reverse resistance R_r2 is 20% smaller than that of R_r1. The resistance between points **b** and **c** changes to

$$R_{bc} = \frac{10\times10^3 \cdot 80\times10^3}{10\times10^3 + 80\times10^3} \tag{3.61}$$
$$= 8.88\ k\Omega$$

Substituting this value for R_{bc} into (3.55) the voltage V_{ab} is

$$V_{ab} = \frac{9.09\times10^3}{9.09\times10^3 + 8.88\times10^3}\cdot 4\times10^3 = 2\,023\,V \tag{3.62}$$

and from (3.56) the voltage V_{bc} is

$$V_{ab} = \frac{8.88\times10^3}{9.09\times10^3 + 8.88\times10^3}\cdot 4\times10^3 = 1\,977\,V \tag{3.63}$$

From (3.62) and (3.63) it is seen that variations in the reverse resistance of the diodes have little effect on the voltage sharing. Therefore it is concluded that the 10 kΩ resistors are suitable for the sharing resistors. Figure 3.26 provides a photograph of the blocking diodes. These diodes are also mounted on fibre-glass bars to isolate them from the frame. A clearance distance of 75 mm is maintained around the DC-blocking diodes and the sharing resistors.

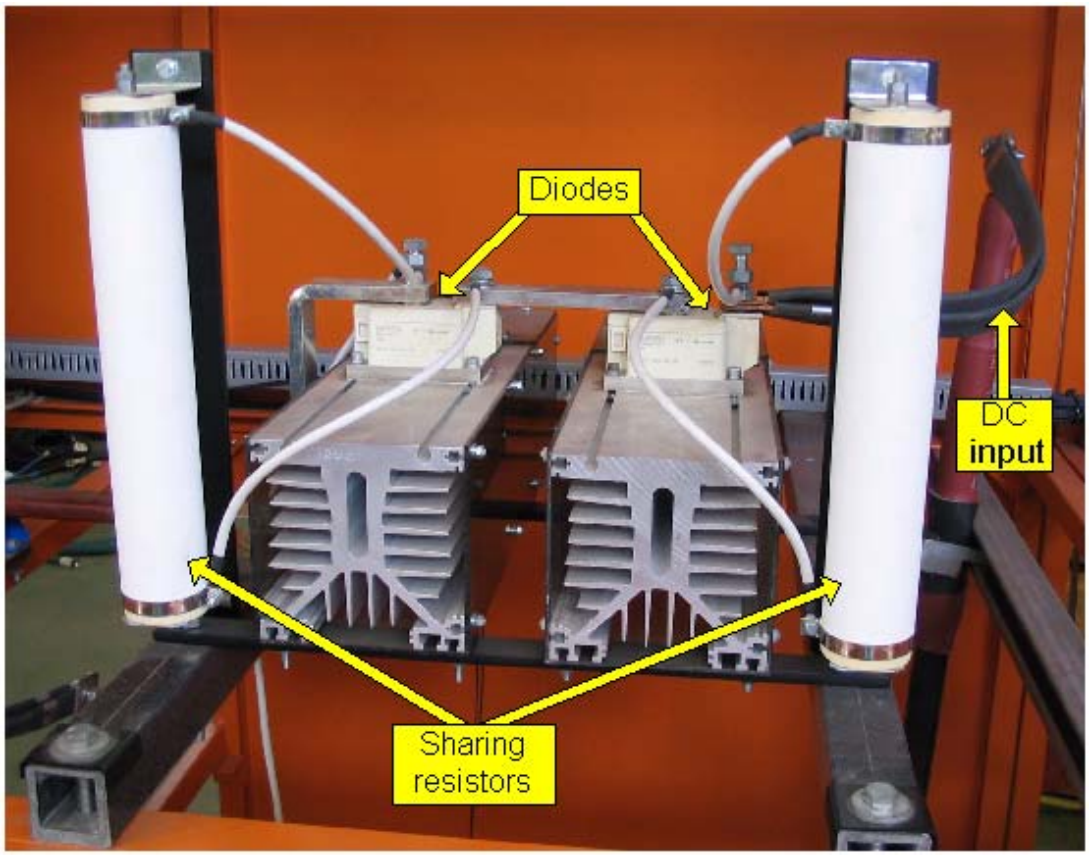

Figure 3.26 – Photograph of the DC blocking diodes at the input of the DC-bus

3.2.8. - Isolated power supply

The power that is supplied to the circuitry of each cell of the inverter is provided by a 24 V DC to DC power supply. The input for this supply is the 110 V DC provided by the substation. Figure 3.27 provides a diagram of the top view of one of the cabinets of the inverter. Due to the series-stacked topology of the inverter each cell is situated at an offset voltage with respect to the DC negative terminal. As shown in Figure 3.27 the negative output terminal of the 24 V supply is also connected to the DC negative terminal. Therefore the power supplied to each cell of the inverter must be isolated from the offset voltage of that cell. An isolated power supply provides the necessary isolation between the high voltage inverter and the low voltage 24 V supply.

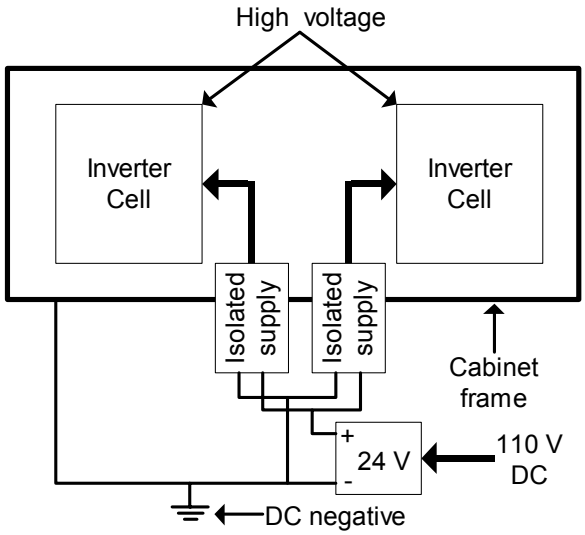

Figure 3.27 – Illustration of the isolated supply

The isolated supply is based on the supply developed in [27] which utilises a half-bridge DC to DC converter topology. A specially designed isolation transformer in the half-bridge topology provides the required isolation. The isolated supply provides the +15 V, -15 V and 5 V that are required by the driver and measurement boards of the inverter. The schematic of the isolated supply is provided in Appendix C.3. Each supply is mounted on a fibre-glass square tube to provide isolation between the supply and the frame. A photograph of the isolated supply is provided in Figure 3.28. As shown the cables from the output of the isolated supply are mounted on an isolated rod to achieve the necessary 75 mm clearance distance.

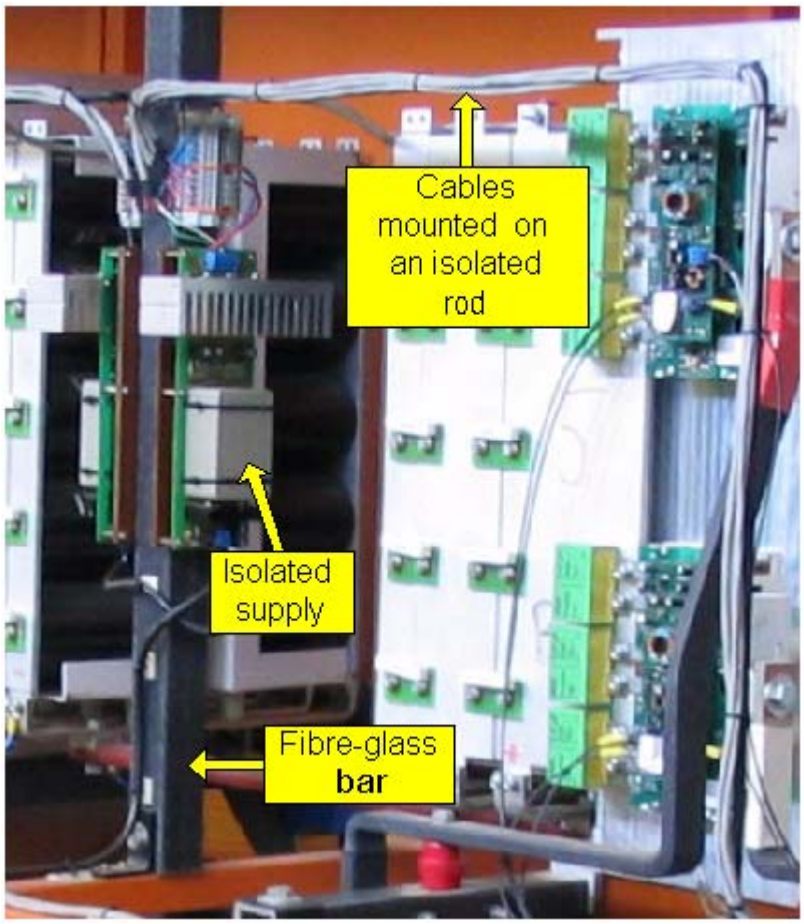

Figure 3.28 – Photograph of the isolated power supply

3.2.9. - Filter inductor

Figure 3.29 provides a diagram illustrating the placement of the filter inductors in the system.

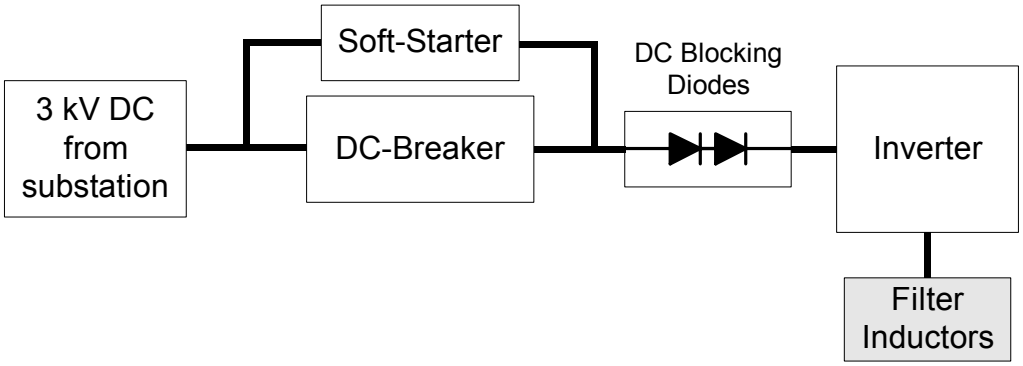

Figure 3.29 – Diagram indicating the filter inductors

The filter inductor reduces the switching harmonics on the current waveform at the output of the inverter. Due to the offset voltage of each cell of the inverter the inductors are also at on offset voltage. Therefore the inductors are mounted on fibre-glass tubing to electrically isolate them from the frame of the inverter cabinet. Care was taken to achieve the 75 mm clearance distance not only from the frame but also from the AC fans above the inductor. A 500 A_{rms}, 50 Hz, 3-phase inductor is used with an output tap at 75 µH and 150 µH. The two taps provide more freedom in the testing of the system. Figure 3.30 provides a photograph of the filter inductor of one of the cells.

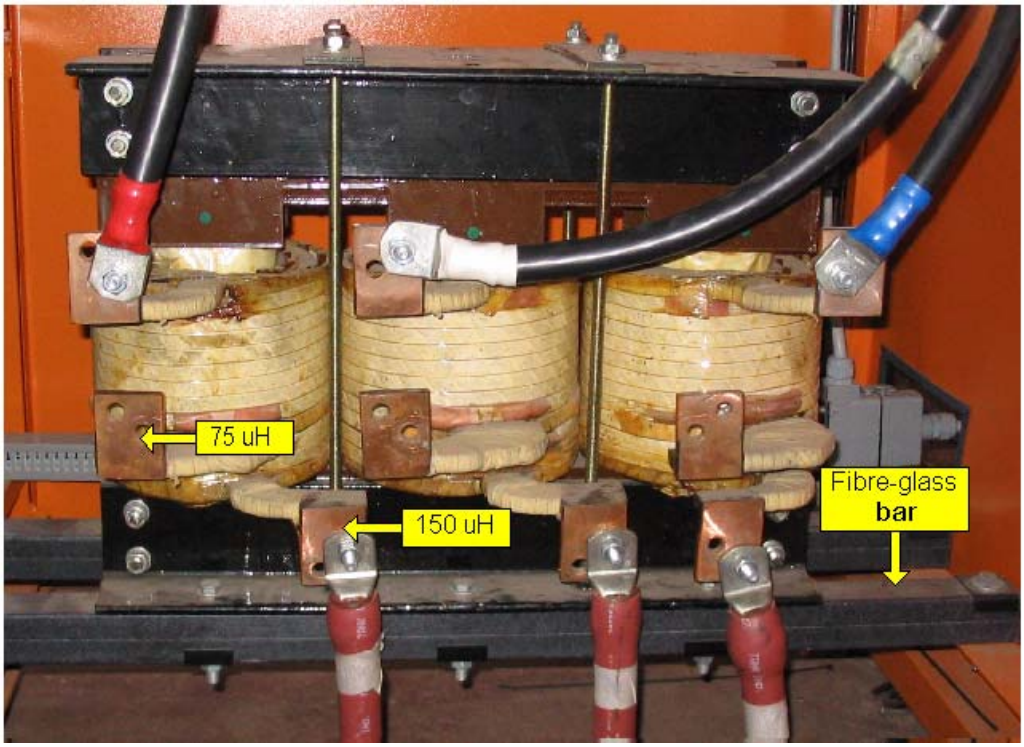

Figure 3.30 – Photograph of the filter inductor

3.3. - Controller

Figure 3.31 provides a diagram illustrating the placement of the controller in the system.

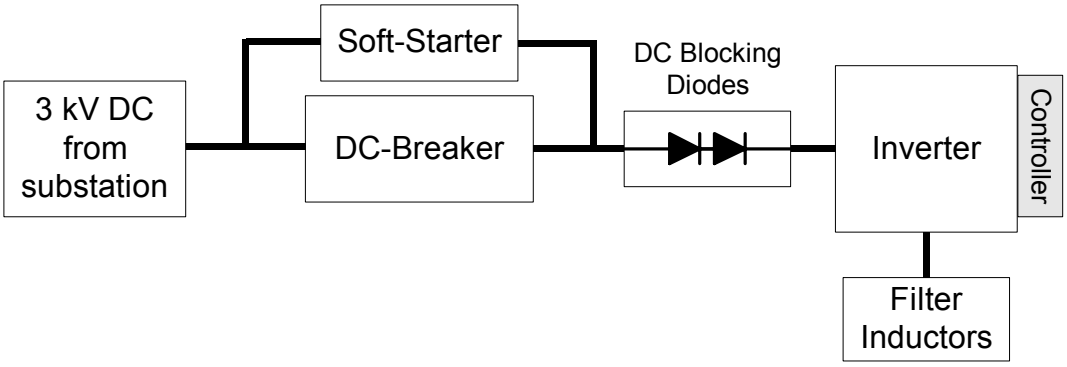

Figure 3.31 – Diagram indicating the controller

The controller can be regarded the "brain" of the system. All the gating signals for the IGBTs, the fault signals from the driver boards, the signals for the switchgear and all the measurements are processed by the controller. DSP and FPGA devices are used for the calculations and control of the system. These devices are sensitive to electro-magnetic-interference (EMI). Due to the high amount of EMI that is created by the switching of the IGBTs, the controller is mounted inside an EMI shielded enclosure. As indicated in Figure 3.31 the controller is mounted on the outside of the cabinet of the inverter. To allow access for the fibre-optic cables connected to the controller, holes must be made in the side of the enclosure. The size of the hole must be small enough so that the shielding ability of the enclosure is not compromised. A "rule of thumb" for the size of a circular hole is that the maximum diameter of the hole must be less than 1/10 of the wavelength of the EMI. The wavelength in free space is defined as

$$\lambda = \frac{c}{f} \tag{3.64}$$

where c = 3 x 10^8 m/s is the speed of light and f is the frequency [30], p17. A general assumption that is used for the EMI created by power electronic devices, is that the frequency of the EMI is less than 100 MHz. The wavelength for a frequency of 100 MHz is

$$\begin{aligned} \lambda &= \frac{3\times10^8}{100\times10^6} \\ &= 3\,m \end{aligned} \tag{3.65}$$

Therefore a hole with a maximum diameter of $\lambda/10 = 300$ mm is acceptable.

Three 6U KM6-II subracks are connected together to form the enclosure for the controller. These subracks consist of aluminium side panels with a conductive clear chromate finish to increase the EMC capability of the enclosure. The controller consists of 3 segments: the power supply segment, the controller board segment and the fibre-optic and current measurement segment. A photograph of the controller is provided in Figure 3.32.

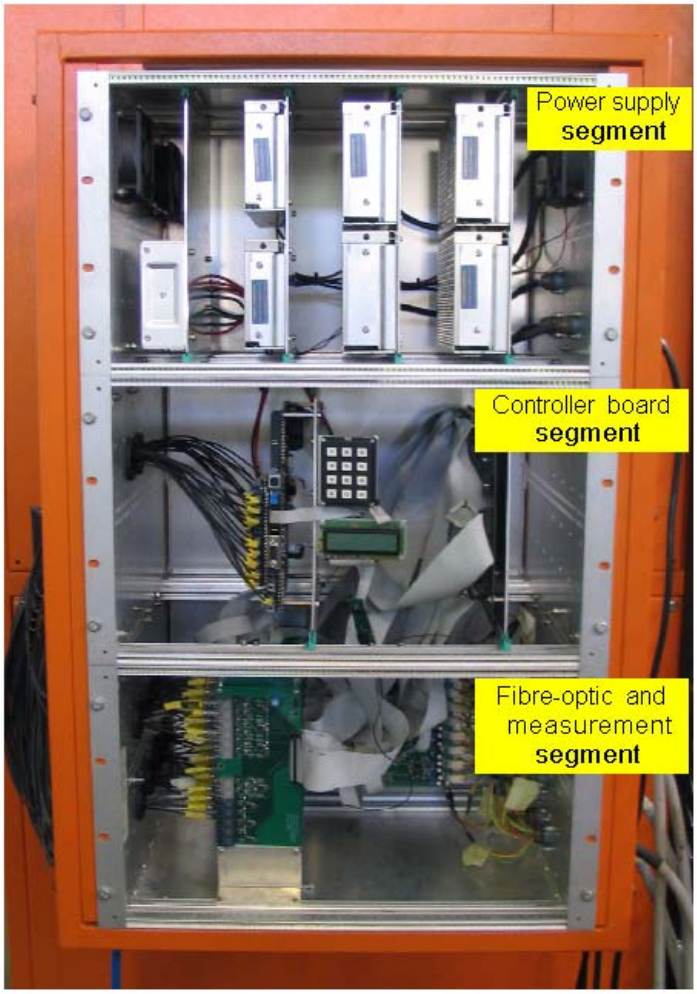

Figure 3.32 – Photograph of the controller

3.3.1. - Power supply segment

This segment houses the power supplies that provide power to the circuitry in the controller and to the circuitry in the inverter cabinets. Table 3.3 lists the power requirements of these components.

Table 3.3 – Power requirements of the circuitry in the system

Voltage	**Component**	**Max current consumption**	**Watt**
+5 V	PEC33	3 A	15 W
	PWM board	8 A	40 W
+15 V	IMB	4.5 A	67.5 W
-15 V	IMB	4.5 A	67.5 W
+24 V	Inverter cabinet	5.5 A	132 W

As previously mentioned, the inverter is divided in 4 cabinets. The circuitry of each cabinet requires a +24 V supply. The input for the power supplies is obtained from the 110 V DC supply from the battery bank of the substation. This ensures that the controller will be able to operate even when the Eskom supply to the substation is lost. If for some reason the battery charger of the 110 V supply fails and the 110 V supply starts to diminish, the substation will shut down at approximately 85 V. An under-voltage relay is connected on the 110 V input to the controller. This relay is calibrated for an under-voltage of 90 V to ensure that the controller can shut the regen-system down before the substation shuts down.

A total of 7 DC to DC power supplies from Mean Well are mounted in the power supply segment of the controller. Table 3.4 list the power supplies that are used.

Table 3.4 – Power supplies in controller

Qty	**Output Voltage**	**Mean Well Type no**	**Power rating**	**Output current**
1	+5 V	SP-100-5	100 W	20 A
1	+15 V	SD-100D-12	100 W	8.5 A
1	-15 V	SD-100D-12	100 W	8.5 A
4	+24 V	SD-150-24	150 W	6.3 A

3.3.2. - Controller board segment

This segment consists of the PEC33 board and the PWM board. The PEC33 is a DSP based controller that orchestrates the operation of the system. All the measurements are channelled to the PEC33 where they are processed and used in the calculations for the gating signals of the inverter. The PEC33 sends the necessary data to the PWM board where the gating signals are generated. The PWM board sends these gating signals to the fibre-optic boards where they are then transmitted to the inverter. The piggy-back board on the PEC33 was originally designed to be used for the transmitting of the gating signals but due to the high number of gating signals, 42, the PWM and fibre-optic boards were developed. The piggy-back board on the PEC33 is now used for the voltage measurements of the system. For more information on the software and hardware of the PEC33 and PWM board please refer to [2]. A photograph of the controller board segment is presented in Figure 3.33

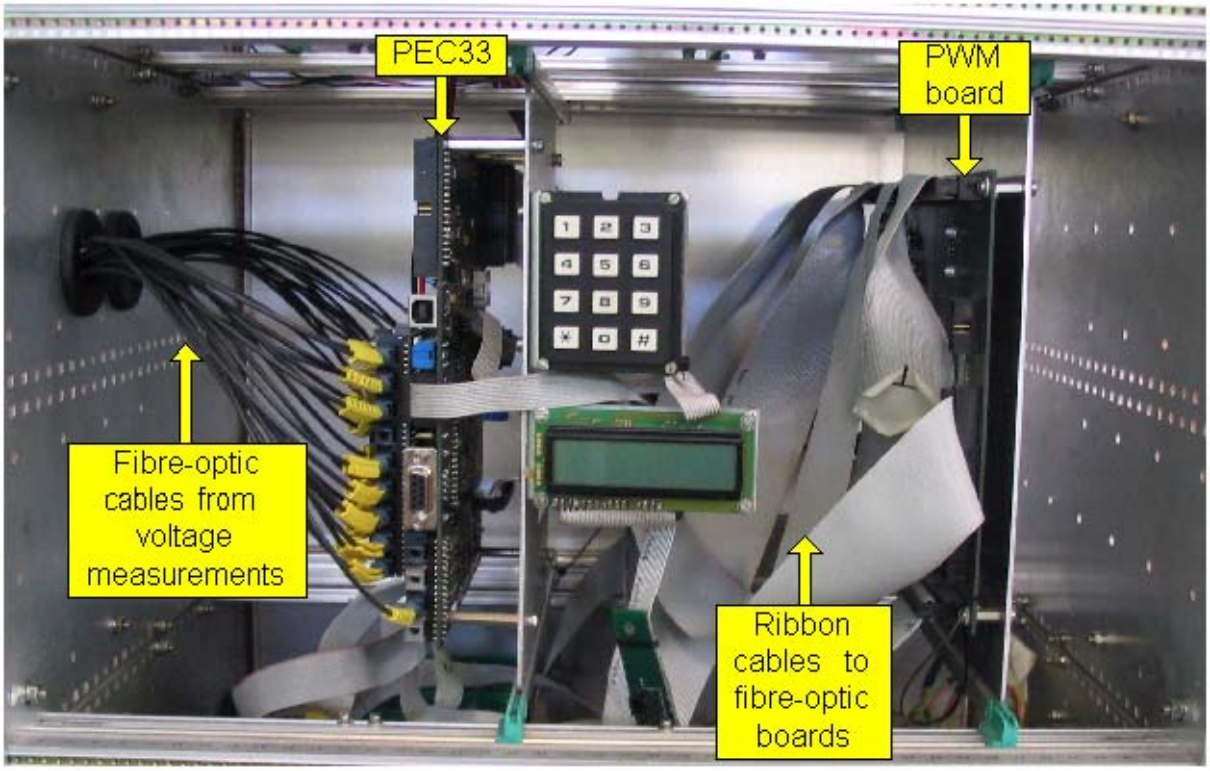

Figure 3.33 – Controller board segment

3.3.3. - Fibre-optic and measurement segment

All the cables from the current measurements are connected to this segment. The measurements are channelled to the PEC33 via the current measurements boards described in

section 4.3. These measurement boards are connected to the analog to digital converters (ADC) on the PEC33 via ribbon cables.

There is 1 fibre-optic board for each cell of the inverter. Each board has 6 fibre-optic transmitters for the gating signals and another transmitter for the control signal of the DC-dump. Furthermore 4 fibre-optic receivers obtain the fault signals from the driver boards of each phase and the fault signal from the DC-dump. An 8th fibre-optic board is used for the transmitting of the control signals for the switchgear in the system and also the receiving of the status signals from the switchgear. Figure 3.34 is a photograph of the fibre-optic and measurement segment.

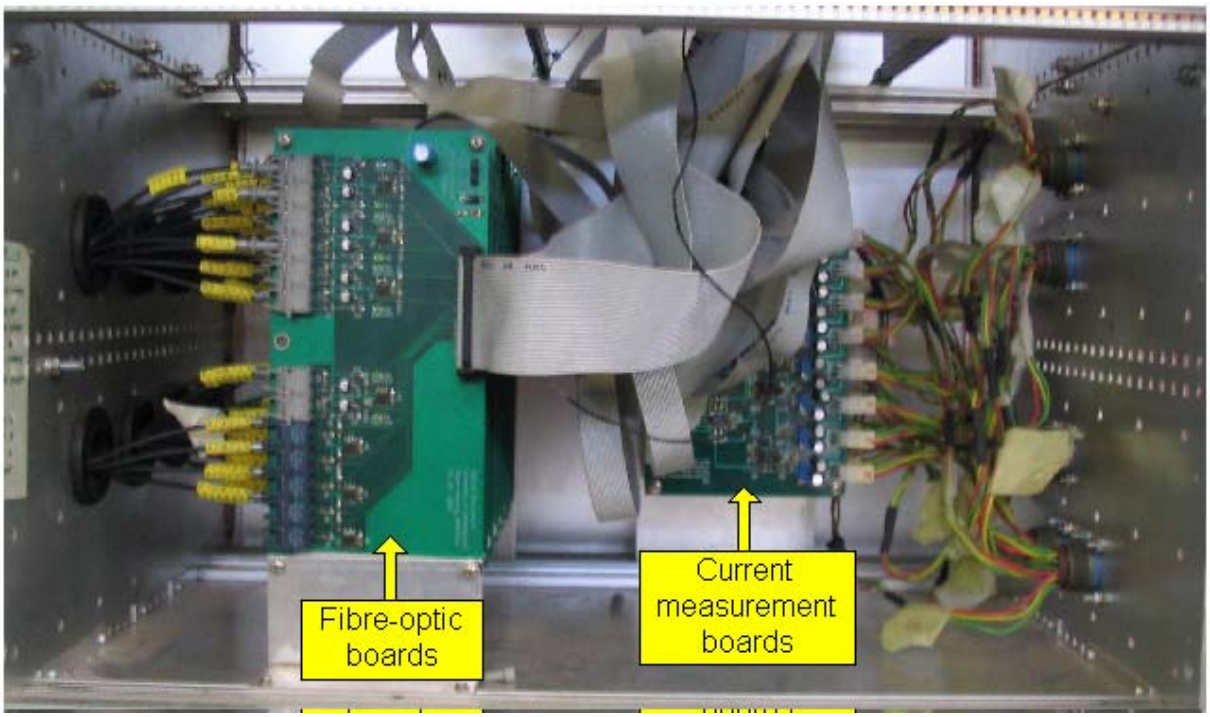

Figure 3.34 – Fibre-optic and measurement segment

3.4. - Conclusion

Chapter 3 describes the 7 level series-stacked inverter that is implemented in the regen-system. The specifications for one cell of the inverter are calculated and the IGBT switching component is described. The losses in the IGBT module are calculated and an analysis of the heatsink is also provided. Other components such as the DC-dump, soft-starter, filter inductor and the isolated power supply are also described. The different segments comprising the controller are explained as well as the EMI enclosure of the controller. To achieve the specified isolation between the inverter and the frame of the inverter cabinet, special mounting methods and components are implemented which are also described.

Chapter 4 - Measurement system

In this chapter the measurement system that is used for the current and voltage measurements is described. The voltage measurement system is described first. Detailed analysis of the hardware as well as the software for the encoding and decoding of the measurement is provided. Subsequently the current measurement system is described. Measurement results indicating that the measurement system is functioning properly are provided. Photographs illustrating the implementation of the measurement system are also provided.

4.1. - Overview of the measurements

The measurement system is necessary for the following:

- Determining when the system will be in the regen-mode or the APF-mode
- Providing voltage and current values to be used in the control algorithms of the system
- Indicate when and where a fault occurs within the system

Figure 4.1 indicates where the measurements are made in the system.

1: The AC voltages and currents at the input of the rectifier

2: The total DC-bus voltage and the DC current at the input of the inverter

3: Each individual DC-bus voltage of each cell

4: The 21 output currents of the inverter

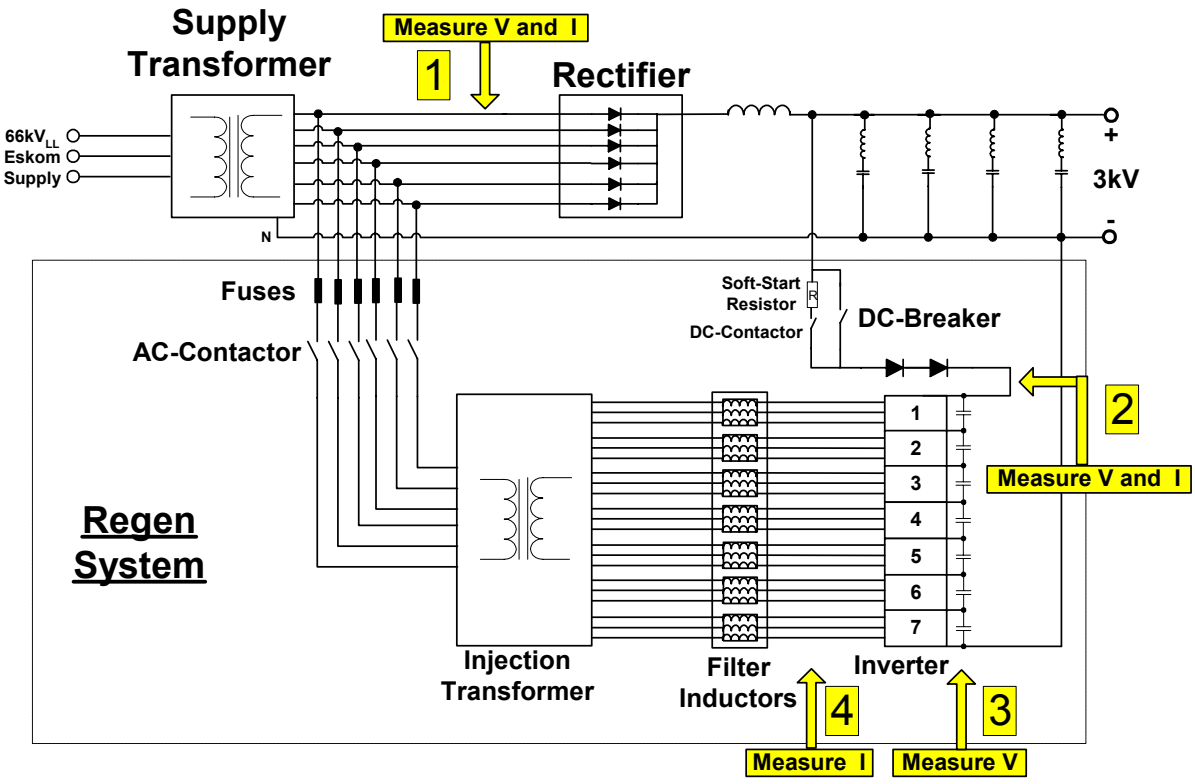

Figure 4.1 – Positions of the measurements in the system

4.2. - Voltage Measurements

The voltages are measured using a Voltage Measuring Board (VMB). Different types of probes are used for the AC and DC voltage measurements. These are described in sections 4.2.1 and 4.2.2 respectively. The types of voltage probes used in the system have to be electrically connected to the measuring point. Therefore there is an electrical connection between the VMB and the controller. By connecting the probes in this manner the possibility exists that through a fault the controller could be connected to the high voltage measuring point. This will damage the controller and it is also dangerous for the person operating the controller. To electrically isolate the VMB from the controller the voltage measurement system utilises a fibre-optic system to transmit the measured data from the VMB to the controller. The fibre-optic cable electrically isolates the controller from the VMB and ensures that a fault on the high voltage side will not damage the controller. Another advantage of the fibre-optic cable is that it is not susceptible to EMI. The data that is transmitted via the fibre-optic cable must be in a digital format. Therefore the VMBs use an Analog to Digital Converter (ADC) to digitise the voltage measurements.

4.2.1. - AC Voltage measurements

The only AC voltage measurements made are the 6 line-to-line voltages at the input of the rectifier. A CV 4-5000 voltage transducer manufactured by LEM Components is used as the voltage probe for these measurements. Table 4.1 lists some of the electrical data for this module.

Table 4.1 – Electrical data for CV 4-5000

Description	**Value**
Primary nominal rms voltage	3535 V
Primary voltage range	0…+/- 5000 V
Conversion ratio	5000 V / 10 V
Rms voltage for AC isolation, 50Hz, 1 min	9 kV

Figure 4.2 provides a diagram that illustrates the connection of the AC voltage measurements modules.

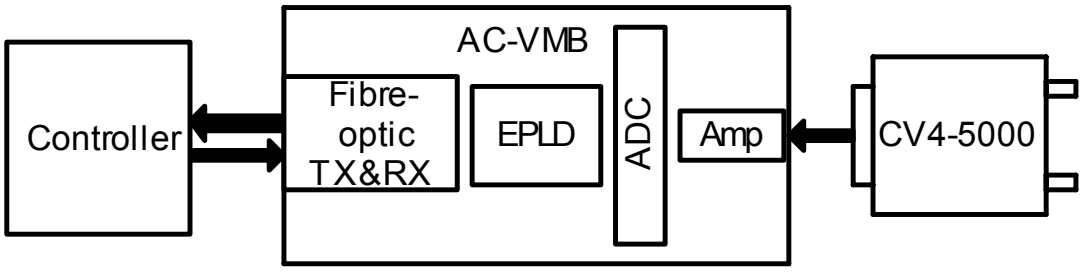

Figure 4.2 – Diagram of the AC voltage measurements

The output of the CV 4-5000 is connected to the ADC of the VMB. An AD7892AN-1 from Analog Devices is used for the ADC on the VMBs. Table 4.2 lists some of the specifications of the AD7892.

Table 4.2 – Specifications of the AD7892

Description	**Value**
Resolution	12 bits
Conversion time	1.47 µs
Analog input range	+/- 10 V
Supply voltage	+ 5 V

From Table 4.1 it is seen that the CV 4-5000 has a conversion ratio of 500:1. The 6-phase line-to-line voltages that are measured have a value of 2 420 V_{rms}. The peak value of the line-to-line voltage is

$$\begin{aligned} \hat{V}_{LL} &= \sqrt{2} \cdot 2420 \\ &= 3422\,V \end{aligned} \tag{4.1}$$

For a measured voltage of 3422 V the output of the CV 4-5000 will be 6.84 V. To utilise the full +/- 10 V input voltage range of the AD7892, the output of the CV 4-5000 must be amplified. An AD620AN instrumentation amplifier from Analog Devices is used for this purpose. The AD620 uses only 1 external resistor to adjust the gain. The AC-VMB is calibrated for a peak value of +/- 4 kV. For a value of 4 kV the output of the CV 4-5000 is 8 V. The gain that the AD620 must provide is calculated as

$$\begin{aligned} G &= \frac{output\ voltage}{input\ voltage} \\ &= \frac{10}{8} \\ &= 1.25 \end{aligned} \tag{4.2}$$

where G is the gain of the amplifier. The gain equation for the amplifier is given by (4.3)

$$G = \frac{49.4 \times 10^3}{R_G} + 1 \tag{4.3}$$

where R_G is the value of the gain resistor [31]. By substituting (4.2) into (4.3) the value of R_G is calculated.

$$R_G = \frac{49.4\times10^3}{G-1} = \frac{49.4\times10^3}{1.25-1} = 197.6\ k\Omega \tag{4.4}$$

A 500 kΩ multi-turn resistor is used to adjust the value of R_G.

A low-pass filter is connected between the CV 4-5000 and the AD620 to filter out noise picked up by the voltage probe. An RC low-pass filter is used as show in Figure 4.3.

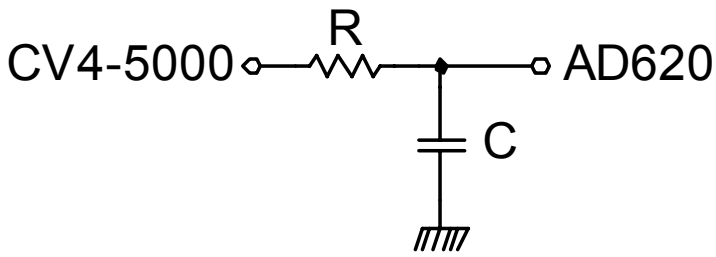

Figure 4.3 – RC low-pass filter for the AC-VMB

The cutoff frequency for this type of filter is defined as

$$\omega_C = \frac{1}{RC} \tag{4.5}$$

where ω_c is the cutoff frequency in rad/s [29], p666. To convert between rad/s and Hz the following relationship is used

$$\omega_C = 2\pi f_C \tag{4.6}$$

where f_C is the cutoff frequency in Hz.

Only the 50 Hz component of the voltage measurements is necessary for the control algorithms [2]. Therefore the cutoff frequency was chosen as 300 Hz. A value of 100 nF was chosen for the capacitor. Substituting these values into (4.5) and (4.6) the resistor value is calculated.

$$\begin{aligned} R &= \frac{1}{\omega_C C} \\ &= \frac{1}{2\pi f_C C} \\ &= \frac{1}{2\pi \cdot 300 \cdot 100 \times 10^{-9}} \\ &= 5.3\ k\Omega \end{aligned} \tag{4.7}$$

Due to availability the resistor value was taken as 5.1 kΩ. Using (4.5) and (4.6) the cutoff frequency is calculated.

$$\begin{aligned} f_C &= \frac{1}{2\pi RC} \\ &= \frac{1}{2\pi \cdot 5.1 \times 10^3 \cdot 100 \times 10^{-9}} \\ &= 312\ Hz \end{aligned} \tag{4.8}$$

The transfer function of the RC filter is

$$H(j\omega) = \frac{\frac{1}{RC}}{j\omega + \frac{1}{RC}} \tag{4.9}$$

Substituting the values of R and C into (4.9) the value of the transfer function for a frequency of 50 Hz is

$$\begin{aligned} H(j2\pi 50) &= \frac{\frac{1}{5.1 \times 10^3 \cdot 100 \times 10^{-9}}}{j2\pi 50 + \frac{1}{5.1 \times 10^3 \cdot 100 \times 10^{-9}}} \\ &= 0.98 \angle -9.1^0 \end{aligned} \tag{4.10}$$

The attenuation of the amplitude at 50 Hz is negligible. The phase shift of 9.1^0 can be adjusted in the software of the controller but it is preferable that the phase shift be reduced by increasing the cutoff frequency or by using a higher order filter. It is concluded that the RC low-pass filter with a cutoff frequency of 312 Hz is suitable for the measurement of the 50 Hz

line-to-line voltages. Figure 4.4 provides a photograph of the AC-VMB. The schematic of the AC-VMB is provided in Appendix C.5

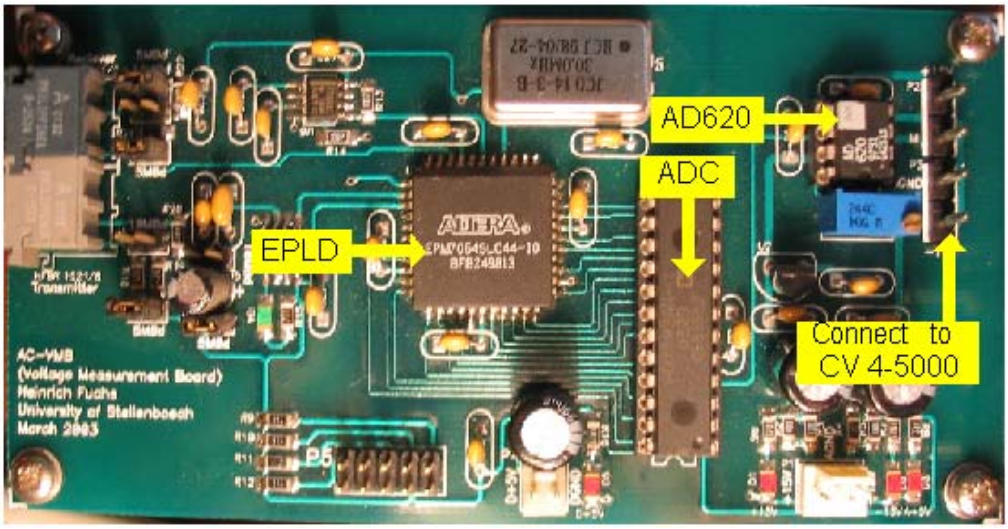

Figure 4.4 – Photograph of the AC-VMB

Figure 4.5 is a photograph of some of the AC voltage measurements. To ensure that the AC voltage measurement system is electrically isolated, the power supply of the AC-VMBs must also be isolated. The same isolated power supply that is used for the inverter is used to isolate the power of the AC-VMBs.

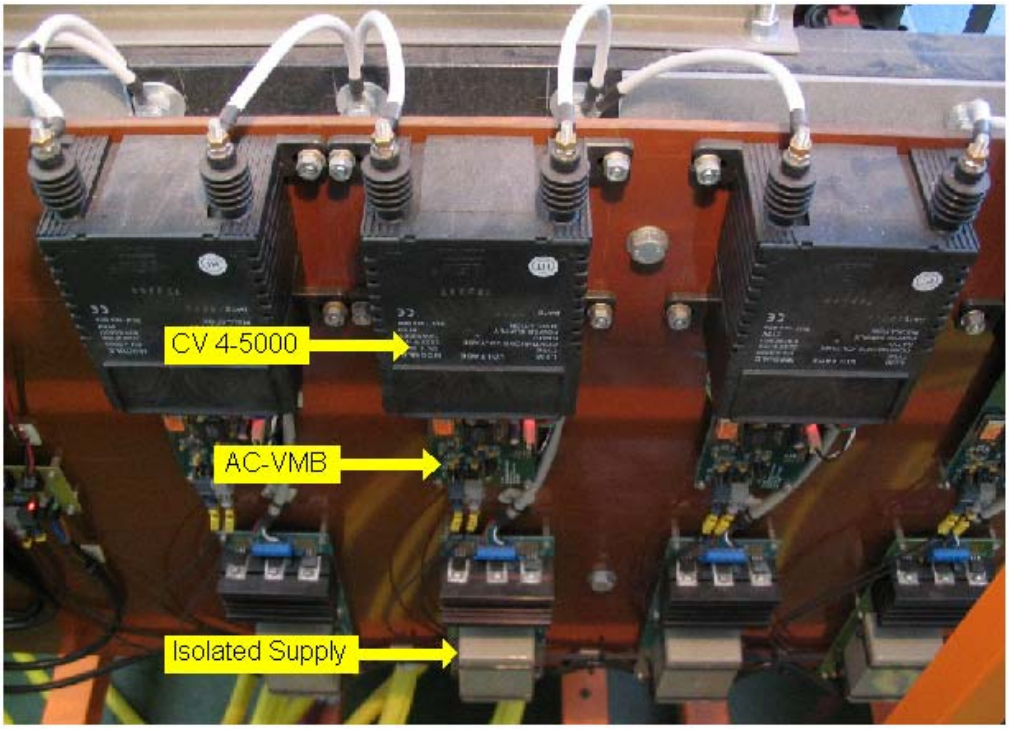

Figure 4.5 – Photograph of AC voltage measurements

4.2.2. - DC Voltage measurements

Due to the high value of the total DC-bus voltage it was decided to use the CV 4-5000 voltage probe for this measurement as well. Figure 4.6 provides a photograph of the total DC-bus voltage measurement.

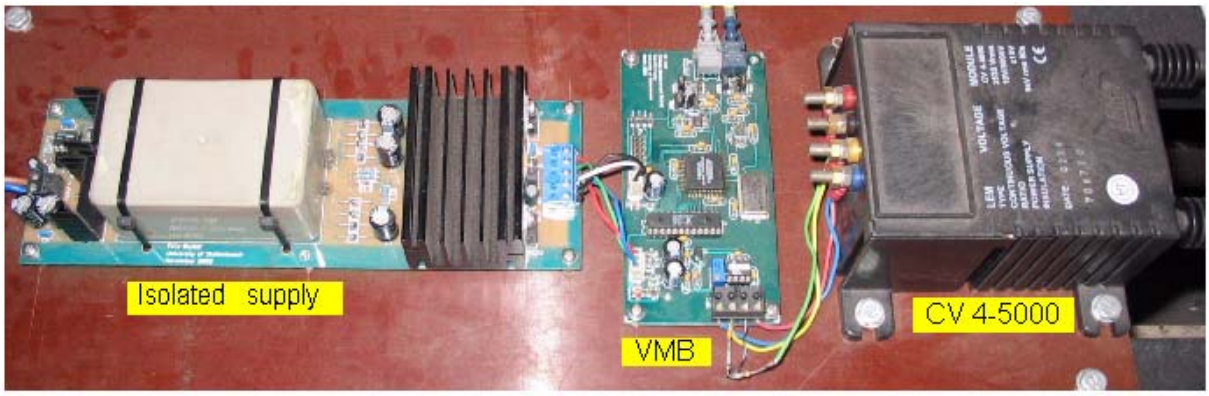

Figure 4.6 – Total DC-bus voltage measurement

For the DC-bus voltage measurement of each cell of the inverter a resistive network is used as the probe. Figure 4.7 presents a diagram of the voltage probe used for the DC-VMB.

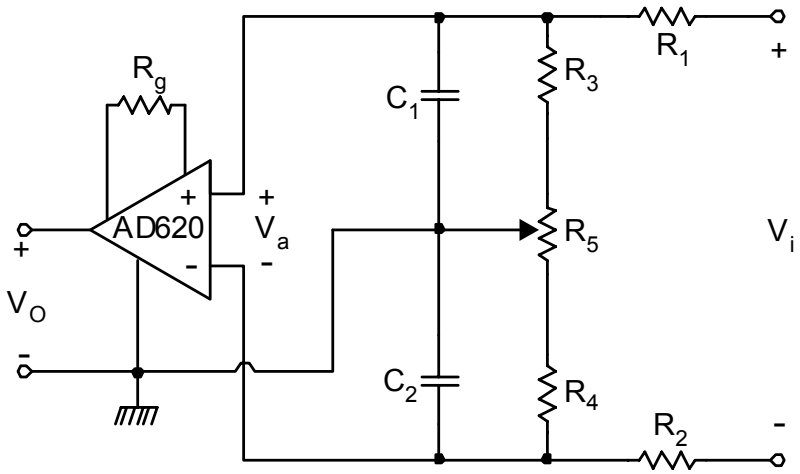

Figure 4.7 – Voltage probe used on the DC-VMB

In order for the voltage probe to have an insignificant effect on the measurement point, the probe's input impedance must be high. For resistors R_1 and R_2, 2.5 kV 10 MΩ resistors are used. Resistors R_3 and R_4 were chosen as 100 kΩ resistors and R_5 is a 50 kΩ multi-turn resistor. Due to the tolerance in the values of resistors R_1 to R_4, the input resistance of the

positive and negative halve of the probe may vary. The multi-turn resistor R_5 is adjusted so that the positive and negative inputs have exactly the same resistance. To calculate the relationship between V_i and V_a, Figure 4.7 is redrawn as shown in Figure 4.8. Due to the DC voltage that is measured, C_1 and C_2 are neglected in these calculations.

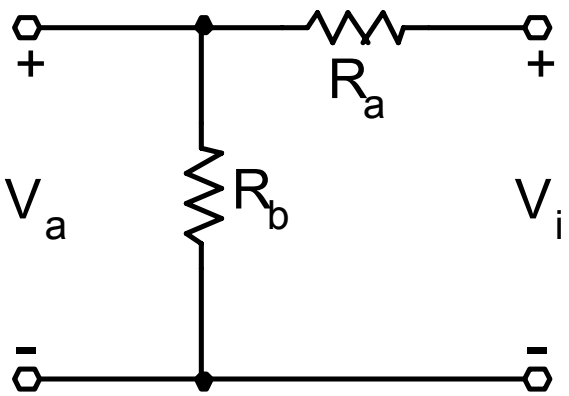

Figure 4.8 – Reduced diagram of the voltage probe in Figure 4.7

The value of R_a is calculated as follows

$$\begin{aligned} R_a &= R_1 + R_2 \\ &= 10\times10^6 + 10\times10^6 \\ &= 20\ M\Omega \end{aligned} \tag{4.11}$$

and R_b

$$\begin{aligned} R_b &= R_3 + R_4 + R_5 \\ &= 100\times10^3 + 100\times10^3 + 50\times10^3 \\ &= 250\ k\Omega \end{aligned} \tag{4.12}$$

The relationship between V_i and V_a is given by (4.13).

$$\begin{aligned} V_a &= \frac{R_b}{R_a + R_b} V_i \\ &= \frac{250 \times 10^3}{20 \times 10^6 + 250 \times 10^3} \cdot V_i \\ &= 12.35 \times 10^{-3} \cdot V_i \end{aligned} \tag{4.13}$$

The maximum of the total DC-bus voltage is 3.9 kV [1]. For each cell the DC voltage will be

$$\begin{aligned} V_{DC\_cell} &= \frac{3.9 \times 10^3}{7} \\ &= 557\,V \end{aligned} \tag{4.14}$$

The DC-VMB is calibrated for a value of 600 V maximum. Substituting this value for V_i into (4.13), the value of V_a is calculated as

$$\begin{aligned} V_a &= 12.35 \times 10^{-3} \cdot 600 \\ &= 7.41\,V \end{aligned} \tag{4.15}$$

As for the AC-VMB it is desired that the full input voltage range of the ADC be utilised. For the maximum input voltage of 600 V, a value of 10 V must be supplied to the input of the ADC. The AD620 instrumentation amplifier must amplify the output of the voltage probe. By using (4.15) as the maximum input value to the amplifier, the gain of the amplifier is calculated.

$$\begin{aligned} G &= \frac{10}{7.41} \\ &= 1.35 \end{aligned} \tag{4.16}$$

Substituting (4.16) into (4.4) the value of the gain resistor, R_g, is calculated.

$$\begin{aligned} R_G &= \frac{49.4 \times 10^3}{G - 1} \\ &= \frac{49.4 \times 10^3}{1.35 - 1} \\ &= 141.14\,k\Omega \end{aligned} \tag{4.17}$$

A 200 kΩ multi-turn resistor is used for R_g.

To filter out noise that is picked up by the probe, the capacitors C_1 and C_2 are added to the resistor divider network so that the probe will be a low-pass filter. Due to the DC voltages that are measured the cutoff frequency of the low-pass filter need not be high. To calculate the cutoff frequency of the probe, consider the positive half of the probe as shown in Figure 4.9.

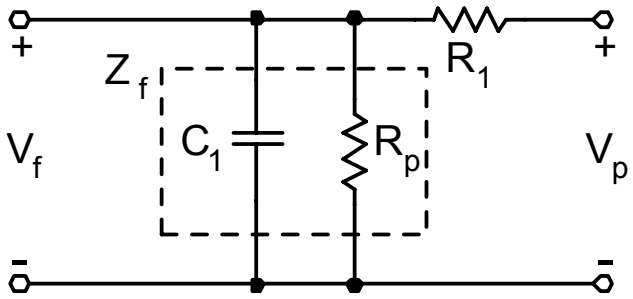

Figure 4.9 – Positive half of the voltage probe

Assuming that the resistors have exact values, the multi-turn resistor R_5 will then be adjusted so that half of its value will be on the positive side of the probe and the other half on the negative side. From Figure 4.7 the resistor R_p in Figure 4.9 is the combination of R_3 and half of R_5.

$$R_p = R_3 + \frac{R_5}{2} = 125\ k\Omega \tag{4.18}$$

The impedance Z_f shown in Figure 4.9 is the parallel combination of C_1 and R_p,

$$Z_f = \frac{Z_C\ R_p}{Z_C + R_p} \tag{4.19}$$

where Z_C is the impedance of C_1. In the frequency domain (4.19) changes to

$$Z_f(j\omega) = \frac{\frac{R_p}{j\omega C_1}}{R_p + \frac{1}{j\omega C_1}} = \frac{R_p}{j\omega C_1 R_p + 1} \tag{4.20}$$

The transfer function, H, of the circuit shown in Figure 4.9 is as follows.

$$H = \frac{Z_f}{Z_f + R_1} \tag{4.21}$$

The parasitic capacitance of the resistors is very small and has little effect on the cutoff frequency and is therefore neglected in the calculations. Substituting (4.20) into (4.21) produces the transfer function as

$$\begin{aligned} H(j\omega) &= \frac{\frac{R_p}{j\omega C_1 R_p + 1}}{\frac{R_p}{j\omega C_1 R_p + 1} + R_1} \\ &= \frac{R_p}{j\omega C_1 R_1 R_p + R_1 + R_p} \\ &= \frac{\frac{R_p}{R_1 R_p C_1}}{j\omega + \frac{R_1 + R_p}{R_1 R_p C_1}} \\ &= \frac{\frac{1}{R_1 C_1}}{j\omega + \frac{R_1 + R_p}{R_1 R_p C_1}} \end{aligned} \tag{4.22}$$

The cutoff frequency, ω_c, of the low-pass filter is defined as follows [29], p660

$$\left|H(j\omega_c)\right| = \frac{1}{\sqrt{2}} H_{\max} \tag{4.23}$$

Equation (4.23) states that the cutoff frequency is that frequency for which the magnitude of the transfer function is decreased by a factor $1/\sqrt{2}$ from its maximum value.

By using (4.22) the maximum value of the transfer function for this RC low-pass filter is defined as

$$\begin{aligned} H_{\max} &= H(j0) \\ &= \frac{\frac{1}{R_1 C_1}}{\frac{R_1 + R_p}{R_1 R_p C_1}} \\ &= \frac{R_p}{R_1 + R_p} \end{aligned} \tag{4.24}$$

and the magnitude of the transfer function is

$$\left|H(j\omega)\right| = \frac{\frac{1}{R_1 C_1}}{\sqrt{\omega^2 + \left(\frac{R_1 + R_p}{R_1 R_p C_1}\right)^2}} \tag{4.25}$$

Substituting (4.24) and (4.25) into (4.23) gives the cutoff frequency as

$$\frac{\frac{1}{R_1 C_1}}{\sqrt{\omega_c^{\,2} + \left(\frac{R_1 + R_p}{R_1 R_p C_1}\right)^2}} = \frac{1}{\sqrt{2}} \frac{R_p}{R_1 + R_p} \tag{4.26}$$

$$\frac{1}{R_1 C_1} = \frac{1}{\sqrt{2}} \frac{R_p}{R_1 + R_p} \sqrt{\omega_c^{\,2} + \left(\frac{R_1 + R_p}{R_1 R_p C_1}\right)^2}$$

$$\omega_c^{\,2} + \left(\frac{R_1 + R_p}{R_1 R_p C_1}\right)^2 = 2 \left(\frac{1}{R_1 C_1}\right)^2 \left(\frac{R_1 + R_p}{R_p}\right)^2$$

$$= 2 \left(\frac{R_1 + R_p}{R_1 R_p C_1}\right)^2$$

$$\omega_c = \frac{R_1 + R_p}{R_1 R_p C_1}$$

A 1% 1 nF capacitor is used for C_1 and C_2. Substituting this value into (4.26) the cutoff frequency is calculated.

$$\omega_c = \frac{10 \times 10^6 + 125 \times 10^3}{10 \times 10^6 \cdot 125 \times 10^3 \cdot 1 \times 10^{-9}} \tag{4.27}$$
$$= 8.1 \times 10^3 \; rad/s$$

Using (4.6) the cutoff frequency is converted from rad/s (ω_c) to Hz (f_c).

$$f_c = \frac{\omega_c}{2\pi} \tag{4.28}$$
$$= \frac{8.1 \times 10^3}{2\pi}$$
$$= 1.3 \; kHz$$

Since the switching frequency of the inverter is 5 kHz, the cutoff frequency of 1.3 kHz for the DC-bus voltage measurements is acceptable. Figure 4.10 provides a photograph of the DC-VMB. The schematic of the DC-VMB is provided in Appendix C.6.

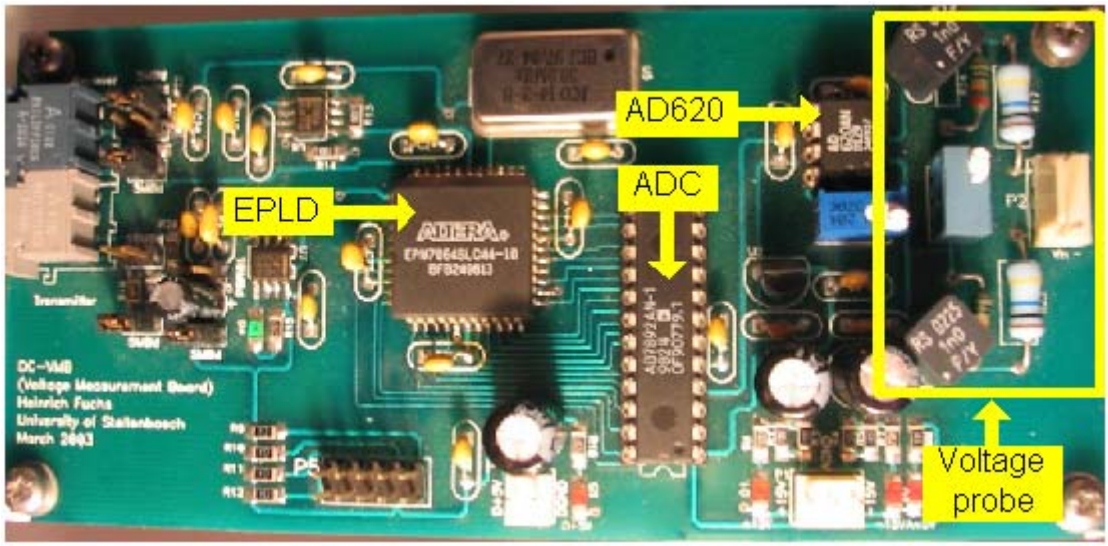

Figure 4.10 – Photograph of the DC-VMB

4.2.3. - Encoding of measured voltages

To ensure a more reliable data transfer, the measured voltages are encoded before it is sent to the controller. A form of Manchester encoding is used [32]. In order for the measurements to be encoded it has to be digitised. As previously mentioned an AD7892AN-1 ADC is used for this purpose. The ADC interfaces with an EPLD that encodes the data and sends it to the fibre-optic transmitter. An EPM7064SLC44-10 EPLD from Altera is used. A 30 MHz crystal oscillator is used for the clock of the EPLD. To electrically isolate the VMB from the controller, the data is sent via fibre-optic cable to the controller. The VMB is designed so that with the adjustment of jumper connections a choice between a 5 MBd and 10 MBd system for the fibre-optic can be made. For the implementation of this project the 5 MBd system is used.

For the encoding process the clock of the EPLD is divided down to form a “chip”. The duration of a chip is defined as the number of clock cycles contained in the chip. The duration of the chip determines the rate of transmission of the data via the fibre-optic system. Determining the number of clock cycles for a chip for the 5MBd system is described later in this chapter. Three different pulses are generated by the encoding process, an S-pulse, 1-pulse and a 0-pulse. The S-pulse is a synchronization pulse that is transmitted during the intervals that data is not requested from the VMB. The 1-pulse and 0-pulse represent a 1 and a 0 bit respectively. The data is encoded so that it is related to the change in the level of the pulse, from a high to a low or low to a high. Each data-bit has a duration of 2 chips. A 1-pulse is at a constant level for 2 chips and a 0-pulse has a level change after 1 chip. The S-pulse is 3 chips

long and has a constant level for this period. Figure 4.11 presents a diagram of the 3 different pulses that is a result of the encoding process.

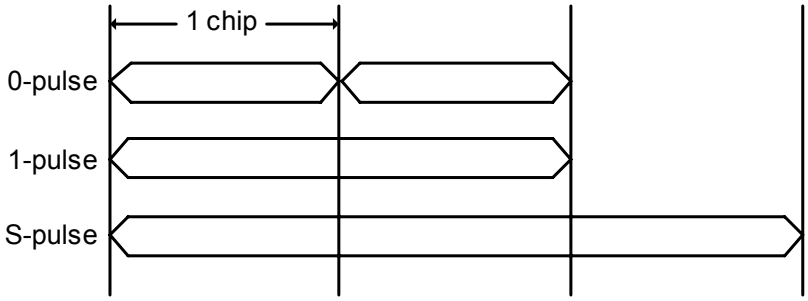

Figure 4.11 – Diagram of the3 different pulses as a result of the encoding process

Due to the fibre-optic system that is used the encoded output data of the EPLD is serial. Figure 4.12 shows how the encoded output would look like for a data sequence of 1 0 1 1 0 0 1. Note that the data has a constant bit-rate of 2 chips / bit.

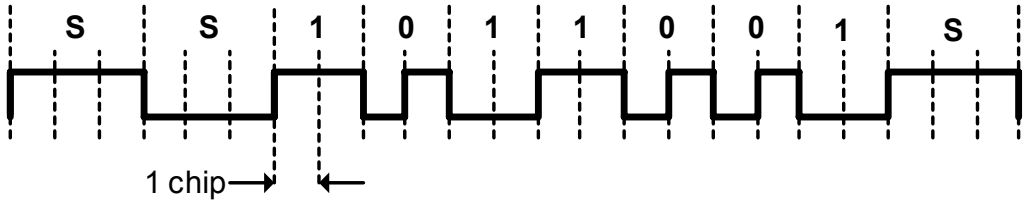

Figure 4.12 – Example of encoded data for a sequence of 1011001

The 5MBd fibre-optic system allows for a maximum of 5×10^6 level changes per second in the transmitted signal. Therefore every 200 ns a level change is allowed. This implies that a chip can not be shorter than 200 ns. The clock of the EPLD is a 30 MHz clock with a period of 33.33 ns. The number of clock cycles for one chip is $200/33.33 = 6$. Figure 4.13 illustrates a 0-pulse for the 5 MBd system.

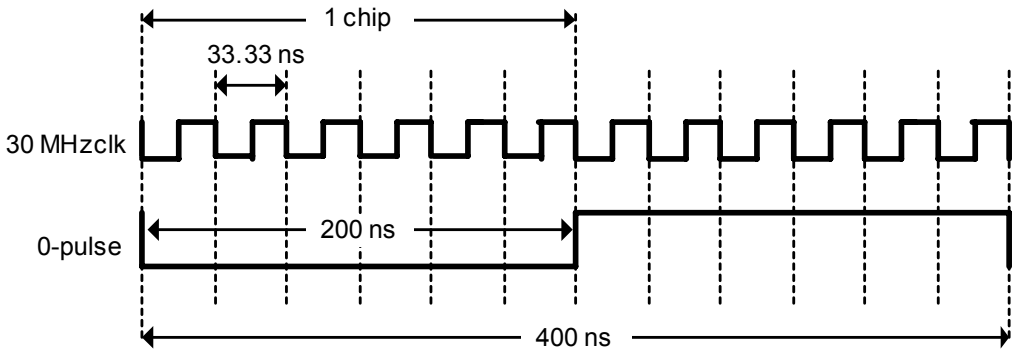

Figure 4.13 – A 0-pulse for the 5 MBd system

As previously mentioned, 1 data-bit is 2 chips long. From Figure 4.13 it is seen that for the 5 MBd system 1 data-bit has a duration of 400 ns. The ADC of the VMB is a 12-bit ADC. The interface between the EPLD and the ADC can either be serial or parallel. The parallel interface is used for this system. In the serial mode the ADC adds 4 leading zeros to the 12-bit data. In the parallel mode the 4 leading zeros is added by the software resulting in a 16-bit data sequence for every voltage measurement. The 4 leading zeros are used by the decoding software to indicate the error status of the data. The ADC on the VMB has a 1.47 µs conversion time but the EPLD provides a 1.6 µs period for the conversion. Adding the conversion time to the time that it takes to encode the 16-bit sequence yields a $16\left(400\times10^{-9}\right)+1.6\times10^{-6}=8\ \mu s$ delay between the request and transmission of the voltage measurement. This calculation provides a rough estimate of the delay between the time that the controller requests the measurement to the time that the measurement is available to the controller. Only the 50 Hz component of the AC voltage measurements is needed for the control algorithms, therefore the delay is not a concern.

Figure 4.14 provides a flowchart of the VHDL code for the encoding of the voltage measurement. The complete code can be found in Appendix B.2.

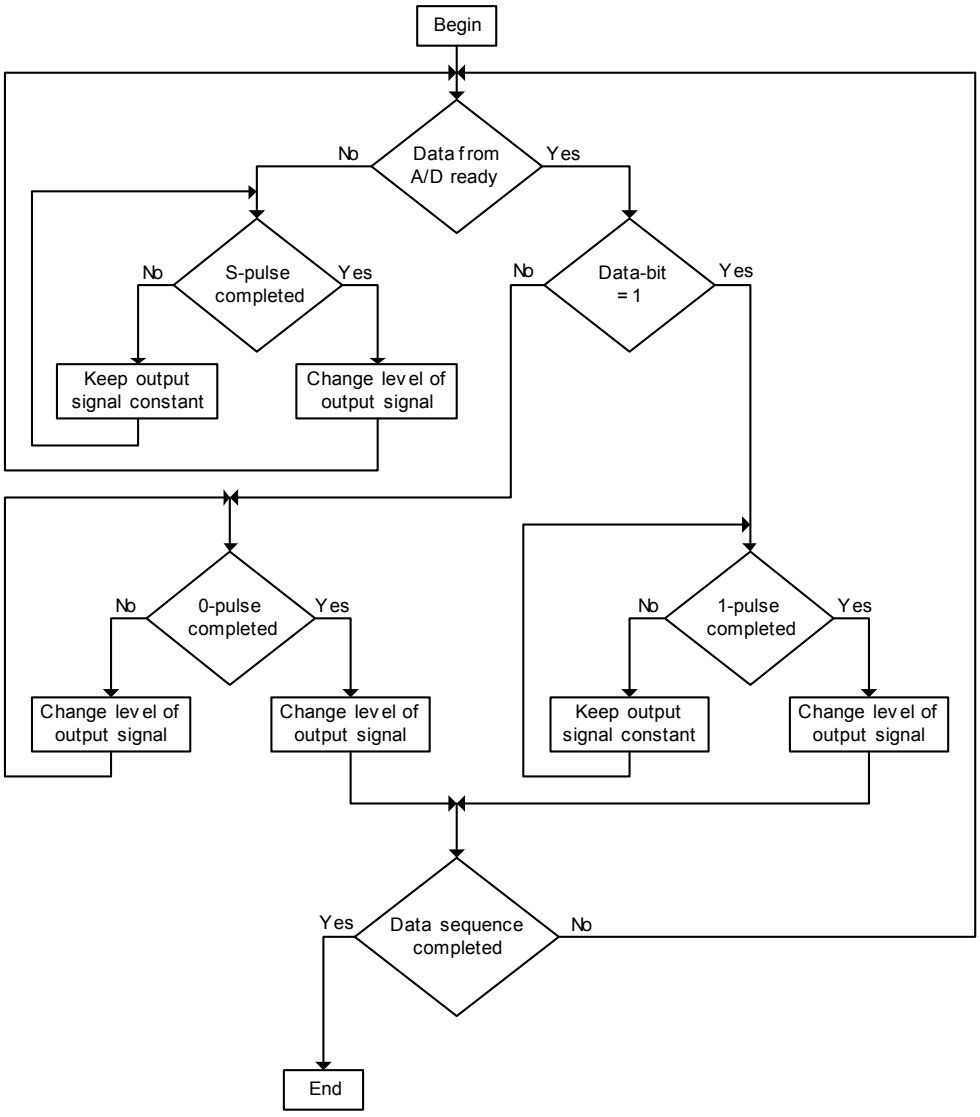

Figure 4.14 – Flowchart of the encoding VHDL code

4.2.4. - Decoding of measured voltages

The decoding of the voltage measurements is done in one of the FPGAs on the PEC33. To compensate for possible drift between the clock on the VMB and the clock on the PEC33, the sampling clock that is generated by the decoding software is synchronised with every falling edge of the received data. By doing this it is ensured that the received data will not be sampled near the edges of the signal. As the received data is decoded it is shifted into a register. When the data sequence is completed the register is made available to the PEC33. The S-pulse has a duration of 3 chips and is the longest bit that is transmitted. If the received data has the same level, high or low, for more than 3 chips, an error is indicated. Assume that the received data is as shown in Figure 4.15.

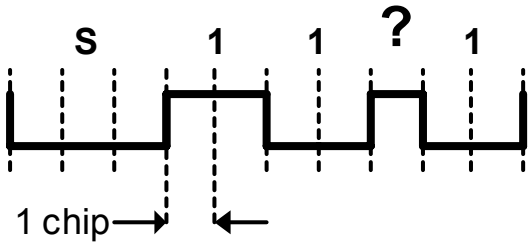

Figure 4.15 – Example of an error in the received data

The bit-rate is not constant and the decoded data will be illogical therefore an error will be indicated. Bit 13 of the 16 bit data is used for the error-bit. When an error is detected bit 13 is loaded with a 1. Figure 4.16 provides a flowchart of the decoding VHDL code. The complete code is provided in Appendix B.3.

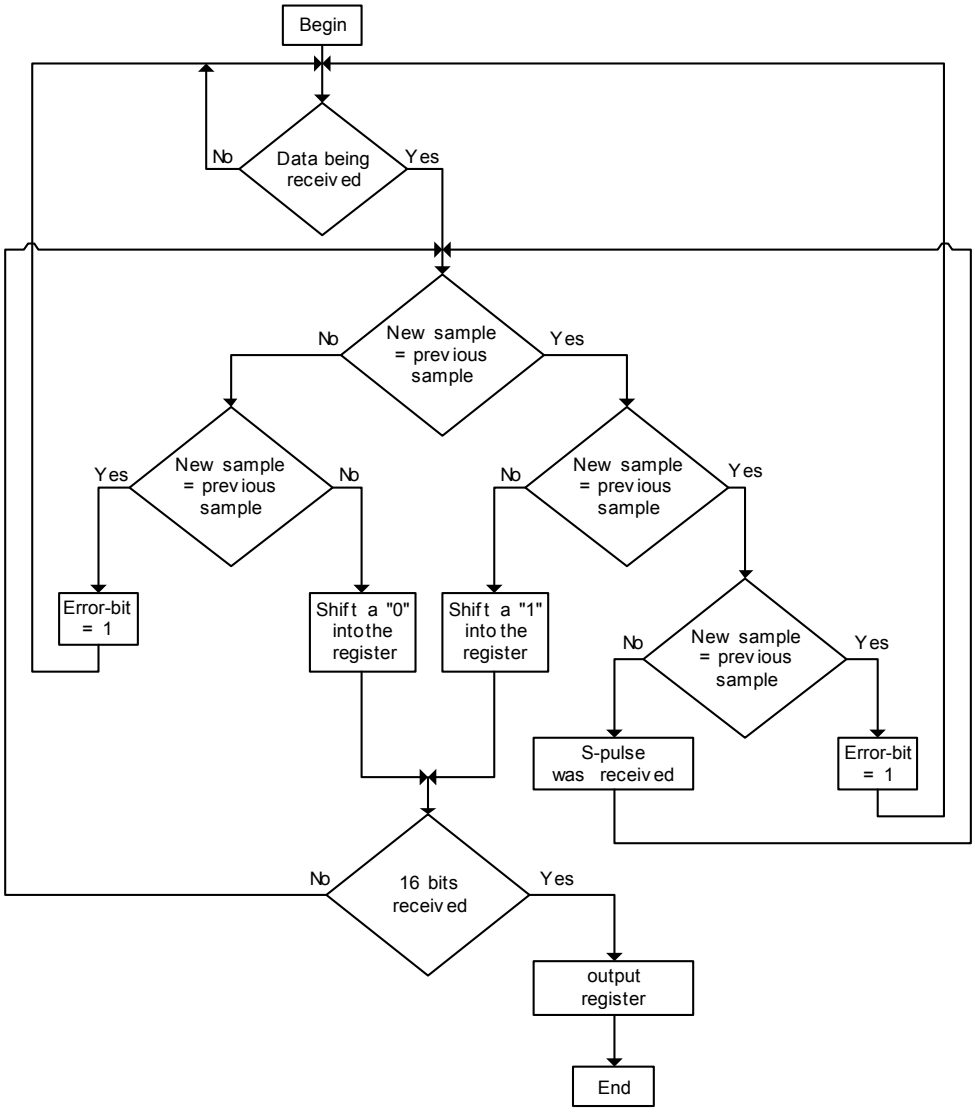

Figure 4.16 – Flowchart of the decoding VHDL code

4.2.5. - Results for the voltage measurements

Figure 4.17 shows an oscillograph of the encoded data that is transmitted by the VMB. The request signal from the controller is also shown. From the oscillograph it is seen that the data is requested every 9.96 µs.

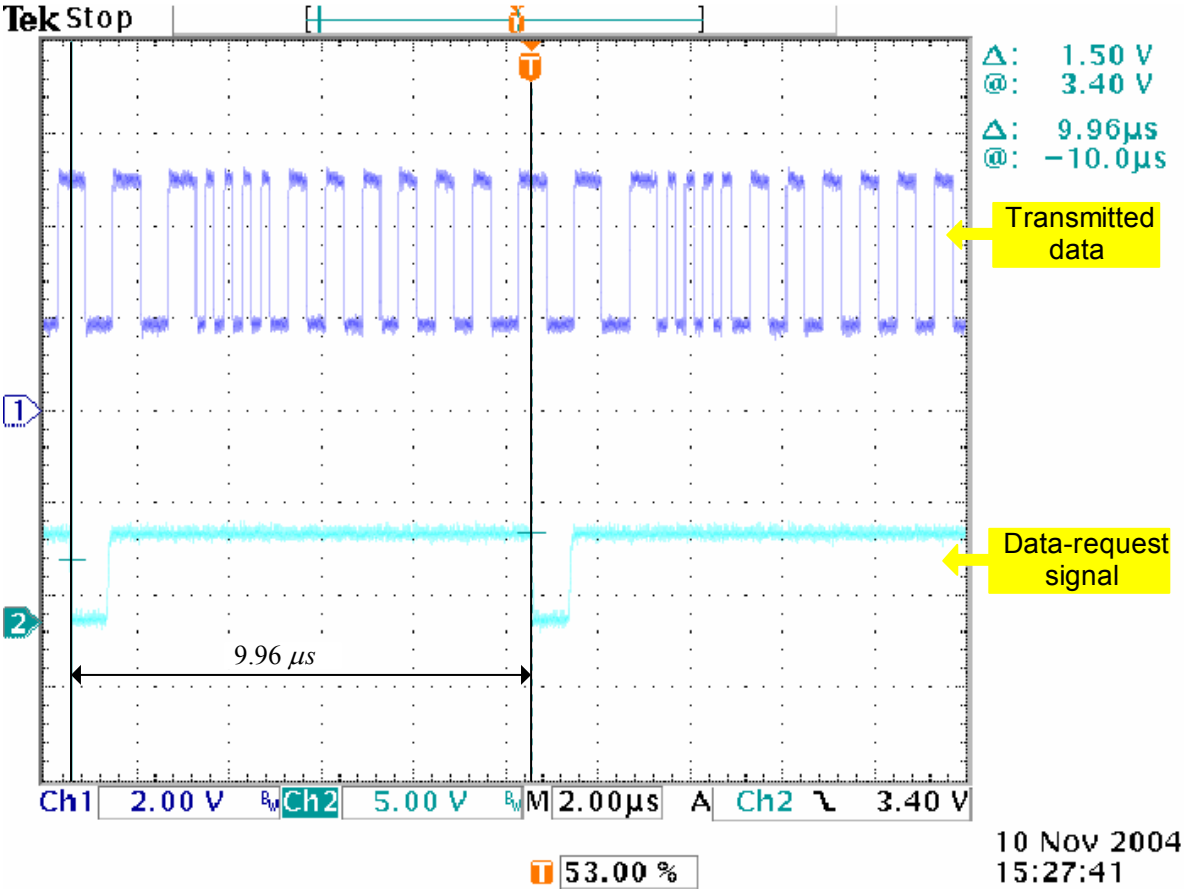

Figure 4.17 – Oscillograph of the encoded data on the VMB

Figure 4.18 is an oscillograph of the encoded data for a data sequence where all 12 encoded bits are 1-pulses. The 4 leading zeros that are added to the data sequence are also indicated. The S-pulses before and after the data sequence have a duration of 600 ns which is exactly as expected.

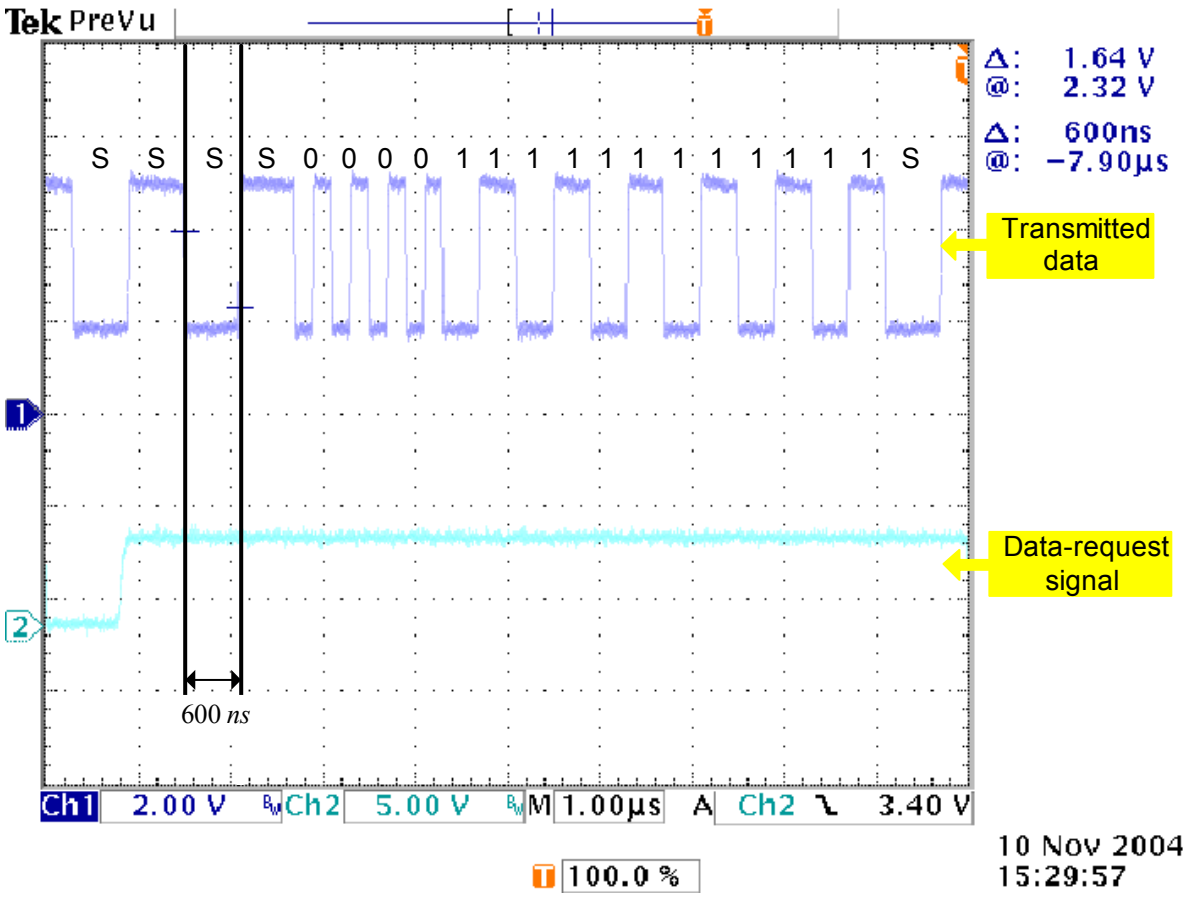

Figure 4.18 – Oscillograph of encoded data sequence

Figure 4.19 provides an oscillograph of some of the voltage measurements. The voltage waveforms in Figure 4.19 are that of the 6 line-to-line voltages measured with the AC-VMBs shown in Figure 4.5. The waveforms are obtained from the digital to analog converters (DAC) of the PEC33. It is concluded that the VMBs are operating satisfactory and that the encoding and decoding are functioning properly. It is also concluded that the PEC33 interprets the decoded data correctly.

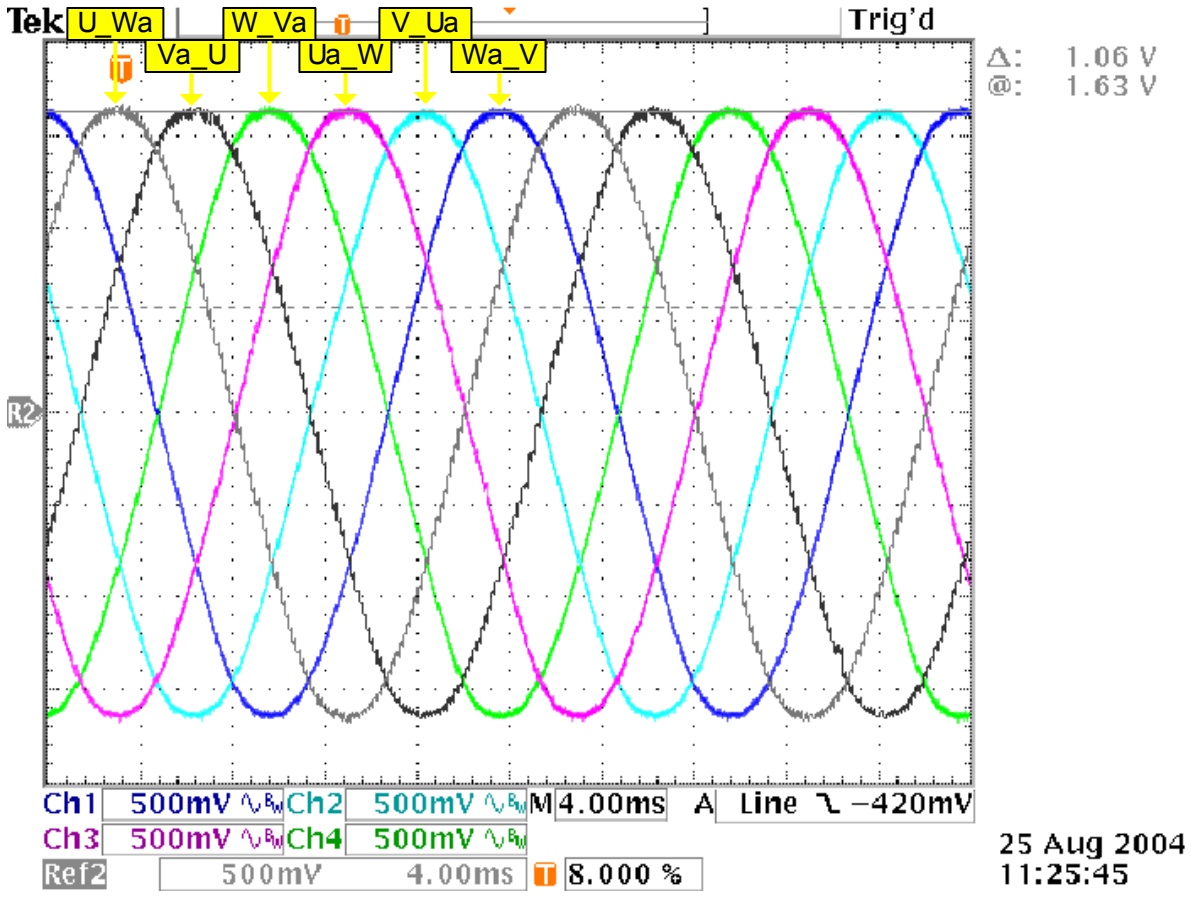

Figure 4.19 – Oscillograph of the voltage measurement results

4.3. - Current measurements

The harmonics created by the traction rectifier are between the ranges of 300 and 1 200 Hz [1]. The higher order harmonic components of the current measurements are required for the control of the system [2]. Therefore a delay in the current measurements, as with the voltage measurements, is not acceptable. To increase the transmission speed of the current measurements they are kept in their analog form. There is no conversion delay in an ADC and there are no encoding and decoding delays as with the voltage measurements. To be able to measure the current harmonics the probe must have a minimum bandwidth of DC to 1.2 kHz.

As mentioned in Chapter 3 the current rating of the 3-phase output of the inverter is 460 A_{rms} for each phase. For these 21 current measurements LEM LT 505-S current transducers are used. Table 4.3 provides some of the electrical data for the LT 505-S current transducer.

Table 4.3 – Electrical data for LT 505-S

Description	**Value**
Primary nominal rms current	500 A
Primary current measuring range	0…+/- 1200 A
Conversion ratio	1 : 5000
Rms voltage for AC isolation, 50Hz, 1 min	6 kV
Frequency bandwidth	DC – 150 kHz

From Table 4.3 it is seen that the current rating of this probe is sufficient. However the isolation for the LT 505-S is only 6 kV. This is lower than the specified isolation for the system [1]. Extra heat-shrink tubing is added between the probe and the bus-bar. BBIT heat-shrink tubing from Raychem is used for the added isolation. This heat-shrink provides isolation up to 36 kV. Figure 4.20 is a picture of 2 of the current probes at the output of the inverter.

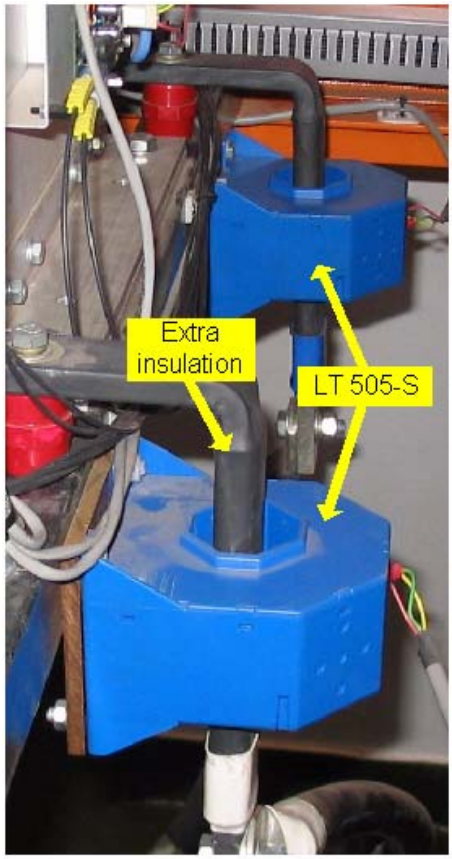

Figure 4.20 – LT 505-S current transducers at the output of the inverter

As shown in Figure 4.1 the 6-phase currents are measured at the input of the rectifier. The main criteria for choosing these current probes are the size of the bus-bar that the probe is mounted on. The bus-bar size is 50 mm by 10 mm. A LEM LT 2005-S current transducer was chosen for these measurements. The size of the hole in the probe is large enough so that it can accommodate the bus-bar. The current rating of the probe must also be sufficient for when the rectifier is under load. The current waveform for when the rectifier is under load is as shown in Figure 4.27. Only 1 diode is forward biased at a time. This implies that for that period when the diode is conducting, the entire load current is passing through that phase. The rectifier in the substation is rated for a load current of 3 kA. Observations have shown that the load current is very seldom more than 2 kA. Therefore the current rating of the LT 2005-S is sufficient. Table 4.4 provides some of the electrical data for the LEM LT 2005-S current transducer.

Table 4.4 – Electrical data for LT 2005-S

Description	**Value**
Primary nominal rms current	2000 A
Primary current measuring range	0…+/- 3000 A
Conversion ratio	1 : 5000
Rms voltage for AC isolation, 50Hz, 1 min	6 kV
Frequency bandwidth	DC – 100 kHz

The LT 2005-S also provides only 6 kV isolation. Extra heat-shrink tubing is added to increase the isolation. The same BBIT heat-shrink that is used on the 3-phase measurements is used here for the 6-phase measurements. Figure 4.21 is a photograph of the 6-phase current measurements.

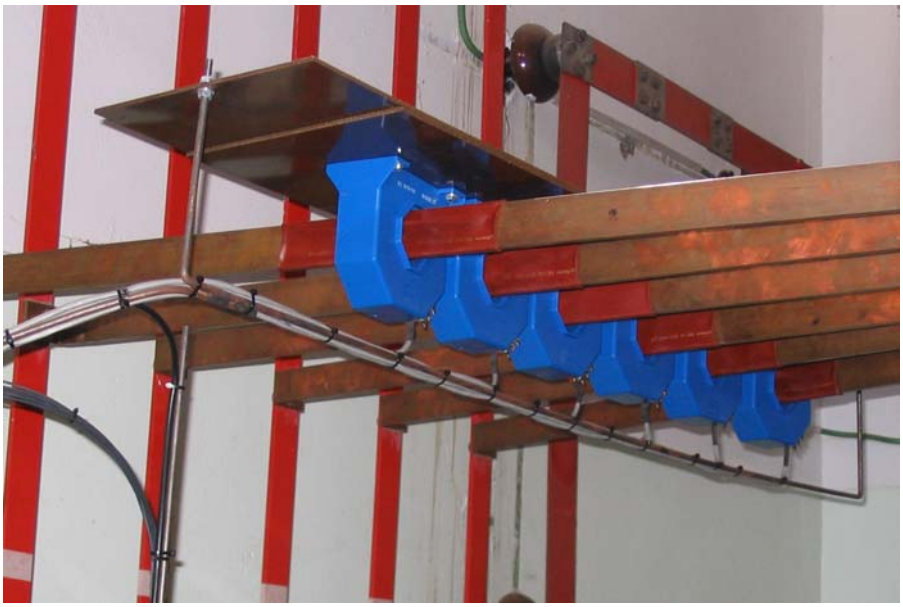

Figure 4.21 – LT 2005-S current transducers at the input of the rectifier

Both the LT 505-S and the LT 2005-S have a current output signal. This current signal is less susceptible to EMI than a voltage signal.

4.3.1. - Current Measurement Board (IMB)

The current measurements are sampled by the ADC of the PEC33. These ADCs require a voltage input signal. The purpose of the IMB is to convert the current signal received from the current probes, into a voltage signal. Furthermore the ADCs of the PEC33 have an input voltage range of 0 V to 4.096 V. The value of 4.096 V is due to the external voltage reference that the ADC uses. A REF198 voltage reference IC from Analog Devices is used for this purpose. The REF198 has a nominal output voltage of 4.096 V. The voltage signal that is obtained from the current measurements, vary around 0 V. In order for this signal to be compatible with the ADCs, the IMB must level-shift the measurements so that it varies around 2.048 V. Figure 4.22 provides an illustration of how the IMB level-shifts a sinusoidal signal.

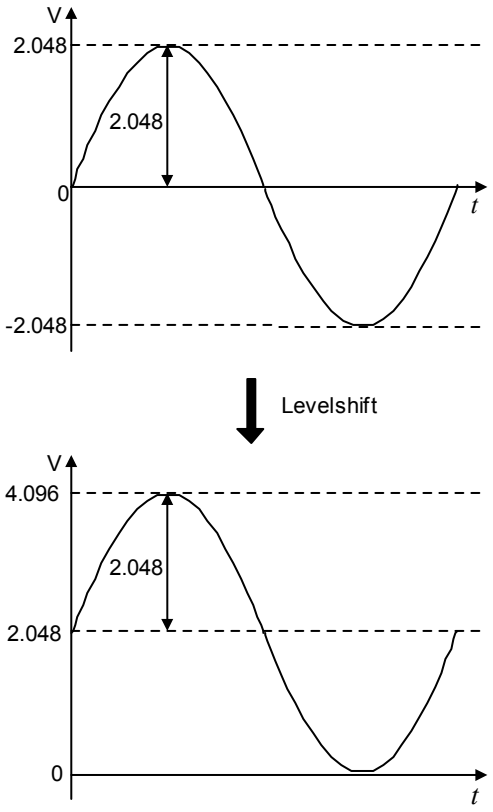

Figure 4.22 – Illustration of the level-shifting function of the IMB

Figure 4.23 provides a diagram of the IMB.

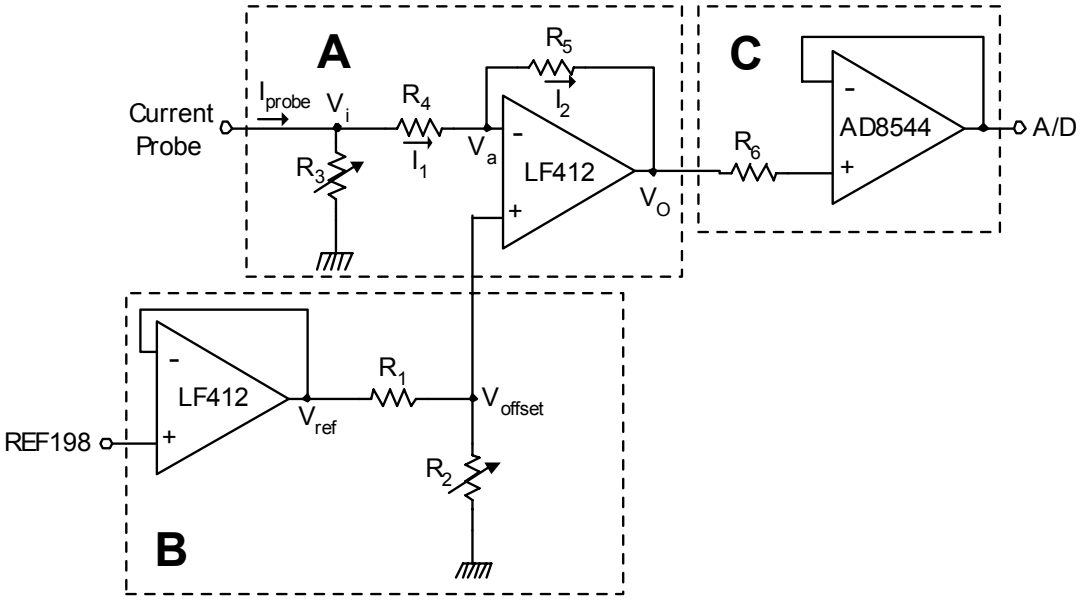

Figure 4.23 – Diagram of the IMB

Section A of the diagram in Figure 4.23 converts the current signal, which is received from the current probe, into a voltage signal with the aid of the multi-turn resistor at the input. The LF412 op-amp then level-shifts the voltage signal. Assuming that the LF412 is an ideal op-amp the following can be stated,

$$I_1 = I_2 \tag{4.29}$$

and

$$V_a = V_{offset} \tag{4.30}$$

Current I_1 is defined as

$$I_1 = \frac{V_i - V_a}{R_4} \tag{4.31}$$

The voltage V_O is defined as

$$V_O = V_a - I_2 R_5 \tag{4.32}$$

By using (4.29), (4.32) can also be written as

$$V_O = V_a - I_1 R_5 \tag{4.33}$$

Substituting (4.31) into (4.33) gives

$$\begin{aligned} V_O &= V_a - \left(\frac{V_i - V_a}{R_4} \right) R_5 \\ &= V_a - (V_i - V_a) \frac{R_5}{R_4} \end{aligned} \tag{4.34}$$

Substituting (4.30) into (4.34) gives

$$V_O = V_{offset} - \left(V_i - V_{offset}\right) \frac{R_5}{R_4} \tag{4.35}$$

A 100 kΩ resistor is used for R_4 and R_5. Substituting these values into (4.35) the output voltage V_O is defined as

$$V_O = 2\ V_{offset} - V_i \tag{4.36}$$

It should be noted from (4.36) that the input signal V_i is inverted and this must be taken into account in the control algorithms. Equation (4.36) also indicates that the gain of the level-shifter is 1. From Figure 4.22 it is seen that the maximum amplitude of the voltage signal that is connected to the ADCs of the PEC33 is 2.048 V. Due to the unity gain of the level-shifter, the amplitude of the voltage that is supplied to the ADCs is determined by V_i which in turn is determined by the resistor R_3 and the current signal received from the current probe. V_i is defined as

$$V_i = I_{probe}\ R_3 \tag{4.37}$$

For the maximum current that is measured by the probes R_3 is adjusted to so that V_i has a value of 2.048 V.

$$R_3 = \frac{2.048}{I_{\text{probe-max}}} \tag{4.38}$$

The 3-phase current measurements at the output of the inverter are calibrated for a peak value of 800 A. The LT 505-S current probe that is used for these measurements has a 1:5000 conversion ratio. For a measured current value of 800 A, the output of the probe will be 160 mA. Substituting this value for I_{probe} into (4.38) the value of R_3 is calculated.

$$\begin{aligned} R_3 &= \frac{2.048}{160 \times 10^{-3}} \\ &= 12.8\ \Omega \end{aligned} \tag{4.39}$$

The 6-phase current measurements are calibrated for a peak value of 2000 A. The LT 2005-S probes that are used for these measurements also have a conversion ratio of 1:5000. Using (4.38) the value of R_3 for the 6-phase current measurements is calculated.

$$R_3 = \frac{2.048}{400 \times 10^{-3}} = 5.12\ \Omega \tag{4.40}$$

A 100 Ω multi-turn resistor is used for R_3 on the IMB. Table 4.5 summarises the calibration values of the current measurements.

Table 4.5 – Summary of the current measurement calibration

Measurement	**Probe**	**Calibration**	**R_3**
3-phase	LT 505-S	800 A	12.8 Ω
6-phase	LT 2005-S	2000 A	5.12 Ω

Section B in Figure 4.23 illustrates the circuitry that provides the offset voltage for the level-shifter in section A. The voltage reference supplied to the ADCs on the PEC33 by the REF198 chip may vary due to changes in the temperature. This will cause variations in the input voltage range of the ADCs which lead to variations in the data that is produced by the ADCs. To minimise the error caused by this variations the same voltage reference from the REF198 is used for the generation of the offset voltage on the IMB. This ensures that the voltage signal that is sampled by the PEC33 varies with the same amount, hence minimizing the sampling error. The LF412 op-amp in section B is used as a buffer between the IMB and the REF198 on the PEC33. V_{offset} is generated by a voltage divider network consisting of R_1 and R_2.

$$V_{offset} = \frac{R_2}{R_1 + R_2}\ V_{ref} \tag{4.41}$$

Figure 4.22 indicates that the voltage signal from the probe must be shifted by a value of 2.048 V. Consequently a 0 V input to the level shifter must produce an output voltage of 2.048 V. Using (4.36) the offset voltage is calculated.

$$\begin{aligned} 2\ V_{offset} &= 2.048 \\ V_{offset} &= \frac{2.048}{2} \\ &= 1.024 \end{aligned} \tag{4.42}$$

A 100 kΩ resistor is used for R_1. Using a value of 4.096 V for V_{ref} and substituting (4.42) into (4.41) the value of R_2 is calculated.

$$\begin{aligned} R_1 V_{offset} + R_2 V_{offset} &= R_2 V_{ref} \\ R_2 \left(V_{offset} - V_{ref} \right) &= -R_1 V_{offset} \\ R_2 &= \frac{-R_1 V_{offset}}{V_{offset} - V_{ref}} \\ &= \frac{-100 \times 10^3 \cdot 1.024}{1.024 - 4.096} \\ &= 33.33\ k\Omega \end{aligned} \tag{4.43}$$

A 50 kΩ multi-turn resistor is used for R_2.

Section C in Figure 4.23 is a buffer between the output of the IMB and the input of the ADCs. The AD8544 op-amp has a supply voltage of 0 to 5 V. This ensures that the output voltage of the IMB will not exceed 5 V. This buffer protects the ADCs of the PEC33 from voltage spikes originating on the IMB. A 10 kΩ resistor is used for R_6. Figure 4.24 provides a photograph of the IMB with the different sections corresponding to Figure 4.23 indicated. The schematic of the IMB is provided in Appendix C.7.

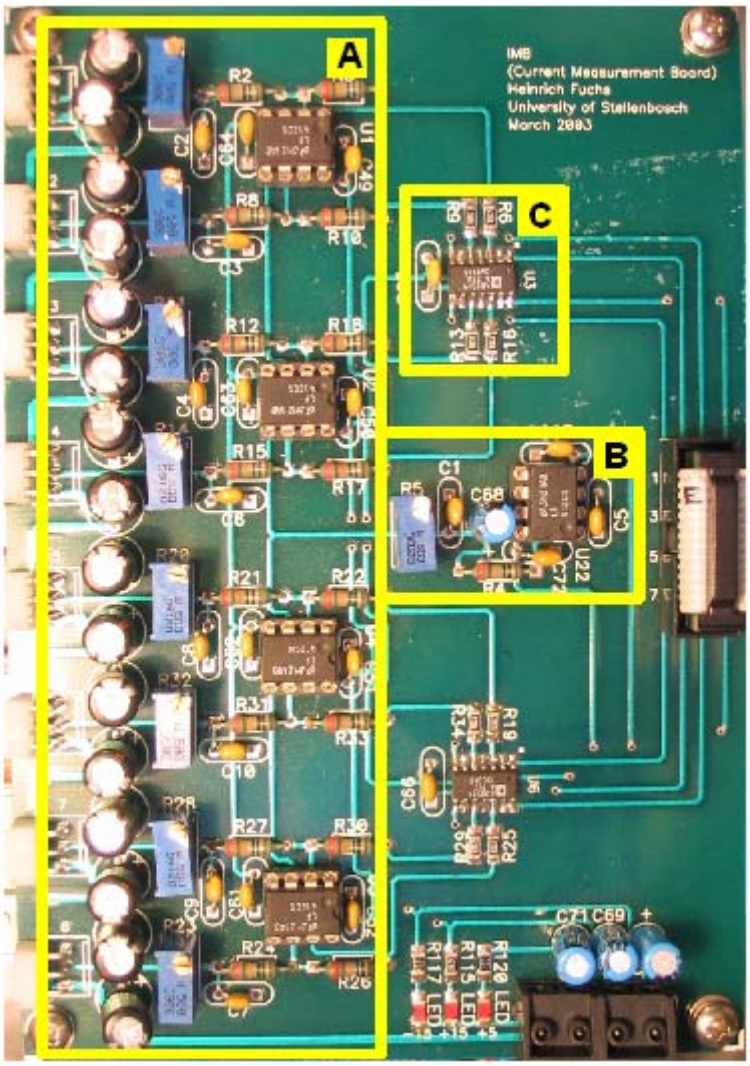

Figure 4.24 – Photograph of the IMB

One IMB has 8 channels to connect to current probes. There are 4 IMBs in the system providing 32 channels for current measurements. The +15 V and -15 V supply that is required by the currents probes is also provided by the IMB.

Figure 4.25 shows a photograph of the Wago terminal blocks that are used for the wiring of the 6-phase current measurements. Connected to each current probe is a 4-core 0.5^2 mm Mylar screened cable. The current probes require only 3 cores of each 4-core cable. The Wago terminal block connects each of the 3 cores from the 6 probes to an 18-core 0.5^2 mm Mylar screened cable. The 18-core cable connects to the controller through a circular connecter shown in Figure 4.26. The circular connector is a MIL-C-26482 Series II connector. The Mylar screen of the multi-core cables is a thin metal film around the cores of the cable to shield them from EMI. The screen of the 18-core cable is connected to the housing of the circular connecter which in turn is earthed through the casing of the controller. The 3-phase

current measurements at the output of the inverter are connected in the same manner as the 6-phase measurements.

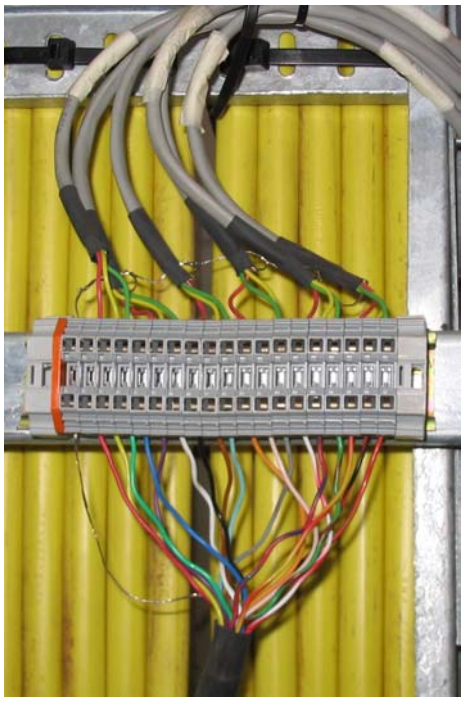

Figure 4.25 – Wago terminal used for the wiring of the current measurements

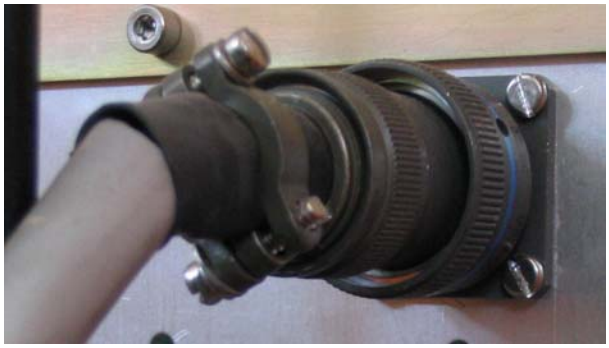

Figure 4.26 – Circular connector used for the current measurements

4.3.2. - Results for the current measurements

Figure 4.27 presents an oscillograph of the 6-phase current measurements on the input of the rectifier while the rectifier is under load. These measurement probes are shown in Figure 4.21. The waveforms in Figure 4.27 illustrate the characteristic current waveform for the 6-pulse rectifier. These measurements are obtained from the DAC of the PEC33. Although the amplitude of the waveforms is arbitrary the result shows that the IMB and the

current probes are operating correctly and that the PEC33 is interfacing properly with the IMB.

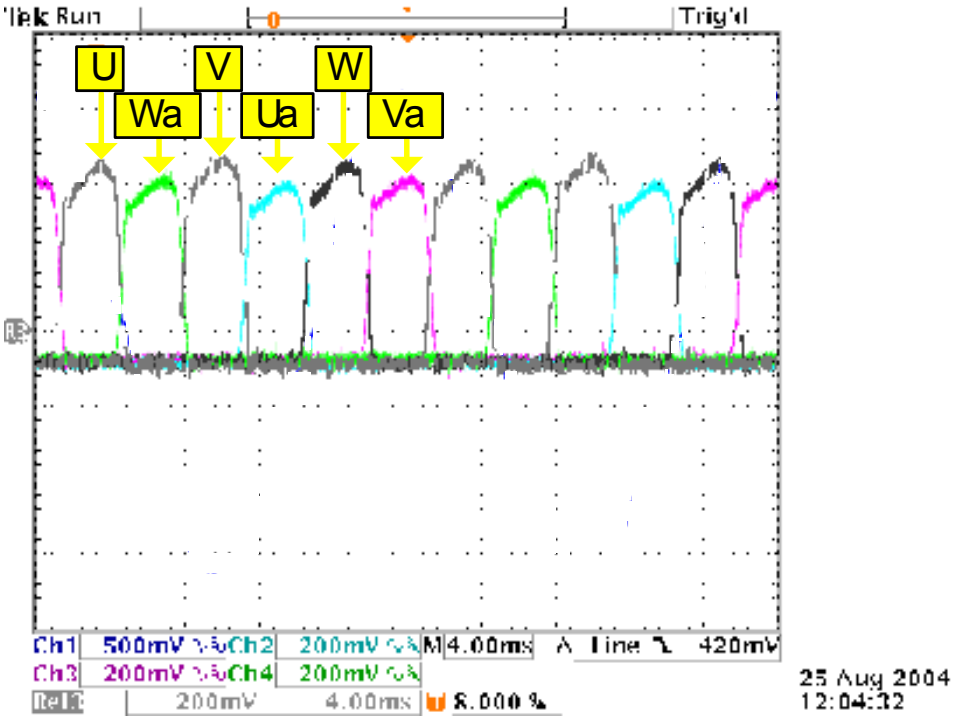

Figure 4.27 – Results for the current measurements

4.4. - Conclusion

Chapter 4 provides detailed descriptions of the voltage and current measurement system. The design, components and construction of the AC and DC voltage measurements as well as the current measurements are described. Explanations of the implementation of the software encoding and decoding of the voltage measurements are provided. The manner in which the current measurements interface with the PEC33 controller are also portrayed. Results are provided which indicate that the voltage and current measurement system is functioning correctly.

Chapter 5 - Injection Transformer

Chapter 5 starts by providing an overview of the supply transformer shown in Figure 1.1. Then the injection transformer is described in detail and the specifications for the injection transformer are calculated. Different loads on the secondary of the injection transformer are considered and the relationship between the primary and secondary currents is derived. Some simulation results are also provided.

5.1. - Supply Transformer

Connected as shown in Figure 1.2 the supply transformer steps the 66 kV_{LL} Eskom feed down to 2 420 V_{LL}. Table 5.1 lists the specifications of this transformer.

Table 5.1 –Specifications of the supply transformer

Description	**Value**
kVA	5 650
Phases	3 / 6
Voltage [V]	66000 / 2420
Current [A]	30.6 / 390
Oil cooled	

Figure 5.1 shows the polarity vector diagram of the supply transformer. The primary is a 3-phase star connection. The secondary is a triple-star connection with a 6-phase output.

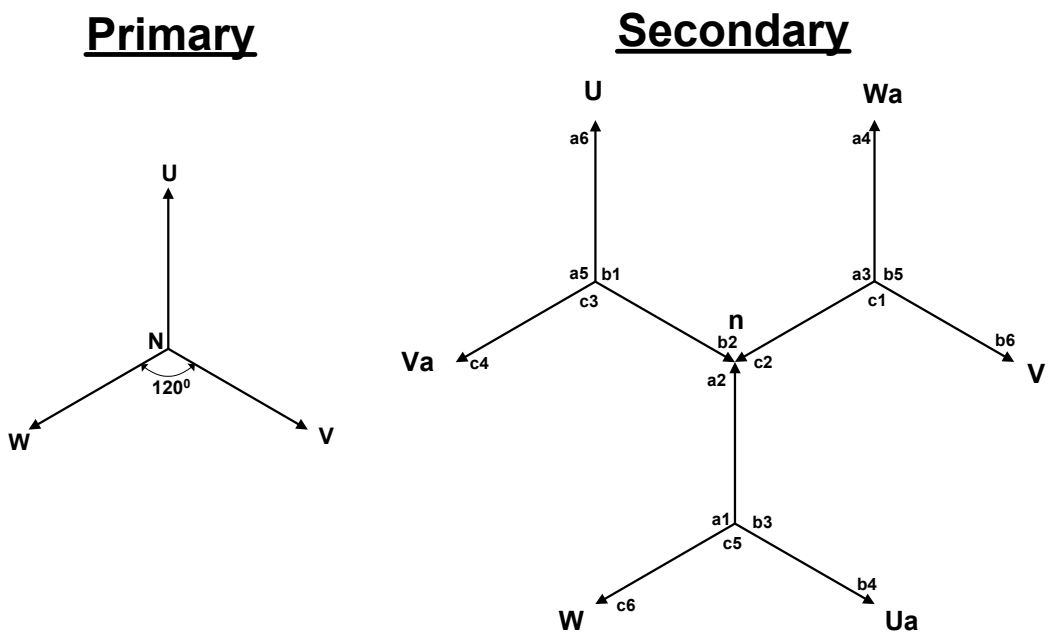

Figure 5.1 – Polarity vector diagram of supply transformer

5.2. - Injection Transformer

The purpose of the injection transformer is to add together the power delivered by each cell of the inverter. The injection transformer also converts the 3-phase output of the inverter to 6-phase so that the 3-phase output of the inverter is compatible with the 6-phase secondary of the supply transformer.

As shown in Figure 1.2 the secondary of the injection transformer connects to the secondary of the supply transformer. In order for the voltages and currents of the injection transformer to be compatible with the supply transformer, the secondary of the injection transformer must have the same configuration as the secondary of the supply transformer. The injection transformer has the same polarity vector diagram as the supply transformer shown in Figure 5.1. The 7 cells of the inverter make it necessary for the injection transformer to have 7 primary star windings. This is illustrated in Figure 5.2.

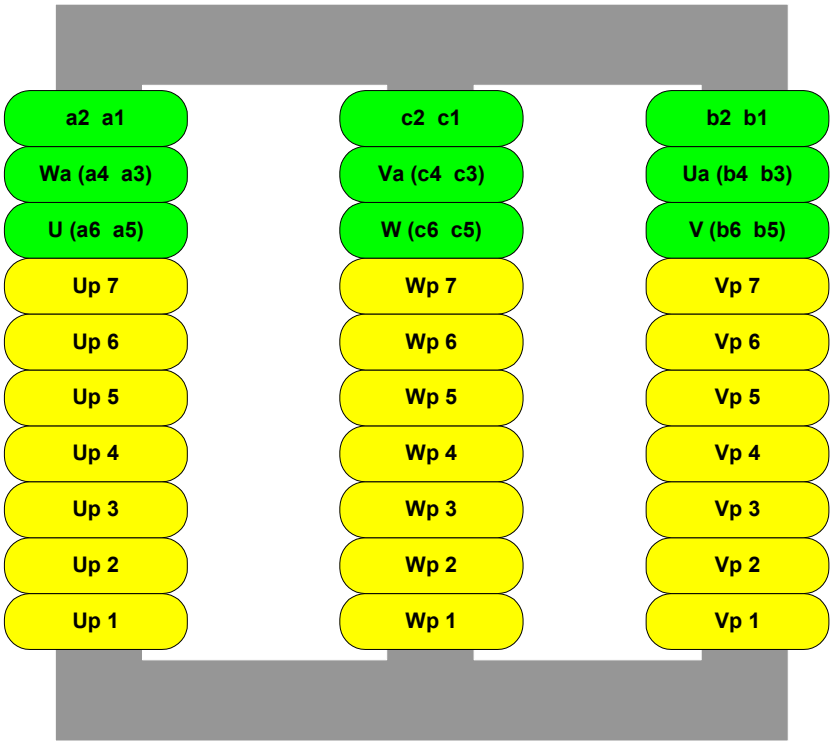

Figure 5.2 – Representation of the Injection Transformer

The flux from all the primary windings that are on the same leg of the core, adds together. From Figure 5.2 it is seen that the flux from all the U-windings, the W-windings and the V-windings adds together respectively, therefore the power from each phase of the inverter is summed by the injection transformer.

5.2.1. - Calculating the specifications for the Injection Transformer

In order to specify the rating of the transformer the voltages and currents for the primary and secondary must be calculated.

The calculations for the injection transformer are done for the regen-mode of operation of the system. During the regen-mode the power in the inverter and injection transformer is determined by the DC voltage connected to the train. The amount of electrical energy generated by the train is a factor of the gradient of the slope that the train is descending. As the descent increases the train must brake harder and thus more electrical energy is generated. As the train generates more energy the DC voltage increases. Two DC voltage values are chosen as the upper and lower limit for the regen-mode of the system. When the train is drawing power from the substation the DC voltages is approximately 3 kV. The lower limit for the regen-mode is chosen as 3.2 kV DC. The train has over voltage protection implemented on the locomotive that is set at 3.9 kV DC, therefore the upper limit of the

regen-mode is chosen as 3.9 kV. The injection transformer must be able to operate when the DC voltage of the substation varies between 3.2 kV and 3.9 kV.

For the following calculations assume that the injection transformer is an ideal transformer and that it is operating at a power factor of 1. The lower limit of 3.2 kV is considered first. Assume the following relationship for the 6-pulse rectifier [28], p105

$$V_{DC} = 1.35\, V_{LL} \tag{5.1}$$

The line-to-line voltage of the secondary of the injection transformer is calculated using (5.1).

$$\begin{aligned} V_{S\_LL} &= \frac{V_{DC}}{1.35} \\ &= \frac{3.2\times10^{3}}{1.35} \\ &= 2\ 370\, V_{rms} \end{aligned} \tag{5.2}$$

Assume the following relationship between the input and output voltages of the inverter [35], pp.376-386

$$V_{LL} = m_a\, V_{DC} \tag{5.3}$$

where m_a is the modulation index for the inverter. Taking m_a as 0.75 the line-to-line voltage of the primary of the injection transformer is calculated.

$$\begin{aligned} V_{P\_LL} &= 0.75\, \frac{V_{DC}/7}{\sqrt{2}} \\ &= 0.75\ \cdot \frac{457}{\sqrt{2}} \\ &= 242\, V_{rms} \end{aligned} \tag{5.4}$$

In order to calculate the current in the primary consider the power for each cell of the inverter.

$$P_{cell} = \frac{P_{tot}}{7} = \frac{1.5\times10^{6}}{7} = 214\ kW \tag{5.5}$$

The power in 1 phase of the primary is

$$P_{P\Phi} = \frac{P_{cell}}{3} = 71\ kW \tag{5.6}$$

The power in 1 phase of the primary is also defined by the following equation.

$$P_{P\Phi} = V_{P\_LN}\ I_{P\Phi} = \frac{V_{P\_LL}}{\sqrt{3}}\ I_{P\Phi} \tag{5.7}$$

Substituting (5.6) into (5.7) the current in 1 phase of the primary is calculated.

$$I_{P\Phi} = \frac{P_{P\Phi}\ \sqrt{3}}{V_{P\_LL}} = \frac{71\times10^{3}\cdot\sqrt{3}}{242} = 507\ A_{rms} \tag{5.8}$$

Assuming an ideal transformer, the power into the transformer equals the power out of the transformer. Therefore the current in 1 phase of the secondary is calculated as follows.

$$P_{S\Phi} = \frac{1.5\times10^{6}}{6} = 250\ kW \tag{5.9}$$

For a 6-phase system the amplitudes of the line-to-line and line-to-neutral voltages are the same.

$$|\mathbf{V_{LL}}| = |\mathbf{V_{LN}}| \tag{5.10}$$

Using (5.10) the power in 1 phase of the secondary is also defined as

$$\begin{aligned} P_{S\Phi} &= V_{S\_LN}\, I_{S\Phi} \\ &= V_{S\_LL}\, I_{S\Phi} \end{aligned} \tag{5.11}$$

Substituting (5.9) into (5.11) the current in 1 phase of the secondary is calculated.

$$\begin{aligned} I_{S\Phi} &= \frac{P_{S\Phi}}{V_{S\_LL}} \\ &= \frac{250\times10^3}{2370} \\ &= 105\ A_{rms} \end{aligned} \tag{5.12}$$

For the upper limit of the regen-mode, $V_{DC} = 3.9\ kV$, the voltages and currents are calculated in the same manner.

Table 5.2 summarises the calculated voltages and currents of the injection transformer for when the DC voltage is equal to 3.2 kV and 3.9 kV.

Table 5.2 – Calculation results for injection transformer

Description	**DC = 3.2 kV**	**DC = 3.9 kV**
V_{P_LL} [V_{rms}]	242	296
V_{S_LL} [V_{rms}]	2370	2889
$I_{P\Phi}$ [A_{rms}]	507	415
$I_{S\Phi}$ [A_{rms}]	105	86

From Table 5.2 it is seen that the highest voltage values on the primary and secondary occur when the DC voltage is at the upper limit of 3.9 kV and the highest current values occur when the DC voltage is at the lower limit of 3.2 kV. The specifications of the injection transformer are based on these values. Table 5.3 lists the specifications of the injection transformer.

Table 5.3 – Specifications of the injection transformer

Description	**Value**
kVA	1 500
V_{P_LL} / V_{S_LL} [V_{rms}]	300 / 3 000
$I_{P\Phi}$ / $I_{S\Phi}$ [A_{rms}]	500 / 100
Insulation between primary and secondary [kV]	12
Insulation between windings and frame [kV]	12
Air-cooled	

The value for the insulation is chosen as 12 kV. This is higher than the specified value of 10.5 kV [1]. The cooling method of the transformer is also specified in [1]. Figure 5.3 provides a photograph of the injection transformer that is installed in the Wolseley substation. Shown is the primary side of the transformer were the 3 phases with the 7 star connections can be seen.

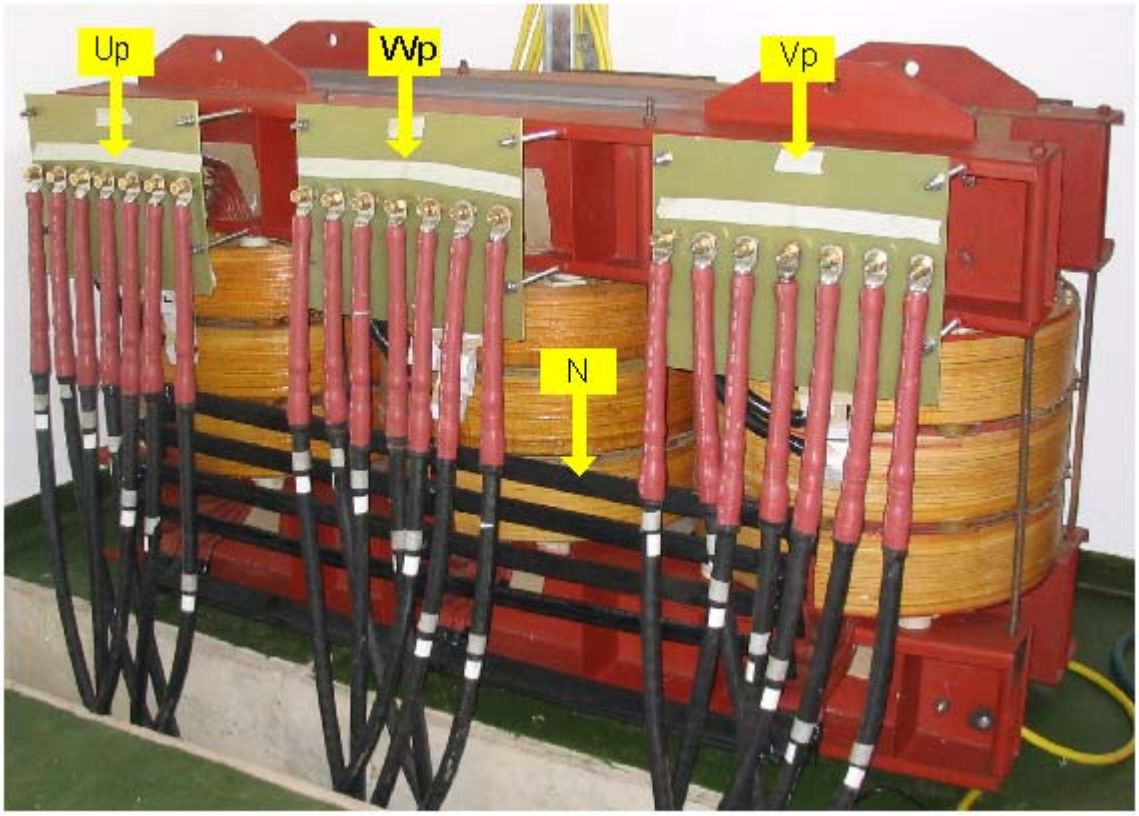

Figure 5.3 – Photograph of the injection transformer

5.3. - Calculating the line-to-line and line-to-neutral voltages of the injection transformer

The injection transformer has the same configuration as the supply transformer, therefore the line-to-line and line-to-neutral voltages are calculated with the help of Figure 5.1.

Figure 5.4 provides the vector diagram of the secondary with some of the line-to-line and line-to-neutral voltages indicated.

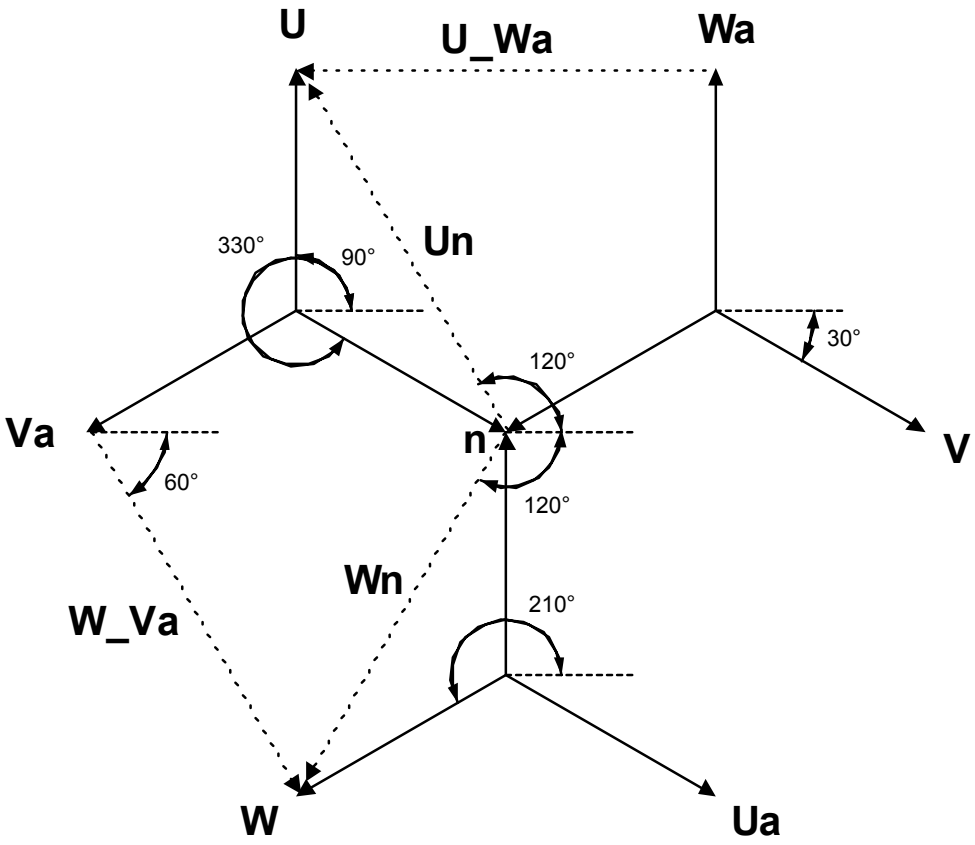

Figure 5.4 – Vector diagram indicating some of the line-to-line and line-to-neutral voltages

Voltages **U_Wa** and **W_Va** are line-to-line voltages and **Wn** and **Un** are line-to-neutral voltages.

5.3.1.- Calculating the line-to-neutral voltages

For the following calculations assume a 1:1 winding ratio and that the magnitude of the primary line-to-neutral voltages is 1.

$$\begin{aligned}\mathbf{U_{P\_LN}} &= 1\angle 90^0 \\ \mathbf{W_{P\_LN}} &= 1\angle 210^0 \\ \mathbf{V_{P\_LN}} &= 1\angle -30^0\end{aligned} \tag{5.13}$$

Due to the 1:1 winding ratio each vector in Figure 5.4 also has a magnitude of 1. From Figure 5.4 the line-to-neutral voltage **Un** is calculated as follows.

$$\begin{aligned}\mathbf{Un} &= -1\angle 330^0 + 1\angle 90^0 \\ &= \sqrt{3}\angle 120^0\end{aligned} \tag{5.14}$$

The voltage **Wn** is calculated in the same manner.

$$\begin{aligned}\mathbf{Wn} &= -1\angle 90^0 + 1\angle 210^0 \\ &= \sqrt{3}\angle -120^0\end{aligned} \tag{5.15}$$

The rest of the line-to-neutral voltages are calculated in the same manner as for **Un** and **Wn**.

Figure 5.5 provides a vector diagram of all the line-to-neutral voltages of the primary and the secondary.

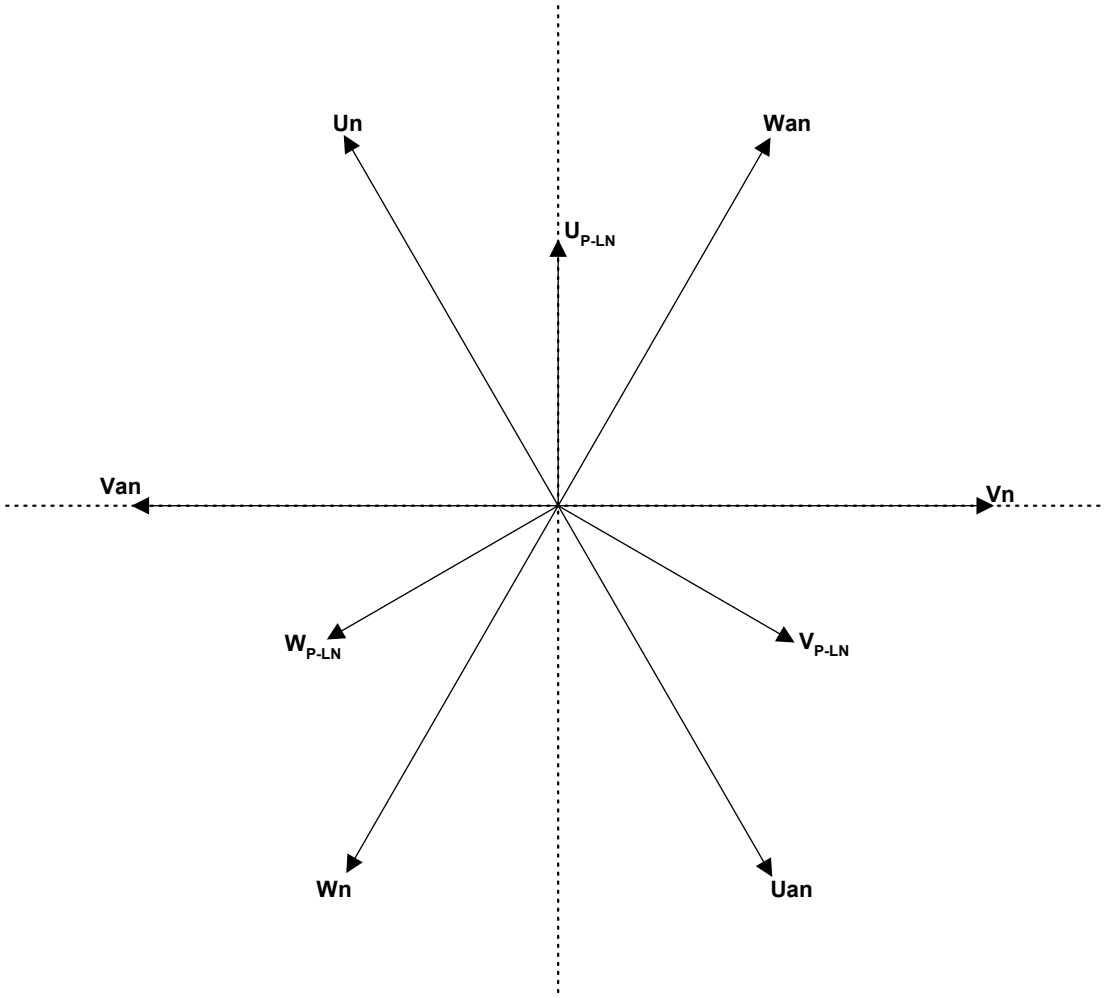

Figure 5.5 – Vector diagram of all the line-to-neutral voltages

The line-to-neutral voltages shown in Figure 5.5 are summarised in Table 5.4

Table 5.4 – Summary of the line-to-neutral voltages

Voltage	**Value**
U_{P-LN}	$1\angle 90^0$
W_{P-LN}	$1\angle 210^0$
V_{P-LN}	$1\angle -30^0$
Un	$\sqrt{3}\angle 120^0$
Wan	$\sqrt{3}\angle 60^0$
Vn	$\sqrt{3}\angle 0^0$
Uan	$\sqrt{3}\angle -60^0$
Wn	$\sqrt{3}\angle -120^0$
Van	$\sqrt{3}\angle 180^0$

The line-to-neutral voltage waveforms of the secondary for a sinusoidal input on the primary are shown in Figure 5.6.

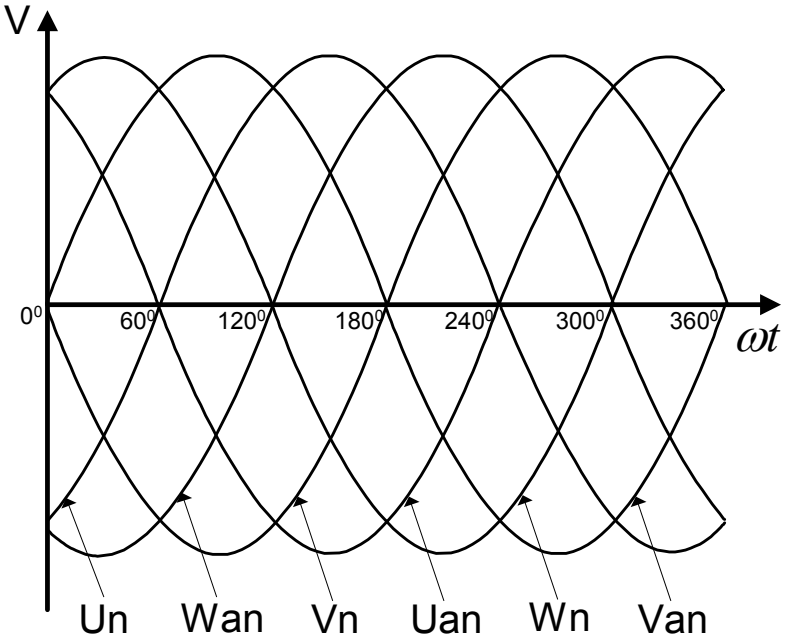

Figure 5.6 – Line-to-neutral voltage waveforms of the secondary for a sinusoidal input on the primary

5.3.2. - Calculating the line-to-line voltages

From Figure 5.4 the line-to-line voltage **W_Va** is calculated

$$\begin{aligned} \mathbf{W\_Va} &= -1\angle 210^0 + 1\angle -30^0 - 1\angle 90^0 + 1\angle 210^0 \\ &= \sqrt{3}\angle -60^0 \end{aligned} \tag{5.16}$$

and the voltage **U_Wa**.

$$\begin{aligned} \mathbf{U\_Wa} &= -1\angle 90^0 + 1\angle 210^0 - 1\angle -30^0 + 1\angle 90^0 \\ &= \sqrt{3}\angle 180^0 \end{aligned} \tag{5.17}$$

Figure 5.7 shows the line-to-line voltage $\mathbf{U_P\_V_P}$ on the primary.

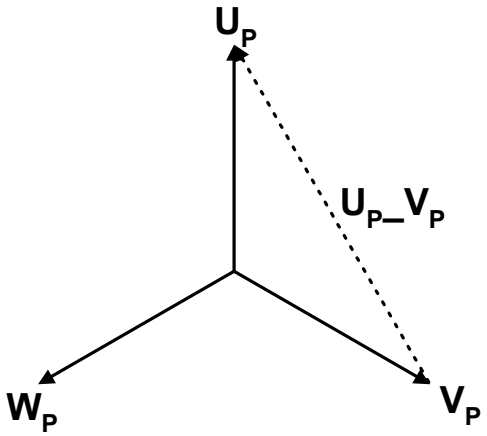

Figure 5.7 - The line-to-line voltage $U_P\_V_P$ on the primary

The voltage $\mathbf{U_P\_V_P}$ is calculated as follows.

$$\begin{aligned} \mathbf{U_P\_V_P} &= -1\angle -30^0 + 1\angle 90^0 \\ &= \sqrt{3}\angle 120^0 \end{aligned} \tag{5.18}$$

Figure 5.8 provides a vector diagram of all the line-to-line voltages.

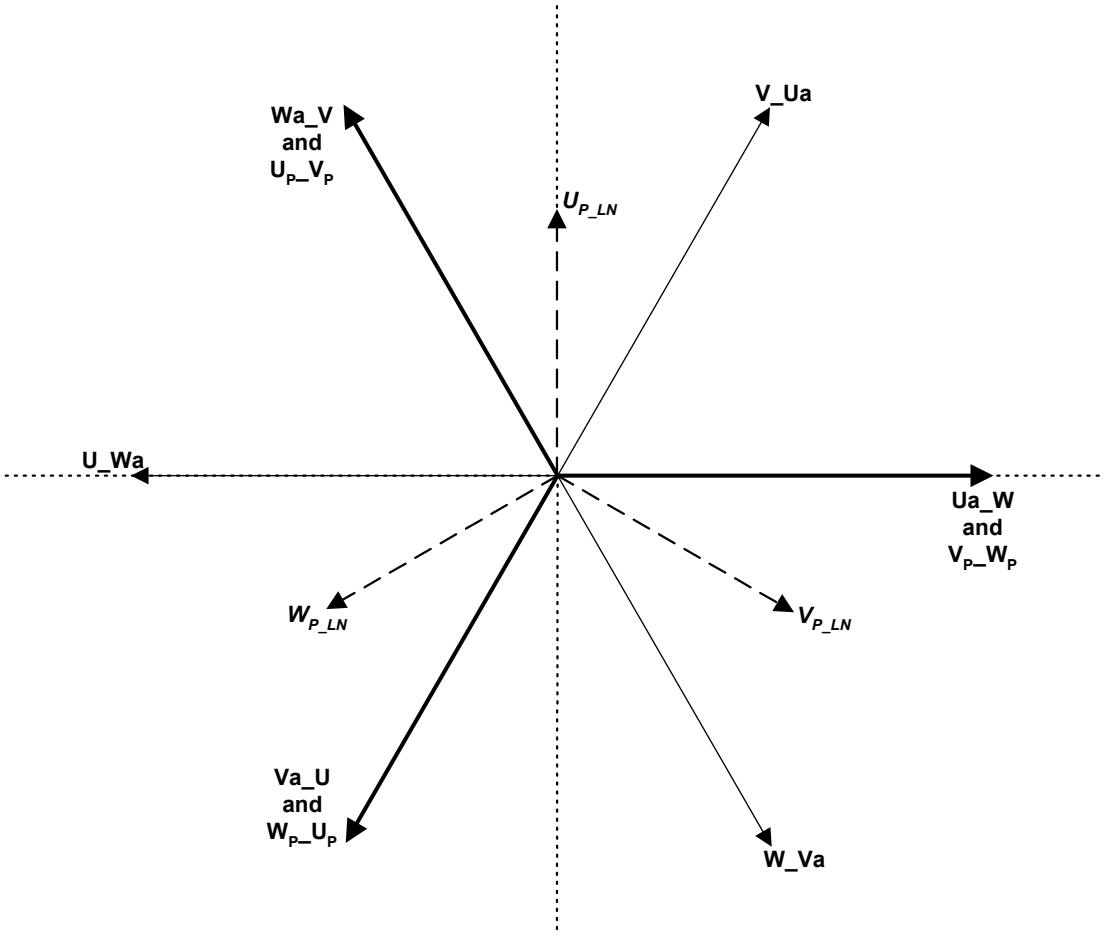

Figure 5.8 – Vector diagram of all the line-to-line voltages

Table 5.5 summarises all the line-to-line voltages.

Table 5.5 – Summary of the line-to-line voltages

Voltage	**Value**
U_P_V_P	$\sqrt{3}\angle 120^0$
V_P_W_P	$\sqrt{3}\angle 0^0$
W_P_U_P	$\sqrt{3}\angle -120^0$
Wa_V	$\sqrt{3}\angle 120^0$
V_Ua	$\sqrt{3}\angle 60^0$
Ua_W	$\sqrt{3}\angle 0^0$
W_Va	$\sqrt{3}\angle -60^0$
Va_U	$\sqrt{3}\angle -120^0$
U_Wa	$\sqrt{3}\angle 180^0$

From Figure 5.5 and Figure 5.8 it is seen that specific line-to-line and line-to-neutral voltages of the secondary corresponds to each other. Table 5.6 summarises this correspondence.

Table 5.6 – The correspondence between the line-to-neutral and line-to-line voltages of the secondary

Line-to-neutral		**Line-to-line**
Un	=	**Wa_V**
Wan	=	**V_Ua**
Vn	=	**Ua_W**
Uan	=	**W_Va**
Wn	=	**Va_U**
Van	=	**U_Wa**

5.3.3. - Relationship between the primary and secondary voltages

As mentioned in Chapter 4 the 6-phase line-to-line voltages on the secondary are measured. The control algorithms of the system need the 3-phase line-to-neutral voltages on the primary of the injection transformer [2]. Therefore it is necessary to transform the 6-phase line-to-line voltages of the secondary to the 3-phase line-to-neutral voltages of the primary. A relationship between the secondary and primary voltages must be established. Using Figure 5.8 and Table 5.5 the primary voltage $\mathbf{U_{P\_LN}}$ is derived from the secondary line-to-line voltages. Figure 5.9 illustrates how this is achieved.

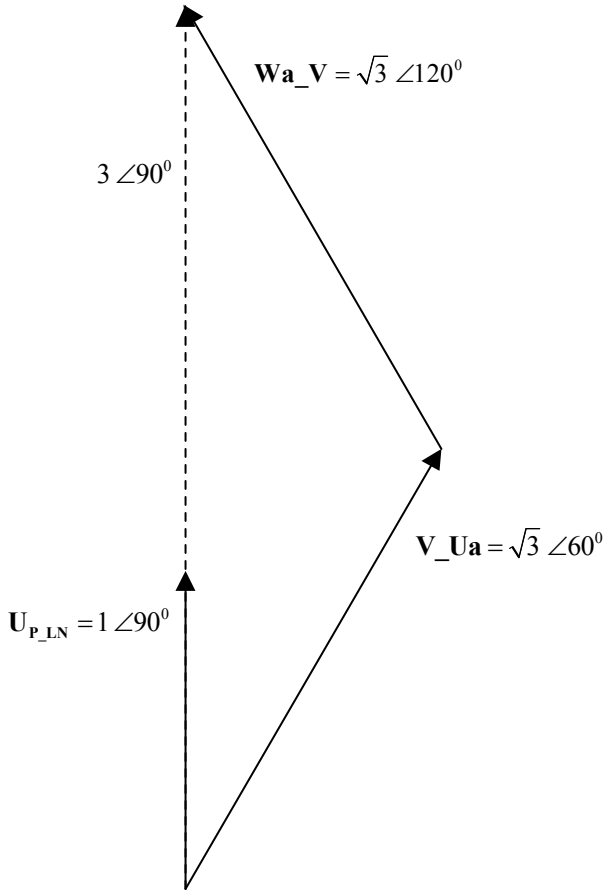

Figure 5.9 – Calculating $\boldsymbol{U_{P\_LN}}$ from the 6-phase voltages

The primary line-to-neutral voltage $\mathbf{U_{P\_LN}}$ is calculated by adding the line-to-line voltages **V_Ua** and **Wa_V** together and dividing the result by 3.

$$\begin{aligned}\mathbf{U_{P\_LN}} &= \frac{\mathbf{V\_Ua + Wa\_V}}{3} \\ &= \frac{\sqrt{3}\angle 60^0 + \sqrt{3}\angle 120^0}{3} \\ &= \frac{3\angle 90^0}{3} \\ &= 1\angle 90^0\end{aligned} \tag{5.19}$$

Voltages $\mathbf{V_{P\_LN}}$ and $\mathbf{W_{P\_LN}}$ are derived in the same manner. By using the method in (5.19) the 3-phase primary voltages can be derived form the 6-phase voltage measurements on the secondary of the injection transformer.

5.4. - Different loads on the secondary of the injection transformer

As with the voltage measurements it is necessary to have a relationship between the secondary and primary currents. As mentioned in Chapter 4 the 6-phase currents on the secondary of the injection transformer at the input of the rectifier are measured. The following calculations establish a relationship between the primary and secondary currents for different types of loads on the secondary.

Four loads are considered

- A resistive load
- Capacitive load
- 6-pulse rectifier
- The supply transformer as a load

A sinusoidal voltage source is used for all the different loads.

5.4.1. - Resistive load

The resistive load is connected in a star connection as shown in Figure 5.10.

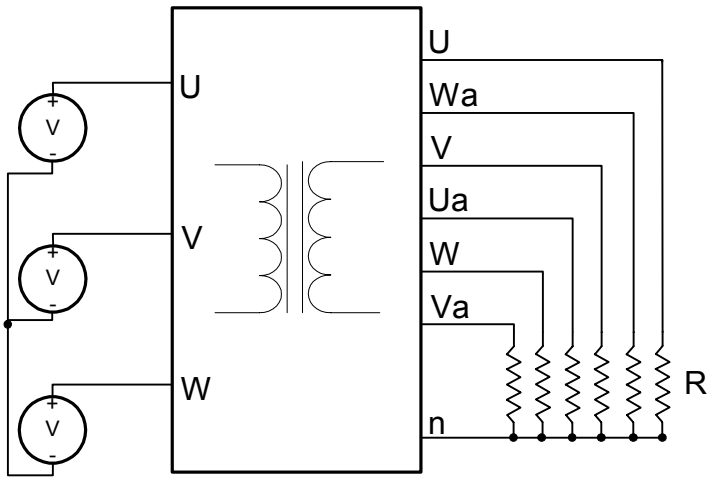

Figure 5.10 – Connection of resistive load

In Figure 5.11 the vector diagram for the secondary of the injection transformer is combined with Figure 5.10.

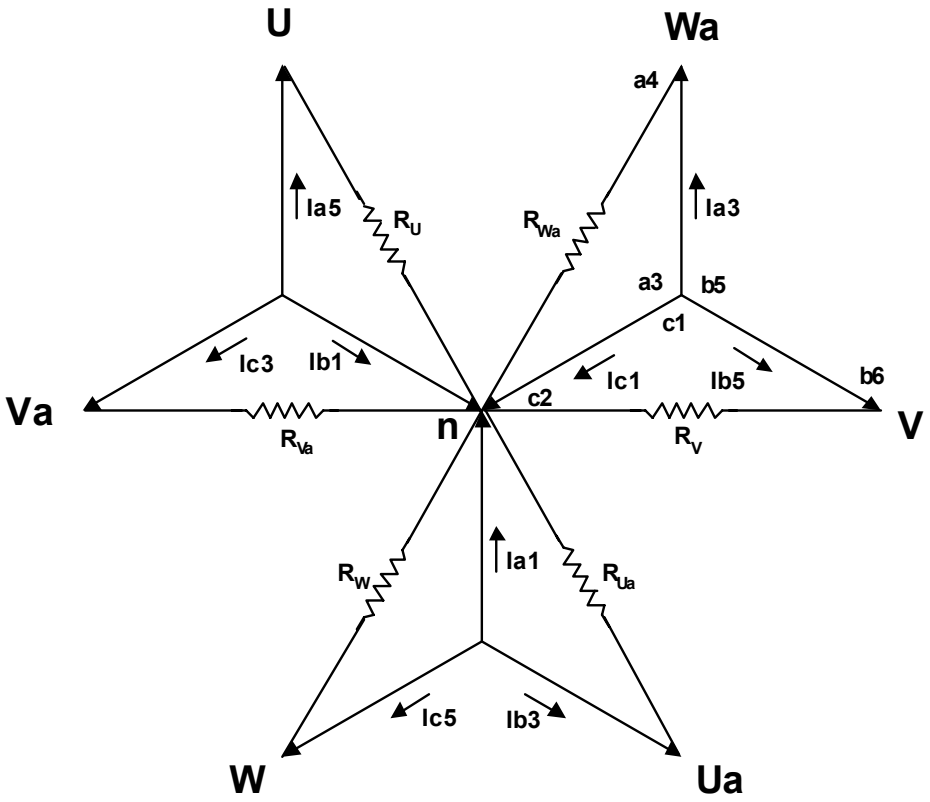

Figure 5.11 – Vector diagram with a resistive load

For calculation purposes Figure 5.11 is simplified to show only one part of the triple-star connection.

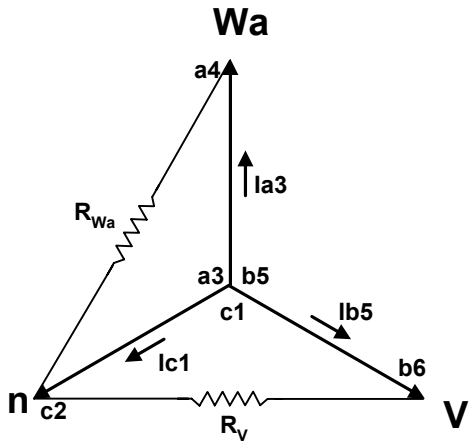

Figure 5.12 – Resistive load for 1 part of the triple star connection of the secondary

The phase of the current **Ia3** is determined by the load $R_{Wa.}$ The voltage across R_{Wa} is the line-to-neutral voltage **Wan**. Therefore the phase of current **Ia3** is the same as the phase of **Wan**

$$\begin{aligned} \angle \mathbf{Ia3} &= \angle \mathbf{Wan} \\ &= 60^0 \end{aligned} \tag{5.20}$$

where the phase of voltage **Wan** is listed in Table 5.4. Current **Ib5** has the same phase as the voltage **Vn.**

$$\begin{aligned} \angle \mathbf{Ib5} &= \angle \mathbf{Vn} \\ &= 0^0 \end{aligned} \tag{5.21}$$

To balance the currents in the star connection the current **Ic1** is the negative of the sum of **Ia3** and **Ib5**. For calculation purposes assume a magnitude of 1 for the currents **Ia3** and **Ib5**. **Ic1** is then defined as

$$\begin{aligned} \mathbf{Ic1} &= -(\mathbf{Ia3} + \mathbf{Ib5}) \\ &= -(1\angle 60^0 + 1\angle 0^0) \\ &= \sqrt{3}\angle -150^0 \end{aligned} \tag{5.22}$$

Figure 5.13 provides a vector diagram for the currents **Ia3**, **Ib5** and **Ic1**.

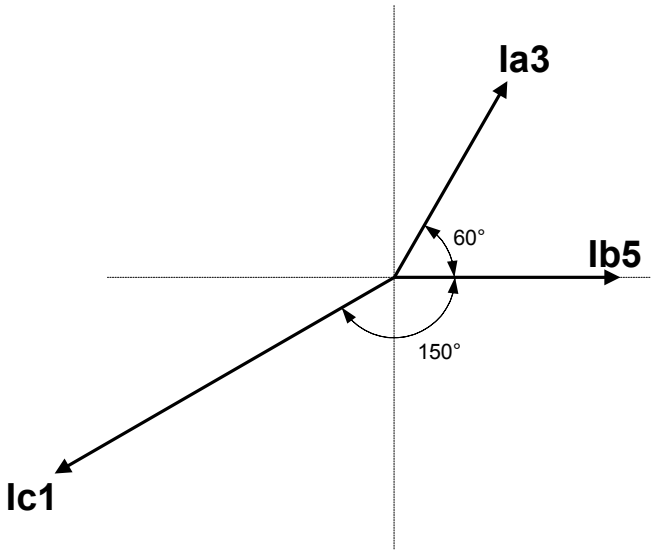

*Figure 5.13 – Vector diagram for currents **Ia3**, **Ib5** and **Ic1***

The currents **Ia5** and **Ia1** indicated in Figure 5.11 are calculated in the same manner.

$$\begin{aligned} \mathbf{Ia1} &= -(\mathbf{Ic5} + \mathbf{Ib3}) \\ &= -(1\angle -120^0 + 1\angle -60^0) \\ &= \sqrt{3}\angle 90^0 \end{aligned} \tag{5.23}$$

and

$$\begin{aligned} \mathbf{Ia5} &= 1\angle Un \\ &= 1\angle 120^0 \end{aligned} \tag{5.24}$$

Assuming a 1:1 winding ratio the relationship between the primary and secondary currents is calculated. Figure 5.2 shows that the coils for phase U of the primary are wound on the same leg of the transformer as the coils, a1 to a6. Also from Figure 5.1 it is seen that the vectors a1 to a6 has the same orientation as that of **IUp.** Therefore the primary current **IUp** is the combination of the currents **Ia1**, **Ia3** and **Ia5**.

$$\begin{aligned} \mathbf{IUp} &= \mathbf{Ia1} + \mathbf{Ia3} + \mathbf{Ia5} \\ &= \sqrt{3}\angle 90^0 + 1\angle 60^0 + 1\angle 120^0 \\ &= 3.464\angle 90^0 \end{aligned} \tag{5.25}$$

Figure 5.14 provides a vector diagram illustrating the relationship between the primary and secondary currents as defined in (5.25).

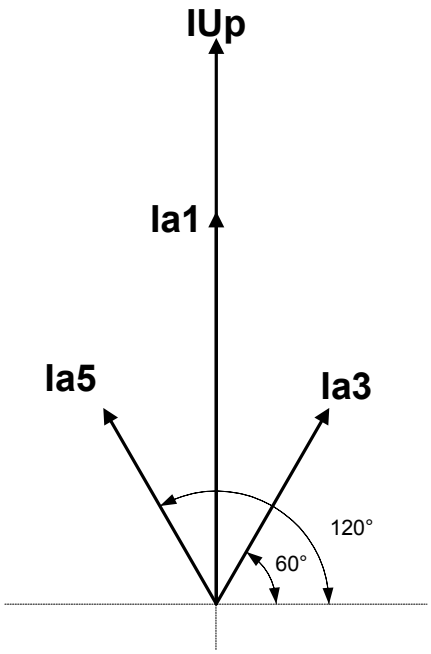

Figure 5.14 – Relationship between the primary and secondary currents

The current **Ia1** can also be defined as the combination of **IW** and **IUa**.

$$\mathbf{Ia1} = -(\mathbf{IW} + \mathbf{IUa}) \tag{5.26}$$

Using (5.26) and noting that the currents **Ia3** and **Ia5** are the same as the phase currents **IWa** and **IU** respectively, (5.25) is rewritten as

$$\begin{aligned} \mathbf{IUp} &= -(\mathbf{IW} + \mathbf{IUa}) + \mathbf{IWa} + \mathbf{IU} \\ &= -(1\angle -120^0 + 1\angle -60^0) + 1\angle 60^0 + 1\angle 120^0 \\ &= 3.464\angle 90^0 \end{aligned} \tag{5.27}$$

The amplitude of the currents **IWa** and **IU** is determined by the load current $\mathbf{I_R}$.

$$\mathbf{I_R} = \frac{\mathbf{V_R}}{R} \tag{5.28}$$

where $\mathbf{V_R}$ is the voltage across the load resistor. Using (5.28) and adding the winding ratio, (5.27) is rewritten to take in account the amplitude of the phase currents.

$$\mathbf{IUp} = 3.464 \ \frac{N_2}{N_1} \mathbf{I_R} \angle 90^0 \tag{5.29}$$

Due to the 7 windings of the primary (5.29) must be divided by 7 to give the current in one of the primary U phases.

$$\mathbf{IUp} = \frac{3.464}{7} \ \frac{N_2}{N_1} \mathbf{I_R} \angle 90^0 \tag{5.30}$$

As mentioned earlier only the 6-phase currents are measured. Therefore it is necessary to derive a relationship between the primary and secondary currents. Combining (5.27) and (5.30) a general equation for the relationship between **IUp** and the secondary phase currents can be written as

$$\mathbf{IUp} = \frac{1}{7} \frac{N2}{N1} \left(-(\mathbf{IW} + \mathbf{IUa}) + \mathbf{IWa} + \mathbf{IU}\right) \tag{5.31}$$

Utilizing the same method that is used tot determine **IUp** the currents **IVp** and **IWp** are defined in terms of the secondary currents as

$$\begin{aligned} \mathbf{IVp} &= \frac{1}{7} \frac{N2}{N1} \left(-\left(\mathbf{IU} + \mathbf{IVa}\right) + \mathbf{IV} + \mathbf{IUa}\right) \\ \mathbf{IWp} &= \frac{1}{7} \frac{N2}{N1} \left(-\left(\mathbf{IWa} + \mathbf{IV}\right) + \mathbf{IW} + \mathbf{IVa}\right) \end{aligned} \tag{5.32}$$

Table 5.7 provides a summary of the currents for a resistive load.

Table 5.7 – Summary of the currents for a resistive load

Current	**Value**
IUn	$\mathbf{I_R}\angle 120^0$
IWan	$\mathbf{I_R}\angle 60^0$
IVn	$\mathbf{I_R}\angle 0^0$
IUan	$\mathbf{I_R}\angle -60^0$
IWn	$\mathbf{I_R}\angle -120^0$
IVan	$\mathbf{I_R}\angle 180^0$
Ia1	$\sqrt{3}\,\mathbf{I_R}\angle 90^0$
Ib1	$\sqrt{3}\,\mathbf{I_R}\angle -30^0$
Ic1	$\sqrt{3}\,\mathbf{I_R}\angle 210^0$
IUp	$\frac{3.464}{7}\frac{N2}{N1}\mathbf{I_R}\angle 90^0$
IWp	$\frac{3.464}{7}\frac{N2}{N1}\mathbf{I_R}\angle 210^0$
IVp	$\frac{3.464}{7}\frac{N2}{N1}\mathbf{I_R}\angle -30^0$

5.4.2. - Capacitive load

The capacitive load is connected in the same way as the resistive load shown in Figure 5.10. A capacitive load produces a 90^0 phase shift between the current and voltage of the load. The voltages are the same as for the resistive load but the currents are shifted so that it leads the voltages by 90^0. Table 5.8 lists the currents for a capacitive load.

Table 5.8 – Summary of the currents for a capacitive load

Current	**Value**
IUn	$\mathbf{I_R}\angle 210^0$
IWan	$\mathbf{I_R}\angle 150^0$
IVn	$\mathbf{I_R}\angle 90^0$
IUan	$\mathbf{I_R}\angle 30^0$
IWn	$\mathbf{I_R}\angle -30^0$
IVan	$\mathbf{I_R}\angle -90^0$
Ia1	$\sqrt{3}\,\mathbf{I_R}\angle 180^0$
Ib1	$\sqrt{3}\,\mathbf{I_R}\angle 60^0$
Ic1	$\sqrt{3}\,\mathbf{I_R}\angle -60^0$
IUp	$\frac{3.464}{7}\frac{N2}{N1}\mathbf{I_R}\angle 180^0$
IWp	$\frac{3.464}{7}\frac{N2}{N1}\mathbf{I_R}\angle -60^0$
IVp	$\frac{3.464}{7}\frac{N2}{N1}\mathbf{I_R}\angle 60^0$

Equation (5.31) and (5.32) can also be used to describe the relationship between the primary and secondary currents for this type of load.

5.4.3. - 6-Pulse Rectifier load

The 6-pulse rectifier in the substation is connected as shown in Figure 1.2. For the following calculations the rectifier is connected as shown in Figure 5.15.

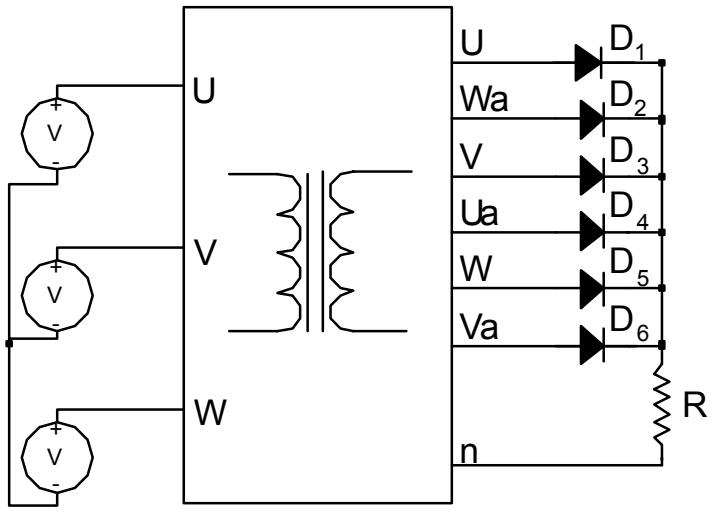

Figure 5.15 – Connection of 6-pulse rectifier for calculations

Due to the 6-phase voltage waveform shown in Figure 5.6 only one diode is forward biased at a time. The resulting current waveform is as shown in Figure 5.16 which shows the waveform of 3 of the phase currents for the rectifier load.

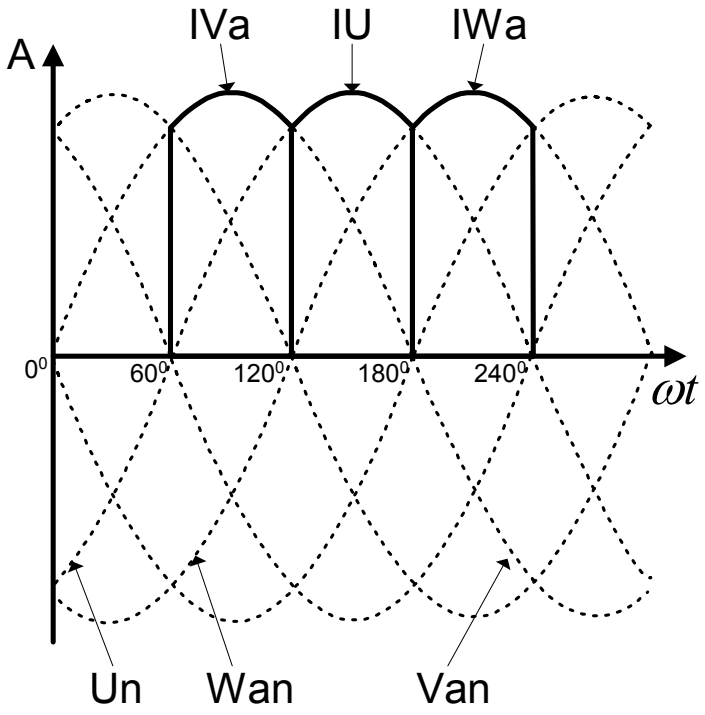

Figure 5.16 – Phase currents with a rectifier load

For the period, $180^0 \langle \omega t \langle 240^0$, diode D2 is conducting. Figure 5.17 presents one part of the triple star connection of the secondary for the time when diode D_2 is conducting.

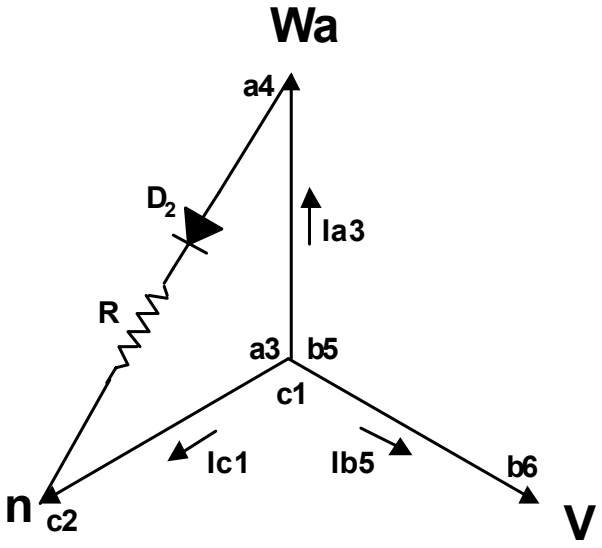

Figure 5.17 – One part of the secondary for when D_2 is conducting

The current for diode D_2 is the same as the phase current **IWa**. Assuming an ideal diode the current for diode D_2 is defined as follows.

$$\mathbf{IWa} = \mathbf{Ia3} = \begin{cases} \mathbf{I_R} & when \quad 180^0 \langle \omega t \langle 240^0 \\ 0 & elsewhere \end{cases} \tag{5.33}$$

where $\mathbf{I_R}$ is the current through the resistor. The current **Ib5** is defined as

$$\mathbf{IV} = \mathbf{Ib5} = \begin{cases} \mathbf{I_R} & when \quad 240^0 \langle \omega t \langle 300^0 \\ 0 & elsewhere \end{cases} \tag{5.34}$$

In the star connection shown in Figure 5.17 the current **Ic1** must balance the currents **Ia3** and **Ib5**. This results in a waveform as shown in Figure 5.18.

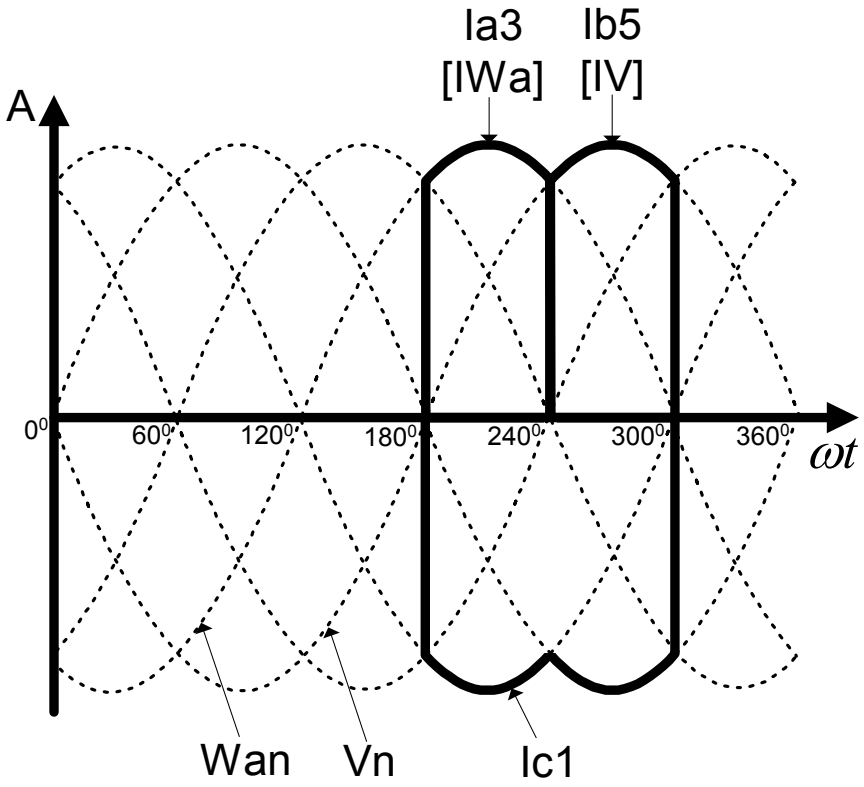

*Figure 5.18 – Current **Ic1** balancing currents **Ia3** and **Ib5***

The current **Ic1** is defined as follows

$$\mathbf{Ic1} = \begin{cases} -\mathbf{Ia3} & when \quad 180^0 \langle \omega t \langle 240^0 \\ -\mathbf{Ib5} & when \quad 240^0 \langle \omega t \langle 300^0 \\ 0 & elsewhere \end{cases} \tag{5.35}$$

The current **Ia1,** indicated in Figure 5.11, must balance the currents **Ic5** and **Ib3. Ia1** is defined as

$$\mathbf{Ia1} = \begin{cases} -\mathbf{Ib3} & when \quad 300^0 \langle \omega t \langle 0^0 \\ -\mathbf{Ic}5 & when \quad 0^0 \langle \omega t \langle 60^0 \\ 0 & elsewhere \end{cases} \tag{5.36}$$

As for the resistive load **IUp** is the sum of the currents **Ia1, Ia3** and **Ia5**.

$$\mathbf{IUp} = \mathbf{Ia1} + \mathbf{Ia3} + \mathbf{Ia5} \tag{5.37}$$

Taking the 7 primary windings into account and adding the winding ratio, (5.37) is rewritten. Also substituting (5.36) into (5.37) produces

$$\mathbf{IUp} = \frac{1}{7}\,\frac{N2}{N1}\begin{cases}\mathbf{Ia1} & when \quad 300^0 \langle \omega t \langle 60^0 \\ \mathbf{Ia}5 & when \quad 120^0 \langle \omega t \langle 180^0 \\ \mathbf{Ia3} & when \quad 180^0 \langle \omega t \langle 240^0 \\ 0 & elsewhere\end{cases} \tag{5.38}$$

From (5.36) and Figure 5.11 the currents **Ia1**, **Ia3** and **Ia5** is defined as the following

$$\mathbf{Ia1} = \begin{cases}-\mathbf{IW} & when \quad 0^0 \langle \omega t \langle 60^0 \\ -\mathbf{IUa} & when \quad 300^0 \langle \omega t \langle 360^0\end{cases} \tag{5.39}$$

$$\mathbf{Ia3} = \mathbf{IWa}$$

$$\mathbf{Ia}5 = \mathbf{IU}$$

Substituting (5.39) into (5.38) the primary current **IUp** is defined as

$$\mathbf{IUp} = \frac{1}{7}\,\frac{N2}{N1}\begin{cases}-\mathbf{IUa} & when \quad 300^0 \langle \omega t \langle 0^0 \\ -\mathbf{IW} & when \quad 0^0 \langle \omega t \langle 60^0 \\ \mathbf{IU} & when \quad 120^0 \langle \omega t \langle 180^0 \\ \mathbf{IWa} & when \quad 180^0 \langle \omega t \langle 240^0 \\ 0 & elsewhere\end{cases} \tag{5.40}$$

Figure 5.19 presents the waveform of the primary current **IUp** as defined in (5.40).

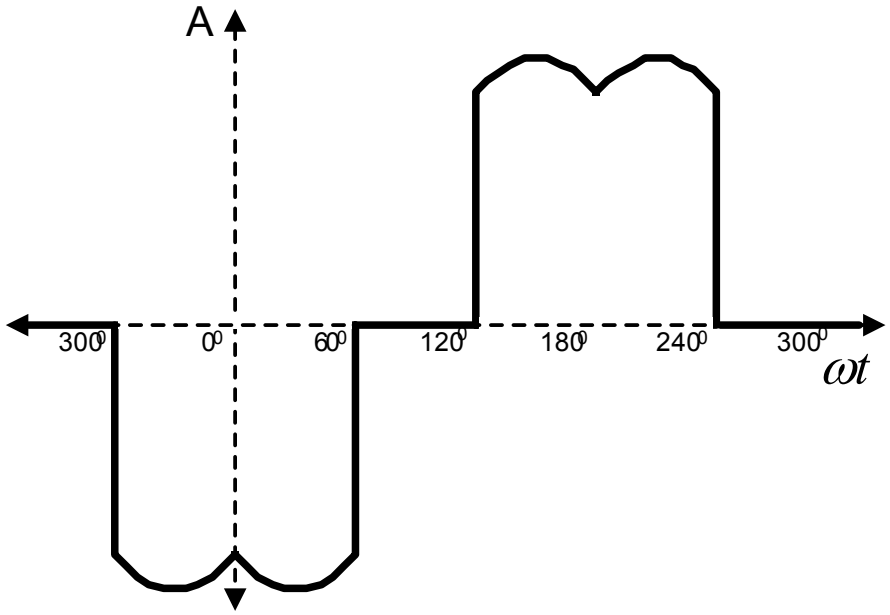

*Figure 5.19 – Current **IUp***

Simplifying (5.40), **IUp** can also be written as

$$\mathbf{IUp} = \frac{1}{7}\frac{N2}{N1}\left(-\left(\mathbf{IUa}+\mathbf{IW}\right)+\mathbf{IU}+\mathbf{IWa}\right) \tag{5.41}$$

this is the same as for the resistive load. Using the same method that is used tot determine **IUp** the currents **IVp** and **IWp** are defined.

$$\mathbf{IVp} = \frac{1}{7}\frac{N2}{N1}\left(-\left(\mathbf{IU}+\mathbf{IVa}\right)+\mathbf{IV}+\mathbf{IUa}\right) \tag{5.42}$$

$$\mathbf{IWp} = \frac{1}{7}\frac{N2}{N1}\left(-\left(\mathbf{IWa}+\mathbf{IV}\right)+\mathbf{IW}+\mathbf{IVa}\right)$$

5.4.4. - The supply transformer as a load

The supply transformer is connected as shown in Figure 5.20.

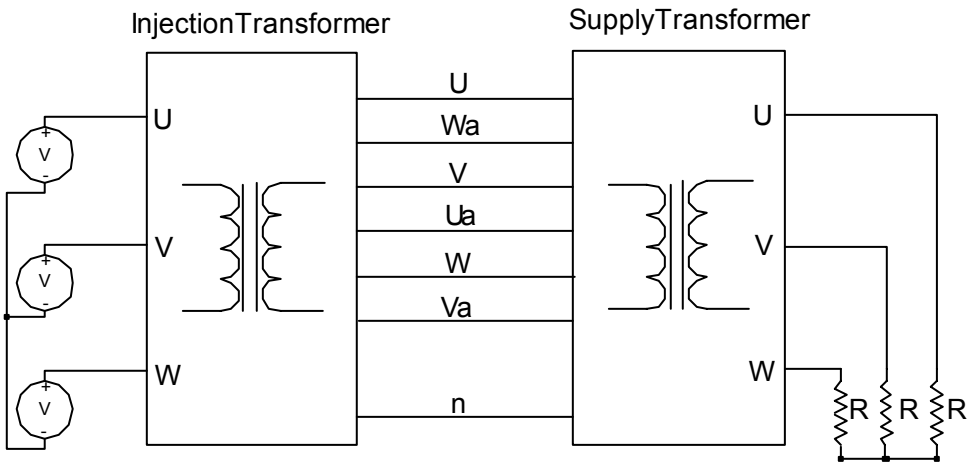

Figure 5.20 – The supply transformer as a load

With the supply transformer as a load the currents **Ia3** and **Ib5** are defined as

$$\begin{aligned} \mathbf{Ia3} &= 1\angle 90^0 \\ \mathbf{Ib5} &= 1\angle 330^0 \end{aligned} \tag{5.43}$$

where a magnitude of 1 is assumed.

Using (5.22) and (5.43) the current **Ic1** is calculated

$$\begin{aligned} \mathbf{Ic1} &= -\left(\mathbf{Ia3} + \mathbf{Ib5}\right) \\ &= -\left(1\angle 90^0 + 1\angle 330^0\right) \\ &= 1\angle 150^0 \end{aligned} \tag{5.44}$$

The currents **Ia3**, **Ib5** and **Ic1** are illustrated in Figure 5.21

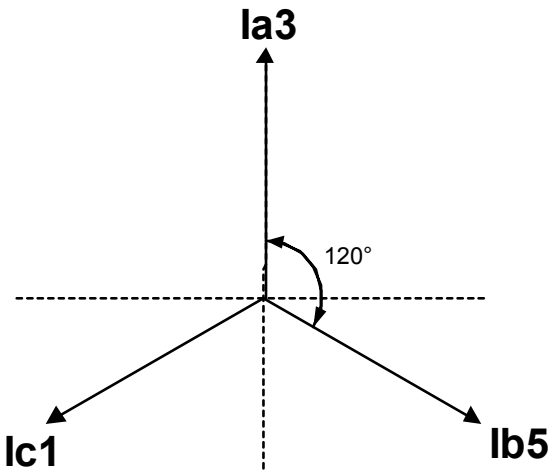

*Figure 5.21 – Currents **Ia3**, **Ib5** and **Ic1** for the supply transformer as a load*

The rest of the currents in the secondary are calculated in the same way, this results in the following

$$\mathbf{Ia1} = \mathbf{Ia3} = \mathbf{Ia5} \tag{5.45}$$

Using (5.37) and (5.45) the current **IUp** is expressed as

$$\begin{aligned} \mathbf{IUp} &= 3\,\mathbf{Ia5} \\ &= 3\,\mathbf{IU} \end{aligned} \tag{5.46}$$

The currents **IVp** and **IWp** can also be written as

$$\begin{aligned} \mathbf{IVp} &= 3\,\mathbf{IV} \\ \mathbf{IWp} &= 3\,\mathbf{IW} \end{aligned} \tag{5.47}$$

Taking the 7 primary windings into account and adding the winding ratio, (5.46) and (5.47) changes to

$$\mathbf{IUp} = \frac{3}{7}\frac{N2}{N1}\mathbf{IU} \qquad (5.48)$$
$$\mathbf{IVp} = \frac{3}{7}\frac{N2}{N1}\mathbf{IV}$$
$$\mathbf{IWp} = \frac{3}{7}\frac{N2}{N1}\mathbf{IW}$$

As for the previous loads the equations (5.31) and (5.32) can be used as a general relationship between the primary and secondary currents.

5.4.5. - Simulation results

The simulations were implemented in the Simplorer 6 simulation package. For the simulations the injection transformer is modelled as an ideal transformer. Aspects such as core losses and leakage inductance are ignored. Figure 5.22 shows the transformer model that is used in the simulations.

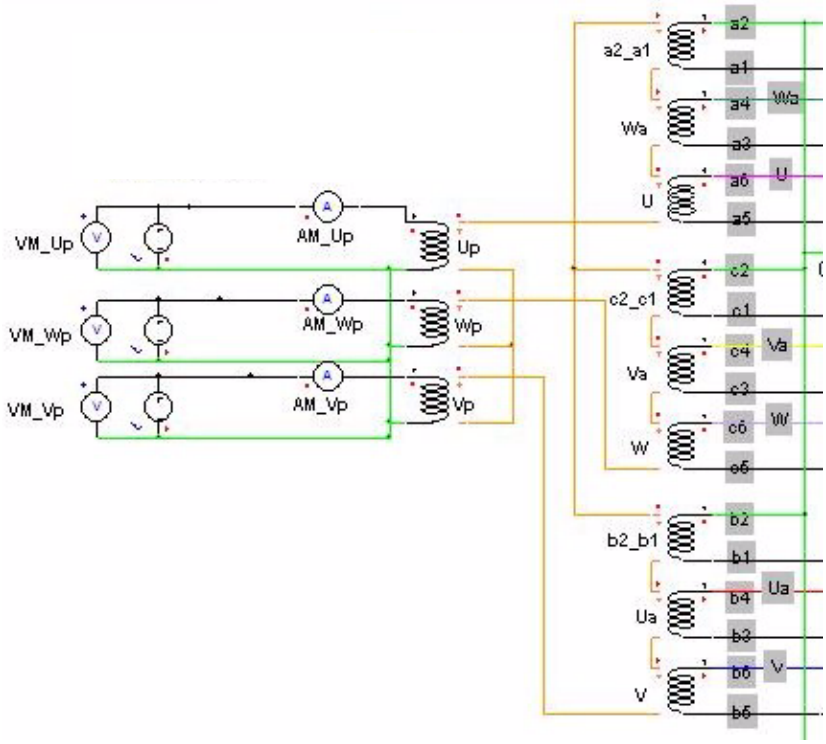

Figure 5.22 – Transformer model used for the simulations

For the simulations a transformer with one primary star winding is used, this results in primary currents that are 7 times larger than that of the injection transformer.

Resistor load

Figure 5.23 provides the simulation results of currents **Ic1**, **Ia3** and **Ib5** of the secondary of the transformer for a resistive load. The vector diagram of these currents is shown in Figure 5.13. The resistor values are chosen so that the 6-phase currents of the secondary have an amplitude of 100 A.

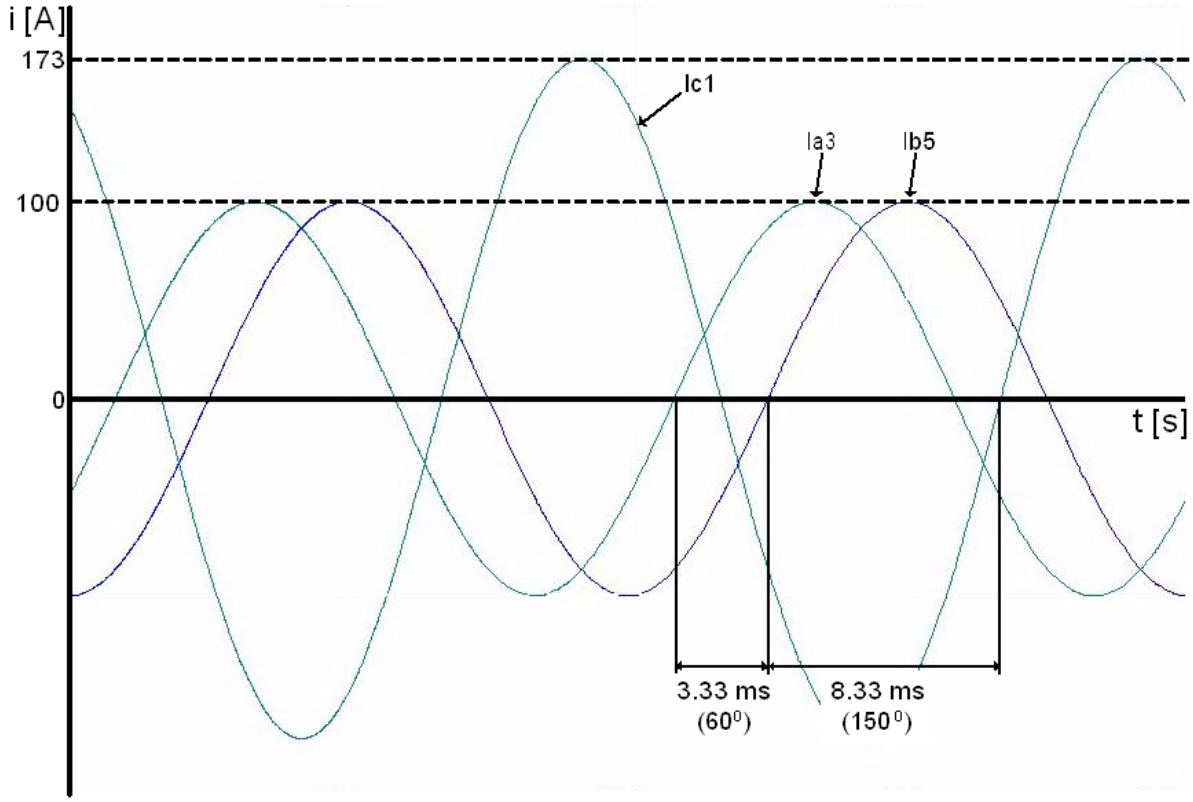

Figure 5.23 – Simulation results illustrating Figure 5.13

Figure 5.24 illustrates the relationship between the primary and secondary currents as shown in Figure 5.14.

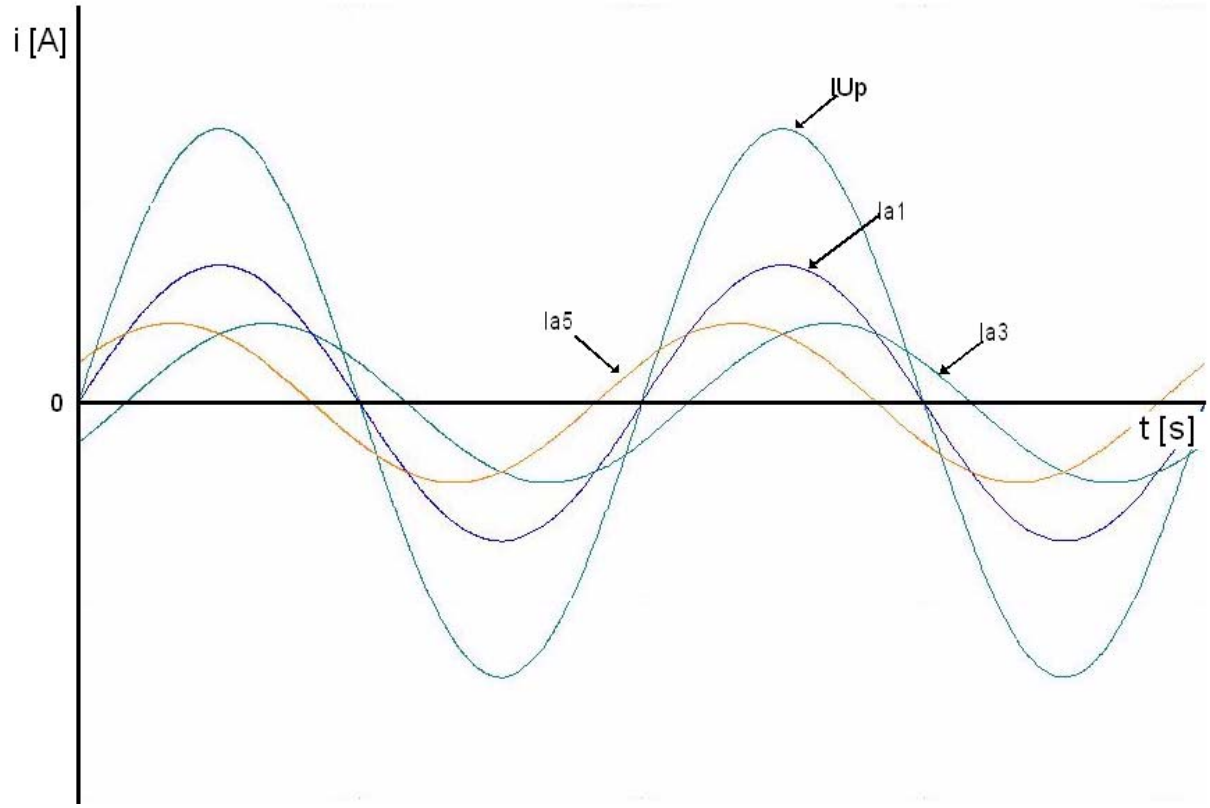

Figure 5.24 – Simulation results illustrating Figure 5.14

Rectifier load

Figure 5.25 provides the simulation results for the currents shown in Figure 5.18.

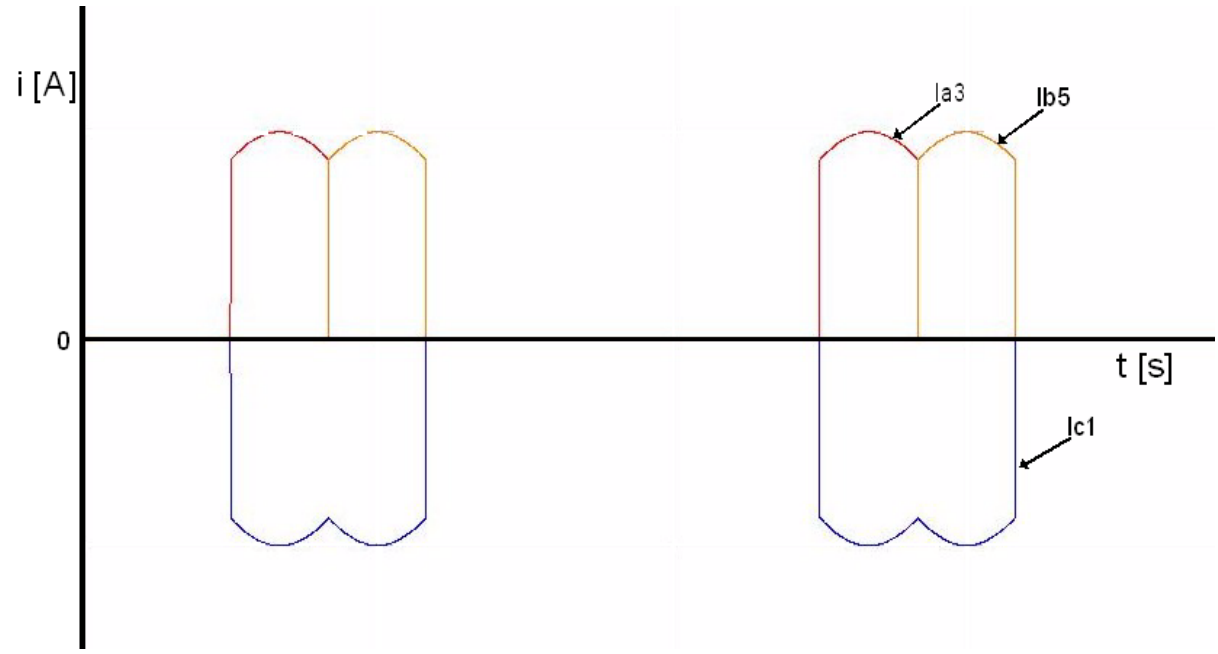

Figure 5.25 – Simulation results illustrating Figure 5.18

Figure 5.26 is the simulation result for equation (5.37) and Figure 5.19 illustrating the primary current **IUp** for the 6-pulse rectifier load.

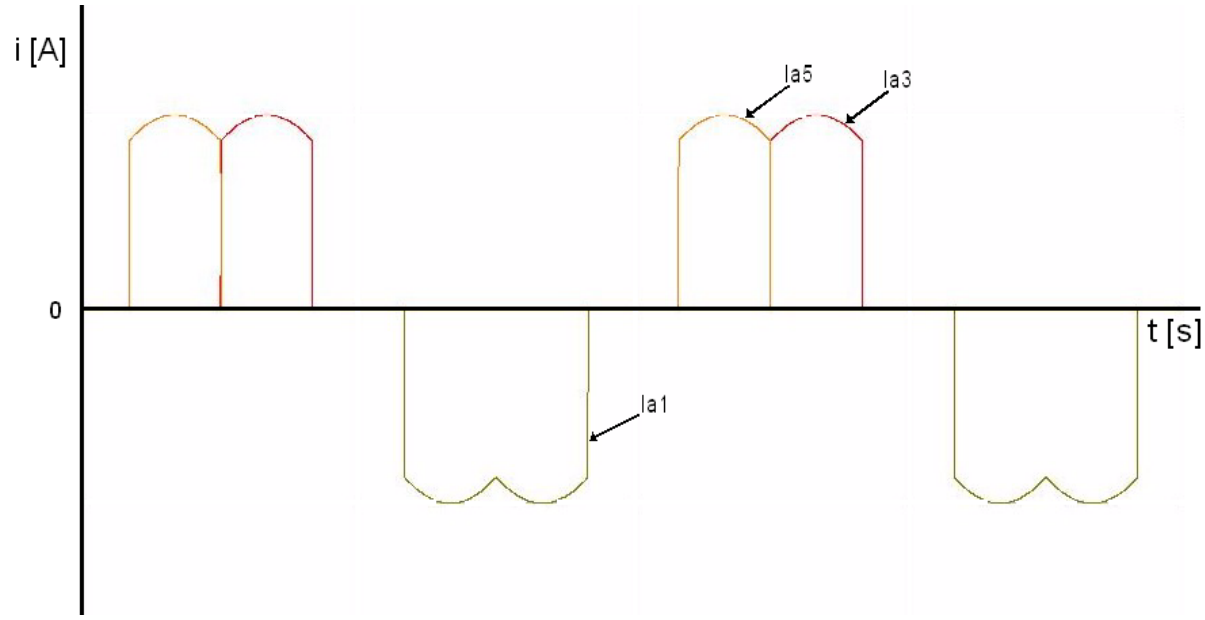

Figure 5.26 – Simulation results illustrating Figure 5.19

5.4.6. - Conclusion

Different loads are considered for the injection transformer which results in different current waveforms on the secondary. From the above calculations it is seen that a general relationship exists between the primary and secondary currents irregardless of the type of load. These equations are summarised in (5.49).

$$\begin{aligned}
\mathbf{IUp} &= \frac{1}{7}\frac{N2}{N1}(-(\mathbf{IW}+\mathbf{IUa})+\mathbf{IWa}+\mathbf{IU}) \\
\mathbf{IVp} &= \frac{1}{7}\frac{N2}{N1}\left(-\left(\mathbf{IU}+\mathbf{IVa}\right)+\mathbf{IV}+\mathbf{IUa}\right) \\
\mathbf{IWp} &= \frac{1}{7}\frac{N2}{N1}\left(-\left(\mathbf{IWa}+\mathbf{IV}\right)+\mathbf{IW}+\mathbf{IVa}\right)
\end{aligned} \tag{5.49}$$

By measuring only the 6-phase currents of the secondary of the injection transformer, (5.49) are used to derive the primary currents.

Chapter 6 - Switchgear and system protection

Chapter 6 presents an overview of the switchgear and protection that is implemented in the regen-system. Switchgear is defined as all the components that utilise mechanical switching to make or break an electrical connection. Figure 6.1 provides a diagram of where the switchgear and system protection is implemented in the regen-system. The shaded components of the diagram are described in more detail in the sections to follow. The soft-starter is also part of the switchgear but is described in detail in section 3.2.5.

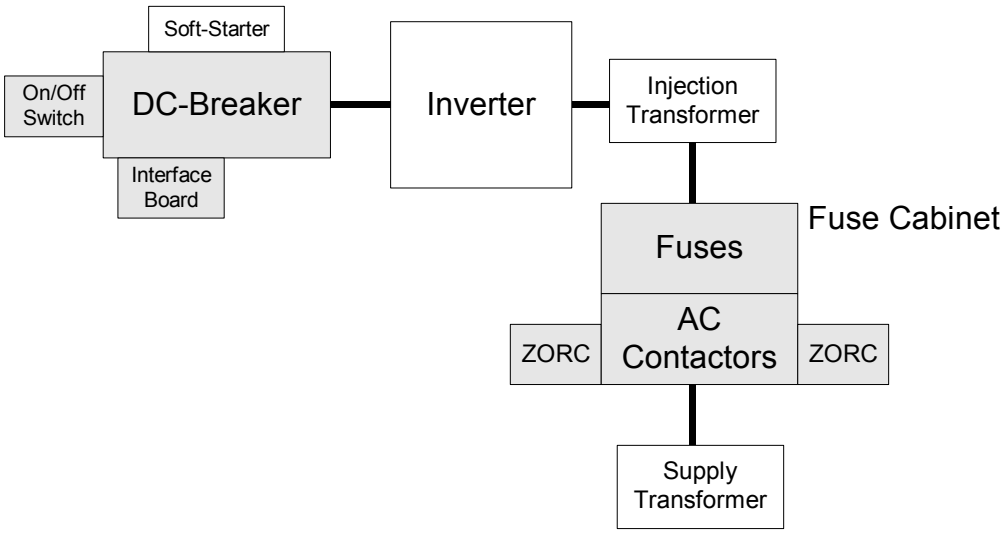

Figure 6.1 – Diagram of switchgear and the system protection

6.1. - On / Off Switch

The On / Off switch is the human interface with the regen-system. By turning the switch clockwise or counter clockwise the regen-system is enabled or disabled. A fibre-optic transmitter is turned on or off by the switch and the signal is transmitted to the controller via a fibre-optic cable. When the switch is turned to the on position the controller commences the soft-start sequence and subsequently the regen-system is activated. When the switch is turned to the off position the regen-system is halted and the shutdown procedure is started. As shown in Figure 6.2 the On / Off switch is mounted on the front panel of the DC-breaker.

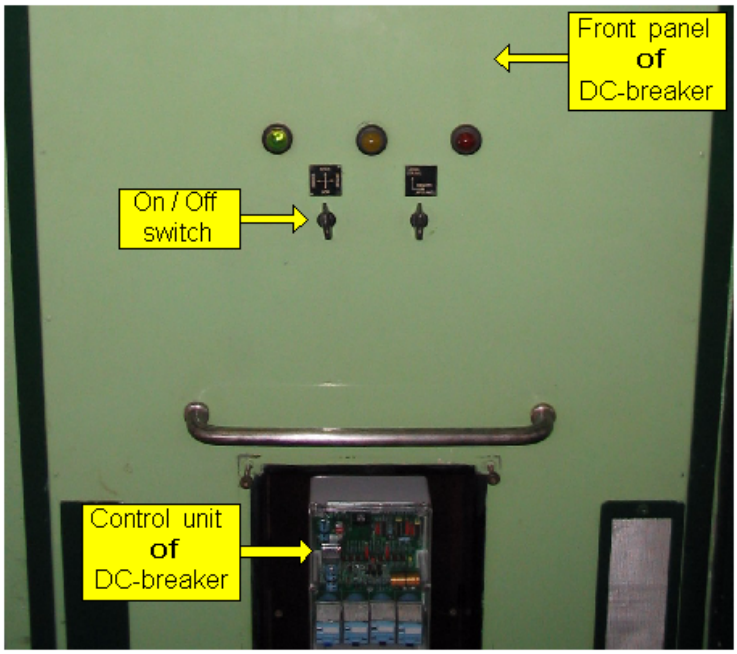

Figure 6.2 – Photograph of the On / Off switch

6.2. - DC-breaker

The same DC-breaker that is used for the DC traction supply is used for the regen-system and is connected as shown in Figure 1.2 and illustrated in Figure 6.1. Although these breakers date back to the 1950 / 60s they still provide reliable over current protection. The status of these breakers is transmitted to the Spoornet control centre where it is monitored. From the control centre the breakers can be remotely operated. The remote operation of the DC-breaker for the regen-system is disabled to ensure that the control centre can not open or close the breaker. Only the controller of the regen-system can operate the DC-breaker. An external fault in the substation such as DC earth leakage will override the controller and open the DC-breaker. The control signal for the DC-breaker is transmitted via a fibre-optic cable to the breaker where it activates a DC-relay. This DC-relay, Kilovac, is the same type of relay that is used for the soft-starter. The relay connects the 110 V DC from the substation to the DC-breaker which then closes. To indicate the status of the DC-breaker an auxiliary contact is used for the activation of a fibre-optic transmitter which transmits the status of the breaker to the controller. An asbestos arc-shoot is mounted on top of the DC-breaker to extinguish the arc created when the breaker is opened under load. The DC-breakers for the traction supply are calibrated for a current of 3 kA but the breaker for the regen-system is calibrated for a current of 900 A. Figure 6.3 presents a photograph of the DC-breaker for the regen-system.

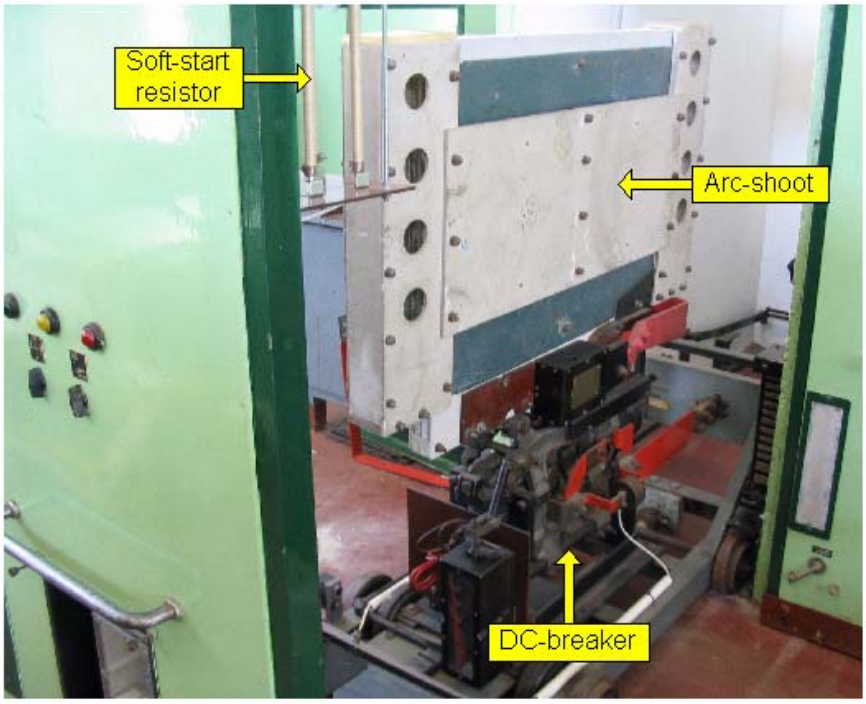

Figure 6.3 – Photograph of the DC-breaker

6.3. - Fuse cabinet

The fuse cabinet houses the fuses and AC-contactors on the 6-phase side between the regen-system and the secondary of the supply transformer as shown in Figure 6.1. The 6 phases of the injection transformer connects to the AC-contactors at the bottom of the fuse cabinet. The fuses are mounted above the AC-contactors which in turn are connected to the 6 phases of the supply transformer. Shown in Figure 6.4 is a photograph of the fuse cabinet.

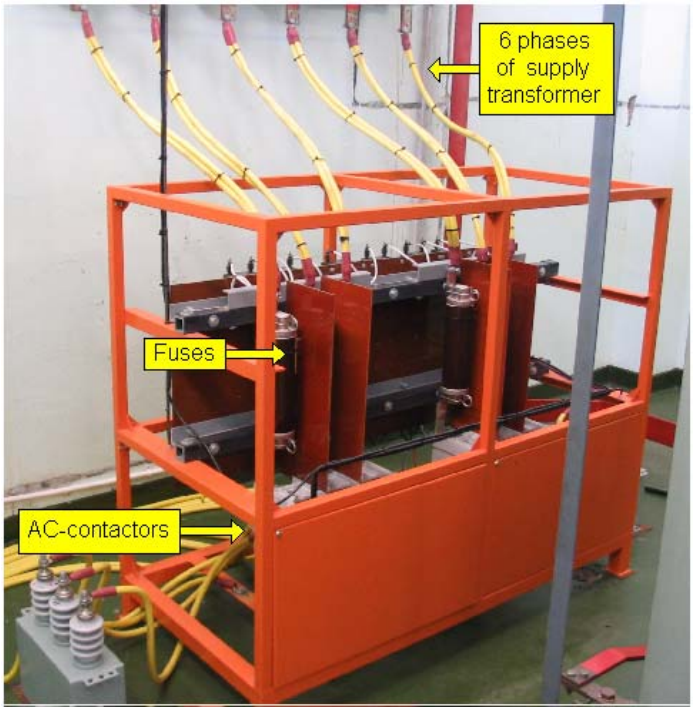

Figure 6.4 – Photograph of the fuse cabinet

6.3.1. - Fuses

In each phase between the AC-contactors and the supply transformer a SIBA 3 kV, 315 A_{rms} fuse is connected. The fuses are mounted on fibre-glass tubing to isolate them from the frame of the fuse cabinet. Tufnol separators are inserted between the fuses to increase the creapage distance between the phases. Figure 6.5 shows a photograph of 3 of the fuses.

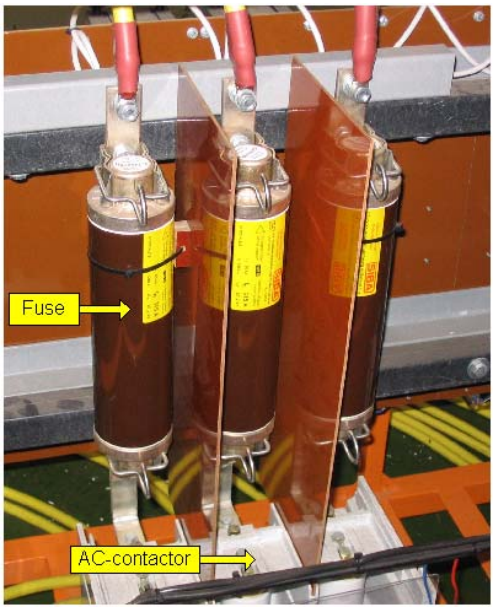

Figure 6.5 – Photograph of the fuses

6.3.2. - AC-contactors

Two 3-phase AC-contactors are connected in parallel to form one 6-phase AC-contactor. The purpose of the AC-contactors is to isolate the regen-system from the substation when the regen-system shuts down. The control signal is transmitted via a fibre-optic cable from the controller to the fuse cabinet. A DC-relay connects the 110 V DC from the substation to the closing coil of the AC-contactors. An auxiliary contact on the AC-contactor is used for the monitoring of the contactor status. This status signal is transmitted to the controller via a fibre-optic cable. A 3.3 kV, 400 A high voltage vacuum contactor from Toshiba Corporation, type: CV-6HA-2, is used for the AC-contactor. Figure 6.6 provides a photograph of one of the 3-phase AC-contactors.

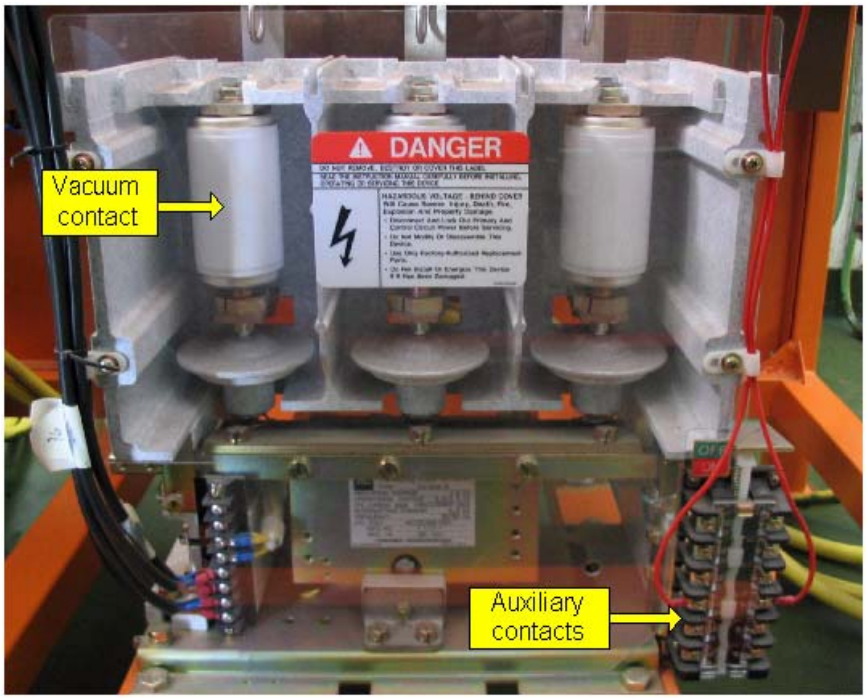

Figure 6.6 – Photograph of the AC-contactor

6.3.3. - ZORC

Energy is stored in the inductance of the cables. When the AC-contactor is opened under load conditions this stored energy in the cables causes high voltage spikes which can damage the inverter. Some contactors use an arc-shoot to dissipate the energy. Due to the vacuum contact of the AC-contactor there are no means to dissipate this energy. To prevent the voltage spikes a transient surge suppressor is connected to the AC-contactor. Two 3.3 kV 3-phase ZORCs from Strike Technologies are used as the surge suppressors. The ZORC can compensate for voltage steps changes in the order of 0.1 – 2 µs. It utilises a patented capacitor, resistor and

Zinc Oxide non-linear arrester network to eliminate voltage transients [33]. In Figure 6.7 a photograph of one of the 3-phase ZORCs are shown.

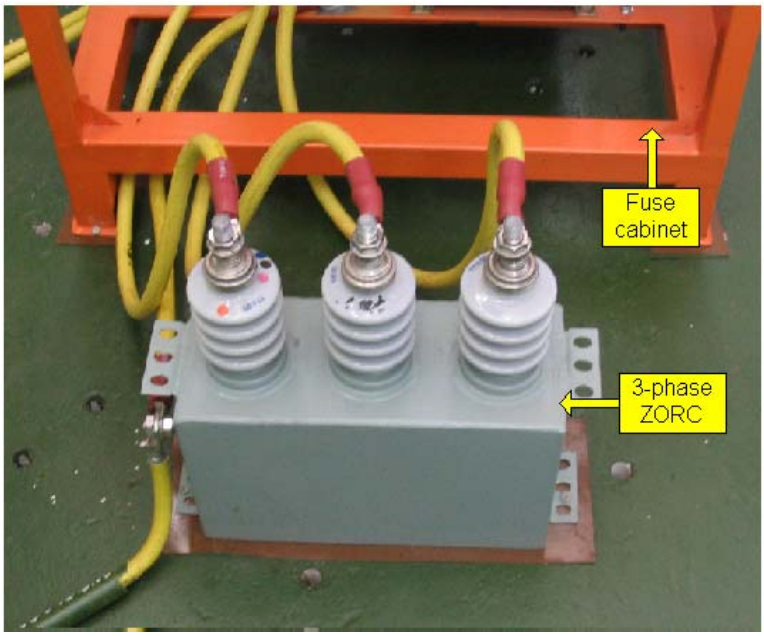

Figure 6.7 – Photograph of the 3-phase ZORC

6.4. - Switchgear interface board

The switchgear interface board is the link between the controller and the switchgear. All the control signals and status signals to and from the controller are sent via fibre-optic cables. This ensures that the controller is electrically isolated from the switchgear. The interface board converts these fibre-optic signals to electrical signals which in turn are connected to the switchgear. The schematic of the interface board is presented in Appendix C.4. The AC-contactors have the same type of interface but it is mounted in the fuse cabinet. Power to the interface board is provided by a 24 V supply from Mean Well. The input power of the supply is obtained from the 110 V DC supply of the substation. Figure 6.8 is a photograph of the switchgear interface board.

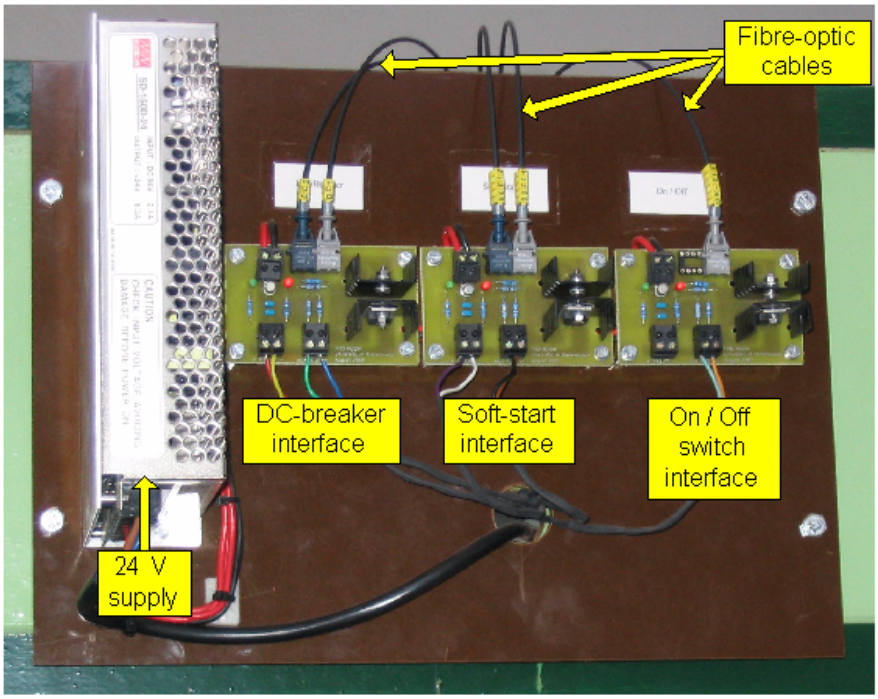

Figure 6.8 – Photograph of the switchgear interface board

Chapter 7 - Results

The regen-system was installed in the Wolseley traction substation and tests were performed to ensure that inverter and measurement system were functioning correctly. Furthermore the regen-system was connected to the AC and DC side of the substation and tests were done when a train was drawing power as well as when a train was generating power.

The oscillographs presented throughout the thesis were obtained with the aid of a Tektronix TDS3014B oscilloscope. The voltage probe that was used for the voltage measurements on the oscilloscope is a Tektronix P6015A 1000X High Voltage probe. Where it was not possible to measure the voltages with the oscilloscope, the measurement system of the regen-system was used. The current measurements on the oscilloscope were obtained with a Tektronix CT4 current probe and a Tektronix TCP202 current probe. In the places where isolation was a problem the LEM current probes of the regen-system was used for the current measurements. For the APF results the waveforms and data points were saved on the oscilloscope. For the regen results the DC voltage and current at the input of the regen-system was measured with the Tektronix voltage and current probes. The data was then logged on a computer with the aid of a Matlab program.

In this chapter results for both the APF-mode and regen-mode of operation are presented. The results for the isolation tests that were performed on the regen-system are also provided.

7.1. – Natural balancing of DC-bus voltages

Due to the offset voltage of each cell it was not possible to measure the DC-bus voltages of the cells directly with measurement equipment. Therefore the voltage measurement system of the regen-system was used to produce these results. The voltage measurements were sent to the DACs of the PEC 33 where the waveforms were measured with an oscilloscope. Figure 7.1 provides an oscillograph of the voltage measurements of the total DC-bus voltage and the DC-bus voltage of cells 1, 2 and 3. Only 4 measurements can be displayed by the oscilloscope but the DC-bus voltage measurements of the remainder of the cells produced the same results. The amplitude of the measurements that are produced by the DACs is scaled in the software in the PEC 33. The total DC-bus voltage measurement was scaled to have a larger amplitude than the DC-bus voltage measurements of the cells of the inverter.

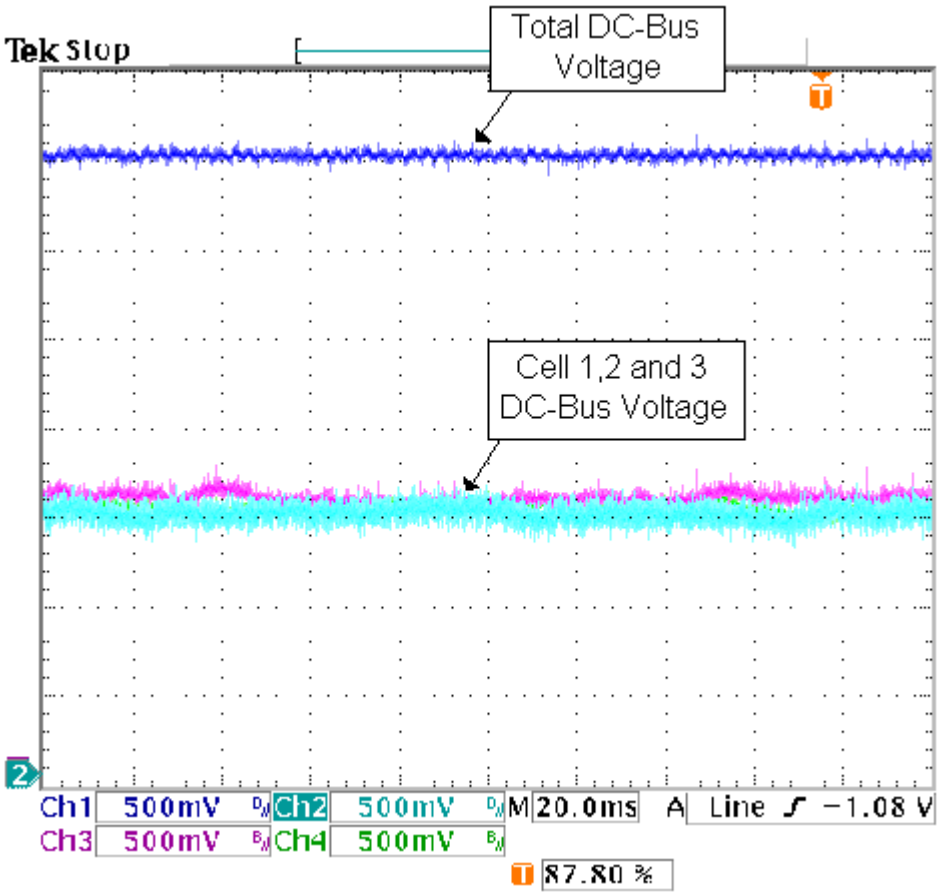

Figure 7.1 – DC-bus voltage measurements

It is concluded that the natural balancing mechanism of the SS inverter is functioning correctly.

7.2. - APF results

Figure 7.2 is an oscillograph of the currents for 2 of the primary phases of the supply transformer. These measurements are obtained from the Current Transformers (CTs) mounted on the over current breakers between the Eskom supply and the supply transformer. The measurements were made during the time when a train was drawing energy from the substation. The distorted sinusoidal waveforms are due to the harmonics drawn by the traction rectifier.

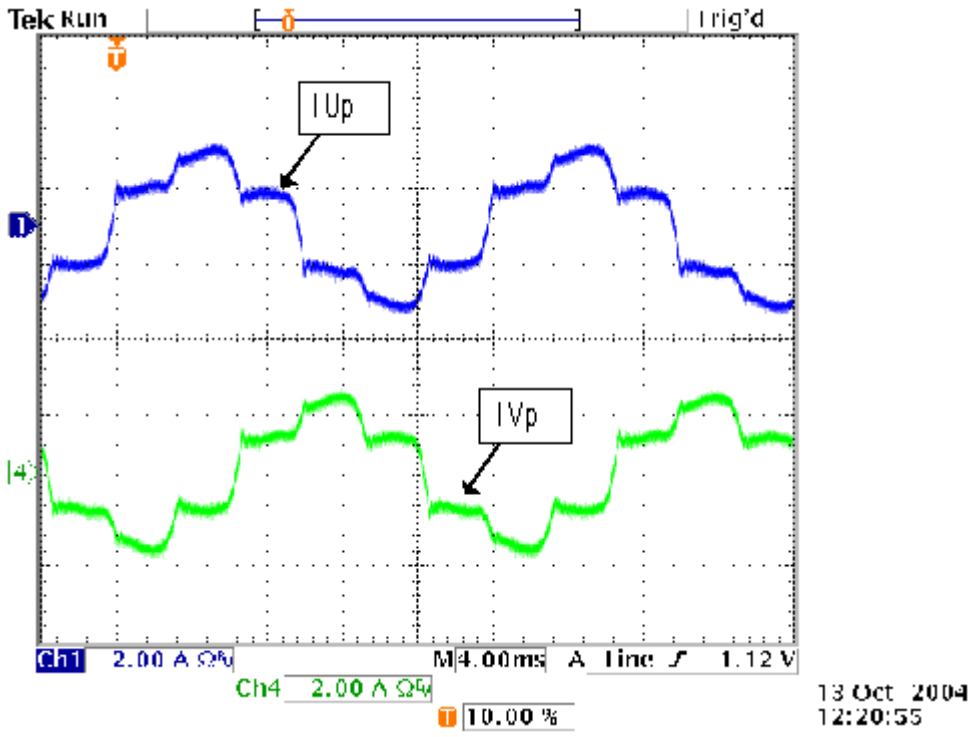

Figure 7.2 – Primary currents of supply transformer under load

Figure 7.3 is the same measurements as in Figure 7.2 but with the APF-mode of the regen-system activated. A significant increase in the quality of the sinusoidal waveform can be noted. The THD calculated for the uncompensated current is 24.93%. This was reduced to 15.55% in the compensated current [2]. Therefore the harmonics created by the traction rectifier is reduced as seen from the Eskom supply.

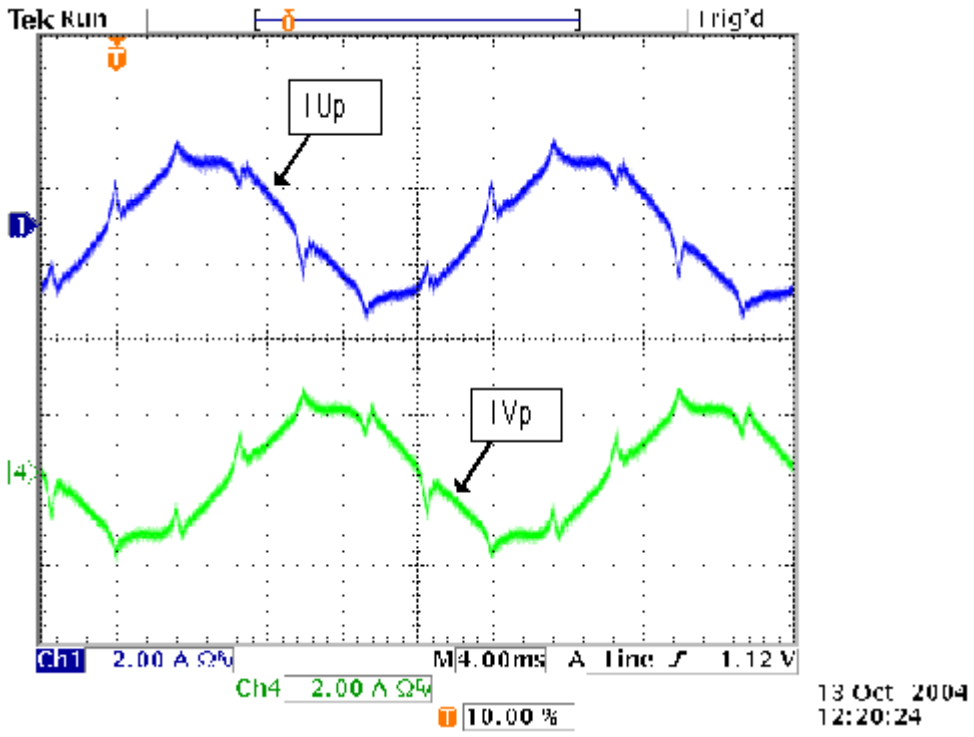

Figure 7.3 – Primary currents of supply transformer with APF

7.3. - Regen results

The results for the regen were obtained by measuring the input voltage and current of the inverter. These measurements are presented in Figure 7.4. For viewing purposes the graph for the DC input current is scaled with an offset value of 3 200. The plateaus in the current graph are due to the current limiting implemented in the controller software. The current limiting also accounts for the rises in the DC voltage. From the graph it is seen that the regen lasted approximately 15 minutes.

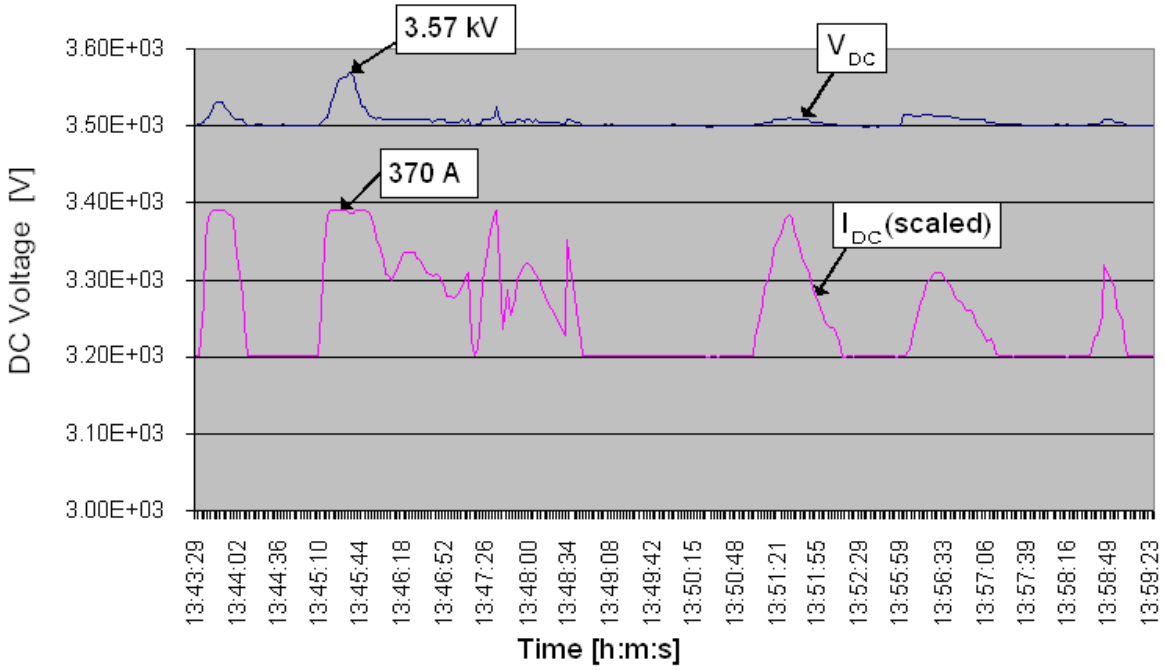

Figure 7.4 – Graph of inverter input voltage and current during regen

Figure 7.5 presents the graph for the input power during regen. The sporadic changes in the power level are due to the train that is braking as required by the track. The plateau in the power graph is due to the current limiting that is implemented by the software. A maximum regen power of 1.32 MW was reached. By increasing the level of current limit, the regen power can also be increased. The value of 1.32 MW is satisfactory and indicates that the regen-system is functioning as desired.

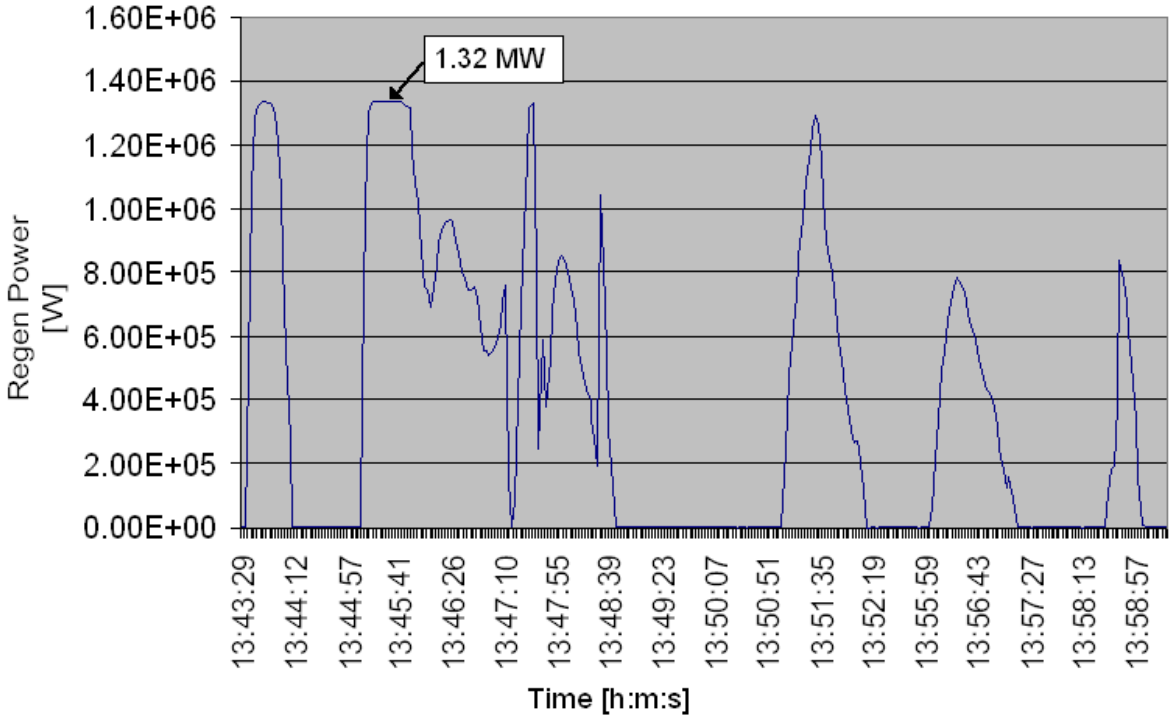

Figure 7.5 – Graph of inverter input power during regen

7.4. - Isolation test results

The insulation of the regen-system is specified as 10.5 kV_{rms} for 1 minute. The isolation tests were performed with the aid of a DC voltage isolation test device. Due to the DC test voltage the specifications were altered to 15 kV DC for 30 seconds. Figure 7.6 indicates the points where the isolation tests were performed. All the tests were done with respect to the frame of the inverter cabinet.

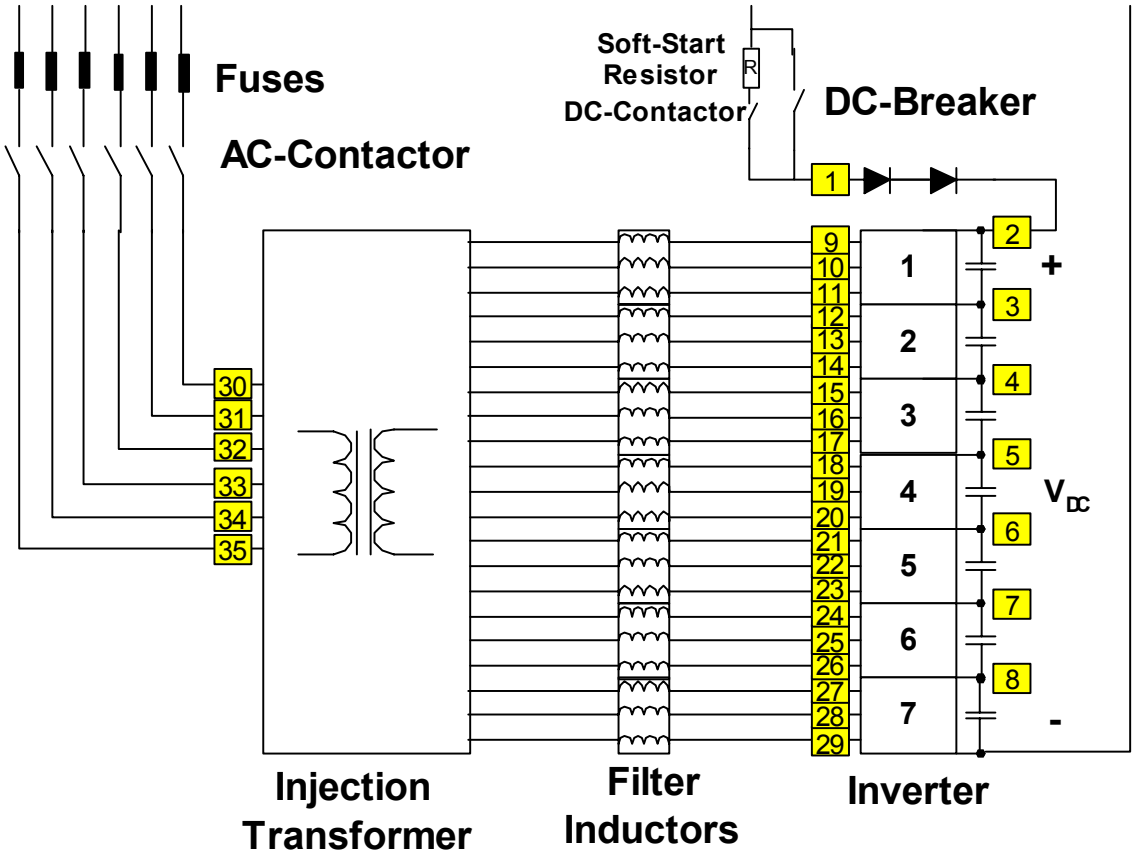

Figure 7.6 – Isolation test points

Table 7.1 lists the results for the isolation tests. All the measured points provided an isolation of 150 GΩ and more, therefore it is concluded that the isolation for the regen-system complies with the specified values.

Table 7.1 – Isolation test results

Test point	Current at 15 kV DC	Test point	Current at 15 kV DC	Test point	Current at 15 kV DC
1	100 µA	13	82 µA	25	84 µA
2	100 µA	14	80 µA	26	86 µA
3	100 µA	15	82 µA	27	88 µA
4	100 µA	16	80 µA	28	86 µA
5	100 µA	17	82 µA	29	88 µA
6	100 µA	18	84 µA	30	5 µA
7	100 µA	19	82 µA	31	3.8 µA
8	100 µA	20	82 µA	32	3.6 µA
9	78 µA	21	84 µA	33	3.2 µA
10	76 µA	22	82 µA	34	3.2 µA
11	78 µA	23	84 µA	35	3 µA
12	80 µA	24	84 µA		

7.5. - Conclusion

Results for both the APF-mode and regen-mode of operation are presented. The results indicate that the system is functioning satisfactory. Although only 88% of the desired rating of the regen-system was reached, it can easily be improved by increasing the current limit level of the inverter. The isolation tests yielded good results and it is concluded that the isolation of the regen-system is satisfactory.

Chapter 8 - Conclusion

8.1. – Recommendations

- At present the regen-system is continuously active. There are large portions of the day when there are no trains within the railway section of the substation. During this time it is not necessary for the regen-system to be active. Software can be implemented that will activate the regen-system only when a train is within the railway section of the substation.

- The system implemented in this thesis connects to the 6-phase secondary of the supply transformer. Although the cost of the injection transformer is reduced due to the lower operating voltage, the control of the system is complicated by the 6-phase to 3-phase transformations that must be done. It can be considered to inject directly into the 3-phase Eskom supply. The cost for the injection transformer to operate at the higher voltage should be compared with the present system.

- During the testing of the APF-mode of the regen-system it was noted that the filter inductors got excessively hot. This is due to the sharp flanks of the current waveforms that are switched by the inverter. The inductors are only rated for 50 Hz waveforms. Increasing the capability of the inductors can be considered.

- The cabinets that house the inverter can be made smaller. There are arias of excessive clearance distances. By re-evaluating these distances the physical size of the inverter can be reduced.

- The cuttoff frequency of the low-pass filter on the AC voltage measurements can be increased to minimise the phase shift introduced by the filter. Higher order filters can also be considered.

8.2. – Summary

The goal of the project for this thesis was to implement the desired inverter system in a Spoornet substation. This is successfully achieved by the installation of the complete regen-system in the Spoornet traction substation at Wolseley. All the construction and isolation specifications are adequately met. The thesis provides detailed descriptions and analysis of the different components of the system.

Results for the APF-mode of operation, indicating the reduction in harmonic distortion on the Eskom supply, are included.

Also included are results that indicate the successful injection of regenerated energy, created by the train, into the Eskom supply.

It is concluded that the implementation of the regen-system in a Spoornet substation was successfully accomplished.

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Appendix A – Spoornet specifications for this project

BBB1769 Version 1

SPOORNET

A DIVISION OF TRANSNET LIMITED

RAILWAY ENGINEERING

SPECIFICATION CONTROL PAGE

THE DEVELOPMENT, INSTALLATION AND EVALUATION OF A 1,5 MW INVERTER FOR REGENERATED ENERGY WITH ACTIVE POWER FILTERING INCORPORATED, FOR APPLICATION IN A 3 kV DC TRACTION SUBSTATION

Statement of authorisation:

There is no SABS specification available for similar material / equipment and as far as can be ascertained no other specification / standard suitably covers Spoornet requirements. The specification has been compiled in a manner which shall favour / encourage local manufacture of material / equipment to a maximum degree.

Author:	Senior Engineer Locomotive Power Supplies Interaction	L.O.Borchard	...
Authorised:	Principal Engineer Railway Engineering	W.A.Coetzee	...

Date: 28 February 2001

This page is for control purposes only and shall not be issued with the specification.

Page 0 of 9

BBB1769 Version 1

SPOORNET

A DIVISION OF TRANSNET LIMITED

RAILWAY ENGINEERING

SPECIFICATION

THE DEVELOPMENT, INSTALLATION AND EVALUATION OF A 1,5 MW INVERTER FOR REGENERATED ENERGY WITH ACTIVE POWER FILTERING INCORPORATED, FOR APPLICATION IN A 3 kV DC TRACTION SUBSTATION

Circulation restricted to:

R&TS: Infrastructure (Maintenance)

Planning and technology: Railway Engineering

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1.0 SCOPE

1.1 This specification covers Spoornet's requirements for the development, installation, performance evaluation and commissioning of a prototype 1.5 MW Inverter with an ACTIVE POWER FILTER incorporated for regenerated energy in a 3 kV DC traction substation to feed excess regen energy into Eskom's transmission system, as an alternative to existing resistive energy absorption equipment.

1.2 The specification also includes a feasibility study to determine whether the existing traction transformers can be used to feed the energy back into the network.

2.0 STANDARDS AND PUBLICATIONS

2.1 Unless otherwise specified all materials used and equipment developed and supplied shall comply with the current edition of the relevant SABS, IEC or Spoornet's publications where applicable.

2.2 The following publications are referred to in this specification:

2.2.1 South African Bureau of Standards

SABS 1019 - Standard voltages, currents and insulating levels for electrical supply.
SABS NRS048:part 2 – National Rationalized User Specification, Electrical Supply –Quality of Supply.

2.2.2 International Electrotechnical Commission

IEC 146 - Semiconductor Converters
IEC 51 – Electrical Measuring Instruments

2.2.3 Spoornet

Electrical Safety Instructions - 1999

2.3 All documents and drawings supplied by Spoornet for the development, installation, commissioning and performance evaluation of the above shall remain the property of Spoornet.

2.4 Information contained in these documents and drawings may only be used for the purpose of the development of the prototype inverter.

3.0 DEFINITIONS

3.1 In this specification the word "shall" is always used to express a mandatory requirement; the words "should ","may" or "is to be" are used for the expression of non-mandatory requirements, i.e. preferences.

3.2 A non-receptive system is defined, as a system where excess regenerative energy exists which cannot be absorbed by the system without excessive voltage rise.

4.0 TENDERING PROCEDURE

4.1 Tenderer shall indicate compliance with the specification. This shall take the form of a separate document listing all the specification's clause numbers indicating clause by clause an individual statement of compliance or non-compliance.

4.2 The tenderer shall motivate a statement of non-compliance.

4.3 The tenderer shall submit descriptive literature consisting of detailed technical specifications, general construction details and principal dimensions, together with clear illustrations of the equipment offered.

5.0 SERVICE CONDITIONS

The unit shall be of a rugged design rated for continuous operation under the following conditions:

5.1 Environmental conditions

5.1.1	Altitude	:	0 to 1800 m above sea level
5.1.2	Ambient temperature	:	- 10 deg C to + 50 deg C.
5.1.3	Relative humidity	:	10% to 90 % non-condensing.
5.1.4	Air pollution	:	Industrial environment and dust.
5.1.5	Lightning conditions	:	11 ground flashes / km^2 / annum.

5.2 Mechanical service conditions

The substation in which the inverter will be installed is situated next to a railway line and the inverter will therefore be subjected to vibration. Therefore the design must take appropriate counter measures to ensure reliability of equipment that are sensitive to vibration.

5.3 Electrical service conditions

5.3.1 The no-load voltage of the DC traction substation varies between 3150 - 3400 volt DC. It may increase during regeneration up to 3900 volt or decrease to 2300 volt under load conditions.

5.3.2 For the purpose of surge and lightning protection of the substation equipment, a 4-MicroFarad capacitor is connected between the positive cable termination and negative rail. A surge arrester, having a residual voltage of 13 kV, is also connected between the positive cable termination and earth mat. Along the overhead line arcing horns are also installed approximately every 800 metres.

5.3.3 The installed substation capacity varies from 3 Mwatt to 12 Mwatt, with individual rectifier capacities varying in multiples of 3 MW or 4,5 MW.

5.3.4 Substation traction transformers have mainly the following output configuration:

a) 2460 Volt, 3 phase (6 pulse) (star or delta vector grouping) for full wave bridge rectification,

b) 1260 Volt, 6 phase (12 pulse) (Two extended deltas or a star and delta vector grouping) for 2 x 1,5 k Volt in series full wave bridge rectification.

5.3.6 The harmonics from the substation rectifier lies in the frequency range 300 - 1200 Hz. The small ripple voltage from the overhead line when the system is non-receptive has a frequency component of around 150 Hz.

5.3.7 The substation has the following overload ratings:

200 percent for 30 minutes
Short circuit proof for 200 milliseconds

5.3.8 Typical fault conditions

	Fault near substation	Fault remote from substation
Prospective current	50 kA	10 kA
Time constant	10 msec	45 msec
Tripping time of HSCB	< 30 msec	< 60 msec

5.3.9 All 3 kV DC substations on a line operate normally in parallel.

5.3.10 Equipment within the substation building environment is subjected to electromagnetic interference as well as voltage surges.

5.3.11 For the purpose of control 110 V DC auxiliary supply is available with the minimum supply voltage being 88 V and the maximum being 118 V.

6.0 TECHNICAL REQUIREMENTS

6.1 The development, installation, commissioning and performance evaluation of a 3 kV DC supply to a 2460 V, 3 phase or 1260 V, 6 phase-AC nominal 50 Hz prototype inverter module that would feed the regenerated power back to the main traction transformer under non-receptive conditions.

6.2 The development, installation and performance evaluation of an ACTIVE HARMONIC POWER FILTER module to remove unwanted harmonic content from the power being fed back into the supply under normal load conditions.

6.3 The development, installation and evaluation of a standalone control unit, with one or more signal processor and/or an embedded controller, to enable setting and adjusting of parameters and saving and retrieving of data.

6.4 The development, installation and evaluation of the control and diagnostic software for the complete system.

6.5 The system shall be able to feed back the regenerated power via the main traction transformer. It is that the inverter's output should be connected on the secondary of the rectifier transformer.

6.6 The quality of the energy, which is fed into the Eskom's transmission network, shall comply with SABS NRS 048.

6.7 The impact of the regenerated energy on the metering on the primary side of the traction substation supply shall also be investigated, and if changes need to be done to the ESKOM/municipal metering, Spoornet must be advised thereof.

6.8 If the prototype inverter is proven successful a further requirement is that the prototype shall be industrialised for future installation in Spoornet's substations where a need is for regenerative energy absorption equipment.

7.0 PERFORMANCE REQUIREMENTS

7.1 The system shall be able to invert 1,5 MW of continuous regenerated energy and feed that to the supply network.

7.2 The power electronic components used for switching on the DC input side shall have a voltage rating of at least 4000 V.

7.3 All semiconductors used in the design shall use the highest voltage rating available to minimise the number of semiconductors stacked in series.

7.4 The system shall respond correctly to the amplitude and frequency of the voltage regenerated by the locomotives.

7.5 The equipment shall be capable of operating satisfactorily at supply voltage variations of ± 5% especially in the active filter mode.

7.6 Supply frequency: The equipment shall be capable of operating satisfactorily at traction substation power frequencies ranging from 49 to 51 Hz.

8.0 CONTROL UNIT REQUIREMENTS

8.1 The control unit shall contain an embedded processor typically of the TMS 320C30 or similar bus type.

8.2 The control unit shall be designed in such a manner that it will be protected against electromagnetic interference as well as voltage surges to ensure normal operation under all substation load and fault conditions.

8.3 The control unit shall have a LCD text type display and a control panel to control the functioning of all modules that form part of the system.

8.4 The unit shall have a keyboard mounted on the front panel of the control unit to enable the user/developer to enter /change/edit parameters select data etc. with a suitable menu displayed on the control unit.

8.5 The control unit shall have at least a flash type storage device as well as at least 8-16MB of random access memory.

8.6 The unit shall have built in watchdog protection circuit, which must be software selectable, as well as a real time clock/calendar.

8.7 The unit shall have one or more serial ports of which at least one must be a RS232 port and the other one could be a RS422/485 port.

8.8 Other functionality in the form of add-on cards may be added to the system if required.

8.9 The control unit must utilise other specialised processors/embedded controllers/signal processors for the sensing, signal processing, control and switching of the power electronics.

9.0 SOFTWARE REQUIREMENTS

9.1 The software for the calculation, control and switching of the power electronics, as well as the display, user interface, communication, diagnostic and recording function.

9.2 A personal computer may be used during the development stages of the project to ease the development of software for the prototype, and for demonstration purposes, but will have to be replaced by an embedded solution for the final system.

9.3 The software shall be written to make provision for the saving and retrieving of a complete history of the time, date, duration, and amplitude of each and every regeneration event, and shall also provide a summary of the total amount of regenerated energy received by the system and the amount of regenerated energy fed into the network.

9.4 The software shall be written to display a number of parameters on a LCD display, to enable the operator to see the parameters and make changes to the setup of the system.

9.5 The software shall enable the operator to change certain set points, but not enable him to make any changes to the limits that could influence the correct working of the regeneration system. The software must allow the operator to increase/decrease the voltage level where regeneration must start, as this is dependent on the ruling gradient of the line in a substation section.

9.6 The software shall make provision for the setup parameters to be stored in non-volatile memory to enable the system to restart reliably and with the setup parameters intact after a power failure.

9.7 The software shall enable the operator to interface to an RS232 serial port for remote downloading of the information.

9.8 An existing protocol may be used or a custom one may be developed for the serial communications via the RS232 port.

9.9 The software must include a soft starting algorithm and hardware to enable the system to start reliably and to isolate it from the AC side of the feedback path in case of a system fault.

9.10 The software shall include a startup diagnostic routine to determine whether all the building blocks are functioning correctly and whether all the input signals are present and within the acceptable limits, and whether all the control signals and outputs are functional.

9.11 All digital outputs must have a readback function to ascertain whether outputs are really in the specified state, after every change in state.

9.12 The software shall make provision for a watchdog function to be incorporated that will ensure a reliable system reset in the event of the system "hanging up" or a total power failure. The diagnostic software shall make provision for fault logging.

10.0 INSULATION AND CLEARANCES

10.1 The minimum clearance distance in air that shall apply from the 3 kV DC circuit to the auxiliary circuits and to the steel base shall be 150 mm. Alternatively, double insulation or barriers shall be provided.

10.2 If the equipment is installed in a fully enclosed cubicle this dimension may be reduced to 75 mm.

10.3 Where these air clearances cannot be fully maintained a suitable insulation barrier made from Celeron/Tuff-Null/GP03 shall be installed. Asbestos is not acceptable.

104 The insulation between the 3 kV DC circuit and the (a) auxiliary circuits, and (b) steel base shall be capable of withstanding a test voltage of 10,5 kV (rms), 50 Hz for one minute.

10.5 All low voltage auxiliary equipment shall be capable of withstanding a test voltage of 2 kV (rms), 50 Hz for one minute.

10.6 All measurement/control signals from the 3kV DC side of the inverter equipment shall be sent via fibre optic cable to any interface, instrument, computer or indicating panel.

10.7 Insulating transformers, if used to supply sensing devices, measuring equipment and controls, shall be insulated to ground and between windings for a test voltage of 20 kV, 50 Hz for one minute. The insulating transformers shall be of the dry type.

10.8 Adequate insulation shall be provided inside the system to ensure that under no circumstances will it be possible for the 110 volt DC battery supply or the 380 volt AC auxiliary supply to come into contact with each other or with the high voltage supplies on the input or the output side of the system.

10.9 No leads, circuits or apparatus energised at, or which may be energised at a voltage of 1000 V or more, shall be installed outside the screened inverter enclosure or be accessible from the outside of the screen or within 450 mm of any mesh type screens provided around high voltage equipment, unless suitable protection is provided in the form of insulation or an insulating barrier.

11.0 CREEPAGE DISTANCES

All equipment installed on the 3 kV DC side shall have a creepage distance of not less than 520 mm.

12.0 GENERAL REQUIREMENTS

12.1 The system shall operate via the 110 volt DC supply, to ensure the backup of the batteries in the case of the failure of the 380 volt AC auxiliary supply.

12.2 The system must be modular so that the different components can be accessed if necessary for maintenance purposes.

12.3 Electronic ammeter, voltmeter and Wattmeter shall be supplied separately or can be part of the LCD display to indicate the amplitude as well as the direction of current flow into and out of the system.

12.4 All material used shall be of class F flame retardant.

13.0 CUBICLE

13.1 A suitable steel cubicle shall be used for mounting and housing the inverter and its control unit. The cubicle shall be provided with access to the control unit from the front, provided that precautions are taken to prevent excessive voltages reaching the control equipment and wiring.

13.2 The cubicle shall be connected to the substation DC earth leakage system.

13.3 The cubicle shall be provided with interlocking such that under no circumstances the cubicle will be opened without the 3 kV DC circuit breaker being switched off and racked out.

13.4 The overall dimensions of the cubicle shall be such as to pass through the doorways of the substation building.

14.0 INSTALLATION

14.1 The site for the installation will be selected to suit both parties, but with due regard for the interests of Spoornet.

14.2 The installation shall be a joint venture between the two parties and the details (including cost) regarding material, transport and labour shall be discussed and agreed to at a later stage.

14.3 Spoornet shall provide a list of all the possible locations where an installation can be done for evaluation.

14.4 Installation shall be done only under the direct supervision of a designated representative of Spoornet in possession of the necessary switching certification in terms of Spoornet's Electrical Safety Instructions.

15.0 PROTECTION AND EARTHING

15.1 For the purpose of regeneration a 3 kV DC high-speed circuit breaker (HSCB) is provided as a free issue.

15.2 All areas that are at 3 kV potential shall be behind a fence with the necessary interlocking to the existing earthing system in the substation.

15.3 The cubicle of the inverter and control equipment shall be connected to the existing DC earth leakage system in accordance to Drawing No. CEE-TBD-7.

15.4 All potential divider/ voltage sensing devices shall be securely connected to the Substation main negative.

15.5 Current sensing shall be done at the Substation negative except where use is made of isolated Hall-effect current transducers where individual currents need to be measured e.g. at the rectifier input.

15.6 The use of fibreoptic cables to transmit measurement signals is allowed. However the fibre optic transmitters must be powered from the high voltage circuit which is being monitored. Batteries would not be allowed, because of problems associated with the replacement of batteries in the high voltage cubicles during routine maintenance.

15.7 All input modules should have adequate lightning protection.

16.0 WIRING AND INTERCONNECTIONS

16.1 All wiring shall be neatly done and tidied with straps etc. to prevent loose wires from lying around.

16.2 All wiring shall be neatly, durably marked and recorded in accordance to a wiring diagram.

16.3 Conductors may be individually connected to terminal strips or use may be made of Military Specification gold plated plugs and sockets.

16.4 All inline plugs and sockets shall be of the lockable type i.e. securing screws or clips.

16.5 All wiring shall be easily accessible for maintenance purposes except for high voltage wiring.

16.6 All wiring shall be laid in the existing trenches where possible.

16.7 All interconnections to and from sensitive equipment shall be made with braided screened wire.

16.8 All the individual conductor screens shall be earthed using standard earthing procedures to minimise stray currents and earthing loops.

16.9 All copper to steel (galvanised) connections shall be tinned or silver plated.

17.0 REPORTING

17.1 The contractor shall provide a project schedule indicating planned progress.

17.2 Two monthly progress meetings will be held at which time the contractor shall provide a written progress report to Spoornet.

17.3 The contractor shall provide full documentation on all main components with the delivery of the prototype inverter on site. The documentation shall comprise Instruction Manuals, Maintenance procedures, faultfinding procedures, component lists and drawings.

17.4 After completion and installation and completion of on site test and commissioning a report shall be presented incorporating the results of all tests as per clause 18.0.

18.0 TESTS, ON-SITE TESTS AND COMMISSIONING

18.1 Full load, overload and performance tests shall be conducted to ensure that the inverter complies with the values specified. The operating temperatures of the power semiconductors shall be checked to ensure that they do not exceed the maximum value specified by the supplier.

18.2 Functional on-site tests shall be conducted on all items of equipment and circuitry to prove the proper functioning and installation thereof.

18.3 Prior to commencement of tests, the contractor shall submit a detailed list of on-site tests for approval by Spoornet.

18.4 The contractor shall arrange with Spoornet's project leader to be present to witness the on-site tests.

18.5 The contractor shall be responsible for carrying out on-site tests and commissioning of all equipment supplied and installed in terms of this specification and the contractual agreement.

18.6 The on-site tests and subsequent commissioning will not commence until **ALL CONSTRUCTION WORK** has been completed. Construction material and equipment not required for testing shall be removed from site prior to the commencement of testing. Testing and commissioning of the inverter equipment will not be allowed to take place in a construction environment.

18.7 Commissioning will only take place after all defects have been rectified to the satisfaction of the appointed project leader of Spoornet.

18.8 Commissioning will include the energising of the equipment from the 3 kV DC regen breaker to the secondary of the rectifier transformer.

END

Appendix B – Software programs

B.1. – Matlab code for conduction losses and modulation function

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Matlab code for the calculation of the conductions %
% losses in the IGBT module and plotting of the      %
% modulation function                                %
% 2005-02                                            %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clear
clf
hold on

xlim([-1e-3 21e-3]);
ylim([-1.1 +1.1]);

%-------------------------------------

% Calculation of Conduction Losses

f = 50;
w = 2*pi*f;
ma = 0.75;
Von = 2.3;
Io = 220;

b = 30e-3/18;
T1 = 20e-3;
t1 = 60e-3/18;
t2 = 120e-3/18;
ta = 90e-3/18;
t3 = 180e-3/18;

% Losses In Top Switch

% Segment 1
A1 = (Io/w)*( 1 - cos(w*t1) );
B1 = (ma*Io)*( ( cos(w*b) )*( 1/(4*w) - ( cos(2*w*t1) )/(4*w) ) +
     ( sin(w*b) )*( t1/2 - ( sin(2*w*t1) )/(4*w) ) );
P1 = (Von/(2*T1)) * (A1 + B1);

% Segment 2 (positive part)
A2 = (Io/w)*(cos(w*t1)-cos(w*ta));
B2 = (sqrt(3)*ma*Io)*( (cos(2*w*t1))/(4*w) - (cos(2*w*ta))/(4*w) );
P2 = (Von/(2*T1)) * (A2 + B2);

PS1 = 2*(P1 + P2)

% Losses In Bottom Diode

% Avg Load Current For Positive Part of Modulation Func
IL = (2*Io)/(T1*w) * (1-cos(w*ta));

% Avg Current For Top Switch
IS1 = 2*(P1/Von + P2/Von);

% Avg Diode Current
```

```
ID2 = IL - IS1;
PD2 = Von*ID2

Ptotcond = PS1 + PD2


%-----------------------------------

% Modulation Function

a0 = 0:0.000001:(60e-3/18);
f0 = ma.*cos(w*(a0-(30e-3/18)));
plot(a0,f0,'b')
a1 = (180e-3/18):0.000001:(240e-3/18);
f1 = ma.*cos(w*(a1-(30e-3/18)));
plot(a1,f1,'b')

a2 = (60e-3/18):0.000001:(120e-3/18);
f2 = sqrt(3).*ma.*cos(w*a2);
plot(a2,f2,'b')
a3 = (240e-3/18):0.000001:(300e-3/18);
f3 = sqrt(3).*ma.*cos(w*a3);
plot(a3,f3,'b')

a4 = (120e-3/18):0.000001:(180e-3/18);
f4 = ma.*cos(w*(a4+(30e-3/18)));
plot(a4,f4,'b')
a5 = (300e-3/18):0.000001:(360e-3/18);
f5 = ma.*cos(w*(a5+(30e-3/18)));
plot(a5,f5,'b')


%-----------------------------------

% Grid Lines

y = -1.2:0.002:1.2;
x0 = 0;
plot(x0,y)
x1 = 60e-3/18;
plot(x1,y)
x2 = 120e-3/18;
plot(x2,y)
x3 = 180e-3/18;
plot(x3,y)
x4 = 240e-3/18;
plot(x4,y)
x5 = 300e-3/18;
plot(x5,y)
x6 = 360e-3/18;
plot(x6,y)

ya = -1.1:0.03:1.1;
Xa = 90e-3/18;
plot(Xa,ya,'k')

y2 = 0;
y3 = 1;
y4 = -1;
```

```
x7 = -2e-3:0.00003:22e-3;
plot(x7,y2)
plot(x7,y3)
plot(x7,y4)

%-----------------------------------
```

B.2. – VHDL code for the encoding of the voltage measurements

```
-- $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
-- $$ 28-06-04 14:44                                                                          $$
-- $$ Program for encoding of the voltage measurements and transmitting to the PEC33         $$
-- $$ Data is received in parallel mode from the ADC                                         $$
-- $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity p_vmb_final is
       port   (clk           : in   std_logic;      --30 MHz clock
               n_reset       : in   std_logic;
               mode          : out  std_logic;      --ADC in parallel or serial mode
               n_standby     : out  std_logic;
               n_rd          : out  std_logic;
               n_cs          : out  std_logic;
               n_eoc         : in   std_logic;
               led           : out  std_logic;      --indicates when data is sent

              --used in the reading of data from the ADC
               db0           : in   std_logic;
               db1           : in   std_logic;
               db2           : in   std_logic;
               db3           : in   std_logic;
               db4           : in   std_logic;
               db5           : in   std_logic;
               db6           : in   std_logic;
               db7           : in   std_logic;
               db8           : in   std_logic;
               db9           : in   std_logic;
               db10          : in   std_logic;
               db11          : in   std_logic;
               n_data_req    : in   std_logic;      --data request from controller
               n_convst      : out  std_logic;      --start of conversion pulse for ADC

              --the following is used in encoding and sending of the data
               data_out      : out  std_logic);            --data sent via the fibre optic

end entity p_vmb_final;

--*********************************************************************
--=====================================================================
--=====================================================================
--*********************************************************************

architecture lyf of p_vmb_final is

--used for reading of data
       type   bla_states is (data_req_state, n_convst_state, n_convst_rise_state,
delay_state,                                 data_read_state);
       signal  conv_state             : bla_states;
       signal  chip_counter           : integer range 0 to 6;
       signal  chip_flag              : std_logic;
       signal  data_ready_flag        : std_logic;
       signal  n_convst_sig           : std_logic;
       signal  p_data                 : std_logic_vector(15 downto 0);
       signal   convst_count          : integer range 0 to 9;

--used for encoding and sending of data
       type   pulse is (decode_state, s_pulse, one_pulse, zero_pulse);
       signal  next_state             : pulse;
```

```
        signal  chip_signal           : std_logic;
        signal  chip_clk              : std_logic;
        signal  output_sig            : std_logic;
        signal  data_done_flag        : std_logic;
        signal  bit                   : integer range 0 to 15;
        signal  s_pulse_counter       : integer range 0 to 4;
        signal  one_pulse_counter     : integer range 0 to 4;
        signal  zero_pulse_counter    : integer range 0 to 4;
        signal   singnal_n_data_req   : std_logic;
begin

n_standby      <= '1';
mode           <= '1';        --ADC in parallel mode
n_convst <= n_convst_sig;
data_out <= output_sig;

--%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
--************************************************************************
--%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

--this process generates the chip_clk used to time the rest of the system
process (clk) is
begin
        if (n_reset = '0') then
                chip_counter <= 0;
        elsif rising_edge (clk) then
                        if (chip_counter = 5) then
                                chip_clk              <= '1';
                                chip_signal           <= '1';
                                chip_counter   <= 0;
                        else
                                chip_clk              <= '0';
                                chip_signal           <= '0';
                                chip_counter   <= chip_counter + 1;
                        end if;
        end if;
end process;

--************************************************************************
--========================================================================
--========================================================================
--************************************************************************

--%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
--%% Control of the signals for reading data from the ADC %%
--%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

-- ************************************************************************
-- This process checks for a data request from the controller and reads data
-- from the ADC

process (clk) is
begin
        if (n_reset = '0') then
                n_convst_sig <= '1';
        elsif rising_edge (clk) then
                case conv_state is
                        when data_req_state =>
                                n_cs <= '1';
                                n_rd <= '1';
                                if (singnal_n_data_req = '0') then
                                        conv_state <= n_convst_state;
                                end if;
                                if (data_done_flag = '1') then
                                        data_ready_flag <= '0';
                                end if;

                        when n_convst_state =>
                                data_ready_flag <= '0';
                                if (chip_signal = '1') then
                                        n_convst_sig <= '0';
                                        conv_state <= n_convst_rise_state;
                                end if;

                        when n_convst_rise_state =>
                                if (chip_signal = '1') then
                                        n_convst_sig <= '1';
```

```
                                conv_state <= delay_state;
                        end if;

                when delay_state =>
                        if (chip_signal = '1') then
                                if ( convst_count = 8) then   -- wait for 1.8us
                                        n_cs <= '0';
                                        n_rd <= '0';
                                        convst_count <= 0;
                                        conv_state <= data_read_state;
                                else
                                        convst_count <= convst_count + 1;
                                end if;
                        end if;

                when data_read_state =>
                        if (chip_signal = '1') then
                                conv_state <= data_req_state;
                                data_ready_flag <= '1';
                                                -- read data from the ADC
                                p_data(15) <= '0';
                                p_data(14) <= '0';
                                p_data(13) <= '0';
                                p_data(12) <= '0';
                                p_data(11) <= db11;
                                p_data(10) <= db10;
                                p_data(9) <= db9;
                                p_data(8) <= db8;
                                p_data(7) <= db7;
                                p_data(6) <= db6;
                                p_data(5) <= db5;
                                p_data(4) <= db4;
                                p_data(3) <= db3;
                                p_data(2) <= db2;
                                p_data(1) <= db1;
                                p_data(0) <= db0;
                        end if;
        end case;
        singnal_n_data_req <= n_data_req;     -- latch the data request signal
                                              -- from the PEC33
    end if;
end process;


--************************************************************************
--========================================================================
--========================================================================
--************************************************************************
--%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
--%% Start to encode and transmit data %%
--%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

process (clk) is
begin
    if (n_reset = '0') then
            next_state <= decode_state;
            bit <= 15;
    elsif rising_edge (clk) then
            case next_state is
                when decode_state =>
                        if(data_ready_flag = '1') then              -- wait for ADC
                                if (p_data(bit) = '1') then         -- check if data is
                                        next_state <= one_pulse;    -- a 1 or 0
                                else
                                        next_state <= zero_pulse;
                                end if;
                        else
                                next_state <= s_pulse;
                        end if;

                when s_pulse =>
                        led <= '1';                                 -- turn led off
                        bit <= 15;
                        data_done_flag <= '0';
                        if (chip_signal = '1') then
                                if (s_pulse_counter = 2) then       --is S-pulse
                                                                    --finished?
```

```
                                        output_sig <= not output_sig; -- change output
                                                                      -- level
                                        s_pulse_counter <= 0;
                                        next_state <= decode_state;   -- back to
                                                                      -- beginning
                                else
                                        s_pulse_counter <= s_pulse_counter + 1;
                                end if;

                        end if;

                when one_pulse =>
                        led <= '0';                                   -- turn led on
                        if (chip_signal = '1') then
                                if (one_pulse_counter = 1) then       --is 1-pulse
                                                                      --finished?
                                        output_sig <= not output_sig;
                                        one_pulse_counter <= 0;
                                        next_state <= decode_state;
                                        if (bit = 1) then
                                                data_done_flag <= '1';
                                        end if;
                                        if (bit = 0) then             -- 16 bits are
                                                                      -- encoded
                                                data_done_flag <= '1';
                                        else
                                                bit <= bit - 1;
                                        end if;
                                else
                                        one_pulse_counter <= one_pulse_counter + 1;
                                end if;

                        end if;

                when zero_pulse =>
                        led <= '1';                                   --turn led off
                        if (chip_signal = '1') then
                                if (zero_pulse_counter = 1) then      --is 0-pulse
                                                                      --finished?
                                        output_sig  <= not output_sig;
                                        zero_pulse_counter <= 0;
                                        next_state <= decode_state;
                                        if (bit = 1) then
                                                data_done_flag <= '1';
                                        end if;
                                        if (bit = 0) then
                                                data_done_flag <= '1';
                                        else
                                                bit <= bit - 1;
                                        end if;
                                else
                                        output_sig <= not output_sig;
                                        zero_pulse_counter <= zero_pulse_counter + 1;
                                end if;

                        end if;
        end case;
    end if;
end process;
end architecture lyf;
```

B.3. – VHDL code for the decoding of the voltage measurements

```
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
--$$ 29-06-04                                                              $$
--$$ This is the code for decoding the data received from the VMB and       $$
--$$ outputs the decoded data to be used in the PEC33                       $$
--$$ If an error is detected the last valid data is kept on the output      $$
--$$ Sync on the falling edge of data_in                                     $$
--$$ Bit 13 of decoded data indicates an error if 1                         $$
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity decode_final is
       port    (clk                          : in   std_logic;     --30 MHz clock
                       reset                 : in   std_logic;

                       data_in               : in   std_logic;     --data received
                                                                   from VMB
                       decoded_data          : out  std_logic_vector (12 downto 0);

                       data_req              : out  std_logic);    --req new data

end entity decode_final;

--*************************************************************************
--=========================================================================
--=========================================================================
--*************************************************************************

architecture lyf of decode_final is
--used to generate the data_req signal
       type    req_states is (data_in_zero_state, data_req_zero_state, data_use_state,
               wait_for_zero_state);
       signal  data_req_state               : req_states;
       signal  wait_count                   : integer range 0 to 50;

--used to sync with s_pulse and chip_clk
       type    bla_states is (sync_low_state, chip_clk_state, wait_state, setup_state);
       signal  chip_sync_state              : bla_states;
       signal  data_in_sync                 : std_logic;
       signal  chip_signal                  : std_logic;
       signal  chip_counter                 : integer range 0 to 6;
       signal  bit_count                    : integer range 0 to 3;
       signal  low_flag                     : std_logic;
       signal  offset_count                 : integer range 0 to 6;
       signal  receive_flag                 : std_logic;
       signal  bit_flag                     : std_logic;
       signal  stop_flag                    : std_logic;
       signal  sync_low_flag                : std_logic;
       signal  req_flag                     : std_logic;

--used for reading and decoding data_in
       type    my_states is (non_data_state, second_bit_state,
               third_bit_state, third_bit_zero_state, forth_bit_state, error_state);
       signal  bit_state                    : my_states;
       signal  error_flag                   : std_logic;
       signal  data_ready_flag              : std_logic;
       signal  data_out                     : std_logic_vector (15 downto 0); --decoded data,
                                                                              -- 12 data bits
                                                                              -- and 4
                                                                              --leading zeros
       signal  data_count                   : integer range 15 downto 0;
       signal  first_bit                    : std_logic;
       signal  second_bit                   : std_logic;
       signal  third_bit                    : std_logic;
       signal  forth_bit                    : std_logic;
       signal  data_in_zero_state_flag      : std_logic;
       signal  wait_for_zero_flag           : std_logic;
       signal   third_bit_zero_state_flag   : std_logic;

--*************************************************************************

begin

decoded_data          <= data_out (12 downto 0);
```

```
--**********************************************************************
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
--$$ Generate the data_req signal $$
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
process (clk) is
begin
	if (reset = '1') then
		wait_count <= 0;
		data_req <= '1';			--data_req is active low signal
		data_req_state <= data_in_zero_state;
	elsif rising_edge (clk) then
		case data_req_state is
			when data_in_zero_state =>
				data_req <= '1';
				if (data_in_sync = '1' and req_flag = '1' and error_flag = '0')
						then		--check for when data_in is a one

					data_req_state <= data_req_zero_state;
				else
					data_req_state <= data_in_zero_state;
				end if;

			when data_req_zero_state =>
				data_req <= '0';	--send a data_req when data_in is a one
				if (data_in_sync = '0') then
					data_req_state <= data_use_state;
				end if;

			when data_use_state =>
				data_req <= '1';	--reset data_req signal

				wait_for_zero_flag <= '0';

				if (data_ready_flag = '0') then --all the data has been received
					data_req_state <= wait_for_zero_state;

				elsif (chip_signal = '1' and error_flag = '0') then
									-- wait to see if data is
									-- sent
					if (wait_count = 45) then
						data_req_state <= wait_for_zero_state;
					else
						wait_count <= wait_count + 1;
					end if;
				elsif (error_flag = '1') then
					wait_count <= 0;
				end if;

			when wait_for_zero_state =>   --wait for the first low s_pulse
				wait_count <= 0;
				wait_for_zero_flag <= '1';
				data_req <= '1';
				if (data_in_sync = '0') then
					data_req_state <= data_in_zero_state;
				end if;
		end case;
	end if;
end process;
--**********************************************************************
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
--$$ This process syncs the data_in with the global clk $$
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
process (clk) is
begin
	if rising_edge (clk) then
		data_in_sync <= data_in;
	end if;
end process;
--**********************************************************************
--**********************************************************************
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
--$$ Sync the chip_clk with the falling edge of data_in $$
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
process (clk) is
begin
	if (reset = '1') then
```

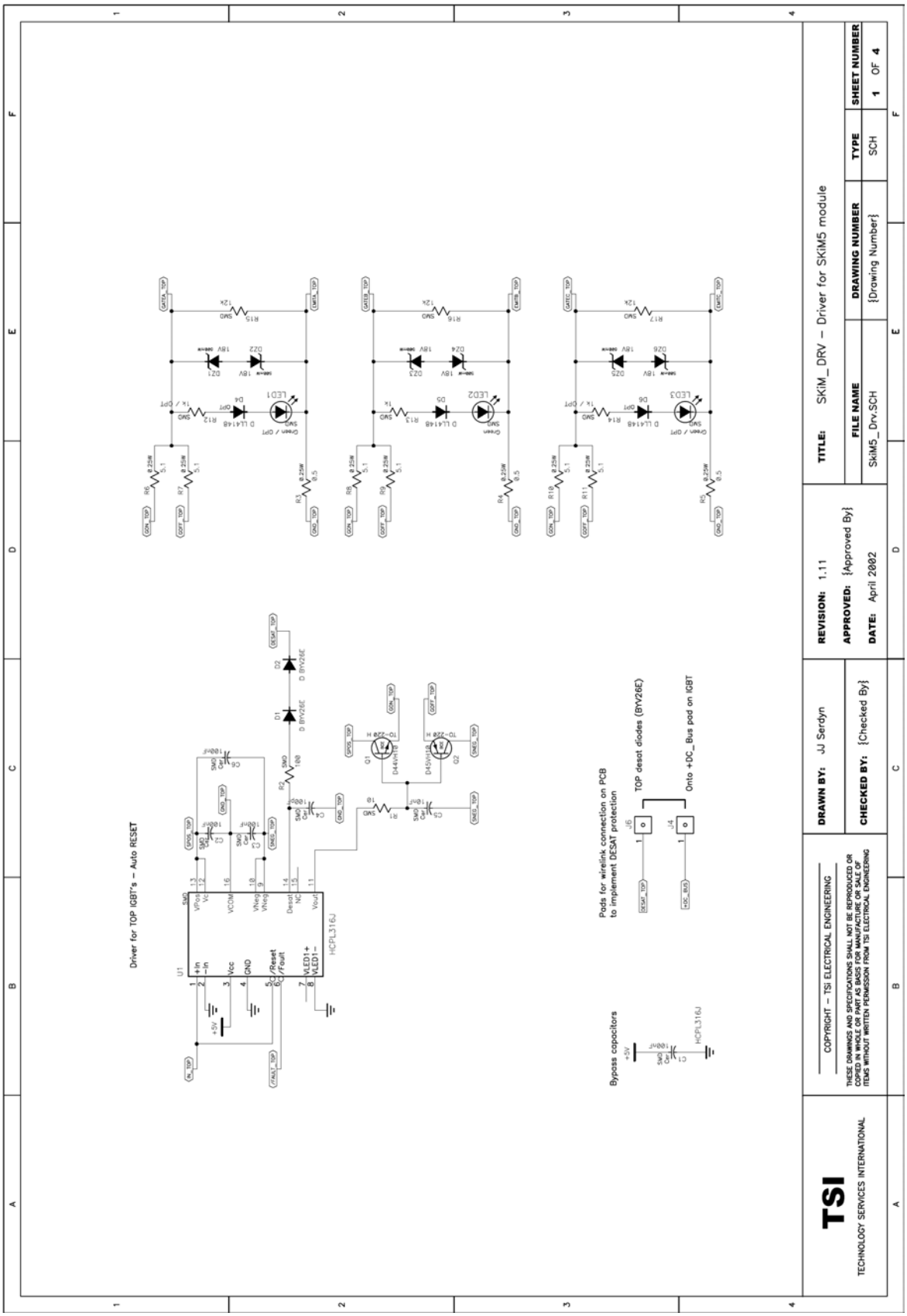
```
                sync_low_flag <= '0';
                req_flag <= '0';
                chip_sync_state <= setup_state;
                chip_signal <= '0';
                chip_counter <= 0;
        elsif rising_edge (clk) then
                case chip_sync_state is
                        when setup_state =>
                                if (data_in = '1') then       --wait for data_in to be a one
                                        chip_sync_state <= wait_state;
                                else
                                        chip_sync_state <= setup_state;
                                end if;

                        when wait_state =>
                                if (data_in = '0') then       --wait for data_in to be a zero
                                        chip_sync_state <= sync_low_state;
                                else
                                        chip_sync_state <= wait_state;
                                end if;

                        when sync_low_state =>
                                if (sync_low_flag = '1') then --resets the data_req signal
                                        req_flag <= '1';
                                end if;

                                if (data_in = '0') then       --reset the counter
                                        chip_counter <= 0;
                                        chip_sync_state <= chip_clk_state;
                                end if;

                        when chip_clk_state =>
                                if (data_in = '1') then       --indicate to send a data_req
signal
                                        sync_low_flag <= '1';
                                end if;

                                if (chip_counter = 5) then
                                        chip_counter <= 0;
                                elsif (chip_counter = 1) then
                                        chip_signal <= '1';
                                        chip_counter <= chip_counter + 1;
                                else
                                        chip_signal <= '0';
                                        chip_counter <= chip_counter + 1;
                                end if;

                                if (low_flag = '0') then
                                        if (data_in = '0') then
                                                chip_sync_state <= sync_low_state;
                                        end if;
                                end if;
                end case;
        end if;
end process;

--**************************************************************************

process (clk) is
begin
        if rising_edge (clk) then
                if (data_in = '0') then
                        low_flag <= '1';
                else
                        low_flag <= '0';
                end if;
        end if;
end process;

--**************************************************************************

process (clk) is
begin
        if (reset = '1') then
                receive_flag <= '0';
        elsif rising_edge (clk) then
                if (chip_signal = '1') then
```

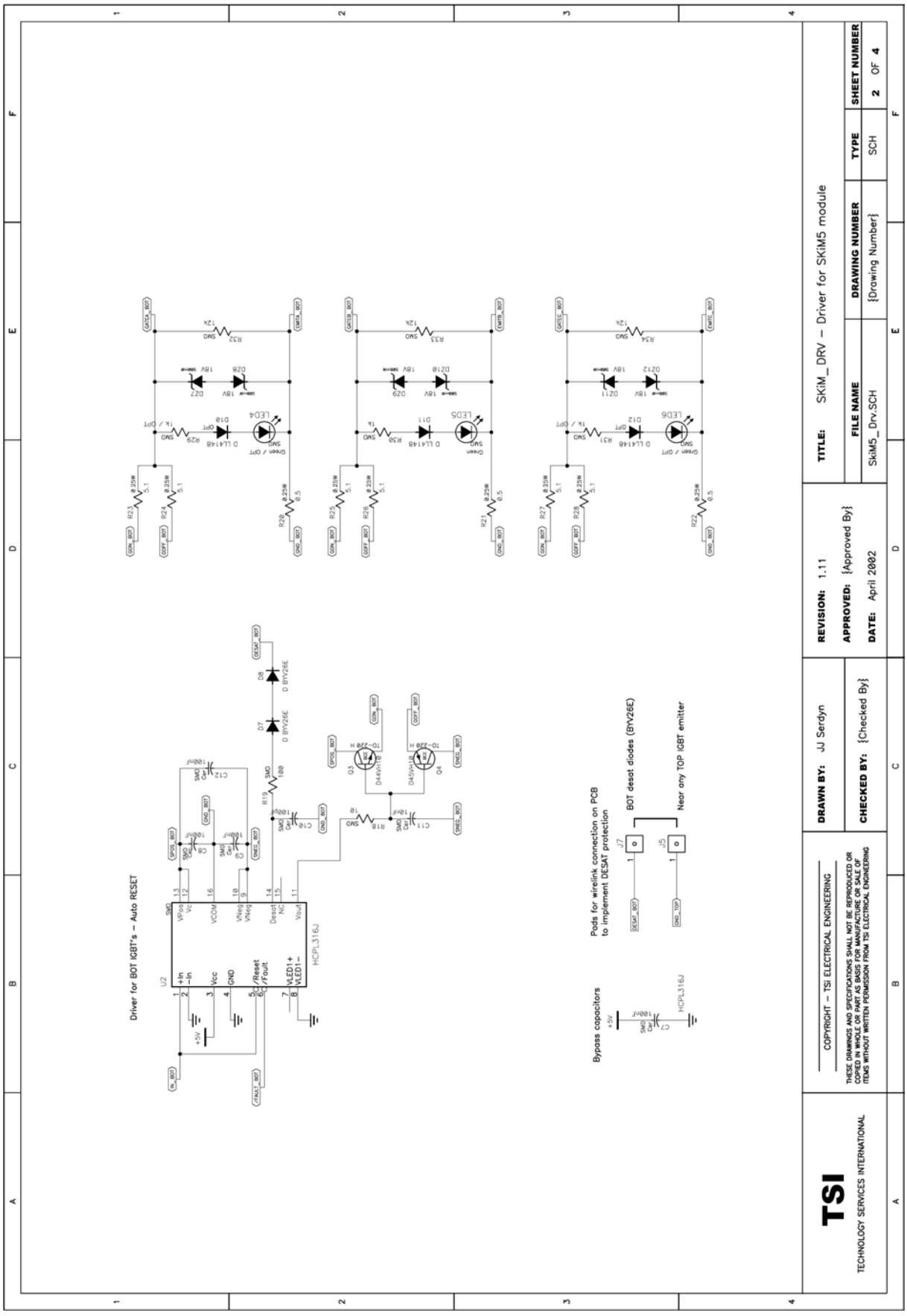
```
                        receive_flag <= '1';
                elsif (error_flag = '1') then
                        receive_flag <= '0';
                end if;
        end if;
end process;

--*************************************************************************
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
--$$ Read data_in and decode it $$
--$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

process (clk) is
        variable reg   : std_logic_vector (15 downto 0);
begin
        if (reset = '1') then
                bit_state <= non_data_state;
                data_ready_flag <= '1';
                data_count <= 0;
                data_out <= "0000000000000000";
                error_flag <= '0';
                reg := "0000000000000000";
        elsif rising_edge (clk) then
                case bit_state is
                        when non_data_state =>
                                data_count <= 0;
                                if (chip_signal ='1') then
                                        if (sync_low_flag = '1' and data_in_sync = '0') then
                                                bit_state <= second_bit_state;
                                                first_bit <= data_in_sync;
                                        else
                                                bit_state <= non_data_state;
                                        end if;
                                end if;

                        when second_bit_state =>
                                if (chip_signal = '1') then
                                        second_bit <= data_in_sync;
                                        data_ready_flag <= '1';
                                        if (first_bit = data_in_sync) then
                                                bit_state <= third_bit_state;

                                        elsif (error_flag = '1') then
                                                bit_state <= non_data_state;

                                        elsif (wait_for_zero_flag = '1') then
                                                data_count <= 0;

                                        else
                                                bit_state <= third_bit_zero_state;
                                                third_bit_zero_state_flag <= '1';
                                        end if;
                                end if;

                        when third_bit_state =>
                                if (chip_signal = '1') then
                                        third_bit <= data_in_sync;
                                        if (second_bit = data_in_sync) then
                                                bit_state <= forth_bit_state;

                                        elsif (error_flag = '1') then
                                                bit_state <= non_data_state;

                                        else
                                                reg := reg (14 downto 0) & '1'; --shifts the new
                                                                                        value
                                                                                into register
                                                first_bit <= data_in_sync;
                                                bit_state <= second_bit_state;
                                                if (data_count = 15) then
                                                        data_ready_flag <= '0';
                                                        data_count <= 0;
                                                        data_out <= reg;       --outputs new data

                                                elsif (wait_for_zero_flag = '1') then
                                                        data_count <= 0;
                                                else
```

```
                                        data_count <= data_count + 1;
                                end if;
                        end if;
                end if;

        when third_bit_zero_state =>
                if (chip_signal = '1') then
                        third_bit <= data_in_sync;
                        if (second_bit = data_in_sync) then
                                bit_state <= error_state;
                                third_bit_zero_state_flag <= '0';
                        else
                                reg := reg (14 downto 0) & '0';
                                first_bit <= data_in_sync;
                                bit_state <= second_bit_state;
                                third_bit_zero_state_flag <= '0';
                                if (data_count = 15) then
                                        data_ready_flag <= '0';
                                        data_count <= 0;
                                        data_out <= reg;       --outputs new data

                                elsif (wait_for_zero_flag = '1') then
                                        data_count <= 0;
                                else
                                        data_count <= data_count + 1;
                                end if;
                        end if;
                end if;

        when forth_bit_state =>
                if (chip_signal = '1') then
                        forth_bit <= data_in_sync;
                        if (third_bit = data_in_sync) then
                                bit_state <= error_state;
                        else
                                error_flag <= '0';
                                first_bit <= data_in_sync;
                                bit_state <= second_bit_state;
                        end if;
                end if;

        when error_state =>
                if (chip_signal = '1') then
                        data_out(12) <= '1';
                        error_flag <= '1';
                        data_count <= 0;
                        bit_state <= non_data_state;
                end if;
    end case;
  end if;
end process;
end architecture lyf;
```

Appendix C – Schematics

C.1. – Schematics for the driver board of the IGBT module

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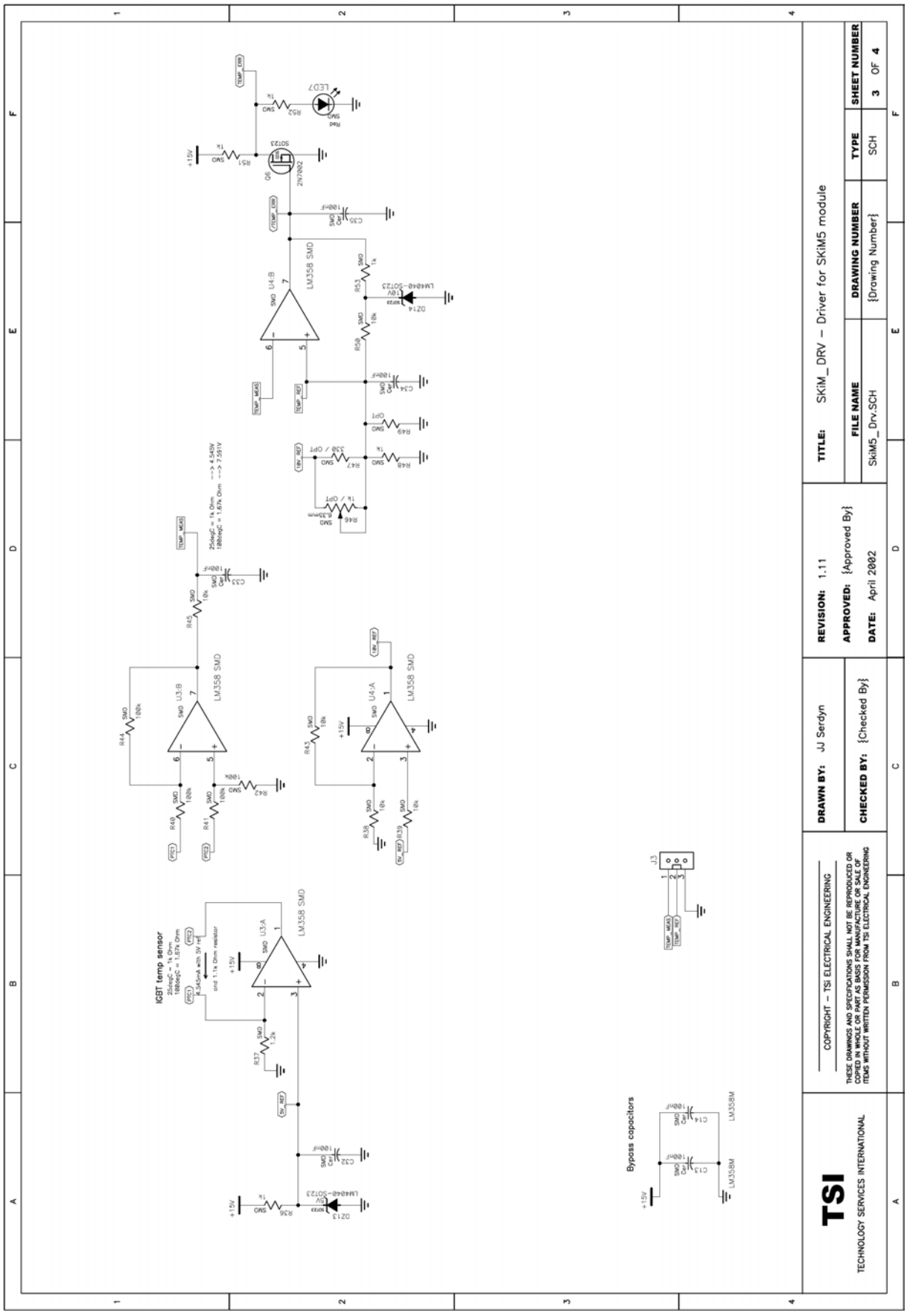
DRAWN BY: JJ Serdyn
CHECKED BY: {Checked By}
REVISION: 1.11
APPROVED: {Approved By}
DATE: April 2002
TITLE: SKiM_DRV – Driver for SKiM5 module
FILE NAME: SkiM5_Drv.SCH
DRAWING NUMBER: {Drawing Number}
TYPE: SCH
SHEET NUMBER: 2 OF 4
Driver for BOT IGBT's – Auto RESET
HCPL316J
Pods for wirelink connection on PCB to implement DESAT protection
BOT desat diodes (BY26E)
Near any TOP IGBT emitter
Bypass capacitors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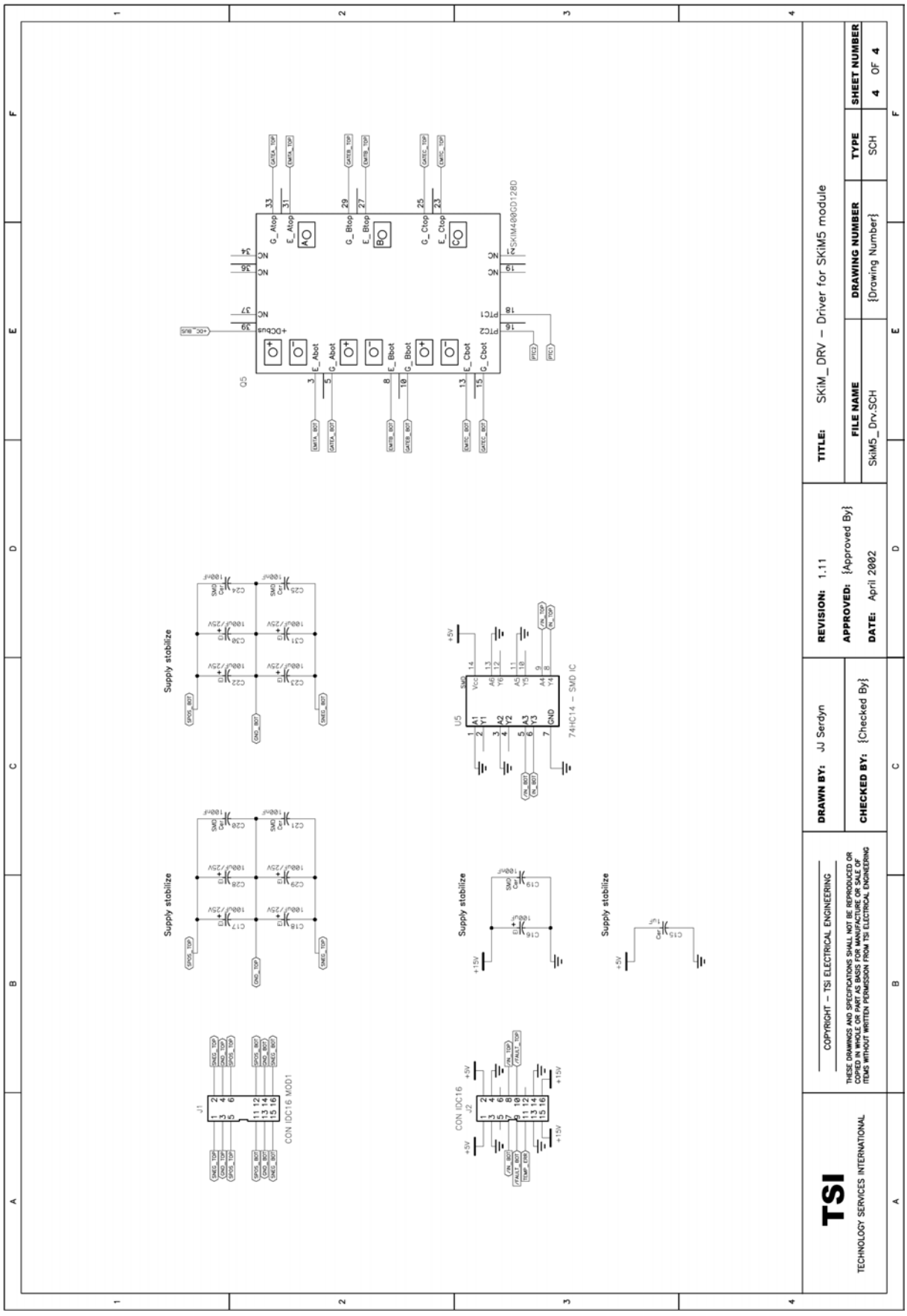
DRAWN BY: JJ Serdyn
CHECKED BY: {Checked By}
REVISION: 1.11
APPROVED: {Approved By}
DATE: April 2002
TITLE: SKiM_DRV – Driver for SKiM5 module
FILE NAME: SkiM5_Drv.SCH
DRAWING NUMBER: {Drawing Number}
TYPE: SCH
SHEET NUMBER: 3 OF 4
IGBT temp sensor
Bypass capacitors
LM358 SMD
LM358M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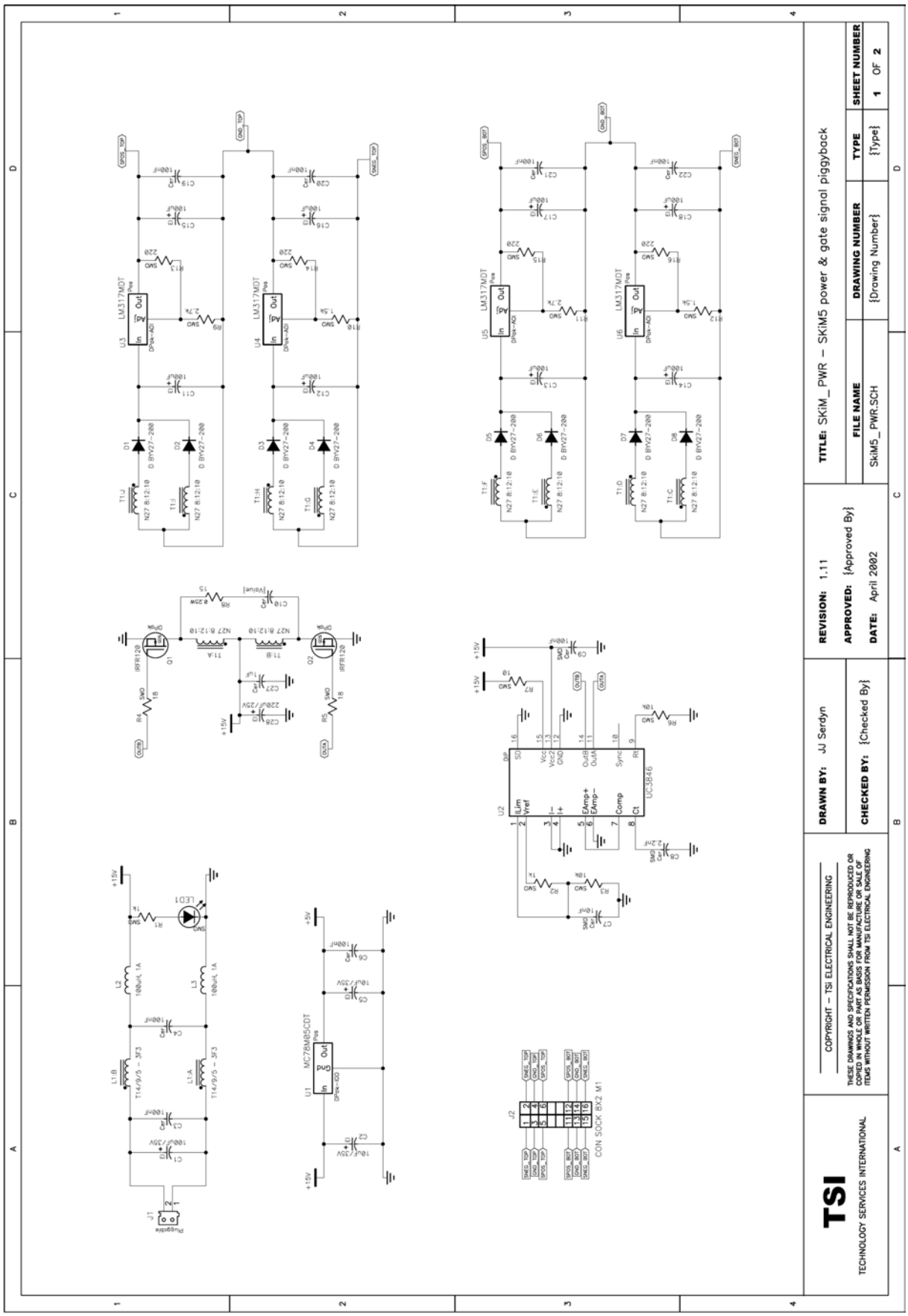
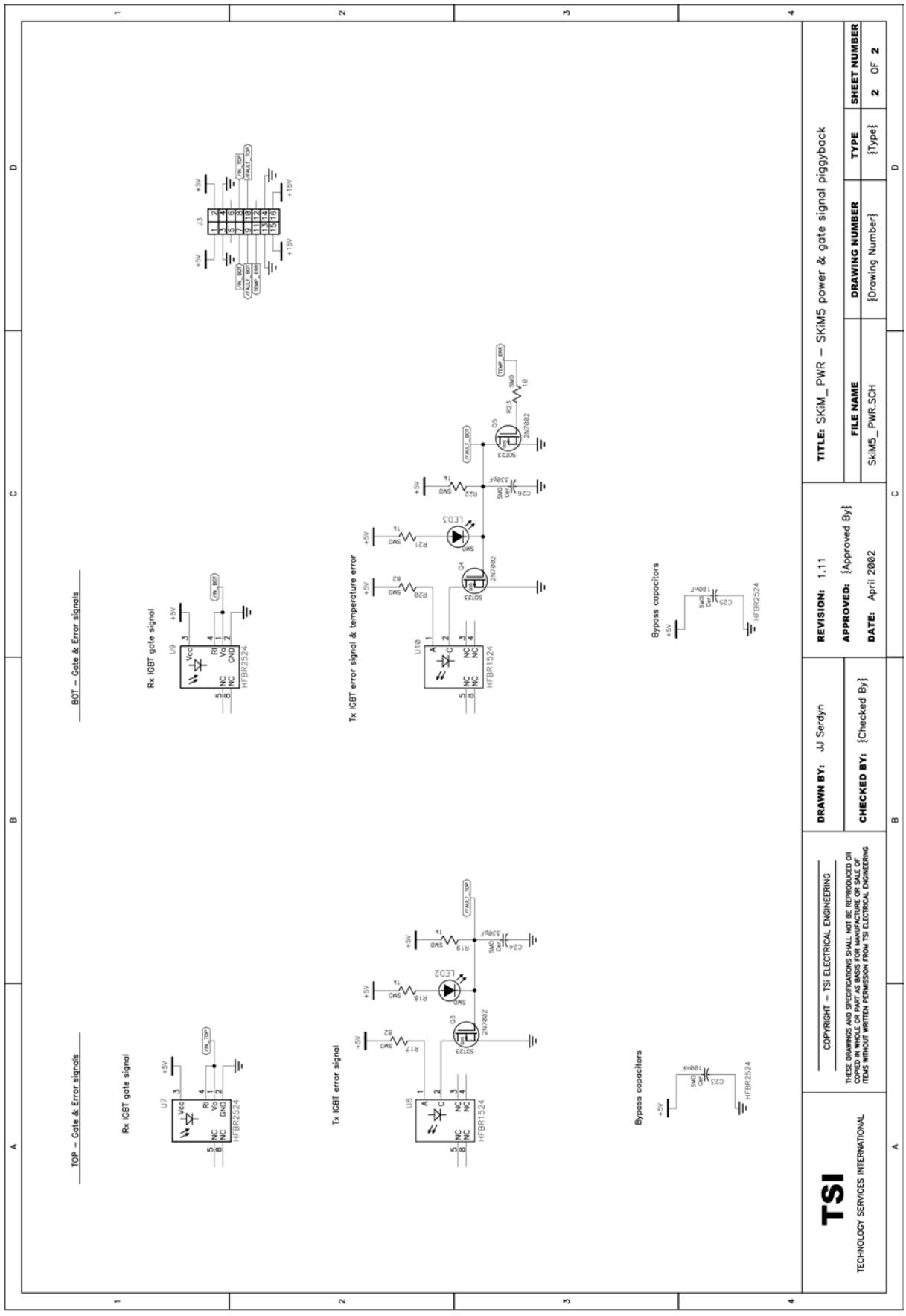
DRAWN BY: JJ Serdyn
CHECKED BY: {Checked By}
REVISION: 1.11
APPROVED: {Approved By}
DATE: April 2002
TITLE: SKiM_DRV – Driver for SKiM5 module
FILE NAME: SkiM5_Drv.SCH
DRAWING NUMBER: {Drawing Number}
TYPE: SCH
SHEET NUMBER: 4 OF 4
SKiM400GD128D
Q5
74HC14 – SMD IC
U5
CON IDC16 MOD1
J1
CON IDC16
J2
Supply stabilize
Supply stabilize
Supply stabilize
Supply stabilize

C.2. – Schematics for the power supply board for the IGBT driver




TOP – Gate & Error signals
BOT – Gate & Error signals
Rx IGBT gate signal
Tx IGBT error signal
Tx IGBT error signal & temperature error
Bypass capacitors
HFBR2524
HFBR1524
2N7002
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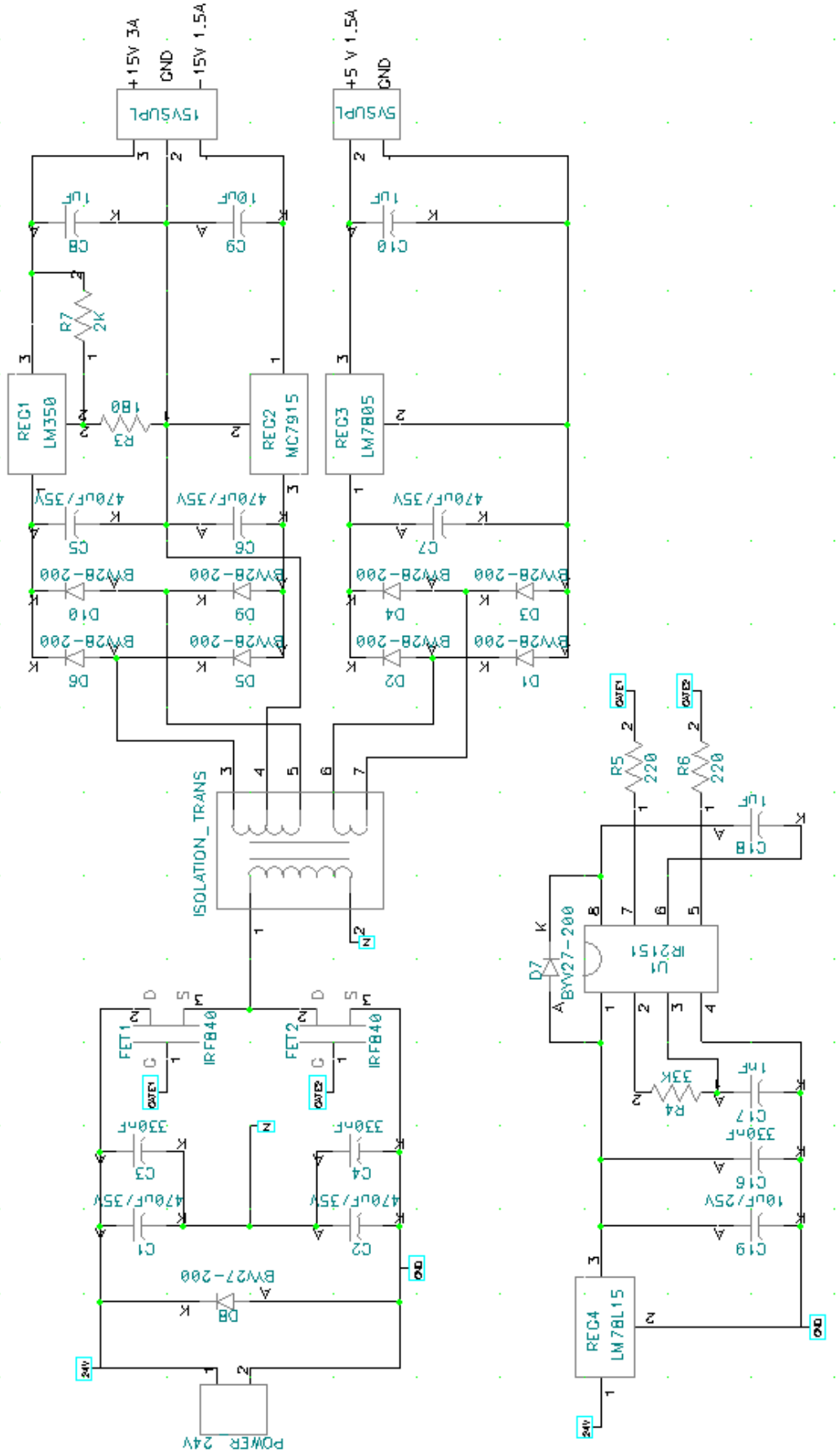
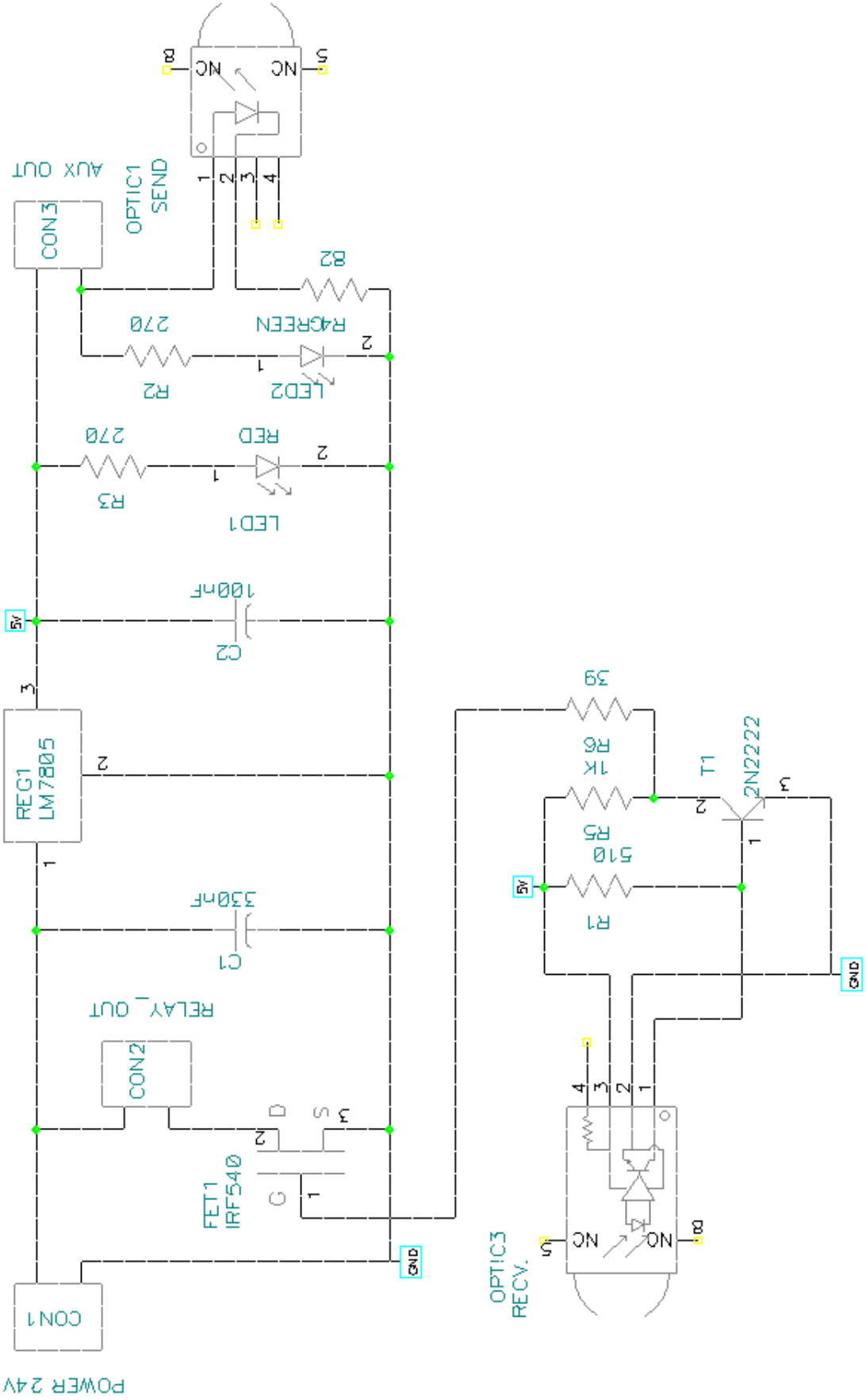
DRAWN BY: JJ Serdyn
CHECKED BY: {Checked By}
REVISION: 1.11
APPROVED: {Approved By}
DATE: April 2002
TITLE: SKiM_PWR – SKiM5 power & gate signal piggyback
FILE NAME: SKiM5_PWR.SCH
DRAWING NUMBER: {Drawing Number}
TYPE: {Type}
SHEET NUMBER: 2 OF 2

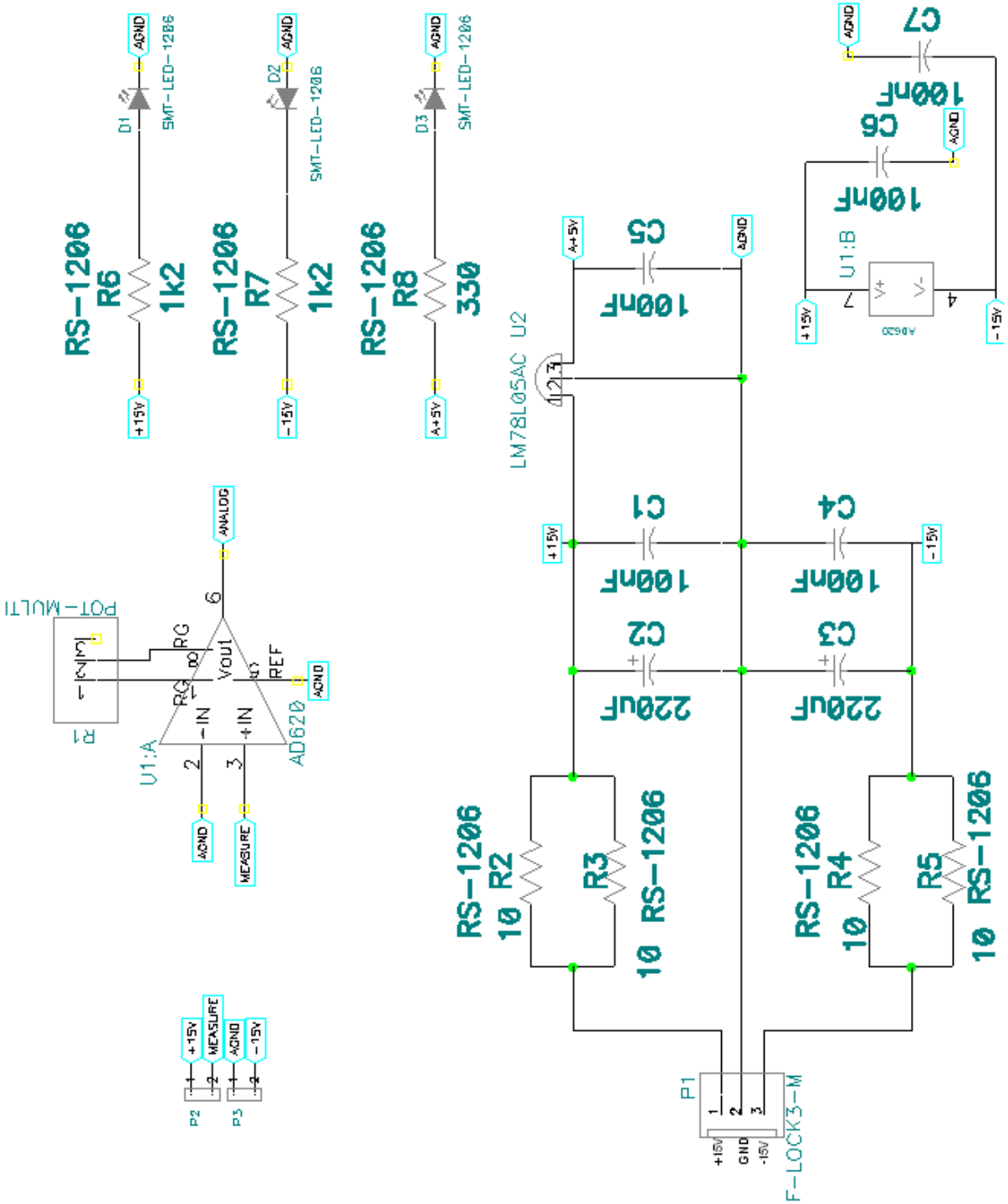
C.3. – Schematic of the isolated power supply

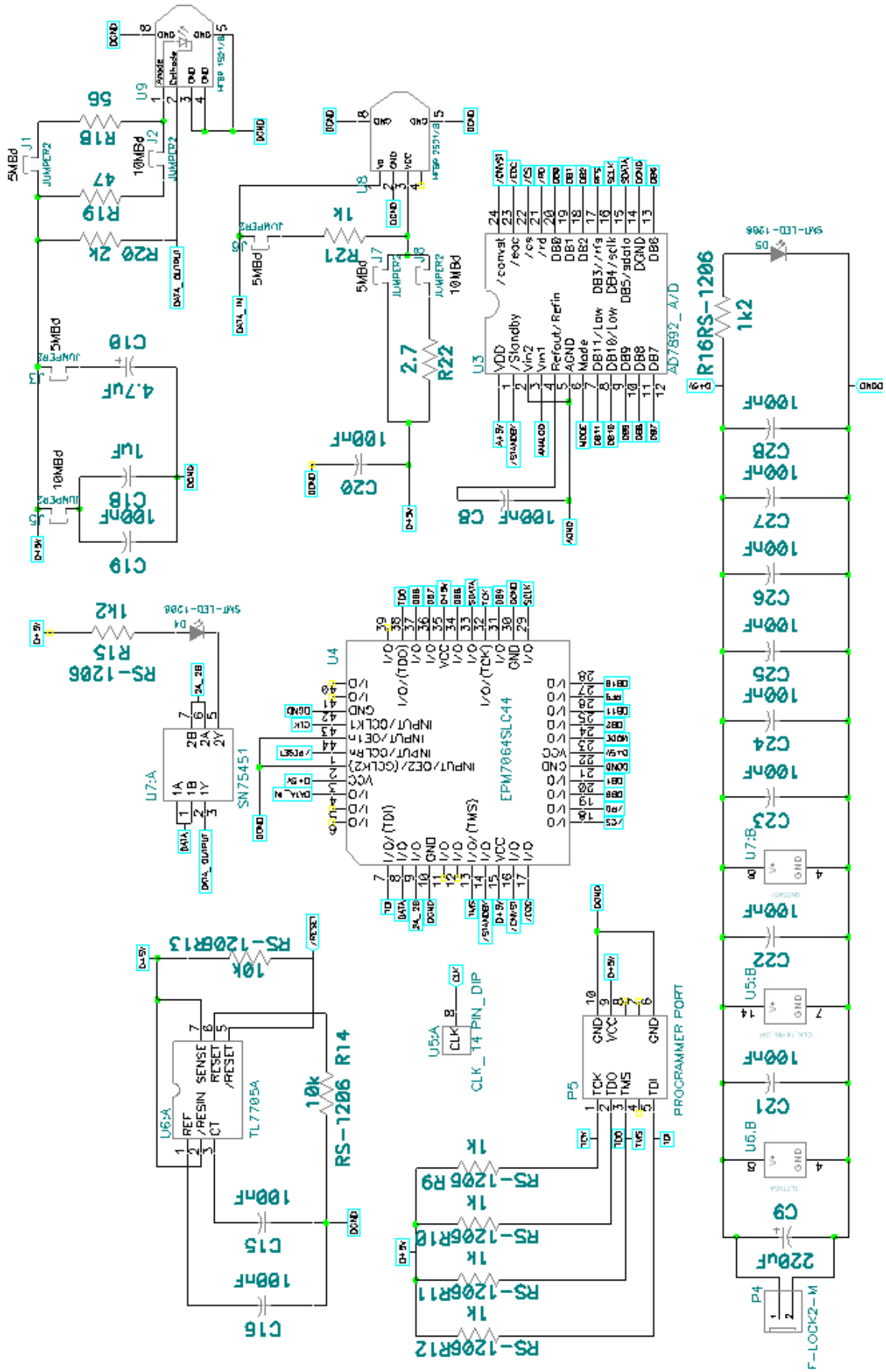


C.4. - Schematic of the switchgear interface board

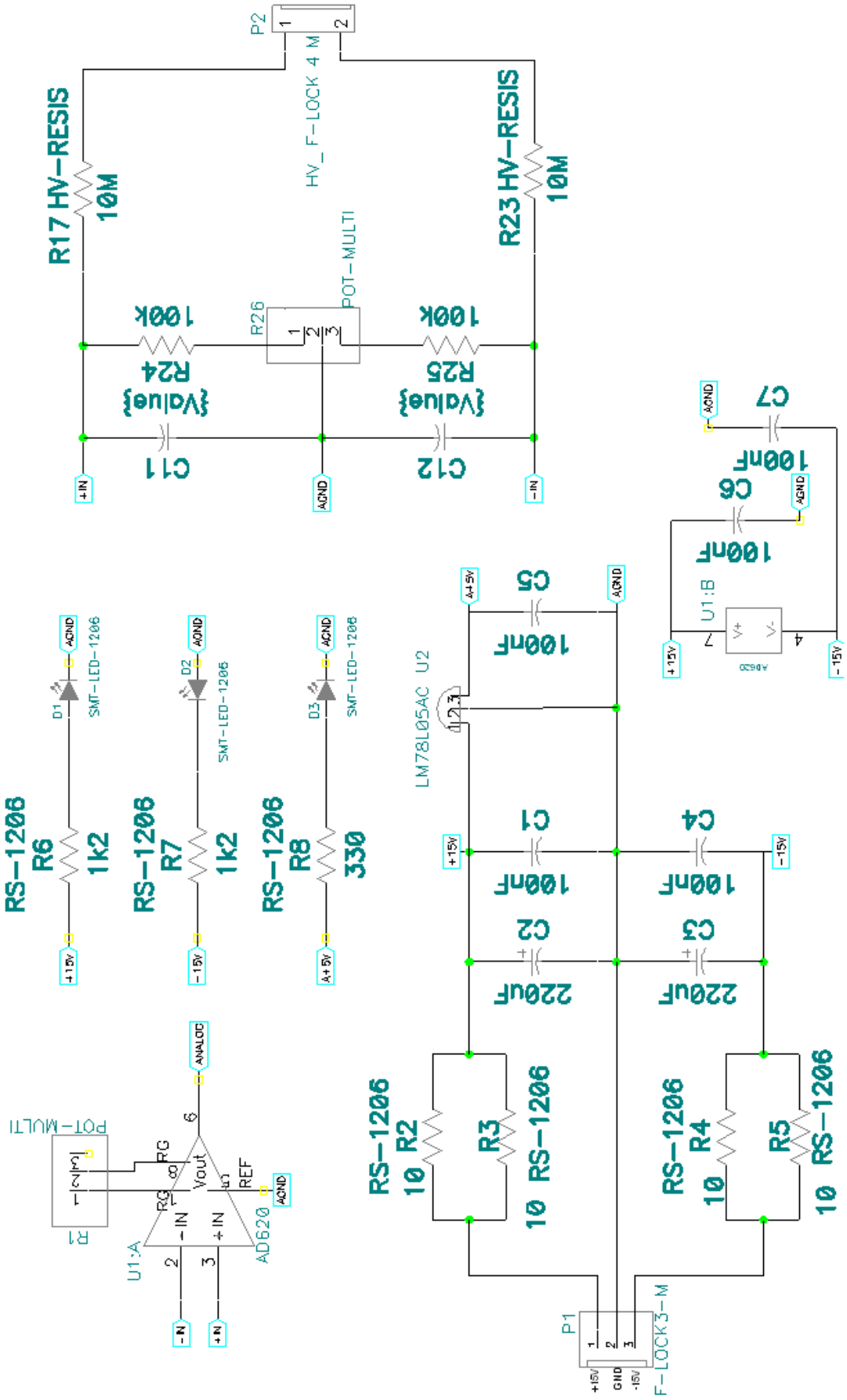


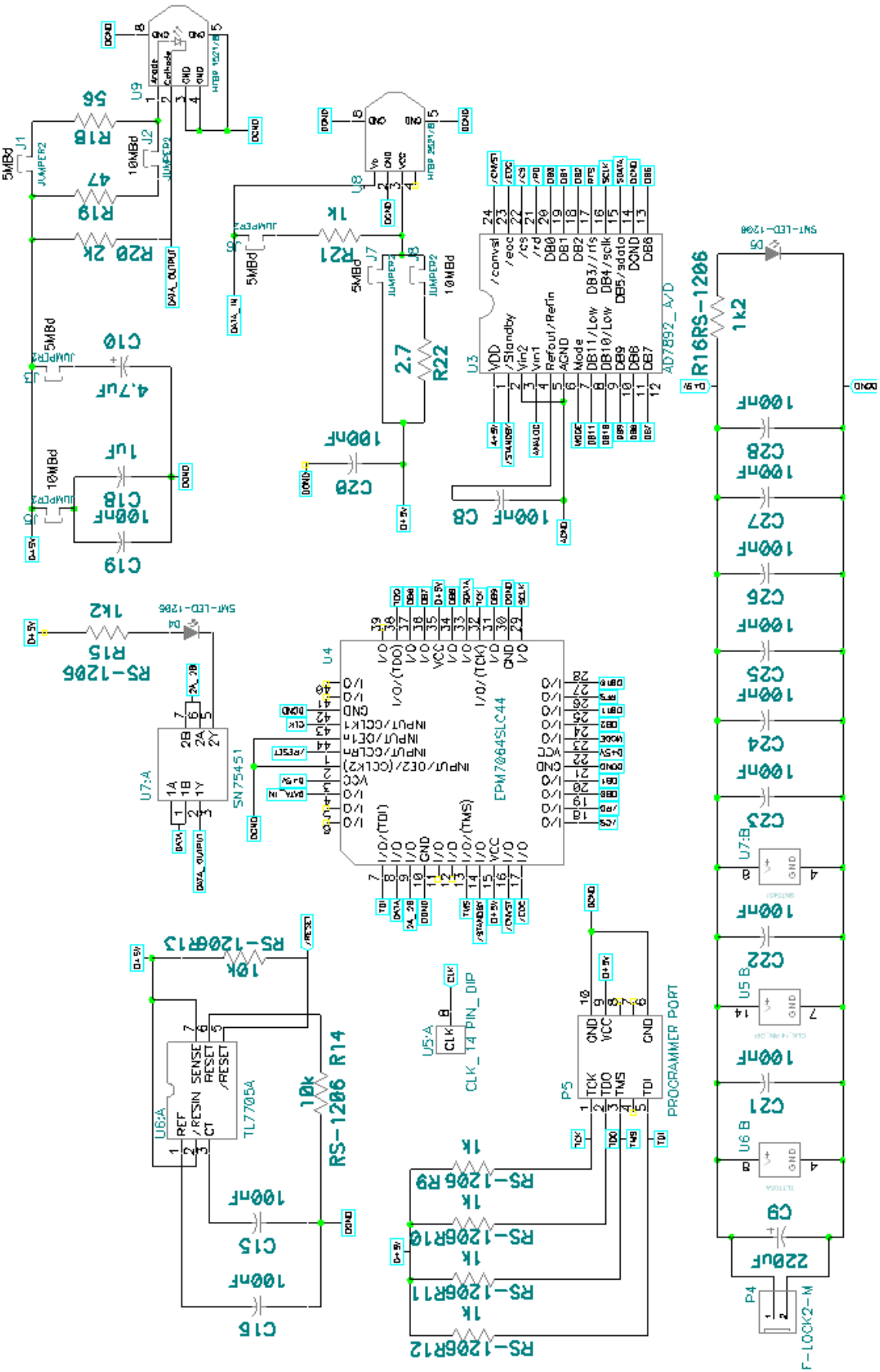
C.5. – Schematic of the AC-VMB



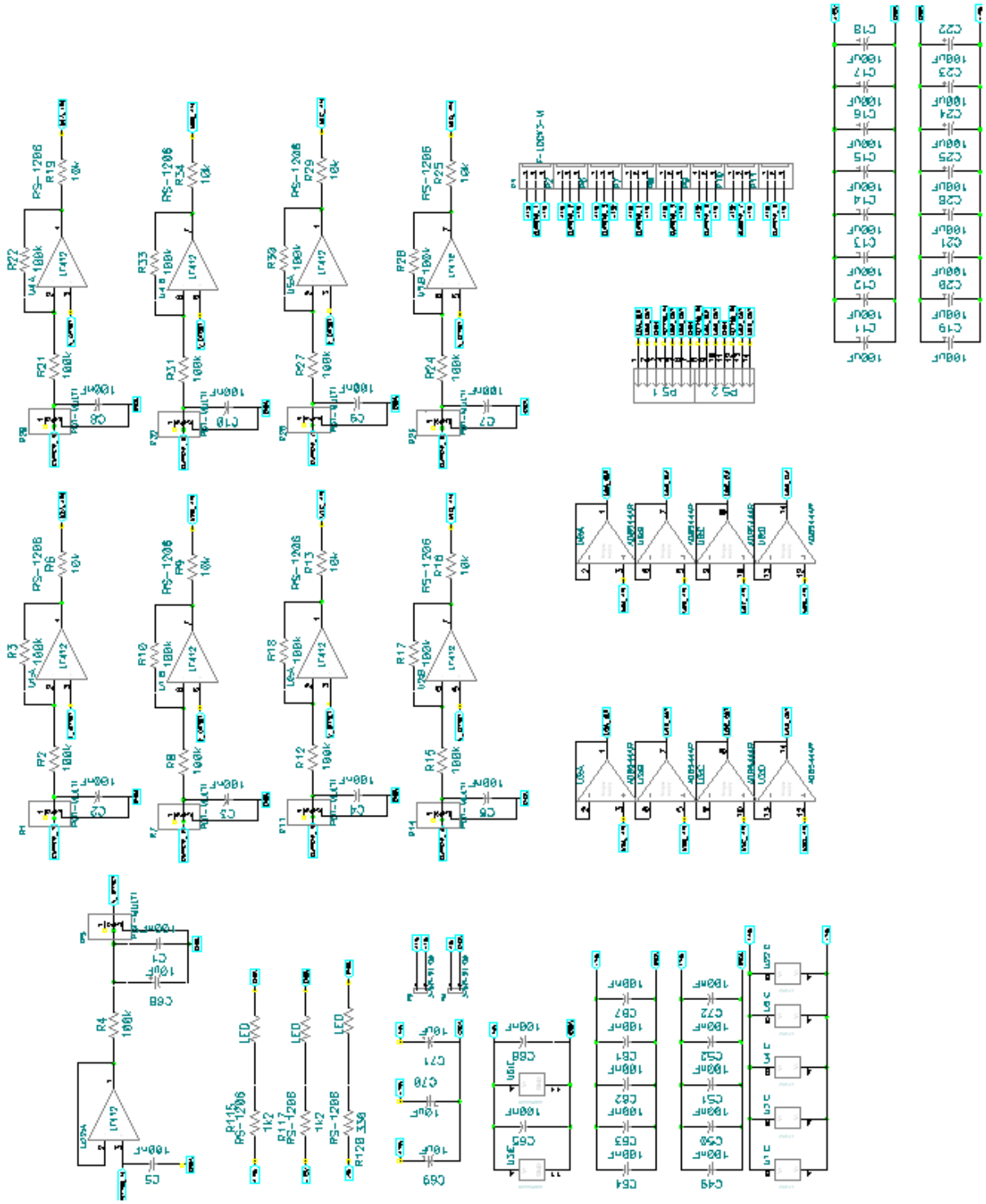


C.6. – Schematic of the DC-VMB





C.7. – Schematic of the IMB



Appendix D – Derivation of equation 3.15

Figure D.1 is a diagram for the derivation of equation (3.11).

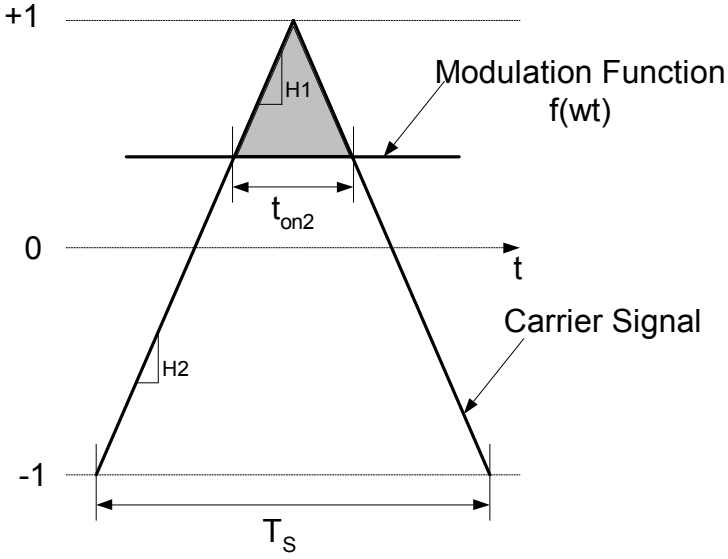


Figure D.1 – Diagram for derivation

For the time t_{on2} the bottom IGBT is conducting. The gradient H1 of the shaded triangle is the same as the gradient H2 for the large triangle.

$$H1 = H2$$
$$\frac{1-f(\omega t)}{t_{on2}} = \frac{2}{Ts} \tag{D.1}$$

The duty cycle for the bottom switch is defined as

$$d2 = \frac{t_{on2}}{Ts} = \frac{1-f(\omega t)}{2} \tag{D.2}$$

The top and bottom switches are complimentary pairs therefore the sum of the two duty cycles must be one.

$$d1 + d2 = 1 \tag{D.3}$$

Appendix D – Derivation of equation 3.15

From (D.2) and (D.3) the duty cycle for the top switch is calculated.

$$\begin{aligned} d1 &= 1 - d2 \\ &= 1 - \left(\frac{1 - f(\omega t)}{2} \right) \\ &= \frac{1}{2}\left(1 + f(\omega t)\right) \end{aligned} \tag{D.4}$$