A Bi-Directional, Direct Conversion Converter
for use in
Household Renewable Energy Systems

By

Adriaan Nicholaas Schutte

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Supervisor: Mr. P-J Randewijk

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DECLARATION

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Summary

A bi-directional, direct conversion switch-mode converter is proposed for use in distributed household renewable energy systems. The converter is intended as the central interface between the household energy system's low voltage Direct Current bus and the high voltage Alternating Current bus. The low voltage DC bus is connected to renewable generation and storage devices, while the high voltage AC bus is connected to the user's equipment and the mains grid.

The converter overcomes the inherent reverse-duty cycle problem associated with bi-directional converters by using a combination step-up / step-down half-bridge converter on the high voltage side of a high frequency transformer. The low voltage side of the transformer is driven by a full bridge inverter that acts as a rectifier during reverse mode.

In order to control the flow of power in both directions the converter implements Average Current Mode Control. A method is developed to determine the transfer functions of common switch-mode converters by inspection alone. This method is applied to the proposed converter, and both current and voltage mode control loops are designed with the frequency response method. The control system is implemented using a Digital Signal Processor.

A method of simultaneously simulating both the converter hardware and software is developed using VHDL. This method greatly reduced the development effort of the converter. The operation of the proposed converter is verified through this method of simulation.

A prototype converter is constructed and successfully tested, thereby proving the viability of the proposed converter topology and control methodology.

Opsomming

A bi-direksionele, direkte-omskakelking skakelmodus omsetter word voorgestel vir gebruik in huishoudelike hernubare energie stelsels. Daar word beoog dat die omsetter die sentrale koppelvlak sal vorm tussen die laagspanning gelykstroom bus en die hoogspanning wisselstroom bus van ‘n huishoudelike energie stelsel. Die laagspanning bus is verbind aan die hernubare energie opwekking en stoor toestelle, terwyl die hoogspanning wisselstroom bus aan die gebruiker se toestelle en die net kragtoevoer verbind is.

Die omsetter bevat ‘n gekombineerde opkapper / afkapper halfbrug omsetter aan die hoogspanning kant van ‘n hoe-frekwensie transformator. Hierdie halfbrug omsetter oorkom die omgekeerde-dienssiklus probleem wat ondervind word in bi-direksionele omsetters. Die lagspanning kant van die transformator word gedryf deur ‘n volbrug omsetter, wat ook as gelykrigter dien tydens die omgekeerde drywingsvloei modus.

Die beheer van drywingsvloei in beide rigtings noodsaak die gebruik van stroomwyse beheer. Die omsetter gebruik die Gemiddelde Stroomwyse Beheer metode. ‘n Metode is ontwikkel om die oordragsfunksies van algemene omsetters deur inspeksie te verkry. Hierdie metode is toegepas op die voorgestelde omsetter, en beide stroom en spannings beheerlusse is ontwerp deur middel van die frekwensie respons metode. Die beheerstelsel van die omsetter is met behulp van ‘n Digitale Seinverwerker ge-implementeer.

‘n Metode is ontwikkel waarmee die omsetter se hardeware en sagteware gelyktydig gesimuleer kan word. Hierdie metode het die werkslas tydens die ontwikkeling van die omsetter aansienlik verlaag. Die simulasie metode is verder gebruik om die korrekte werking van die omsetter te toon.

‘n Prototipe omsetter is gebou en suksesvol getoets. Daardeur is die lewensvatbaarheid van die omsetter en die beheer metodologie bewys.

Acknowledgements

I extend my deepest gratitude towards:

My wife, for her unwavering encouragement and support, specifically for her help with the mechanical construction of the converter prototype and support during the revision process.

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Above all, the Lord Almighty, who is in control of everything.

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Glossary of Acronyms and Abbreviations

A	Ampere
AC	Alternating Current
ADC	Analogue to Digital Converter
ACMC	Average Current Mode Control
BJT	Bipolar Junction Transistor
C	Capacitance, Coulomb
CAD	Computer Aided Design
CPU	Central Processing Unit
D	Duty Cycle
dB	Decibel
DC	Direct Current
DSP	Digital Signal Processor
ELV	Extra Low Voltage
F	Farad
H	Henry
HV	High Voltage (>100V in this report)
Hz	Hertz
I/O	Input / Output
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group
K	Kelvin
L	Inductance
LSB	Least Significant Bit
LTI	Linear Time-Invariant
LV	Low Voltage (<50V in this report)
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
P	Power
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PV	Photo Voltaic
PWM	Pulse-Width Modulation
R	Resistance
RAM	Random Access Memory
RMS	Root Mean Square
s	Second(s)
SELV	Safety Extra Low Voltage
SMT	Surface Mount Technology
THD	Total Harmonic Distortion
UPS	Uninterruptable Power Supply
V	Volt
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VSD	Variable Speed Drive
W	Watt
Z	Complex Impedance

1 Introduction

1.1 Background

Due to the increasing demand for electric power generation by means of clean renewable energy resources, several large-scale generation schemes utilising natural energy resources have been proposed and implemented. To date these schemes have mostly followed the traditional (fossil and nuclear fuelled) model consisting of large centralised generation facilities with widespread distribution networks.

It is opinion of the author that this centralized-generation, distributed consumption model is fundamentally flawed when applied to renewable energy resources. Globally, research and growing knowledge of renewable energy have shown that more efficient usage of renewable energy sources is possible with a distributed generation model. Currently usable forms of renewable energy are mostly distributed in nature, which suits a distributed generation and utilization model. Distributed generation is considered an important part of most countries' renewable energy development and implementation strategy.

The above statements are substantiated by the following media release by the European Commission. It quoted from a European Distributed Resources Project synopsis report (European Commission, 2004: 5):

> "The greatest potential market for DG (distributed generation) is displacing power supplied through the grid. On-site production minimises the transmission and distribution losses as well as the transmission and distribution costs, a significant part (above 30%) of the total electricity cost. As the demand for more and better quality electric power increases, DG can provide alternatives for reliable, cost-effective, premium power for homes and business. It can also offer customers continuity and reliability of supply, when a power outage occurs at home or in the neighbourhood, by restoring power in a short time."

Distributed generation does not only refer to household size generation but includes larger generation facilities situated close to communities or industries. This project will however focus on a power electronic converter for a household renewable energy system, since this application holds the greatest potential gain from renewable energy usage. It is generally accepted within renewable energy circles that households in future will be expected to generate a significant portion of their own energy requirements as the efforts to stem global warming increase and fossil fuel resources becomes more expensive.

This chapter will show that a central component of a typical distributed household renewable energy system is a power electronic converter that accepts low voltage DC input (from batteries, photovoltaic panels and wind

generators) and converts this to a high voltage AC output, for interface to user equipment and the mains grid.

The development of this DC-AC converter is the topic of this thesis.

1.2 Project Objectives

1.2.1 Main Objective

The objective of this project is to develop a direct conversion, bi-directional, low voltage DC to high voltage AC converter, which will enable the implementation of household distributed renewable energy systems using currently available power generation devices. Direct conversion here means that an intermediate DC bus is not used. Most converters currently available use intermediate DC busses, as discussed in section 2.2. A converter without an intermediate DC bus may be more cost effective and potentially improve the efficiency of conversion.

1.2.2 Project Deliverables

Achieving the main project objective will consist of achieving several sub-objectives or deliverables. These deliverables can be used as measures of the progress and overall success of the project.

The following deliverables have been defined for this project:

1.2.2.1 Deliverable 1: Development of a Suitable Converter Topology

Develop a converter topology that accepts a low voltage DC input and produces high voltage output that can be both positive and negative with respect to the input. In addition, the output current of the converter may be positive and negative for both positive and negative voltage outputs (that is, it must support four-quadrant operation).

1.2.2.2 Deliverable 2: Development of Suitable Control Methodologies

Develop control methodologies and compensation means in order to perform both current and voltage mode control of the converter. Special emphasis is placed on the development of current mode control methodologies.

1.2.2.3 Deliverable 3: Combined Hardware and Software Simulation

Simultaneously simulate the power electronic, control components and software in a single simulation in order to verify the operation of the converter, as well as minimise faultfinding and debugging on the prototype system.

1.2.2.4 Deliverable 4: Design and Construct Prototype Converter Power Section

Design and prototype the power electronics sections of the converter using commercially available components.

1.2.2.5 Deliverable 5: Design and Construct Prototype Converter Control Section

Design and prototype a Digital Signal Processor (DSP) based controller including necessary drivers, sensors and power supplies.

1.2.2.6 Deliverable 6: Demonstrate 4 –Quadrant DC Operation of Converter

Demonstrate that the converter is capable of positive and negative DC power flows, with both positive and negative DC voltage outputs (that is, operate in all four quadrants).

1.2.2.7 Deliverable 7: Demonstrate AC Operation of Converter

Demonstrate that the converter is capable of producing an AC output at mains frequency with resistive and reactive loads.

1.3 Converter Function and Requirements

In order to establish the need for the proposed converter, as well as to extract requirements for the design of the converter, it is necessary to analyze the household renewable energy system of which the converter is the central component.

Section 1.3.1 discusses the individual components that typically constitute a household renewable energy system. The characteristics of each of the components discussed will both influence the design of the final system and the converter itself.

In Section 1.3.2, the individual components are synthesized into a representative household installation, where the central position of the proposed converter is clearly shown.

This section is based on the personal experience of the author who has for several years researched the design of cost competitive renewable energy systems.

1.3.1 Typical Household Renewable Energy Components

1.3.1.1 Energy Capture Devices

Although a multitude of alternative methods of harnessing renewable energy for household use have been proposed, to date only Photovoltaic (PV) Panels and wind generators have become freely commercially available. Although these devices have relatively low conversion efficiencies, especially PV panels, they are widely available and are extensively used in installations that require energy independency, e.g. remote farms and villages, telecommunications installations and ocean-going yachts.

Note that all PV panels, and most small wind generators, provide an unregulated Direct Current (DC) output, which is typically interfaced with a storage device via linear or switch-mode power electronic converters.

1.3.1.2 Energy Storage Devices

Whenever energy is generated that cannot immediately be used, storage is required. This is particularly true in renewable energy systems, whose output is mostly dependent on fluctuating atmospheric conditions and often does not coincide with energy usage patterns. Electrical energy storage is therefore an indispensable part of almost all renewable energy systems.

Batteries have to date dominated the renewable energy storage market. Lead acid, calcium and gel batteries are all widely available, due in part to the widespread use of automotive batteries.

It should again be noted that almost all types of electrical storage devices, perhaps with the exception perhaps of flywheel and pumped storage systems, store energy directly as an accumulation of electrical charge (either on conductors, in dissolved ions, etc.). It is therefore reasonable to claim that most storage devices that are suitable for household use accept and provide electrical energy as a DC flow of electrons.

1.3.1.3 User Equipment

Electrical power is almost universally distributed to households by means of Alternating Current (AC) systems with a Root Mean Square (RMS) voltage of between 110 and 250 V, and a frequency of 50-60 Hz. A multitude of reasons for this situation exist, including:

- It is relatively easy to convert between AC voltages using transformers.
- A relatively high system voltage results in low currents for a given power requirement, thereby limiting transmission losses.

The average household therefore has numerous devices that require a regulated AC supply to operate satisfactorily. The overall cost of a renewable energy system would be greatly increased if users were to replace all equipment with devices that are capable of operating from DC alone.

It should be noted that many household items can be purchased in low voltage DC versions. These include all types of chargers, computers, lights and fridges / freezers. These devices are however considered specialized and are not as readily available as AC powered versions, and are typically more expensive.

1.3.1.4 Mains Grid Connection

Experience has shown that the peak household energy consumption may easily be 5 times the average weekly consumption. These peaks are due to the simultaneous use of high power devices like kettles, welders, heaters, ovens and stoves. If a renewable energy system were to be designed to supply this peak energy demand, the size of the system would be significantly increased,

only to cope with a demand situation that represents perhaps 5% of the system operational time.

The effect of peak maximum demand may be averaged to some extent by interconnecting a number of household renewable energy systems. This allows each individual system to be sized slightly above the household's average consumption (including daily morning and evening peaks). The individual systems must be interconnected to both each other or to a traditional mains grid. This allows each system to buy additional electricity from the grid when required, and sell electricity back into the grid when an excess is available.

1.3.1.5 Backup Energy Sources

If the mains grid supply is not reliable, as is the present case in South Africa, a means for generating electrical power during times of peak household demand and grid unavailability is required.

The most widely used form of backup generation is a petrol or diesel generator. These generators typically generate the same voltage and frequency as the mains supply, so that they can be directly connected to user equipment. For the purpose of this converter, the generator is taken as a mains connection without the option of sinking energy into it.

1.3.2 Typical Household Energy Installation

The individual components discussed in section 1.3.1 can now be synthesized into the system of Figure 1:

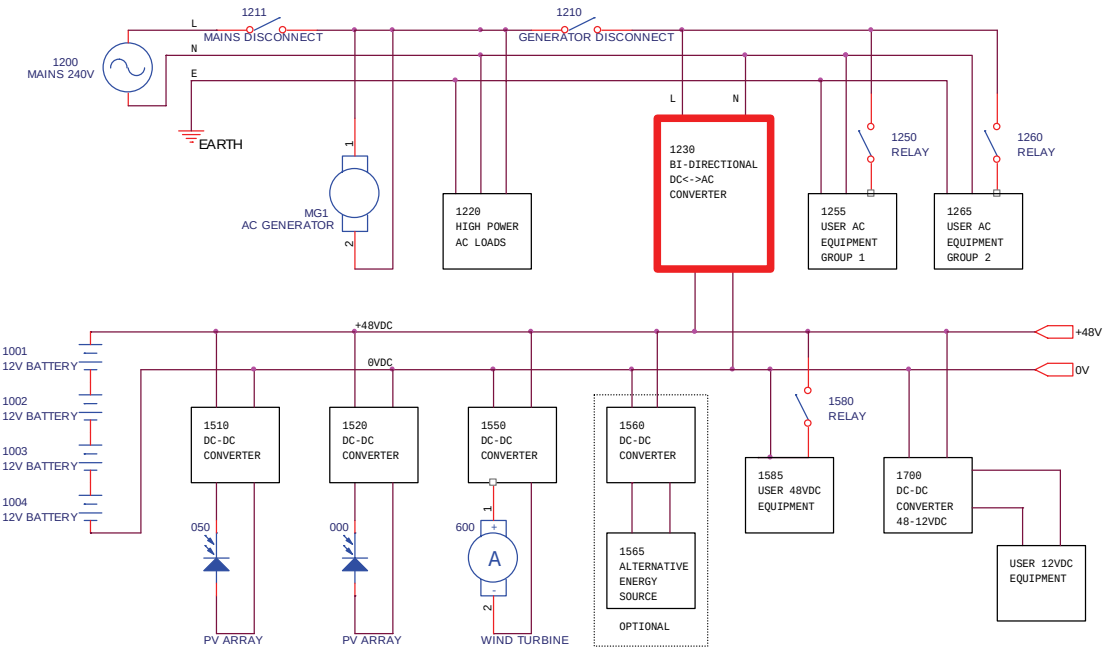

Figure 1: Typical Household Renewable Energy System

This is a representative system only, since each household's system has to be designed according to the local weather conditions, energy usage, grid availability and budget. It does however facilitate the discussion of the

interconnection of the individual components, thereby clearly showing the functional and performance requirements of the converters.

The following paragraphs discuss the design of the system in Figure 1 and how it influences the design of the proposed converter.

1.3.2.1 System DC Bus

Since the PV panels (000 and 050), wind generator (600), DC user loads (1585 and 1700) and storage batteries (1001 – 1004) all operate on DC voltages, they are connected to a common DC bus. It is desirable that the system contains as few DC buses as possible, since every DC-DC conversion increases the system cost and introduces losses.

Typical DC bus voltages may range from 12 V / 24 V for small households, motor homes and yachts, to 36 V and 48 V for larger installations. From a power transfer point of view, a high DC bus voltage is desirable, since this will result in significantly smaller DC current when the converter is supplying high-power AC loads. 48 VDC was selected for the present system since it is high enough to transfer a relatively large amount of power and it is the industry standard for telecommunications systems. Subsequently a large range of suitable semiconductors is available at relatively low prices.

The PV panels and wind generator are connected through DC-DC regulators, which will likely support maximum power point tracking. Any 48 VDC user loads are directly connected to the bus, and 12V or 24V user equipment can be connected through a DC-DC converter.

1.3.2.2 System AC Bus

The system shows a single-phase AC bus. Two contactors are provided to isolate the system in case of mains failure. The Mains Disconnect contactor (1211) enables the system to continue to provide the user's equipment with power during a mains failure, without attempting to provide power back into the grid.

The Generator Disconnect (1210) contactor is used to isolate the generator, as well as any high-power loads that cannot be powered from the batteries, from the remainder of the system. If the user wishes to run these high-powered loads, the generator must be run.

The Mains Disconnect and Generator Disconnect contactors are placed in series to allow the batteries to be charged from the generator during a mains failure.

It is a statutory requirement (according to SANS 10142 in South Africa and AS/NZS 3000 in Australia) for the mains grid, generator, converter and user equipment to share common earth and neutral conductors. Any discontinuity in either the earth or neutral conductors would render earth-leakage protection devices inoperable, and would be illegal in most countries.

The user's equipment is connected in groups to allow selective operation of low and high priority equipment.

1.3.3 Proposed Converter

The proposed converter, which is the topic of this thesis, is shown in heavy red lines in Figure 1. It can be seen that the proposed converter acts as a bridge between the high voltage AC and the low voltage DC buses of the system. It controls all power flow between the DC and AC busses. Since the output of the converter is an AC waveform, the converter must be able to produce both positive and negative outputs with respect to the battery polarity.

During normal system operation power typically flows from the DC bus to the AC bus so that at least some of the user's equipment energy usage is offset by the output from the PV panels and wind generators. When excess energy is available due to low user demand, the converter must be able to sink the excess energy into the mains grid. To ensure that transmission losses are kept to a minimum, the converter must be able to source and sink power from the mains grid at unity power factor.

When the mains grid or the generator is not connected, all AC bus power is supplied by the converter from the batteries and / or PV panels and wind generators. In this case, the batteries could be discharged to a deep level, so that it is desirable to recharge them when mains power is restored, or the generator is run. Although a separate charger may be used, the system may be simplified and the cost lowered by using a bi-directional converter, since the inverting and charging functions would then share at least some power and control components, as well as a housing and operator interface.

It is thus clear that the converter must be able to provide a bi-directional flow of power to and from the AC bus.

There is also a more subtle reason for requiring bi-directional power flow. Since the AC loads may be reactive, which is more often the case than not, the voltage and current supplied to the AC bus may not be in phase, and therefore could have opposite polarities. In this case, the instantaneous power transfer to the AC bus could oscillate between positive and negative at twice the mains frequency.

1.4 Converter Requirements

The requirements for the design of the proposed converter is taken directly from the preceding discussions of the suggested household renewable energy system (section 1.3.2), as well as the individual components of the system the converter is required to interface with (section 1.3.1). These discussions can be condensed into the following set of requirements:

- Requirement 1: The low-voltage side of the converter shall be connected to a DC bus with a nominal potential of 48VDC. The bus

voltage may vary between 36 VDC and 60VDC, depending on the charge state of the bus storage batteries.

- Requirement 2: The high-voltage side of the converter shall be connected to a single phase AC bus, and be capable of producing positive and negative voltages on the AC bus in a continuous range of -325 V to + 325 V, which corresponds to the peak values of a 230 Vrms waveform.
- Requirement 3: The converter shall be able to support both positive and negative current flow for both positive and negative output voltages.
- Requirement 4: The converter shall support both current and voltage output modes, depending on whether the mains or generator supply is available.
- Requirement 5: The converter shall contain an internal switch that will connect and disconnect the mains or generator supply and the output capacitor to the AC bus. When mains supply is available, the switch will connect the mains and disconnect the output capacitor, and the converter will function in current control mode. When the mains supply is not available, the mains will be disconnected and the capacitor connected, and the converter shall operate in voltage control mode.
- Requirement 6: In voltage control mode, the converter output voltage shall be capable of being modulated to produce a sinusoidal AC waveform of 230 VAC magnitude and a frequency of 50Hz (for use in South Africa and Australia).
- Requirement 7: During voltage control mode, user loads that can be reasonably expected at a household installation shall not distort the converter output waveform significantly.
- Requirement 8: In current control mode, the converter output current shall be capable of being modulated to produce a sinusoidal current waveform of selectable amplitude that is in-phase or 180 degrees out of phase with reference to the mains voltage.
- Requirement 9: In voltage control mode the converter shall be able to drive reactive loads without significant output waveform distortion.
- Requirement 10: The converter shall be capable of supplying or sourcing 2 kW of electrical power to / from the AC bus.
- Requirement 11: The converter shall be able to operate at full power in ambient temperatures of up to 40 degrees Celsius.
- Requirement 12: The high voltage and low voltage sides of the converter shall be galvanically isolated.
- Requirement 13: The converter, the mains grid and the user equipment shall share common neutral and earth conductors.

These requirements form the basis of the design of the proposed converter as described in the following chapters.

1.5 Document Structure and Chapter Summary

This document can broadly be divided into five sections, namely:

- Topology Development Section
- Hardware Design Section
- Software Design Section
- Results Section
- Appendices

1.5.1 Topology Development Section

Chapters 1 to 3 detail the intended function of the converter, what literature sources were consulted during the design of the converter, and the development of the actual topology.

Chapter 1 (Introduction) established the need for the converter and the requirements for its design. A typical household renewable energy system of which this converter will be the central component was considered. The individual components typically used in such systems was discussed. The system requirements were detailed and the project goals and deliverables were defined.

Chapter 2 (Literature Study) reviews the literature sources used during the development of the converter. These sources reviewed covers two areas within the field of power electronic, namely the design of bi-directional DC-DC converters with intermediate transformers, and current mode control in switch mode converters.

Chapter 3 (Proposed Converter Topology) develops the converter topology based on the requirements of Chapter 1 and the literature study of Chapter 2. The topology is developed by first considering simple uni-direction DC-DC converters. These will be synthesized into a bi-directional DC-DC converter. A transformer is included in the topology to enable the one side of the converter to operate at voltages typically encountered in mains grids.

1.5.2 Hardware Design Section

Chapters 4 to 6 detail the hardware design of the converter.

Chapter 4 (Hardware Design: Power Section) describes the design of the converter power section. It covers the selection of all components as well as the circuit and manufactured component design. The topology developed in Chapter 3, together with the practical considerations mentioned in that chapter are directly used as the basis for Chapter 4.

Chapter 5 (Hardware Design: Drivers and Sensors) describes the transistor gate drivers and the voltage and current sensors that form the interface between the power section and the control system. This chapter therefore

forms the link between the power design of Chapter 4 and the digital controller design of Chapter 6.

Chapter 6 (Hardware Design: Digital Controller and Power Supply) details the design of both the control power supply and the digital controller. A switch-mode converter is used to convert input power to five isolated supplies to feed the driver boards as well as the digital controller board. The digital controller board is designed around a Digital Signal Processor (DSP) that contains all necessary functions to implement the complete converter control system.

1.5.3 Software Design Section

Chapters 7 to 9 describe the design of the control methodology, compensation equations, digital controller software, as well as the converter simulation.

Chapter 7 (Converter Control Methodology and Compensation Equations) details the calculation of the compensation equations that are used by the DSP to control the current and voltage feedback loops of the converter. A method is also detailed by which the transfer functions of switch mode converters can be obtained through inspection.

Chapter 8 (DSP Configuration and Software) describes the design of the Digital Signal Processor software. The software discussion covers both the control code that implements the control methodologies developed in Chapter 7, as well as DSP hardware configuration code. The design of the software was an iterative process, since the software design both drove the simulation of Chapter 9, but was influenced by the problems identified through the simulation.

Chapter 9 (Converter Simulation) presents a method for simultaneously simulating both the converter hardware and software. Chapter 9 details this method as well as the results of the converter simulation. The simulation identified several problems with the original converter design and allowed these problems to be corrected before the prototype was constructed. The final simulation results proved the operation of the proposed converter topology.

1.5.4 Results Section

Chapter 10 (Physical Implementation) briefly describes the construction of the converter prototype and provides images of the final product.

Chapter 11 (Measurements and Results) reports the results of measurements made with the prototype converter. Measurements are shown that verify the correct operation of the various sub-systems of the converter. The converter is operated in DC output mode and the resulting measurements verified the operation of the converter in all four quadrants. A ringing effect was observed during these tests, which significantly affected on the operation of the converter. The DC efficiency of the converter in the forward mode was also determined. The results of measurements with the converter operating in

closed-loop AC mode are also reported. These results confirm that the converter is capably of feeding AC loads of any power factor.

Chapter 12 (Conclusions and Recommendations) evaluates the success of the project by considering the achievement of the deliverables defined in Chapter 1. For each deliverable, the degree of success, the successful and unsuccessful design elements and the recommendations for future work is given.

1.5.5 Appendices

Two appendices to this thesis are provided, namely Appendix A and Appendix B.

Appendix A contains all tables, schematics and PCB layouts referred to in the main text.

Appendix B contains all computer code that was generated for the project. Code generated includes Matlab, VHDL and C programs.

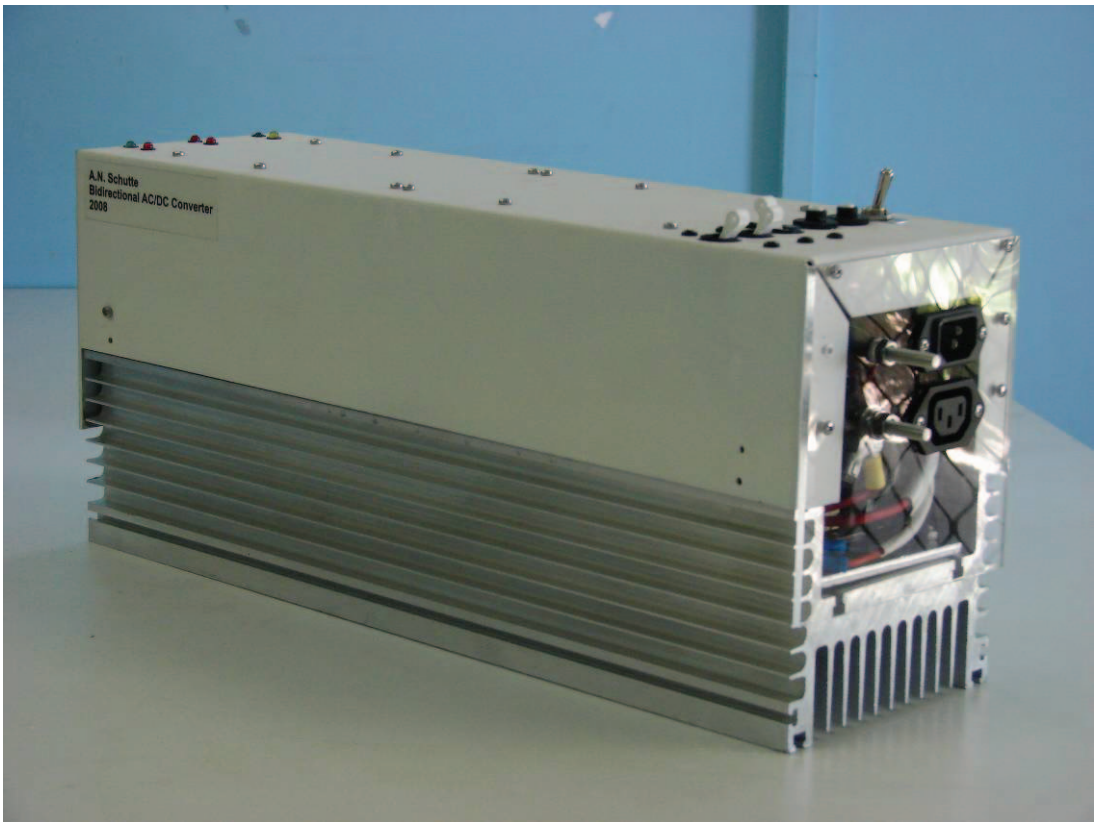

Figure 2: Prototype Bidirectional Bipolar Converter

2 Literature Study

2.1 Chapter Introduction

Within the field of Power Electronics, there are two areas that are of particular interest for the development of the proposed bi-directional, direct conversion, DC-AC converter. These two areas are namely that of bi-directional converter design, as well as that of current mode control methodologies.

Within the area of bi-directional converter design, there is a definite boundary between DC-DC and DC-AC converters. Almost all commercially available bi-directional low voltage DC to high voltage AC converters consists of a DC-DC converter with a transformer, followed by a DC-AC inverter. As such, the original literature review for this thesis found no applicable references that describe a direct conversion DC-AC converter. An overview will therefore be given of the bi-directional DC-DC converters with transformers that formed the basis of the proposed converter design.

All of the converters discussed in this section require some form of current more control. Current mode control of switch-mode converters is viewed as an advanced method for controlling converters that cannot be satisfactorily controlled by voltage mode control. Although several methods of current mode control are described in literature, Average Current Mode Control (ACMC) has recently become popular. It will be shown that ACMC is suited for use with the proposed converter topology.

Chapter 3 develops the topology of the proposed converter from basic step-up and step-down converters. The operation of the proposed converter is similar to that of the converters evaluated in this chapter. Since the operation of the proposed bi-directional converter is described in detail in Chapter 3, a detail description will not be repeated here for every converter discussed. Instead, the reader is invited to refer to Chapter 3 if the operation of the converters in this chapter is not entirely clear.

2.2 Overview of Bi-Directional DC-DC Converter Topologies

2.2.1 Usage of Bo-Directional DC-DC Converters

Consider again the main topic of this report, the bi-directional converter shown as part of the household renewable energy system of Figure 2. A requirement was defined in Chapter 1 that the converter shall directly convert between the low voltage DC and high voltage AC sides in a single step. This requirement attempts to reduce the converter cost and increase the efficiency by not using an intermediate high-voltage DC bus. If the requirement for direct conversion is omitted, the converter of Figure 2 is in fact a relatively common device, often referred to as an Uninterruptible Power Supply (UPS).

Figure 3 shows a typical arrangement for an on-line UPS.

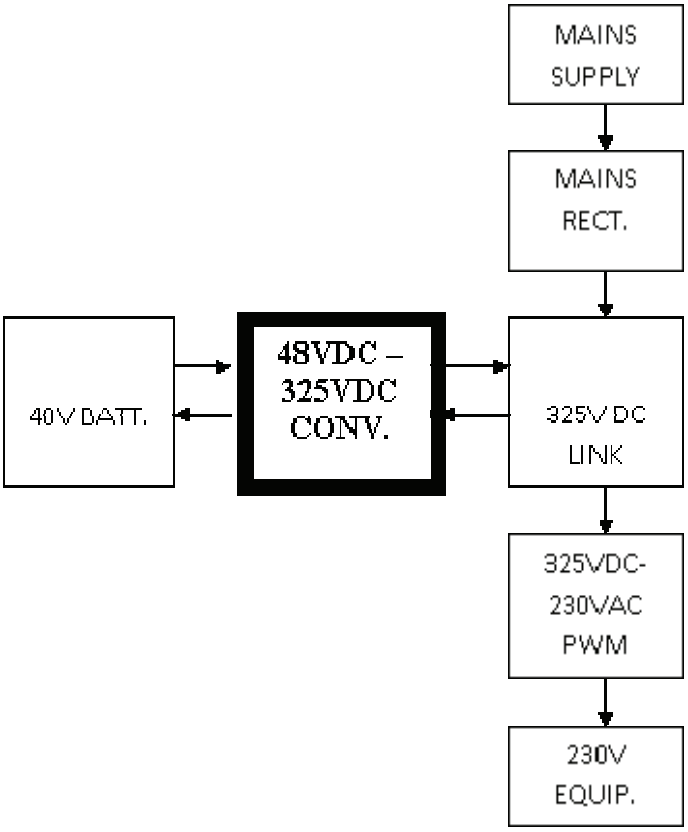

Figure 3: Typical On-Line UPS Layout

In this system arrangement, a DC link capacitor is used on the high-voltage side of the DC-DC converter. It is fed from the mains supply through a bridge rectifier, and supplies user loads via a DC-AC PWM controlled bridge inverter. Note that in addition to not supporting direct conversion, this system layout requires two DC-AC inverters if energy is to be supplied back into the mains grid.

The interface between the low and high voltage buses (that is between the DC link capacitor and the batteries) in Figure 3 is now a bi-directional DC-DC converter. Although some lower cost UPS systems use separate charging and discharging circuits, many systems use a bi-directional converter similar to that of the proposed converter.

The following two converters represent typical topologies for this bi-directional DC-DC converter, and are closely related to the proposed converter of this thesis.

2.2.2 Current Source DC-DC Converter

The original reference for this project is the converter of Figure 4 proposed by (Jain et al, 2000: 595). It is referred to as a current source converter due to the inductor at its battery side.

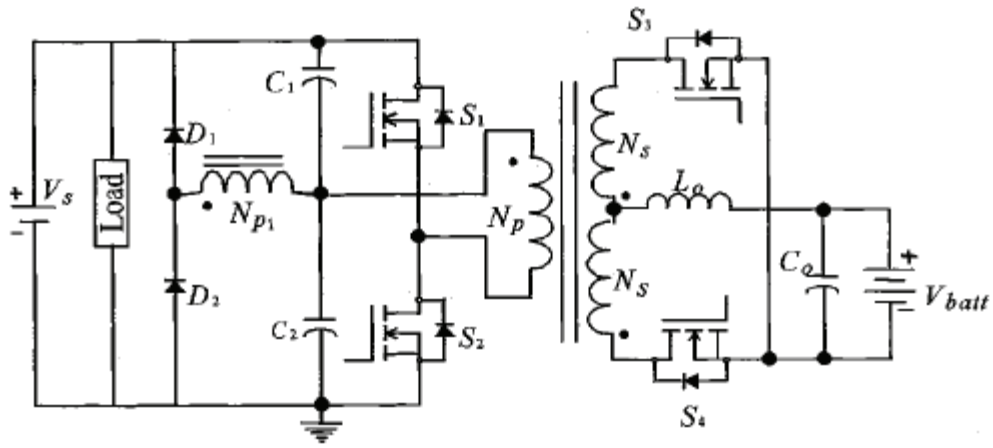

Figure 4: Current Source DC-DC Bi-Directional Converter

Capacitors C1 and C2 are used on the high voltage side of the transformer to provide a midpoint reference at $0.5V_s$. During the forward mode (battery charging), switches S1 and S2 operate as a half-bridge converter driving the primary winding of the transformer with a square voltage waveform. It is customary to include a resistor across each of C1 and C2, in order to ensure that the midpoint reference does not drift. These resistors typically dissipate a relatively large amount of power and reduce the converter efficiency. In the topology of Figure 4, these resistors are replaced with an auxiliary primary winding that has the same amount of turns and is in phase with the main primary winding. Together with diodes D1 and D2, this auxiliary winding maintains the midpoint reference.

2.2.2.1 Forward Operation

Figure 5 shows the forward operation of the current source DC-DC converter (Jain et al, 2000: 596).

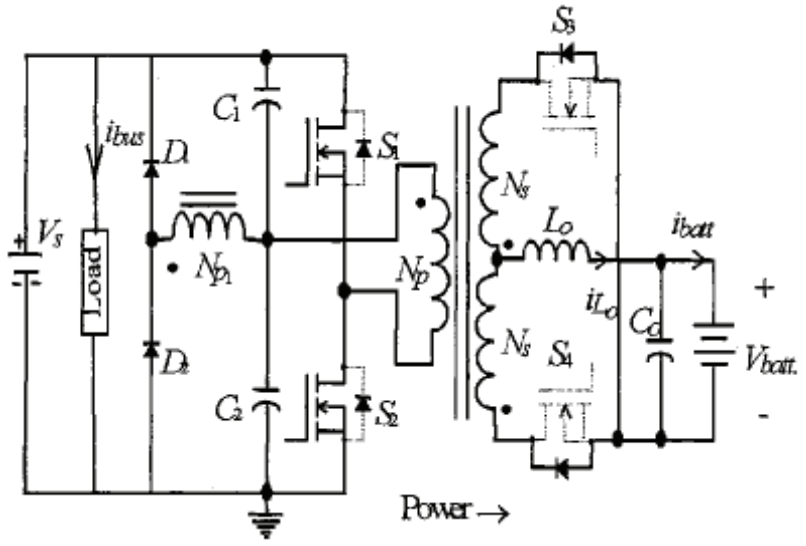

Figure 5: Current Source Converter: Forward Operation

During the forward mode, the body diodes of S3 and S4 act as a half-bridge rectifier, and the switches S3 and S4 are not actively switched. When voltage is applied to the primary winding, one of the secondary windings will alternately induce a voltage at its switch (S3 or S4) that is negative with regards to the battery negative terminal. Since the body diode of that switch will be forward biased, it will conduct and current will build up in the inductor.

When voltage is not applied to the primary winding, the inductor current will drive the centre tap of the secondary winding negative, and both the body diodes of S3 and S4 will conduct. Since the current flow will be in opposite directions in the two windings, their magnetic fields will cancel and no power will be coupled to the high voltage side. In this case, the centre tap of the transformer, and thus the inductor, in effectively shorted to the negative battery terminal and the inductor current is sustained through both body diodes. This effect is discussed in more detail in Chapter 3.

The inductor and output capacitor act as the usual LC filter found in a basic step-down converter.

Note that the operation of the present converter is identical to that of a step-down converter, with the exception of the inclusion of the transformer. It may also be noted that the forward mode can be easily controlled with a voltage-mode controller.

2.2.2.2 Current Source Converter Reverse Operation

Figure 6 shows the reverse operation of the current source DC-DC converter (Jain et al, 2000: 596).

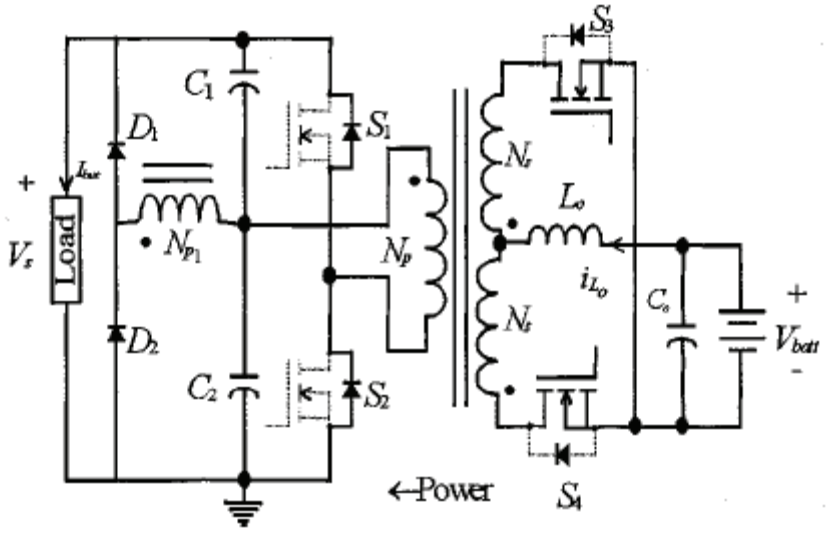

Figure 6: Current Source Converter: Reverse Operation

For the reverse mode, the body diodes of switches S1 and S2 on the high-voltage side act as a half-bridge rectifier. The auxiliary primary winding again ensures that the midpoint reference does not drift during operation.

In order to reverse the direction of power flow, switches S3 and S4 are switched in simultaneously. As with the forward mode, the currents in the two secondary windings then flow in opposite directions, so that their magnetic fields cancel and no power is coupled to the primary side. The effect of this is that the transformer side of the inductor is effectively shorted to the battery negative terminal, so that the current inductor current increases in the reverse direction. When S3 or S4 is now alternately switched off, the inductor current is forced through one of the secondary windings, and the power is coupled to the primary winding, where it is rectified.

Note that the operation of the converter in the reverse mode is identical to that of a basic-step converter, with the addition of the transformer. The inductor is placed in series with the battery, so that a higher voltage is applied to the secondary windings than what was possible during the forward mode.

The reason for the inclusion of this step-up converter in the topology is the non-unity duty cycle problem in bi-directional converters. This problem is discussed in Chapter 3 during the development of the proposed topology.

This converter requires current mode control during the reverse mode, as discussed in the section 2.2.2.3.

2.2.2.3 Evaluation of Current Source DC-DC Converter

The author designed and constructed a converter based upon this topology for his final year engineering project (Schutte, 2002). Although the topology does provide a means for bi-directional power flow between two DC levels, it does have several disadvantages.

The major disadvantage is that the inductor is on the low-voltage side, where the current is the highest. With power ratings in the order of 1-2 kW, the currents in the inductor become large, and therefore the inductor itself becomes uncomfortably large.

The large currents are also present in the secondary windings. When S3 or S4 switches off, the current through the concerned secondary winding has to be completely blocked by the switch. There is no freewheeling path for the winding current, and the switch transistor must do a hard turn-off. Since the secondary windings have inductance, the switch turn-off exhibit large voltage spikes that required the use of significant snubber circuits. It was found that the snubbers dissipate a relatively large amount of energy.

Furthermore, current mode control of the converter was required for the reverse mode. Voltage mode control cannot be used, since the output voltage does not necessarily increase with an increase in duty cycle. This can be seen by considering a 100% duty cycle, where both S3 and S4 is permanently on. The inductor current increases linearly, but the actual output voltage decreases since no power is transferred to the high voltage side. The inductor current will therefore increase unbounded until component failure occurs.

No current mode control integrated circuit is available for this topology, and the author developed a complex analogue current mode controller for this purpose. Its operation however did not prove reliable.

2.2.3 Dual Inductor Current Source DC-DC Converter

A similar but more advanced topology has been suggested by (Tolbert et al, 2002: 2). This topology was developed for use in the military generator / UPS combination of Figure 7:

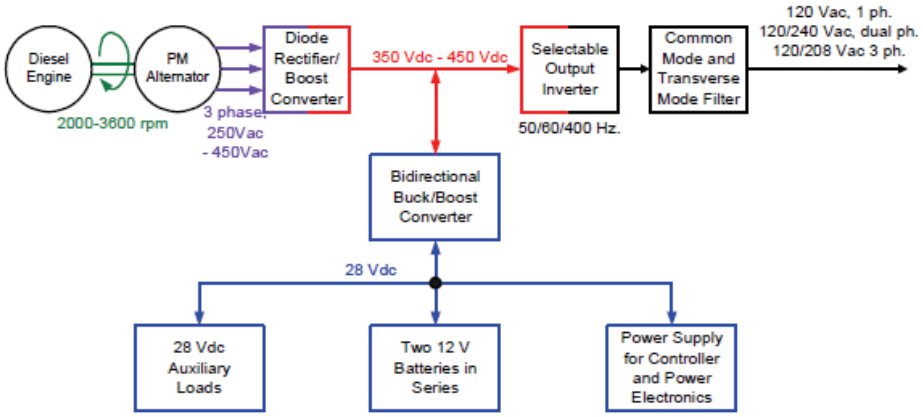

Figure 7: Combined Generator / UPS System

The batteries are used as a source of power when high power loads are connected to the output. During normal operation they are charged by the permanent magnet alternator through the bi-directional DC-DC converter. During backup operation the current flow is reversed and power is supplied to the DC link. The following discussion will focus on the DC-DC converter of this system.

The bi-directional DC-DC converter topology developed for this system attempts to solve some of the problems of the previous topology by using two inductors, as shown in Figure 8 (Tolbert et al, 2002: 3).

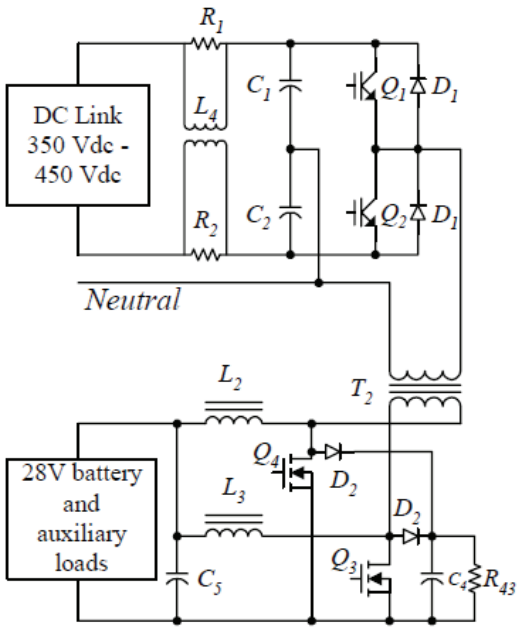

Figure 8: Dual Inductor DC-DC Converter

In addition to the two-inductor layout, the topology also uses a RL link damper (R1, R2 and L4) in order to prevent oscillations between C1 and C2, and the alternator converter capacitors. R43 and C4 are used as a snubber circuit.

The operation of this converter is similar to that of the current source converter of the previous section. The discussion of section 2.2.3.1 therefore focuses on the differences between the two topologies.

2.2.3.1 Operation of Dual Inductor DC-DC Converter

During the forward mode, the high-voltage side again acts as a half-bridge converter driving the transformer primary winding. The topology however uses two inductors on the low-voltage side, coupled to a single secondary winding. This arrangement acts as a current doubler rectifier, which is basically two step-down converters in parallel. When the secondary winding voltage is positive, the body diode Q3 conducts and current in L2 builds up. When the secondary winding voltage is negative, the body diode of Q4 conducts and current builds up in L3.

During the reverse mode, switches Q3 and Q4 is operated in exactly the same way as for the previous topology. Both are switched on simultaneously, and are then alternately switched off. When a switch turns off, the associated inductor current is forced through the secondary winding, and power is coupled to the primary side where it is rectified. Note that the switch that is switched on when the other is turned off has to carry the currents of both inductors.

2.2.3.2 Evaluation of Dual Inductor DC-DC Converter

The dual inductors of Figure 8 have the major advantage of not requiring large snubber circuits as with the current source converter. When Q3 or Q4 turns

off, the inductor current is forced through the secondary winding. Thus, it is not a hard turn-off where the current through an inductive component (winding) has to be stopped, as in the previous topology. This greatly increases the efficiency and simplifies the design.

A further advantage is that the large battery current is now evenly split between two inductors, so that the inductors can be significantly smaller than for the previous topology.

As with the current source topology, the reverse or boost operation of this converter also requires a specialized current mode controller. Forward operation can be by simple voltage mode control.

The dual inductors are also the major disadvantage of this topology. It adds significantly to the cost of the converter. The size of the low-voltage (high-current) switches is also significantly increased, since they have to carry the current of both inductors when power is fed to the secondary winding.

If the current in the two inductors are to be accurately controlled, it is necessary to include two current transducers, one for each inductor. In the paper under discussion, a single transducer was however used to measure the sum of the two-inductor currents. It was therefore assumed that the two-inductor currents are equal.

2.2.4 Bi-Directional DC-DC Converter Conclusion

The two bi-directional converter topologies discussed have several features in common.

In both these topologies, an inductor is used to step down (buck) the voltage in one direction, while stepping it up (boost) in the other. It will be shown in Chapter 3 that this is due to a fundamental requirement for bi-directional converters, where it is referred to as the non-unity duty cycle problem.

The non-unity duty cycle problem is the result of having to control the flow of power in two directions, between voltage levels that do not necessary change significantly through the reversal of power flow. For example, in both the above converters, the battery and DC link voltages remain essentially constant in both forward and reverse modes. The inductor is therefore used as a method to control the flow of power by being able to buck or boost the input and output voltages in order to determine the flow of current.

A further common element of both converters is the need for current mode control. During the reverse (boost) mode, the output voltage is not a linear function of the switch duty cycle. In fact, a detail analysis of the control of a boost converter was performed in an earlier draft version of this report. The analysis showed that the transfer function of a boost converter actually contains a term that subtracts the inductor current from the output with an increase in duty cycle. This leads to a Right-Hand Plane Zero, which is notoriously difficult to compensate, since it causes the output to initially “go

the wrong way" following a duty cycle change, and it is dependent on the inductor current magnitude.

The RHP requires the use of current mode control during the reverse mode of a bi-directional buck/boost DC-DC converter, since it is not possible to compensate for the RHP zero with only a voltage mode controller. The design of current mode controllers are therefore of great importance in the field of bi-directional converter design, and is reviewed in section 2.3.

2.3 Overview of Current Mode Control Methods

A voltage mode controller attempts to regulate the output voltage of a converter by varying the duty cycle of the switch or switches in the converter. As such, it has not information regarding the inductor current, and no control over the current.

In contrast, a current mode controller attempts to directly control the inductor current. As such, current mode controllers typically exhibit much faster transient response, and have an integral current limiting function. Therefore current mode controllers are often be used inside an outer voltage loop in order to improve the frequency response and limit the inductor current.

For the converters described in section 2.2, current mode control is mandatory due to the Right Hand Plane Zero evident in their transfer functions during boost mode operation.

Furthermore, if the converter output is a current, and not a voltage, current mode control is required. When the proposed converter is connected to the mains grid, its output is a current that is in phase with the mains voltage. In this case, the output reference is a sinusoidal current command, which the current controller has to accurately track.

The implementation of current mode control is therefore of importance in the design of the proposed converter. A search of available literature on current mode control shows that one manufacturer completely dominates the field of current mode controllers, both in terms of the number of controller IC's available, as well as by the amount of literature available from them.

The numerous Application Notes issued by Unitrode, now a subsidiary of Texas Instruments, on the implementation of current mode control by both analogue and digital means forms a complete reference for this field. Almost all of the work done in this report regarding current mode control is based on the Unitrode Application Notes.

In this section an overview of current mode control methods is given, with focus on Average Current Mode Control (ACMC). The ACMC method, with some modification, was chosen for the inner current- loop control of the proposed converter.

2.3.1 Current Mode Control Methods

Since the converter is operated in switch mode, the inductor current cannot be linearly controlled and it must be allowed to deviate around some command value. Several methods exist by which the inductor current may be controlled around this command value. This section discusses these methods, and evaluates them for use in the proposed converter.

Consider a simple step-up (boost) converter that is controlled by an outer voltage loop and an inner current loop. The block diagram for this system is shown in Figure 9. This figure is based on (Dixon, 1999: 3-43)

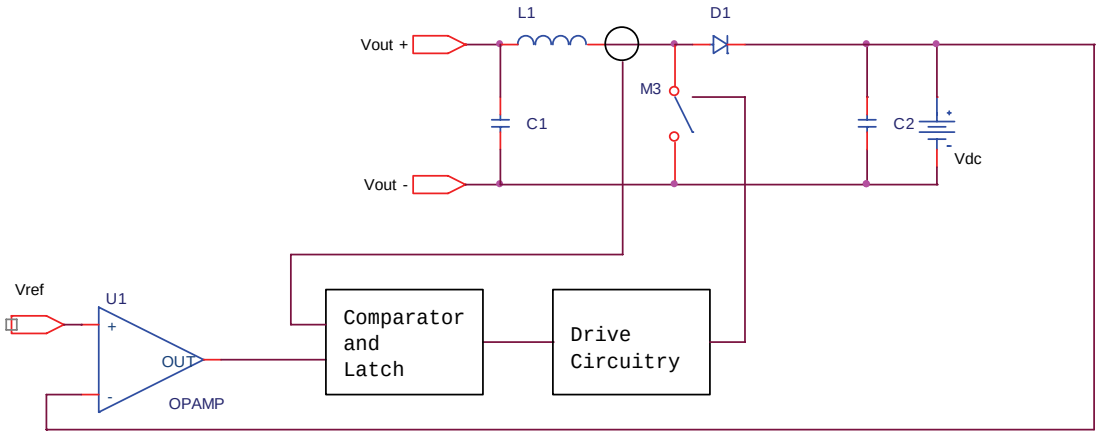

Figure 9: Basic Current Mode Control

The inner current loop comparator compares the inductor current directly with the current control command (which is either a reference current, or as shown the output of a voltage error amplifier). Since the inductor current generally increases linearly with time when the switches are on, and decreases when they are off, no comparison with an external saw-tooth voltage waveform is necessary.

Several methods exist by which the comparator and latch of Figure 9 can control the current. These include:

A. Tolerance Band Control: The inductor current is allowed to deviate around the commanded value by a fixed amount. When the inductor current is lower than the command value minus the lower band offset, the switch is turned on. Similarly, when the inductor current is larger than the command current plus the upper band offset, the switch is turned off. If the inductor current is significantly below the command value, the switch may be on permanently until the command value is reached.

B. Constant “off”-time Control: When the switch is turned on, the inductor current will increase. Once the inductor current reaches the command value, the switch turns on for a fixed period. After this off-period has elapsed, and switch turns on again until the inductor current reaches the command value.

C. Constant Frequency with Turn-On at Clock Time: The switch turns on at a fixed frequency and the inductor current increases linearly. When the command value is reached, the switch is turned off, and the inductor current decreases. If the inductor current is significantly below the command value, the switch may be on permanently until the command value is reached.

Methods A and B have a significant drawback that excludes them from further consideration, namely that their switching frequencies are not fixed. Their switching frequencies are primarily determined by the input and output voltages. This greatly complicates the design of frequency dependent components, like transformers, and excludes them from further consideration. These methods are normally only used at very low powers and for simple DC-DC converters.

The switching frequency of method C is fixed, which makes it the preferred method. It is also called peak current mode control, since the peak inductor current is used to turn off the switch.

Despite its popularity, according to (Dixon, 1999: 3-44) there are several drawbacks to the peak current mode control method, namely:

- **Instability at Duty Cycles > 0.5**: The control method is inherently unstable at duty cycles exceeding 0.5. This effect can be explained by means of Figure 10, which is taken from (Dixon, 1999: 3-44).

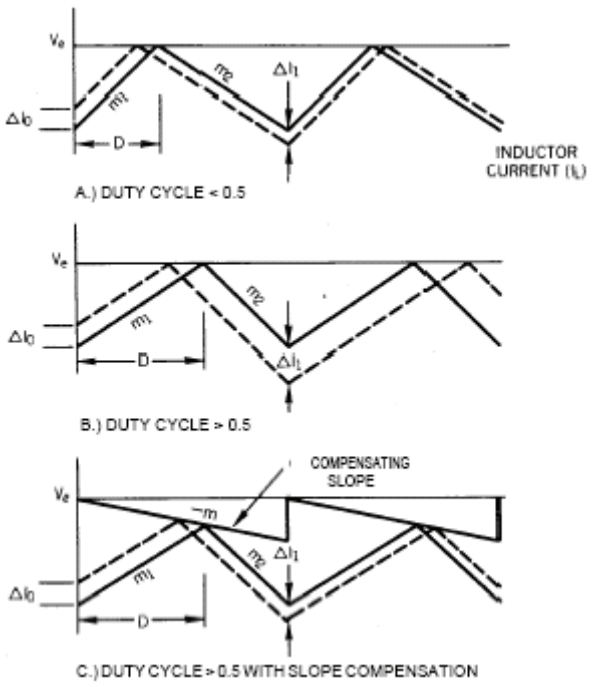

Figure 10: Slope Compensation

The solid lines indicate the inductor current of a converter operating in the steady state. The dashed lines represent the inductor current after a perturbation of ΔI_0 has occurred. The slopes of the dashed and solid lines are equal, since the inductor current can only change at fixed rates. The top graph (A) shows the inductor current for a duty cycle of < 0.5. Since the upward slope is larger than 45°, and the downward slope less than 45°, the turn-off time error and current error decreases with time.

The middle graph, Figure 10(B) shows the situation where D > 0.5. Since, the upward slope is now less than 45°, and the downward slope more than 45°, the turn-off time and current errors increase with time. This leads to instability and it must be compensated for.

By sloping the command value down during each switching period can rectify this instability. The effect of this technique, called slope compensation, is to ensure that the current error decreases over time, as shown in the bottom graph, Figure 10(C).

- **Poor Noise Immunity:** The up sloping inductor current is compared directly with the command value, and the switch turned off when they become equal. The ripple in the inductor current is usually small in comparison with the command value (usually about 5-10% of the nominal inductor current). Thus, even a slight spike in the measured current or the command value may turn the switches off prematurely. This makes the peak method very susceptible to switching and other electrical noise. In fact, the transient peaks caused by the switch-on of transistors in some cases cause the immediate turn-off of these transistors.

- **Sub-harmonic Oscillation:** The gain peaking of the inner current loop may cause the system to oscillate at half the switching frequency.

Many of these drawbacks may be overcome by averaging the inductor current, and comparing this with the command value. This is called Average Current Mode Control.

2.3.2 Average Current Mode Control

The Average Current Mode Control Method (ACMC) (Dixon, 1990: 3-357) overcomes the difficulties associated with peak current mode control by introducing a high-gain integrating current-error amplifier into the current loop.

A schematic of the ACMC technique, as applied to the step-up converter of Figure 9, is shown in Figure 11. This figure is based on (Dixon, 1990: 3-358).

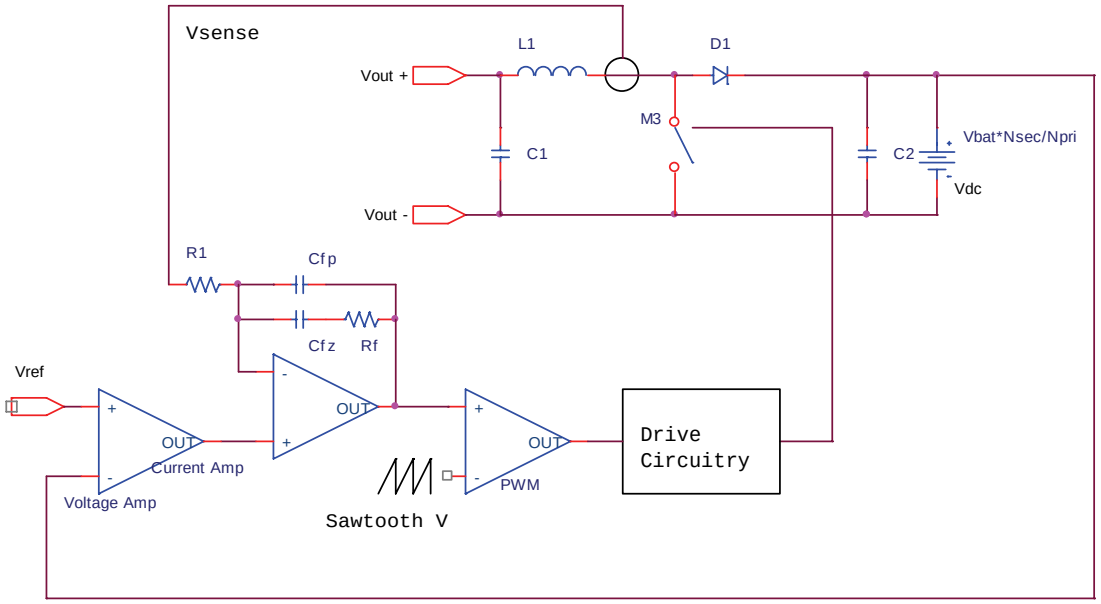

Figure 11: Average Current Mode Control

The technique requires the addition of two components, a high gain current amplifier (with feedback network), and a saw-tooth waveform generator. The desired average current level is applied to the non-inverting input of the current amplifier. The actual instantaneous inductor current value is measured by the current sensor, and translated into a voltage (V_{Sense}). The amplified and averaged difference between the desired and actual levels, i.e. the current error, is the output of the current amplifier. This is compared to the saw-tooth voltage. If the error is larger than the saw-tooth voltage, the switch is turned on, and vice versa.

The integrating feedback network of the current amplifier can be designed for optimum frequency response of the amplifier. The crossover frequency can be designed to be approximately the same as for peak current mode control, but the low frequency gain will be much higher. This high gain will assure accurate tracking of the current to the command value.

2.3.3 Current Mode Control Conclusion

The Average Current Mode Control method is in all instances superior to the other methods of current mode control discussed. The average current is directly compared with the command value, so that the current loop is therefore both fast and accurate.

This method has been selected for use with the proposed converter. Although the discussions used analogue circuitry as examples, the actual control system of the proposed converter is implemented using a Digital Signal Processor. This requires the ACMC method to be slightly modified, as discussed in detail in Chapter 7

2.4 Chapter Conclusion

This chapter gave an overview of converter topologies and control methodologies that are pertinent to the development of the proposed topology.

The converter topologies that were examined indicate the need for a method to control the current flow independent of the input and output voltages. In both cases, this was done by using an inductor as both a step-down and a step-up converter. This concept will be fully described in Chapter 3, when the proposed converter topology is developed.

All the converters that were examined also required some form of current mode control. The types of current mode control generally used was therefore investigated, with focus on the advantages and disadvantages of these methods. Only two methods are suitable for the present converter, namely peak current mode and average current mode control. It was shown that peak current mode control exhibits several disadvantages, and that average current mode control is the clear choice for the proposed converter. The development of the average current mode control methodology for the present converter is the subject of Chapter 7.

3 Proposed Converter Topology

3.1 Chapter Introduction

This chapter will develop the proposed DC-AC converter topology in order to fulfil the requirements established in Chapter 1.

The topologies discussed in the literature study of Chapter 2 have significantly influenced the development of the proposed topology, and the reader is invited to compare the final topology with those discussed in Chapter 2. The proposed topology will however be developed sequentially from basic step-up and step-down converters.

Initially, two simple uni-directional (step-down and step-up) DC-DC converters will be considered in order to facilitate discussion of the non-unity duty cycle problem encountered with reverse power flow in switch-mode converters. These uni-directional converters will then be combined into a bi-directional DC-DC converter, which will in turn be generalized to enable bi-polar outputs. Since the bipolar converter is able to operate in four quadrants, its operation is discussed in detail for later reference.

A transformer will then be included in the topology to enable the output side of the converter to operate at voltages typically encountered in mains grids. This is the final topology, and its operation will be discussed, after which two equivalent alternative topologies are given for reference. Hereafter the AC operation of the converter is discussed, including some additional features that is included in the topology to enable the converter to be directly used with the system of Figure 1 described in Chapter 1.

The chapter closes with several practical considerations regarding the implementation of the proposed topology.

It is assumed that the reader is familiar with the theory of operation of basic step-up and step-down converters.

3.2 Uni-directional Converters

Consider a simple uni-directional converter that provides a regulated output from battery (or other DC source). In order to provide a controllable output voltage and current from the battery, a step down converter is proposed:

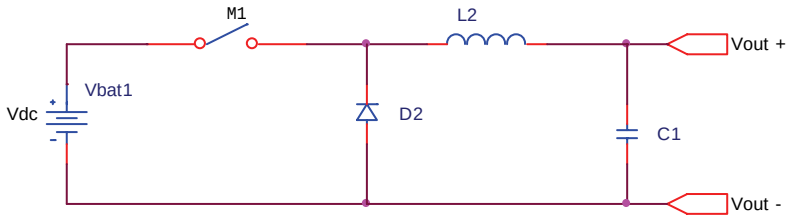

Figure 12: Step Down Uni-directional Converter

The step down converter of Figure 12 is able to provide a continuous output voltage and current from zero up to the battery rating. It contains a minimum number of components.

Typically, a step down switch mode converter is designed so that the desired output voltage is produced at a switch duty cycle of approximately 70-80%. This provides excess output capability, which is necessary for control during transient load changes. For direct output systems (i.e. without an intermediate transformer), this limits the nominal output voltage to 70-80% of the input voltage. In systems with a transformer, the turns-ratio of the transformer is typically decreased by the same percentage that the maximum duty cycle is reduced by, thereby raising the output voltage to the desired level at the reduced duty cycle.

This non-unity forward duty cycle prevents the basic step down converter from supporting reverse power flow.

3.3 Reverse Power Flow: The Non-Unity Duty Cycle Problem

Consider the system of Figure 12 when power flow is to be reversed (from the utilising device to the storage device). Initially, a step down or bridge converter with its terminals reversed with regards to the forward converter shown in Figure 12 may be considered. However, if the utilising equipment voltage remains unchanged, this will result in a reverse output (battery) voltage that is substantially lower than the original input voltage. If a duty cycle of 70% is assumed for both forward and reverse directions, the reverse output voltage will be approximately 50% (= 70% x 70%) lower than the original forward input voltage.

This is a major obstacle in the design of bi-directional DC-DC converters when the output voltage does not increase beyond the level of the input voltage. It is referred to as the non-unity duty cycle problem. The following methods of addressing this problem have been investigated:

- Including a tap-changing transformer in the design (in systems containing a transformer).
- Incorporating a boost converter variation in the topology.

The tap changing transformer option is conceptually simple and may be cost effective in some situations. A simple topology might consist of a transformer with two full-bridge converters on either side. The transformer will have at least two taps on one of its windings, with a relay or solid-state switching device to select between taps.

However, since the power flow in the present DC-AC converter can reverse at a rate of 100-120 Hz due to reactive loads, the tap changing topology is not considered further. The tap changing topology is best suited to bi-directional DC-DC converters where power flow reversal does not occur at a high rate.

The second option of electronically reversing the power flow by boosting the output voltage is therefore selected. Consider the step-up converter in Figure 13:

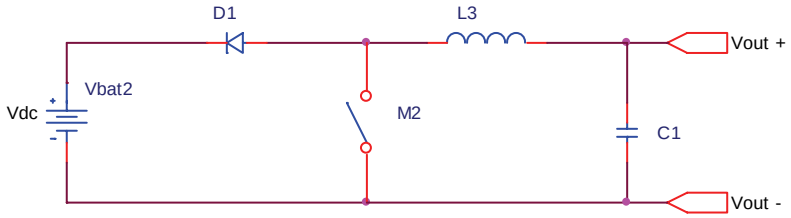

Figure 13: Boost Uni-directional Converter

This converter boosts the (lower) output voltage to the level of the (higher) battery voltage, which has the effect of reversing the current in the inductor and thereby reversing the flow of power, as required.

3.4 Uni-polar Bi-Directional Topology

Closer inspection of the topologies of Figure 12 and Figure 13 reveal that these topologies can be combined to form an elegant uni-polar, bi-directional DC-DC converter:

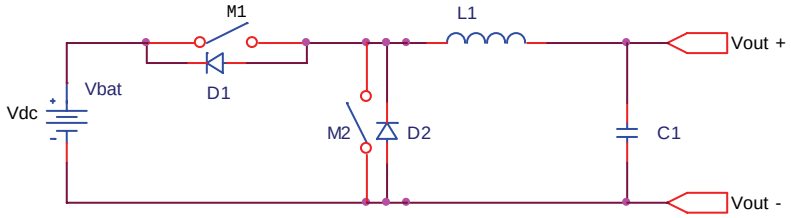

Figure 14: Proposed Uni-polar Bi-directional Topology

The converter of Figure 14 can be operated in two modes, forward (battery discharging) and reverse (battery charging). The forward or reverse mode is selected by either actively switching M1 or M2.

During the forward mode, switch M1 is operated at duty-cycle D < 1 and M2 is permanently off. While M1 is on, a forward current builds up in inductor L1. When M1 is turned off, the current is sustained in L1 via freewheeling diode D2. The converter therefore operates as a step-down converter and the output voltage in the forward mode is given by:

$$V_{out} = V_{bat} D_{M1} \qquad \textbf{(3-1)}$$

During the reverse mode, M2 is operated at duty-cycle D < 1 and M1 is permanently off. While M2 is on, a reverse current builds up in L1. When M2

is turned off, the current in L1 is sustained through freewheeling diode D1 into the battery. The converter therefore operates as a step-up converter and the output voltage in the reverse mode is given by equation 3-2 (Mohan et al, 1995: 173).

$$V_{bat} = V_{out} \frac{1}{1 - D_{M2}} \qquad \textbf{(3-2)}$$

This topology satisfies all requirements for a uni-polar bi-directional DC-DC converter whose output voltage and current can be electronically controlled, and the power flow direction rapidly reversed. However, as was mentioned in Chapter 2, this converter has a Right Hand Plane Zero in its transfer function during reverse mode, and requires current mode control.

3.5 Bi-polar Bi-directional Topology

The topology of Figure 14 can be further developed to enable bi-polar output. Firstly, Figure 14 can be redrawn as shown in Figure 15:

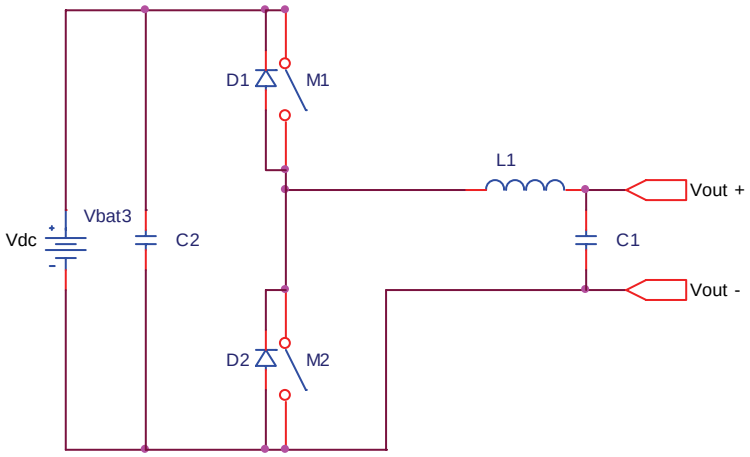

Figure 15: Redrawn Uni-polar Bi-Directional Converter

Where filter capacitor C2 has been added to the topology to shield the battery from ripple currents.

As can be seen in Figure 15, the left hand side of inductor L1 is switched alternately to the positive and negative sides of the battery. Recognition of this alternate switching of the inductor suggests that a bi-polar converter can be obtained by additionally switching Vout- to either the battery negative or positive side. This is shown in the topology of Figure 16:

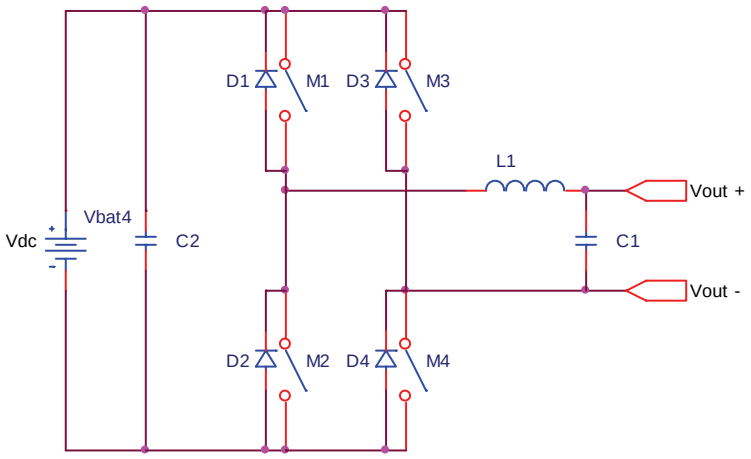

Figure 16: Proposed Bi-polar Bi-Directional Converter

The topology of Figure 16 resembles that of a bridge rectifier with a LC filter. However, the switching scheme of the switches M1 – M4 operates the converter in one of four modes, which correspond to the operation of the uni-directional converters previously discussed.

It may be noted that M3 and M4 are not switched together with M1 and M2 as pairs, as is usual with bridge converters. M3 and M4 determine the output polarity the converter, and in order to minimise switching losses, they are not switched at Fs (the switching frequency), and are only switched whenever a polarity change occurs.

Each of the four modes is discussed in the following sections, after which the general operation of the converter is discussed.

3.5.1 Mode 1: Positive Voltage, Forward Current

In Mode 1, the output voltage is of the same polarity as the battery, and current flows from the battery to the output (positive power flow).

Switch M4 is permanently on during this mode, and connects the negative output terminal to the negative battery terminal.

Switch M1 is operated at duty-cycle D < 1. While M1 is on, a forward current builds up in inductor L1. When M1 is turned off, the current is sustained in L1 via freewheeling diode D2. The output of the converter in the forward mode is given by:

$$V_{out} = V_{bat} D_{M1} \qquad \textbf{(3-3)}$$

The operation of the converter is identical to that of the uni-polar step-down converter.

3.5.2 Mode 2: Positive Voltage, Reverse Current

In Mode 2, the output voltage is the same polarity as the battery, and the current flows from the output to the battery (negative power flow).

Switch M4 is on permanently during this mode, and connects the negative output terminal to the negative battery terminal.

Switch M2 is operated at duty-cycle D < 1. While M2 is on, a reverse current builds up in L1. When M2 is turned off, the current in L1 is sustained through freewheeling diode D1 and into the battery. The output voltage of the converter in the reverse mode is given by:

$$V_{bat} = V_{out} \frac{1}{1 - D_{M2}} \qquad \textbf{(3-4)}$$

The operation of the converter is identical to that of the uni-polar boost converter.

3.5.3 Mode 3: Negative Voltage, Reverse Current

In Mode 3, the output voltage is reversed with reference to the battery and the current flows from the battery to the output (positive power flow).

Switch M3 is on permanently during this mode, and connects the negative output terminal to the positive battery terminal.

Switch M2 is operated at duty-cycle D < 1. While M2 is on, a reverse current builds up in L1, since V_{out+} is less negative than the negative battery voltage. When M2 is turned off, the current in L1 is sustained through freewheeling diode D1 and into the battery. The output voltage of the converter in the reverse mode is given by:

$$V_{out} = -V_{bat} D_{M2} \qquad \textbf{(3-5)}$$

The operation of the converter is identical to that of an inverted uni-polar step down converter.

3.5.4 Mode 4: Negative Voltage, Forward Current

In Mode 4, the output voltage is reversed with reference to the battery and the current flows from the output to the battery (negative power flow).

Switch M3 is permanently on during this mode, and connects the negative output terminal to the positive battery terminal.

Switch M1 is operated at duty-cycle D < 1. While M1 is on, a forward current builds up in inductor L1, since Vout+ is negative with regards to Vout-. When

M1 is turned off, the current is sustained in L1 via freewheeling diode D2. The output of the converter in the forward mode is given by:

$$V_{bat} = -V_{out} \frac{1}{1 - D_{M1}} \qquad \textbf{(3-6)}$$

The operation of the converter is identical to that of an inverted uni-polar boost converter.

3.5.5 General Operation of Bi-polar, Bi-directional Converter

The converter of Figure 16 is operated in one of the four modes discussed in sections 3.5.1 to 3.5.4. During the operation the converter's controller will switch M3 and M4 depending on whether a positive or negative output voltage is required. Switching M4 on will result in a positive output voltage, and M3 will result in a negative output voltage with respect to the battery. As an example, the selection of positive and negative output voltages can occur at twice the output frequency in order to generate a sinusoidal output voltage.

To further illustrate the operation of the bi-directional bi-polar converter, assume that the converter output is connected to a DC motor of an electric vehicle. Output polarity selection will then correspond to the driver of the vehicle selecting forward and reverse directions of travel.

Once a voltage polarity has been selected, the switching of M1 and M2 determines the direction of power flow to and from the motor. Switching of M1 and M2 occurs at Fs, the switching frequency, and the duty cycles of M1 and M2 determines the power flow magnitude.

Acceleration in the forward direction will correspond to switching M1 at a duty cycle 0<D<1, and acceleration in the negative direction will correspond to switching M2 a duty cycle 0<D<1.

Regeneration in the forward direction will correspond to switching M2, and regeneration in the reverse direction to switching of M1. Note that the functions of M1 and M2 are reversed during a reversal of polarity.

M3 should not be switched on while C1 is positive or M4 on while C1 is negative, as this will result in a shorting of the inductor and may lead to a large current build-up and resulting voltage spikes. The selection of M3 and M4 should therefore always correspond with the actual polarity of C1, and not the driver's intended direction of travel.

Furthermore, it is not possible to accelerate the motor in the negative direction from standstill if M3 is not selected, nor to accelerate in the positive direction from standstill if M4 is not selected. This is due to the fact that the boost converters require a voltage across the output in order to build up current in the inductor. Thus, in order to reverse direction, the DC motor first needs to be

brought to a standstill via regeneration, the direction changed via M3 and M4, and then accelerated in the reverse direction.

This effect manifests itself as a reduction of current loop gain during low output voltages. It causes voltage distortions near the zero current crossings in the AC output converters, as will be shown during simulation.

3.5.6 Alternative Methods of Operation

The converter of Figure 16 may also be operated by using M2 and M4 to select the output polarity. Thus, for the forward mode, M4 is switched on permanently, and M1 and M2 are used to determine the direction of power flow. For the reverse mode, M2 is switched on, and M3 and M4 are used to control the power flow.

This method of operation has the advantage that the low side transistors are switched on permanently, while the high side transistors are only switched at the switching frequency. Thus, a floating channel ("flying capacitor") transistor driver circuit may be used. This is in contrast with the first method, where M3 is required to be permanently on, which precludes the use of flying capacitor drivers, or necessitates that M3 must be switched at the switching frequency, which increases switching losses.

Since the inductor current is equal to the sum of the output capacitor and load currents, this method is completely equivalent to the first method, and may be used if the simplifications in driver circuits and power supplies are substantial.

3.6 Extended Range Bi-polar Bi-Directional Converter

It is a requirement for the final converter to have an output that is several times the voltage of its input. The converter of Figure 16 is therefore further developed by including a transformer, in order to extend the output range. This leads to the topology of Figure 17:

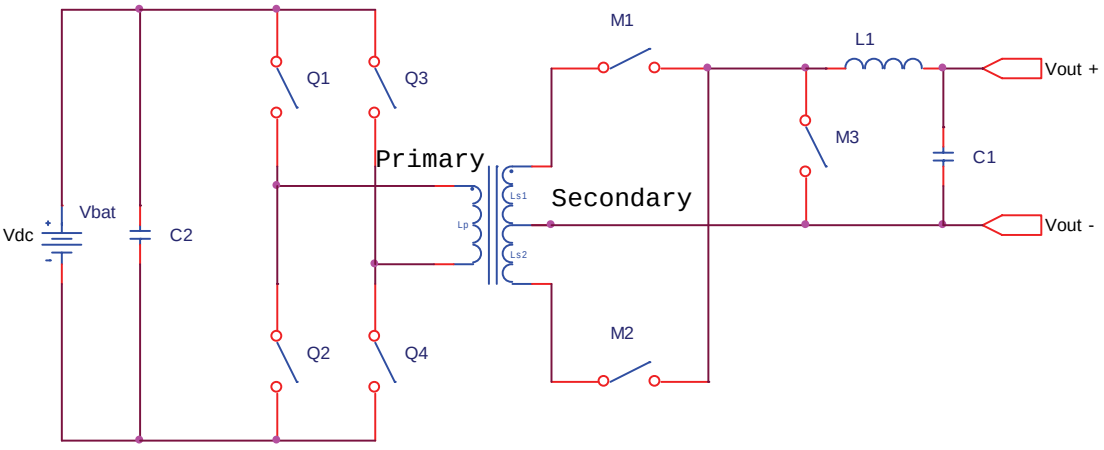

Figure 17: Extended Range Bi-polar Bi-directional Converter

This converter uses a bridge topology one the battery side to drive a high-frequency switching transformer. On the output side, switches M1, M2 and M3 perform the functions of synchronous rectification during the forward mode and that of a boost converter during reverse mode.

As with the previous converter, the operation of the converter of Figure 17 is best described by considering the modes the converter can operate in. Since the output polarity of the converter is only determined by the synchronisation of the switches, the positive and negative modes are discussed together.

3.6.1 Forward Mode

In this mode power flows from the battery to the output, with either positive or negative output polarity. Q1-Q4 and Q2-Q3 are treated as switch pairs that are turned on alternately at duty cycle D<0.5. The duty cycle of the two switch pairs determines the output voltage magnitude.

The output voltage polarity is determined by M1 and M2, which are synchronously switched with the pairs Q1-Q4 and Q2-Q3 respectively. If M1 is switched on together with Q1-Q4 and M2 with Q2-Q3, the output voltage will be positive. If M2 is switched with Q1-Q4 and M1 with Q2-Q3, the output voltage will be negative.

When Q1-Q4 are all off, Q3 is switched on in order to provide a freewheeling path for the inductor current. During this mode, the operation of the converter is identical to that of a step-down converter (Equation 3-1), with the addition of the factor to reflect the transformer voltage ratio:

$$V_{out} = \pm 2 D_{Qpair} V_{bat} \frac{N_{\sec}}{N_{pri}} \qquad \textbf{(3-7)}$$

The factor 2 in Equation 3-7 indicates that the overall duty cycle is twice that of each individual Q-pair.

3.6.2 Reverse Mode

In this mode power flows from the battery to the output, with either positive or negative output polarity. M1, M2 and M3 are actively switched and Q1-Q4 is switched synchronously for rectification. In order to reverse the power flow (and therefore the current), M3 is switched on, and reverse current will build up in the inductor as long as the output voltage is non-zero. If the output voltage is positive then a negative current will build, and for a negative output a positive current will build (in both cases a negative power flow).

Once the desired current level is reached, M3 switches off and either M1 or M2 is switched on. M1 and M2 are switched on for alternate cycles in order to ensure symmetrical magnetization of the transformer core. At the same time

M1 or M2 is switched off, either Q1-Q4 or Q2-Q3 is switched on for rectification.

The operation of the converter in this mode is identical to that of the step-up converter (Equation 3-2) with the addition of the transformer voltage ratio factor:

$$V_{bat} = \pm \frac{V_{out}}{1 - D_{M3}} \frac{N_{pri}}{N_{\sec}} \qquad \textbf{(3-8)}$$

Note that the factor of two that was included in Equation 3-7 is not present in Equation 3-8, since M3 is switched on at twice the frequency of M1 and M2.

3.6.3 Alternative Topologies

It may be argued that M3 in the topology of Figure 17 is not strictly required. Indeed, the following two topologies are equivalent in functionality to the proposed topology of Figure 17:

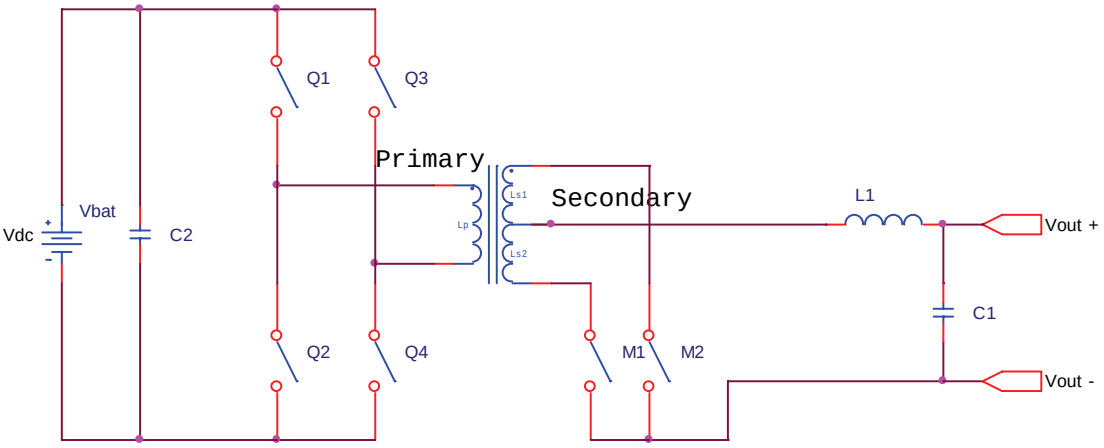

Figure 18: Alternative Topology 1

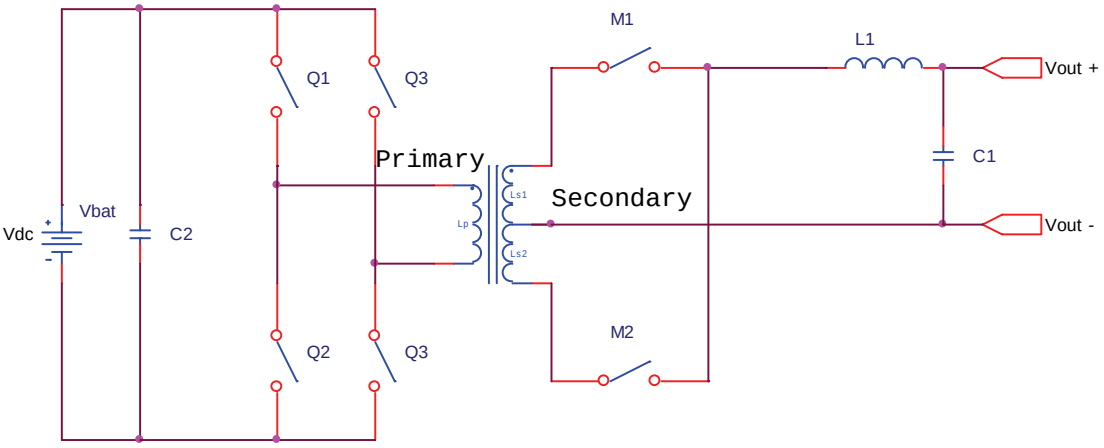

Figure 19: Alternative Topology 2

In both these alternative configurations, switch M3 is removed by switching on both M1 and M2 simultaneously. Since the currents in the two secondary windings are then in opposite directions, their magnetic fields cancel and the transformer is effectively shorted out of the circuit. When the inductor current reaches the desired level, either M1 or M2 is switched off, and the current is forced through one of the windings. These two topologies are similar in operation to Current Source Inverter described in section 2.2.2.

Although these topologies do eliminate M3, they have a significant drawback that excludes them from further consideration. When either M1 or M2 is switched off, the current through the associated winding (which has a relatively large inductance since it is on the high voltage side and therefore contains many turns) must decay to zero, while at the same time the voltage across the switch is twice that of the inductor. The energy that must therefore be dissipated during switch off is substantial, and must be absorbed by snubber circuits. The losses of these topologies are therefore substantially higher, and the elimination of M3 is offset by the addition of large snubber circuits.

In contrast, topology of Figure 17 uses M3 to build up inductor current. When M3 switches off, M1 or M2 switches on, so that the inductor current is forced through either M1 or M2, so that no snubbers are required. The switching losses of M3 are much less than that of the snubbers, and it is therefore the preferred topology.

One last alternative topology that has been considered is that of using full bridges on both sides of the transformer, as shown in Figure 20:

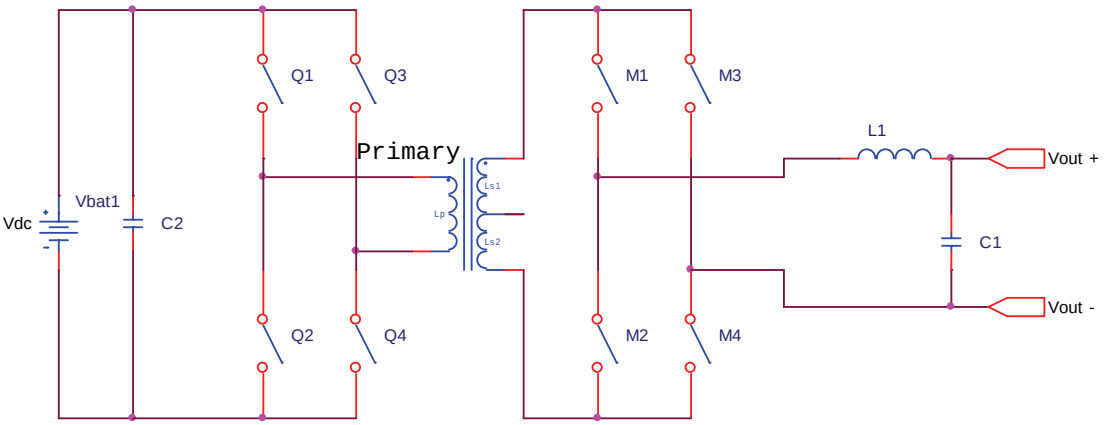

Figure 20: Alternative Topology 3

In the forward mode of this converter, M1-M4 / Q1-Q4 and M2-M3 / Q2-Q3 would be switched synchronously for a positive output voltage. The synchronisation of the two sides is reversed for a negative output. For the reverse mode, M2-M4 or M1-M3 are switched on alternatively in order to short the inductor and build up current. Once the current has reached the desired level, one of the transistors is switched off and the complementary

transistor in that leg is switched on, in order to direct the current through the transformer windings.

The major drawback of topology in Figure 20 is that the current on the high-voltage side of the converter flows through two switches at any instant. Since the switches have to be bi-directional, they must consist of back-to-back transistors. This implies that the current will flow through four semiconductor junctions, resulting in significant power dissipation within the converter. The power loss of the high voltage section in topology of Figure 20 is approximately twice that of the proposed topology.

The major advantage of this topology is that the switches need only be rated for the maximum voltage of $V_{BAT}*N_{PRI}/N_{SEC}$, compared to the switches of the proposed topology that are subjected to twice this voltage, due to the use of the centre-tapped transformer.

3.7 AC Converter Operation

In sections 3.5 and 3.6 it was shown that the proposed topology of Figure 17 is capable of producing bi-polar outputs, and enables power flow both to and from the batteries. The topology therefore enables four-quadrant operation of the converter.

In sections 3.5 and 3.6 the four modes of the converter have been considered separately. However, since the converter controls the output polarity and current direction by the switching of transistors, it is capable of rapidly changing both output polarity and current direction. This enables the implementation of the direct conversion DC-AC converter that is the topic of this thesis.

For an AC output, the converter will attempt to track a sinusoidal reference waveform that is equal in magnitude and frequency to the mains grid supply. Since the voltage and current waveforms supplied to the AC bus may not be in phase (due to reactive loads), the converter must be able to separate control output current direction independent of the output voltage. This task is significantly simplified if the converter uses an inner current control loop in addition to the outer voltage control loop.

A further reason for using an inner current loop is that this enables the converter to directly interface with the mains grid. Since the mains grid solely determines the AC bus voltage when connected, the outer voltage loop is then disabled and the inner current loop commanded to either source or sink a sinusoidal current. This current waveform should be at unity power factor that is either in phase for sourcing power, or 180 degrees out of phase for sinking power into the mains grid. The output capacitor must be removed from the circuit when connected to the mains grid, otherwise reactive power will be fed into the grid. This will defeat the goal of supplying power to the grid at unity power factor.

With the above considerations in mind, a relay is included in the proposed topology of Figure 17:

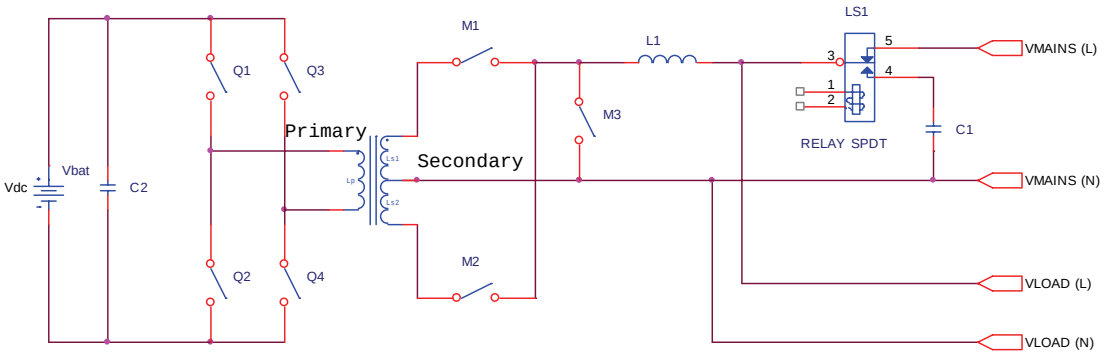

Figure 21: Bi-Directional AC Topology

The operation of the converter topology of Figure 21 is as follows: When power from the mains grid (or generator) is available, the relay is switched off and the inductor and user load is connected directly to the mains. The converter then generates a sinusoidal current in the inductor that is either in phase or 180 degrees out of phase with the mains voltage, depending on whether energy is to flow to or from the mains grid.

When the mains (or generator) supply is interrupted, the relay disconnects the converter and load from the mains, and connects a small filter capacitor in parallel with the load. The converter then generates a sinusoidal output voltage by commanding either positive or negative current flow, as required by the load.

3.8 Practical Considerations

3.8.1 Topology Refinements

Since it is necessary to control power flow in two directions through M1, M2 and M3, these switches must consist of two back-to-back transistors. Since the voltage drop across this serial combination might be substantial, the efficiency of the circuit can be increased considerably if these transistors are placed at the high voltage side of the transformer, where the current is low. This was implicitly done in the preceding topologies. Since these transistor have to withstand a voltage that is much higher than the maximum output voltage (due to the step-up converter design), IGBT's are the most suitable choice for these switches.

The current at the low voltage side is approximately 50A. The on-voltage of these transistors therefore has to be as small as possible. The most suitable choice for switches is two or three MOSFET's in parallel, since they act as resistors and can be easily placed in parallel, with the corresponding reduction in resistance and power dissipation.

During forward operation, it is not necessary to switch M1, M2 or M3 at the switching frequency, which helps reduce switching losses. If it is assumed that the switches will consist of back-to-back IGBT's with integral anti-parallel diodes, the IGBT's that have to conduct in its forward direction can be switched on permanently. The switch combination will then only conduct when the IGBT that is off is reversed biased so that its diode will conduct. Which IGBT in the pair is switched on will determine what the output polarity will be. It will be necessary that the corresponding IGBT in all three switch pairs be switched in simultaneously. For example, M1A, M2A, and M3A will have to be switched on for positive output, while M1B, M2B, and M3B will have to be switched on for a negative output (see detail schematic in Figure 22 of Chapter 4).

During reverse operation, it not necessary to switch Q1-Q4, and they can be left switched off. Their body diodes will act as a rectifier bridge and ensure that a positive voltage is always applied to the battery. It is not necessary to switch on M1A/B or M2A/B just as M3 switches off. M1A/B or M2A/B can be left switched on for the entire switching period, the diode of the second transistor in the series pair will prevent current flowing in the undesired direction.

Lastly, if the two back-to-back IGBT's are connected so that they share a common emitter connection (instead of a common collector), the design of the gate drive circuits can be greatly simplified. This is since a common ground point exists for the two transistors. In this case, two parallel low-side drivers, with a single power supply, may be used.

3.8.2 Safety Isolation

The national standards bodies of every country prescribe the minimum safety standards that an electrical installation should adhere to. In South Africa, the South African Bureau of Standards (SABS) has issued SANS 10142 as the primary standard governing electrical installations.

This standard proclaims that Extra Low Voltages (ELV) that do not pose a significant shock hazards to humans do not require any form of protection if certain criteria are adhered to. These criteria can be summarized as:

- The nominal voltage cannot exceed 50VAC or 120VDC.
- An approved source feeds the system.
- Basic insulation is provided between the ELV system and other systems.

A further distinction can be made between ELV systems that share the earth connection of another system, and those that are completely isolated. The latter being called Safety ELV or SELV.

The low-voltage side of the proposed converter can be regarded as an SELV system provided it is isolated from the high-voltage side of the converter. This

classification of SELV will significantly reduce the cost of the converter and associated battery installations, and is therefore desirable.

One of the approved types of sources that may feed an SELV system is an isolation transformer. In the proposed topology, the main transformer acts as an isolation transformer that galvanically isolates the high and low voltage power sections.

The only other connections between the high and low voltage sections are:

- The control power supplies.
- The digital I/O (gate drive circuits).
- The analogue I/O (voltage and current measurements).

The isolation of these connections is discussed in Chapters 6 and 8.

3.9 Chapter Conclusion

This chapter developed the proposed converter topology in stages. From an initial discussion of basic step-up and step-down converters, a topology was developed that satisfies all requirements that were captured in Chapter 1.

The final topology as shown in Figure 21 is capable of four quadrant operation, as well as rapidly changing voltage and current polarities. This enables the generation of AC outputs at mains frequencies.

With the addition of the output relay, it is capable of acting as both an AC voltage source to user loads, as well as an AC current source to the mains grid. The latter enables the converter to source energy from the mains grid, as well as sink energy into the mains grid at unity (or any other) power factor.

The topology of Figure 21, together with the practical considerations discussed in this chapter, form the basis of the following chapter, which details the design of the power components of the proposed converter.

4 Hardware Design: Power Section

4.1 Chapter Introduction

This chapter details the design of the power section of the converter as proposed in Figure 21 of Chapter 3.

The schematic of Figure 22 shows all power and measurement components of the proposed converter, but not the gate drive circuits.

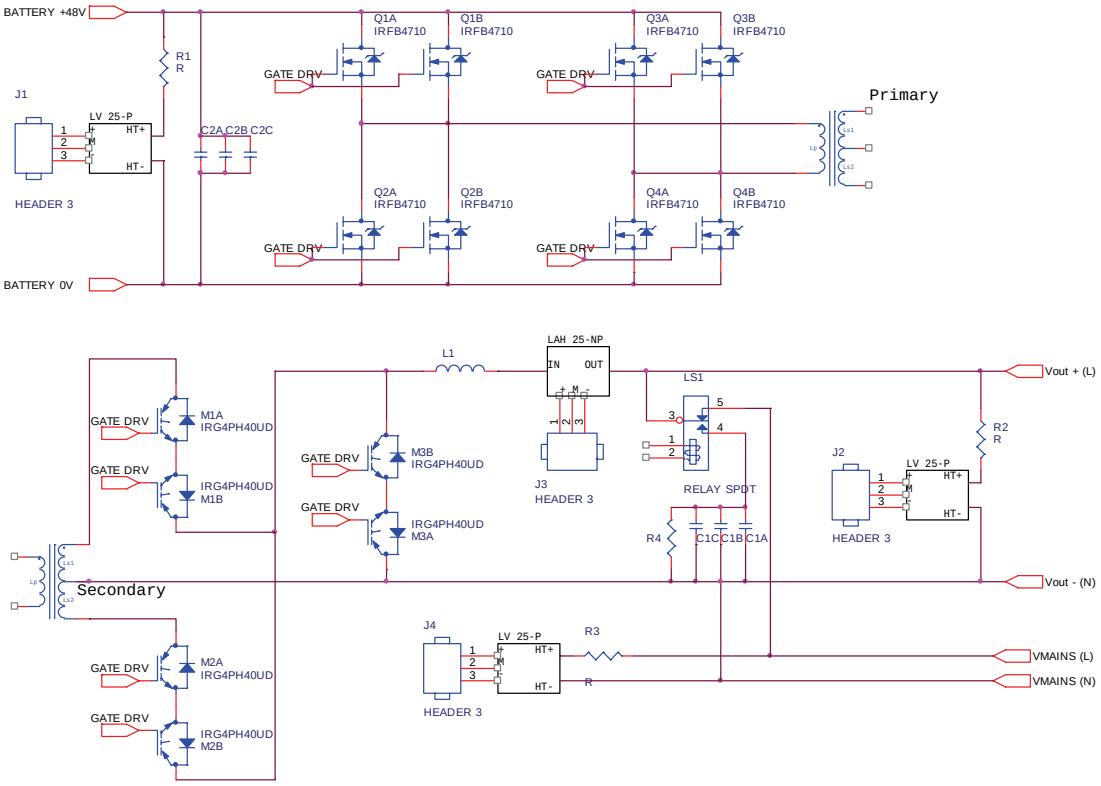

Figure 22: Converter Power Section Schematic

It should be noted that the power transformer is shown twice to facilitate splitting of the schematic into a format to fit the page. The details schematics of the Printed Circuit Boards that implement the schematic of Figure 22 are given in Appendices A.3, A.4 and A.5.

A comparison with Figure 21 shows that the practical considerations that were discussed at the end of Chapter 3 have been included in Figure 22. More specifically, Q1-Q4 has been expanded to show two MOSFET's in parallel per switch, while M1-M3 shows the two IGBT's in series per switch. The IGBT's are connected with their emitters together, which greatly simplify the design of the gate drive circuits.

The positions of the current and voltage measurement devices are also shown. The converter output and the mains supply will need to be synchronized

before the relay may be switched from on to off. Two voltage measurement devices are therefore required.

Resistor R4 is provided to discharge the output capacitors when mains power is available. Additionally, the control system should preferably only switch the relay on and off during zero voltage crossings to prevent surge currents.

The remainder of this chapter discusses the design of each of the components shown in Figure 22, with the exception of the voltage and current sensors. These are discussed in the chapter on the control system design.

4.2 Transformer Design and Switching Frequency

4.2.1 Turns Ratio Determination

The turns ratio of the transformer is determined by considering the peak output voltage of the converter during forward mode (power flowing from the batteries to the output). In this mode, the transformer's average secondary side output voltage is given by (Equation 3-7):

$$V_{out} = 2D_{Qpair}V_{bat}\frac{N_{\sec}}{N_{pri}} \qquad \textbf{(4-1)}$$

Where D is the duty cycle of either Q1-Q4 or Q2-Q3.

Equation 4-1 shows that the output voltage is determined by both the duty cycle and the turns ratio. The higher the maximum duty cycle in the forward mode, the lower the turns ratio of the transformer will be for the required peak voltage. A low turns ratio is desirable, since the step-up converter would not need to boost the input voltage during the reverse mode by a large factor.

If the duty cycle were however very high, the converter would not be able to exercise adequate control during transient load changes in the forward mode. The maximum switch duty cycle is chosen as D = 40%, so that the turns ratio can be expressed as

$$\frac{N_{pri}}{N_{\sec}} = \frac{V_{out}}{V_{bat}}\frac{1}{0.8} \qquad \textbf{(4-2)}$$

Equation 4-2 shows that the turns ratio can be determined if the battery voltage and the peak output voltage is known. To protect the batteries during operation, the cells should not be allowed to discharge below 25% of their capacity. This is equal to approximately 1.95V per cell, or $V_{BAT=}$ 46.8V for the battery bank. For an output voltage of 250 V(rms), the high voltage capacitor potential should be able to maintain a peak voltage of

$$V_{out} = \sqrt{2}V_{AC,rms} = 325V \quad \textbf{(4-3)}$$

Thus, if these values are substituted in Equation 4-2, the turns ratio can be calculated as:

$$\frac{N_{\sec}}{N_{pri}} = 8.76 \approx 9 \quad \textbf{(4-4)}$$

In an emergency, the batteries may be allowed to discharge deeper than the 25% specification. With the selected turns ratio of 9, and 100% duty cycle, the output voltage can be maintained for a minimum battery voltage of 325/9 = 36V. For still lower battery voltages, the sine wave output may be over modulated to maintain the correct RMS voltage output, although this will almost certainly damage the batteries.

The maximum nominal duty cycle of the converter in the charging mode can be calculated using the expression derived for the charging voltage, Equation 3-8. For a maximum charging voltage of 2.85 volts per cell (60V for the battery), the maximum duty cycle is:

$$D_{M3} = 1 - V_{out}\frac{N_{pri}}{N_{\sec}}\frac{1}{V_{\sec}} = 39.8 \approx 40\% \quad \textbf{(4-5)}$$

The inductor thus boosts the high voltage capacitor potential by a factor of

$$\frac{1}{1 - D_{M3}} = 1.66 \quad \textbf{(4-6)}$$

which is well within the acceptable practical limits for a conventional step-up converter.

4.2.2 Core Selection Considerations

Several factors influence the selection of a transformer core, e.g. window areas, core magnetization, etc. From previous experience, the author has found that the simplest method of selecting a core is to perform the calculations for several cores, and then select the smallest core that fulfils are the requirements. This selection procedure was performed via a spreadsheet table that is given in Appendix A.1.

Throughout this section, the EPCOS Data Book (Epcos Ag, 2001) and the MMG Neosid Catalogue (MMG Neosid Ltd, 1997) were used as references.

4.2.2.1 Maximum Power Transfer Capability & Switching Frequency

The maximum power transfer capability of a transformer is given in the datasheets for each core type and core material combination. This is estimated by the manufacturer by considering the following factors (Epcos Ag, 2001):

- Material Properties
- Thermal Design
- Winding Design
- Core & Bobbin Geometry

The tabulated values are accurate as long as the following assumptions remain valid:

- Transformer is operated in free air.
- Winding conductors are small enough to neglect the skin effect.
- $\Delta B < 400mT$ for push-pull type converters.

Since all these assumptions are valid for the present design, a thermal analysis of the transformer was not performed, and the tabulated values were used.

The power transfer of a transformer increases approximately linearly with frequency (Mohan et al, 1995: 752), since a shorter on-period results in less magnetization of the core, with the effect that the core can accept larger currents. The power transfer capability of a transformer is typically given at a certain reference frequency (e.g.100 kHz), which can be approximately linearly scaled to the desired frequency. It is therefore desirable from a power transfer point of view to have the switching frequency as high as possible.

On the other hand, several types of losses in a switching converter increase linearly with frequency. These include transistor switching losses and transformer core losses. In addition, some transistors families, e.g. IGBT's, do not have readily available products at high switching frequencies (e.g. above 100 kHz).

The selection of the switching frequency is therefore a compromise between size, losses and availability. A simple but effective method that was followed is to select the lowest switching frequency that will yield sufficient power transfer in the smallest possible core.

In order to be useful in a typical household renewable energy system a power rating of 2 kW has been chosen for the present converter. To control switching losses, and to enable widely available IGBT's to be used, a switching frequency of 50 kHz or less has been selected. From the table (Appendix A.1) it can be seen that both the ETD 54/28/19 and the ETD 59/31/22 cores can transfer 2 kW. However, the ETD59/31/22 can attain the transfer at 30 kHz. The calculations below justify the selection of the larger core, especially regarding the bobbin window area.

It shall also be noted in the section on digital design that a low switching frequency is also a desirable from a DSP point of view, since a considerable amount of calculation has to be performed during each switch cycle.

The switching frequency is therefore selected as F_S = 30 kHz.

4.2.2.2 Determination of the Low Voltage Side Turn Count

For a coil, ampere's law can be written as

$$E = N\frac{d\phi}{dt} \qquad \textbf{(4-7)}$$

Where E is the voltage across the terminals of the coil, N is the number of turns and ϕ is the flux inside the coil.

It is assumed that while power is applied to the coil, the voltage across the coil does not change appreciably due to the inclusion of storage capacitors. This results in an approximate linear increase of flux in the coil. In addition, it is assumed that coil conductors are adequately supported, so that the area enclosed by the coil does not change. Therefore, Equation 4-7 can be written as:

$$E = NA\frac{\Delta B}{\Delta T} \qquad \textbf{(4-8)}$$

Where B is the flux density. Since approximately the battery voltage is applied to the low-voltage winding of the transformer, Equation 4-8 can be rewritten as:

$$V_{BAT} = N_L A_e \frac{\Delta B}{\Delta T} \qquad \textbf{(4-9)}$$

Where A_e is the effective transformer core area.

This voltage is applied to the low voltage winding while switches Q1-Q4 or Q2-Q3 is on, so that ΔT can be replaced by the product of the switching period and the steady state duty cycle, or $D*T_S$. Although the steady state value of D was chosen as 40%, a value of D = 0.5 is selected to ensure that the core cannot be saturated during transient conditions when the maximum duty cycle is commanded. Equation 4-9 therefore becomes

$$V_{BAT} = N_L A_e \frac{\Delta B}{DT_s}$$
$$N_L = \frac{V_{BAT}\,0.5T_s}{A_e \Delta B} \qquad \textbf{(4-10)}$$

If the converter reverses the power flow direction just after the batteries had been fully charged, the maximum battery voltage of 60 V will be applied to the windings. ΔB is the maximum allowable change in core flux density. For the materials that are considered for use, the maximum flux density is given as 200 mT, which gives a ΔB of 400 mT.

Thus, for a given core area, the Equation 4-10 may be used to determine the required low voltage turns count. If a fractional value is obtained, the next highest integer number is selected. The table shows the turn counts calculated for the candidate cores. The final turn counts were chosen as N_L=7 and N_H = 60.

It should be noted that the battery clamps the voltage across the transformer windings, since there is no inductor connected between it and the windings. The voltage across the high-voltage windings is therefore also clamped to the value of $V_{BAT}*N_H/N_L$. Since M1 and M2 also have a maximum duty cycle of 50%, the core cannot be saturated in the reverse direction. The reverse mode is therefore not considered further.

4.2.2.3 Bobbin Window Area

The datasheets give the bobbin windows area (A_n) of each core type, as duplicated in the selection table. This indicates the cross sectional area that is available in the bobbin to pass conductors through.

Since the conductors that will be used are circular in cross section, the sum of the areas of all the conductors will be less than the sum of the space required to pass them through. This fill factor shall be less than one, and is practically around 50-60%. (Mohan et al, 1995: 753). For the present design a fill factor of 50% has been assumed, to account for the circular shape of the conductors and the hand winding procedure.

The conductor size is chosen as large as practically possible in order to minimise power losses in the transformer windings. The amount of power dissipated in a copper conductor of length L and area A is given by:

$$\begin{aligned} P_{Cu} &= I_{RMS}^2 R \\ &= I_{RMS}^2 \left(\rho_{Cu} \tfrac{L}{A}\right) \\ &= \left(J_{RMS} A\right)^2 \left(\rho_{Cu} \tfrac{L}{A}\right) \\ &= J_{RMS}^2 \rho_{Cu} \left(V_{Cu}\right) \end{aligned} \qquad \textbf{(4-11)}$$

Where V_{Cu} is the volume of the conductor. It can be seen that the power dissipation per volume of copper decreases as a power of two with a decrease in current density. However, since a decrease in current density implies a linear increase in volume (assuming the length stays constant), the power dissipated decreases linearly with an increase in conductor area (as can be seen

in line two of the Equation 4-11). It would therefore be advantageous to have the conductors as thick as possible.

From the tables it can be seen that a current density of 6 A/mm^2 yields a required area of 353 mm^2, which is just under the A_n value of the selected core of 365 mm^2. Indeed it was found that during construction the windings just fitted onto the bobbin when conductor where selected for a current density of 6 A/mm^2.

4.2.2.4 Skin Effect

As the frequency of the current increases in the windings, the charge carriers tend to concentrate towards the edges of the conductor. This is called the skin effect, and t increases the current density near the conductor edges, thereby increasing the losses.

The effect of skin depth can be ignored if the diameter of the conductors is kept less than twice the skin depth (Mohan et al, 1995: 753). At the switching frequency of 30 kHz, the skin depth is approximately 0.5 mm. The windings are therefore constructed from several strands of 1 mm diameter isolated transformer wire.

The low voltage winding therefore consists of 7 parallel 1 mm diameter conductors, while the high voltage windings use a single 1 mm diameter conductor.

4.3 Switch Design

This section will describe the selection of low and high voltage switching transistors. The transistors are selected based on anticipated voltage, current and switching conditions of the converter. Once the selection has been made, the power dissipation is calculated for all switches, since this will be used in the section 4.3.4 on heat sink design.

4.3.1 Switch Type Selection

Step-up, step-down and all converters derived from these basic topologies act as DC transformers that convert one voltage to another. Since power is not added during the conversion, and only a small fraction is dissipated, the product of the current and the voltage at the input and output terminals is approximately equal. Thus, for a low voltage terminal, the current will be high, and at the high voltage terminal, the current will be low.

For low voltage applications, MOSFET's are the transistors of choice. Several reasons for this can be given:

- MOSFET's act like a resistor with a very low on-resistance. Typical values are in the order of 10 milliohms for 50-100 V devices. The on-resistance however increases rapidly with device blocking voltage rating.

- MOSFET's can be paralleled since they have a negative temperature coefficient. This ensures that parallel MOSFET's that are closely spaced on the same heat sink automatically distribute the current load evenly between them.
- The resistance of a parallel arrangement of MOSFET's is equal to the parallel equivalent of their resistances (i.e. they act like resistors), making very low resistances possible.
- MOSFET's support very fast switching times, thereby minimising switching losses.
- MOSFET's have an insulated gate that only requires current flow when it is being switched on or off.

For high voltage applications, IGBT's are the best suited. Reasons for this selection include:

- IGBT's have high blocking voltage ratings.
- IGBT's have small on-state voltages even for high voltage blocking ratings. Typical values are in the order of 2 V for devices with a 1000 V rating.
- Although not as fast as MOSFET's, IGBT's have relatively fast switching times.

Thus, MOSFET transistors are selected for switches Q1-Q4 and IGBT's for switches M1-M3.

4.3.2 Low Voltage Transistors

4.3.2.1 Low Voltage Transistor Selection

The IRFB4710 transistor family was released during January 2002. It is one of the latest generations of MOSFET's, and is specifically designed for 48V half and full bridge converters in telecommunications power supplies.

The IRFB4710 device is rated at 75 A in the TO-220 package, or 30% higher current than previous generation devices, and have a 40% lower on-resistance, or R_{DS}(on), than previously available devices. This results in higher efficiency and lower operating temperature.

Leading particulars of the IRFB4710 are:

- R_{DS}(on) = 0.014 Ohm (max)
- V_{DS}(BR) = 100 V (min)
- I_D (max) = 53 A (@100°C)

4.3.2.2 Low Voltage Transistors: Forward Operation

In order to increase reliability, it was decided that all devices shall be rated at least 100% higher than the maximum anticipated operating conditions for voltage and current. (US Department of Defence, 1998: 7-30)

For the low voltage transistors, the maximum current is approximately 50 A, which thus requires a device rating of 100 A. To attain this rating, two IRFB4710's were placed in parallel to form a single switch. The resulting maximum on-resistance is R_{DS} (on) = 0.014/2 = 0.007 Ohm.

During the forward mode, the maximum power dissipated by each parallel combination is:

$$\begin{aligned} P_{conduction,50\%} &\approx \tfrac{1}{2} I^2 R \\ &\approx 0.5 \times (50)^2 \times 0.007 \\ &\approx 8.75W \end{aligned} \qquad \textbf{(4-12)}$$

The factor of a 0.5 reflects the fact that each switch has a maximum duty cycle of 50%.

The switching losses of a transistor can be approximated by (Mohan et al, 1995: 21):

$$P_{switch} = \tfrac{1}{2} V_d I_o f_s \left(t_{c(on)} + t_{c(off)} \right) \qquad \textbf{(4-13)}$$

If the values of the design parameters and the switching times from datasheet are inserted, the switching loss of each parallel combination is calculated as 8.75W, which coincidentally the same as the conduction loss per switch. The total maximum power dissipation of each switch in the forward mode is thus P_{TOT}= 17.5W.

Since there are four switches that each have the above power dissipation, the total maximum power that may be dissipated is 70W. This maximum will be attained when each switch pair operates at a duty cycle of 50%, so that the pairs have a combined duty cycle of close to 100%.

4.3.2.3 Low Voltage Transistors: Reverse Operation

During the reverse mode, the integral body diode of the IRFB4710 conducts the current. For a forward voltage of 1.3V, the power dissipation for each switch at the maximum charging current of 25A is:

$$\begin{aligned} P_{REV} &= \tfrac{1}{2} V_{ON} I_O \\ &= 16W \end{aligned} \qquad \textbf{(4-14)}$$

Where it is assumed that each switch is operated at its maximum duty cycle of 50%. Again, since there are four switches, the total power dissipation is 64W.

This condition will not be realised in practice, since the converter operates as a step up converter at a typical duty cycle of 20% per switch. However, it does show that the power dissipated during the reverse condition is significantly

less than the forward operation loss, so that the forward mode is therefore used for the design of the heat sink.

4.3.3 High Voltage Transistors

4.3.3.1 High Voltage Transistor Selection

With the maximum battery charging voltage being specified as 60V, and the turns ratio of the transformer as N_{PRI}/N_{SEC} = 9, the maximum voltage that is expected is approximately 540V. Since a centre-tapped transformer is used, the voltage at the common ground of the driver circuits will vary between -540V and +540V with respect to the neutral voltage. Transistors are therefore needed that can block at least 1080V.

For the high-voltage transistors, the IRGP30B120KD IGBT's with integral soft recovery reverse diodes have been selected. These transistors have a breakdown voltage rating of V_{CES} = 1200V. In addition, they feature low $V_{CE(ON)}$ and V_F (diode forward) voltages. They are capable of conducting a collector current of up to 25A.

Leading particulars of the IRGP30B120KD are:

- $V_{CE(ON)}$ = 2.5V (typ @125°C, 22A)
- V_F = 1.7V (typ @125°C, 22A)
- V_{CES} = 1200V (max)
- I_C (max) = 30A (typ @100°C)

Note that the design specification of 100% derating does not apply to this transistors voltage rating, due to the unavailability of suitably rated IGBT's.

4.3.3.2 High Voltage Transistors: Power Dissipation

It should be noted that, no matter what mode and state the converter is operating in, the high-voltage side current will always flow through one IGBT junction and one reverse diode. Thus, the voltage drop will always be the sum of the IGBT and diode drops.

Since the power delivered in the forward mode is much greater than during the reverse mode, the forward current is used for the power dissipation calculation. For an average HV output of 2 kW at 230 VAC, the RMS inductor current is approximately 8.70 A. Thus, the power dissipated is given by (assuming for simplicity that the voltage drops remain constant with collector current):

$$\begin{aligned} P_{conduction} &\approx I_{\max}\left(V_F + V_{CE}\right) \\ &\approx 36.54W \end{aligned} \qquad \textbf{(4-15)}$$

The current during the reverse of operation is approximately one half, which again implies that the forward mode be used for the design of the heat sink.

The switching losses are by using the same method as for the MOSFET's. It is assumed that the diode does the switching on and off, since the IGBT of each switch can be kept on or off, depending on the output polarity. The result is:

$$P_{switch,diode} = \tfrac{1}{2} V_d I_o f_s \left(t_{c(on)} + t_{c(off)}\right) = 3W \qquad \textbf{(4-16)}$$

This power will be dissipated by M1 and M2. However, M3 is switched at twice the rate of either M1 or M2, so that the switching losses of Q3 is 6 W.

The total power dissipated by the IGBT's during the forward operation is therefore 48.54 W.

4.3.4 Heat Sink

The performance specifications of the power transistors were calculated at a case temperature of 100 °C. To ensure reliable operation, this temperature must be maintained in all environmental extremes. For this design, it is assumed that the maximum ambient temperature expected is 40 °C

As shown, the total power dissipated has the largest value during the forward mode, and is calculated at approximately 118.54 W for all devices. According to the datasheets, the TO-220 package has a case to sink thermal resistance of 0.5 K/W and the TO-247 of 0.24 K/W.

It is preferred that all the transistors be mounted on a single heat sink, which can also act as the chassis for the converter. Since the power dissipated and the case resistance is not uniform for all transistors, the temperature of their cases will not be the same even if the heat sink is at a uniform temperature throughout. The table below summarises the power dissipated by each transistor and the temperature rise between the case and the sink. The calculations were performed using the methods and values of the preceding sections:

Transistor	Conduct. Loss (W)	Switch. Loss (W)	Total Loss (W)	Case Therm. Res. (K/W)	Temp. Rise (K)	Condition	Quantity
Q1A-Q4B	3.5	4.375	7.88	0.5	3.94	@40% D/C	8
M1A, M2A	9.5352	0	9.54	0.24	2.29	@40% D/C	2
M1B, M2B	6.5076	3	9.51	0.24	2.28	@40% D/C	2
M3A	4.7676	0	4.77	0.24	1.14	@20% D/C	1
M3B	3.2538	6	9.25	0.24	2.22	@20% D/C	1

The above table was constructed for the converter operating in the forward mode at 40% MOSFET duty cycle (80% overall). It was assumed that each of the individual MOSFET's in the low voltage switches dissipates the 50% of

the power. It was also assumed that M1A, M2A and M3A were operating as IGBT's and are permanently switched on. M1B, M2B and M3B were operating as diodes.

It can be seen that the highest temperature rise is in the MOSFET's. Thus, to maintain a case temperature of 100 °C, the heat sink temperature should be kept below 96 °C, which equates to a maximum allowable rise of 56 K above ambient. The sum of all the losses in the above table is 115.1 W, which results in a maximum allowable heat sink thermal resistance of 0.49 K/W.

The H6 heat sink profile from Fastron Technologies, Victoria, Australia has been selected:

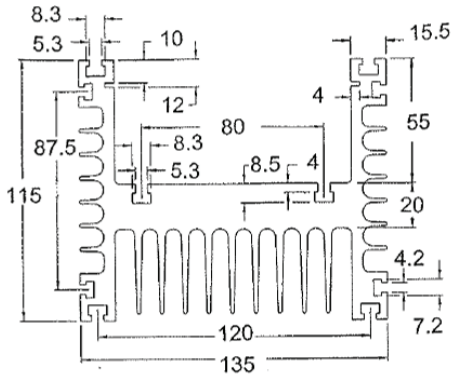

Figure 23: Fastron H6 Heat Sink Profile

This profile provides several mounting options for transistors and PCB's and partially forms an enclosure. Mounting of the heat sink to a panel or wall should be simple.

The graph of Figure 24 shows the H6 heat sink's performance as a function of length. The graph assumes the heat sink is placed vertically in free air, and operates at a temperature rise of 50 K above ambient, which is close the design value of 56 K.

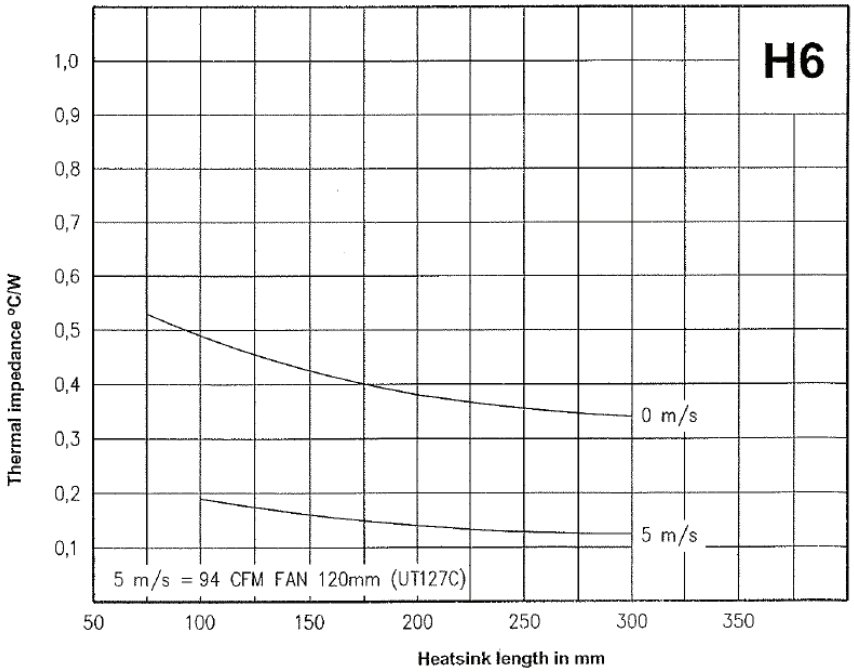

Figure 24: Fastron H6 Heat Sink Performance

It can be seen that this profile reaches the specified thermal resistance of 0.49 K/W with a length of approx 110 mm.

In addition to heat management, the heat sink also acts as mechanical support for the components and PCB's, and functions as an enclosure. The size and length of the PCB's therefore greatly influences the selection of the heat sink.

The overall length of the Power PCB's in their connected configuration is approximately 370 mm. However, the power devices to be thermally connected to the heat sink only have a total length of 260 mm. The efficiency of a heat sink typically decreases with its length, i.e. while the power dissipation capacity of the heat sink increases with length, the rate of increase of power dissipation capacity decreases with length (Fastron Pty Ltd, -). Thus, it will be cheaper to select a heat sink that attains the required thermal resistance with the shortest possible length, which in this case is approximately 260 mm.

Two options are therefore available, either select a full-size heat sink, or use a partial heat sink with a mechanical support for the remainder of the non-power components. It was decided that, due to rigidity and ease of manufacturing considerations, a full-length heat sink would be implemented. The cost of this option is however significant. The heats ink length was chosen as 428.6 mm. This is approximately equal to $1/7^{th}$ of a standard 3 meter extrusion length, and provides ample space for the mounting of the power PCB's and the end connections. The full heat sink would also make it much simpler to prevent dust and water spray ingress into the converter.

The selected heat sink length is much greater than required for thermal heat dissipation. From the graph of Figure 24 it can be seen that the heat sink

thermal resistance asymptotically approaches approximately 0.34 K/W for lengths greater than 300 mm. This value will yield a maximum heat sink temperature rise of 39.1 K above ambient, which is significantly lower than the 56 K design value. The converter will therefore operate much cooler, increasing safety in case of hand contact, prolonging component life, and enabling operation in harsher climates.

Lastly, since the front as well as top and bottom sides of the heat sink inside cavity will be enclosed, thereby preventing airflow across these surfaces, it is expected that the actual value of thermal resistance might be slightly higher than the tabulated values. This effect is however not considered further due to the large margin of safety regarding the thermal resistance, as mentioned in the preceding paragraphs.

4.4 Inductor and Capacitor Design

4.4.1 Output Capacitor

4.4.1.1 Output Quality Standard

IEEE standard 519-1992 can be used to specify the maximum allowable voltage distortion on an electricity distribution system (IEEE-519, 1992). This standard specifies that, for most installations, the individual harmonics' amplitudes must all be less than 3% of the fundamental, and that the Total Harmonic Distortion (THD) must be less than 5%. The measurement of the above values must be made at the Point of Common Coupling (PCC).

In a distributed power distribution system, the PCC is normally the connection of a customer's premises to the distribution grid. Analysis of the harmonic values at this point typically involves complex modelling of the customer's equipment, the distribution grid, and even closely located neighbour's equipment, which share a feeder line or transformer.

In the present system, however, the converter only delivers power to the user's equipment when the mains supply has failed. When the mains supply is available, it is directly connected to the user's equipment and the converter has no control over the voltage waveform and therefore the power quality.

Thus, when the power quality is under control of the converter, it is isolated from the mains system, and only the design of the converter and the user load affects the voltage waveform. The PCC is therefore the converter output terminals, which is internally directly connected to the output capacitor.

4.4.1.2 User Loads

For a power supply with finite output resistance, the user load current waveform contributes greatly to the Total Harmonic Distortion of the Voltage Waveform (THD_V). In passive systems (i.e. composed of generators, transformers and transmission lines) THD_V is controlled by ensuring that the supply impedance at the PCC is sufficiently low so that the current waveform

drawn by the user's equipment does not distort the voltage waveform significantly.

Active systems, like the present converter, can however rely on control methods to control the output voltage of the converter directly, thereby presenting a much smaller output impedance to the load. This would be analogous to the use of a voltage follower operational amplifier on the output of an analogue sensor, to greatly increase its apparent output impedance.

Thus, the converter should be so designed to be agile enough respond to load demands with a frequency response higher than the expected load current frequencies, while still having some amount of suppression built in, in order to suppress high-frequency switching noise.

Several standards exist which specify typical current waveform for use in THD_V calculations, e.g. IEC61000 and IEC62052. Experimentally determined waveforms are also available. The National Research Council of Canada maintains a Waveform Library of over 30 standards and experimental based current waveforms (National Research Council of Canada, 2006). A typical residential load waveform is shown in Figure 25 and Figure 26:

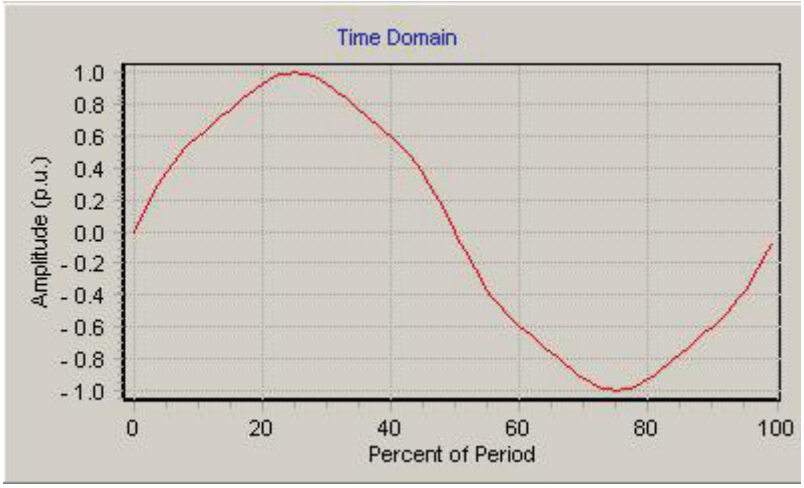

Figure 25: Typical Residential Current Waveform, Time Domain

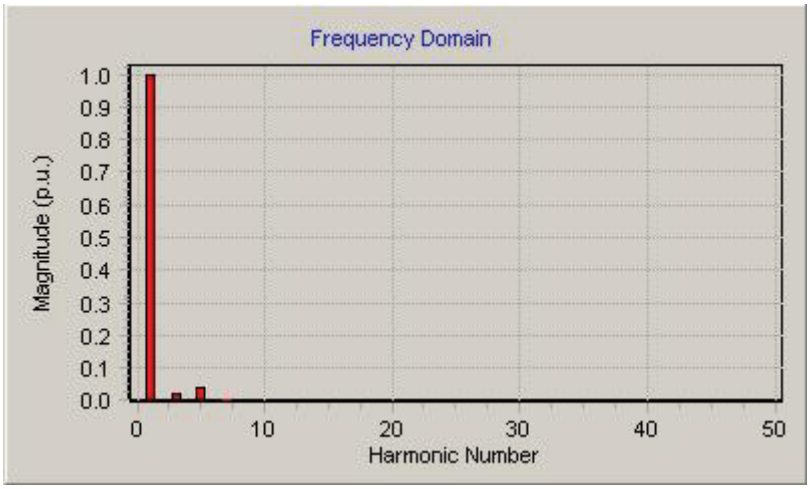

Figure 26: Typical Residential Current Waveform, Frequency Domain

The amplitudes of the harmonics of this waveform are as follows:

Harmonic	Amplitude	Phase
0	0	0
1	1	0
3	0.0225	0
5	0.0398	0
7	0.0054	0

This load has little harmonic distortion, with a 7^{th} order harmonic amplitude of only 0.55%. Indeed, only a few highly distorted examples of the waveforms in the Waveform Library have any significant harmonic content above the 10^{th} harmonic.

Individual electronic devices do however have a significantly larger harmonic content. Since only a few devices may be connected to the converter, these highly distorted waveforms must be taken as worst-case design scenarios. The waveform of Figure 27 and Figure 28 is typical for a load consisting of a number of computers (or other switching power supplies). It is particularly distorted, and is suitable for use as a design basis:

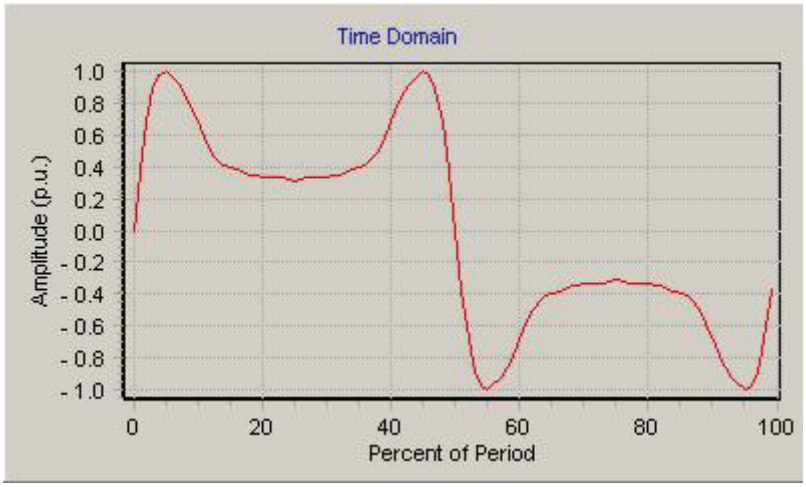

Figure 27: Typical Computer Current Waveform, Time Domain

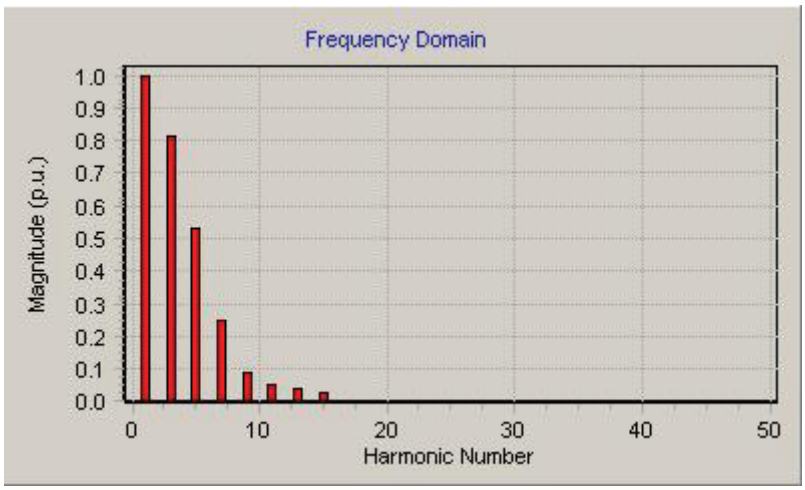

Figure 28: Typical Computer Current Waveform, Frequency Domain

The harmonics of this waveform is as follows:

Harmonic	Amplitude	Phase
1	1	0
3	0.81	0
5	0.53	0
7	0.25	0
9	0.09	0
11	0.05	0
13	0.04	0
15	0.03	0

Again, it can be seen that the harmonic content above the 15th order harmonic is negligible. Indeed, none of the library's waveforms has any significant

harmonic content above the 15th Harmonic. For 50 Hz, the 20th harmonic is 750 Hz.

Thus, if the converter has a frequency response that still has a relatively large gain and low phase shift at 750 Hz, it will be able to accurately track the sinusoidal reference voltage with the given current harmonics, and present a low output impedance to the user loads. To ensure that this is the case, a converter overall response corner frequency of 1.5 kHz (double the highest harmonic frequency) is chosen as basis to design the converter output stage and control system.

4.4.1.3 Switching Harmonics and LC Filters

The second type of harmonics that may be present are the high-frequency switching harmonics generated by the converter itself. Since the voltages generated by the transistors are essentially square waves, they have significant harmonic content. Due to the high frequencies involved (all harmonics are multiples of the switching frequency of 30 kHz), these are easily dealt with using a two-pole, low-pass LC filter.

The output section of the present converter effectively consists of exactly such an LC filter. Although this LC filter is normally analysed individually as a capacitor and inverter for the purposes of designing a DC output converter, they could also be analysed together as an analogue filter. As mentioned above, this LC filter must be designed to effectively suppress the high frequency switching transients, while still having enough high-frequency gain to accurately track the reference voltage in the present of current harmonics.

The present configuration (consisting of a high-frequency switching output stage, which produces a Pulse Width Modulated sine wave that is passed through an LC filter) is similar to a system used extensively in industry, namely a Variable Speed Drive with a sinusoidal (LC) output filter. Figure 29 illustrates such a system (with a DC midpoint connection):

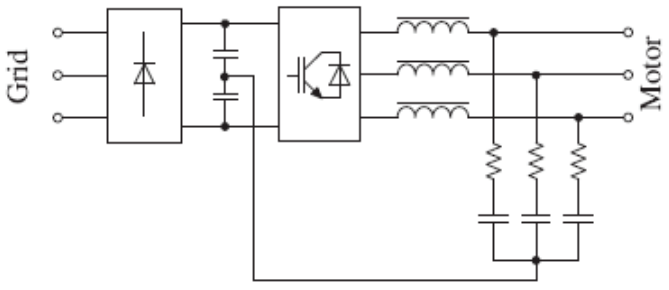

Figure 29: VSD with LC Output Filter

The operation and control of such systems have been well documented. Reference (Salomäki, 2007) gives an overview of such systems, and their control. The frequency response of an LC filter is shown in Figure 30 for several values of Q (Unitrode Corporation, 1992):

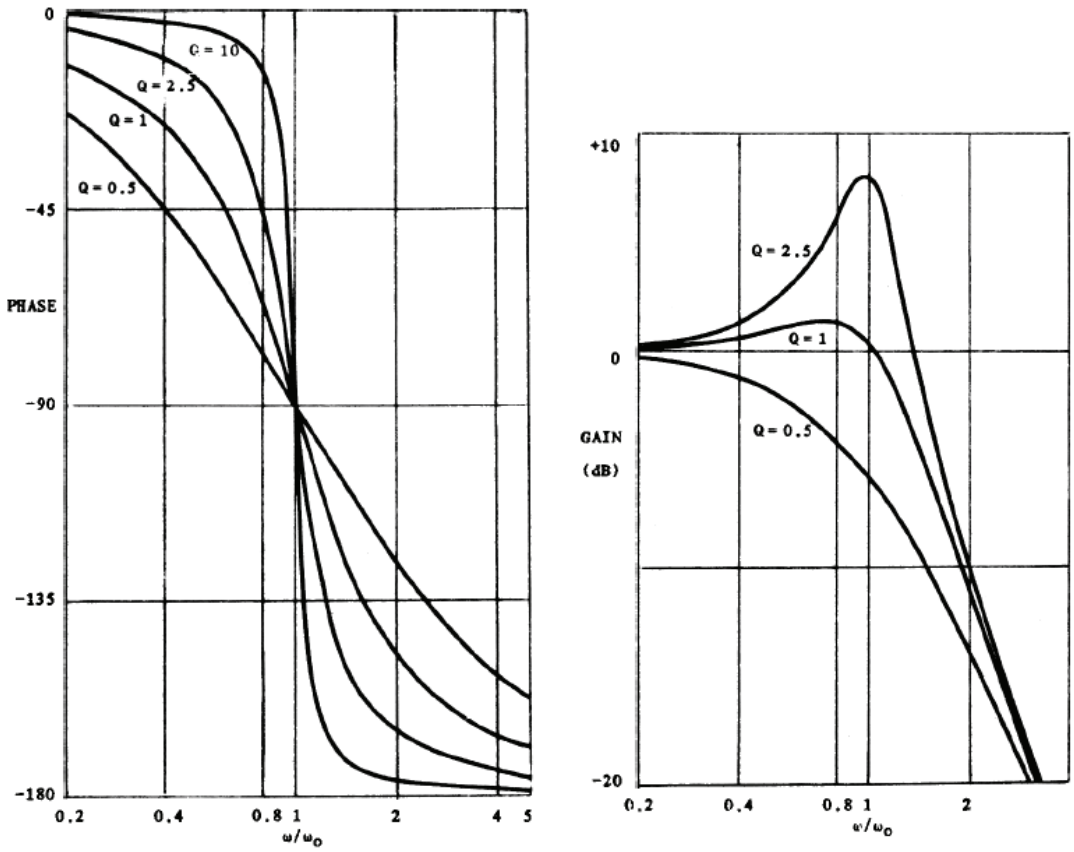

Figure 30: LC Filter Frequency Response

Where Q is referred to as the quality factor, and is determined by the internal resistances of the inductor and capacitor, and ω_0 is the resonance frequency.

Several design philosophies have been proposed for the design of such filters. One that has proven successful and is widely used according to (Salomäki, 2007), is to select the filter resonance frequency as $1/10^{th}$ of the switching frequency. This effectively eliminates high frequency switching harmonics from entering user loads, and has been selected for this design. Other design philosophies include selecting a resonant frequency of 30% of the switching frequency, or selecting one in a range from 10 times the highest fundamental, but less than half of the switching frequency. During simulation it was however determined that selecting a filter resonant frequency at $1/20^{th}$ of the sampling frequency or lower results in the significantly reduced voltage overshoot and ripple when compared to the 10% criterion, and it was therefore used.

For the present converter, a switching frequency of 30 kHz results in a chosen filter resonance frequency of 1.5 kHz. This is equal to the selected value of the overall converter resonance frequency. Using the inductor value calculated in the following section, the output capacitor value for the converter can be calculated as:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

$$C = \frac{1}{L}\left(\frac{1}{2\pi f_{res}}\right)^2 \qquad \textbf{(4-17)}$$

$$= 3.2\,uF$$

This value initially appears relatively low, especially when compared to the output capacitance of comparable DC output converters. However, the capacitors used to achieve this capacitance cannot be polarised, since they have to accept both positive and negative voltages. Thus, electrolytic capacitors with their extremely high energy densities cannot be used. Instead, metalized polypropylene suppression capacitors have been selected. Due to board size constraints, five 0.68 uF, 250 V capacitors have been placed in parallel.

In order to provide some load during the discharging mode, and to discharge the high-voltage capacitors when power has been disconnected, a 50 kOhm, 5 W resistor has been placed in parallel with the capacitors.

4.4.2 Inductor

4.4.2.1 Inductor Currents

For the design of the inductor, both the forward and reverse modes are taken into account. Since the output voltage changes slowly when compared to the switching frequency (50-60 Hz versus 30 kHz), the calculations of this section assumes DC operation of the converter at the peak AC voltage and current values.

First, consider the reverse mode when energy flows to the batteries. Lead acid batteries should generally not be charged at a current (in amps) of more than 12.5% of their capacity (in Ampere-hours). For a typical 4-battery, 48 V, 105 A-h installation, this maximum average charge current equates to approximately 12.5 A.

It is customary to select an inductor ripple current amplitude of 10% of the nominal inductor current as design basis. However, it was found during simulation of the converter that this specification makes the inductor current difficult to control at the sample frequency selected for the DSP. It was also found experimentally that a 5% current ripple resulted in much improved controllability at sample rates of 15 and 30 kHz, and was therefore selected.

For an average reverse mode current of 12.5A, the average secondary winding current will be equal to

$$
\begin{aligned}
I_{\sec,ave} &= I_{charging}\frac{N_{pri}}{N_{\sec}} \\
&= 12.5\times\frac{1}{9} \\
&= 1.39\,A
\end{aligned}
\qquad \textbf{(4-18)}
$$

The inductor current can be calculated from the secondary winding current by recognising that the high-voltage side operates as a step up converter. Thus, for the reverse mode:

$$
\begin{aligned}
I_{L,ave} &= \frac{I_{\sec,ae}}{(1-D)} \\
&= 2.3\,A
\end{aligned}
\qquad \textbf{(4-19)}
$$

For the forward mode, the maximum energy transfer is specified as 2 kW. This equates to an average inductor current of

$$
\begin{aligned}
I_{L,ave} &= \frac{P_{\max}}{V_{out}} \\
&= \frac{2000}{325} \\
&= 6.15\,A
\end{aligned}
\qquad \textbf{(4-20)}
$$

Although the reverse current is the smallest, the secondary winding current, and therefore the charging current, is discontinuous. This is in general true about the output current of a step-up converter. The inductor ripple current magnitude is therefore not as relevant in the reverse mode, and the forward current is used as basis for selecting the inductor value.

Thus, a 5% ripple current in the forward mode is approximately equal to 0.31 A.

4.4.2.2 Inductance Values

Using the ripple current of 0.31 A for the forward mode, the inductance value of the inductor may be calculated. This inductance value will be used in the following section to investigate the dynamic response of the system.

The rate of change of current in an inductor is related to the voltage over the inductor by Faraday's law:

$$
V(t) = L\frac{dI_L}{dt} \qquad \textbf{(4-21)}
$$

If a constant voltage V is applied over an inductor for a time ΔT, the differential of Equation 4-21 can be written in terms of current and time changes:

$$\Delta I = \frac{V \times \Delta T}{L} \qquad \textbf{(4-22)}$$

Therefore, if the current increase over the period is specified, the value of the inductance may be calculated by recasting Equation 4-22 into:

$$L = \frac{V \times \Delta T}{\Delta I} \qquad \textbf{(4-23)}$$

During the steady state forward mode, a (reverse) voltage of V_{out} is applied to the inductor when both M_1 and M_2 are off. This voltage is applied for a period of

$$\begin{aligned} \Delta T &= \frac{1}{F_s}\left(\frac{1}{2} - D_{M1,2}\right) \\ &= \frac{1}{30000}0.1 \\ &= 3.33us \end{aligned} \qquad \textbf{(4-24)}$$

The value of the inductor can now be calculated by substituting 4-24 and the known parameters into Equation 4-23:

$$\begin{aligned} L_{Forward} &= \frac{V \times \Delta T}{\Delta I} \\ &= \frac{325 \times 3.33 \times 10^{-6}}{0.3075} \\ &= 3.52\,mH \end{aligned} \qquad \textbf{(4-25)}$$

4.4.2.3 Inductor Core Selection

The inductance of conductors wound upon a core is given by

$$L = A_L N^2 \qquad \textbf{(4-26)}$$

where A_L is the inductance factor (as given in the core's datasheet), and N the number of turns around the core. Since L is specified, and A_L is known for a specific core is known, N can easily be calculated.

The selection of a suitable core is dependent on the energy the core can store. The maximum energy present in the core can be calculated from the maximum steady state inductor current, which is given as 6.15 A, plus the current ripple. The energy in the core is given as:

$$U_B = \tfrac{1}{2} L I_{\max.}^2 = 0.0734\,J \qquad \textbf{(4-27)}$$

The energy stored in the inductor can also be written in terms of the magnetic fields within the core:

$$U_B = \frac{V_{core} B_{\max}^2}{2\mu_0 \mu_e} \quad or \quad \mu_e = \frac{V_{core} B_{\max}^2}{2\mu_0 U_B} \qquad \textbf{(4-28)}$$

Where B_{max} is the maximum magnetic field strength in the core, V_{core} is the volume thereof, μ_0 the permeability of free space and μ_e the effective permeability of the core. In this equation, V_{core} and μ_e is given in the datasheet for each core, μ_0 is a physical constant, U_B has already been calculated and B_{max} is specified.

To select a suitable core, the minimum effective permeability (μ_e), as required by the other parameters for the specific core, may be calculated. In cores where the value given for μ_e in the datasheet is smaller than the calculated value, the magnetic field strength will surpass the maximum specified value (B_{max}).

The core selection is also dependant on the window area of the bobbin. For a current density of 6 A/mm^2, the wire cross section can easily be calculated. The window area required is then given by

$$A_{window} = \frac{A_{wire} N}{K_{fill}} \qquad \textbf{(4-29)}$$

where K_{fill} is the fill factor.

The remainder of the inductor design procedure is based on the short paper given in (Randewijk, 2004) and accompanying spreadsheet. Since that reference was authored by the study leader of this project, it will not be repeated.

The tabulated and calculated values for several candidate cores are given in the Appendix A.2, which is the spreadsheet of (Randewijk, 2004). Although several cores satisfy the criteria, the ETD59/31/22 has been chosen. The selection was primarily based on the availability of the core, since it is used for the main transformer as well.

4.4.3 Low Voltage Capacitor

The function of the low-voltage capacitor is twofold:

- Firstly, the full bridge converter on the primary (low-voltage) side of the converter should be presented with a constant DC voltage. The inductance of the potentially long cables to the batteries may lead to large voltage fluctuations when the load current changes suddenly.
- Secondly, to limit the high frequency ripple current to the batteries. Lead acid batteries are very susceptible to damage by ripple currents. To limit the ripple, a capacitor is inserted in parallel to the battery, close to converter. The inductance of the wiring to the battery will force the ripple current to flow through the capacitor, and not the batteries.

The ripple voltage in the batteries is assumed to be less than 1% of the rated voltage, which is approximately 0.5 V. For a rated current of 50 A, the capacitance required can be calculated by considering the definition of capacitance and substituting known parameter values:

$$\begin{aligned} C &= \frac{\Delta Q}{\Delta V} \\ &= \frac{I_{\max} \times \Delta T}{V_{bat} \times 0.01} \\ &= \frac{50 \times 0.4}{48 \times 0.01 \times 30000} \\ &= 1400\,uF \end{aligned} \qquad \textbf{(4-30)}$$

The actual capacitors chosen consist of two 1500 uF, 100 V electrolytic capacitor, as well as a 33 uF Plastic Film capacitor, to ensure that high frequency ripples do not reach the battery.

4.5 Power PCB Design

The layout of the power PCB's are shown in Appendices A.3 to A.5.

Due to PCB size restrictions imposed by the layout design software the author used (EAGLE v4.16 Standard) only boards of Eurocard size (160x100 mm) or smaller could be designed. To circumvent this problem, the power design was split over three PCB's. This also facilitated experimentation to a certain extent

without having to manufacture all the PCB's repeatedly. The three PCB's were:

4.5.1 Low Voltage (MOSFET) PCB

This PCB contained the MOSFETS, low voltage capacitor and battery voltage measurement arrangement.

The philosophy behind the design of this PCB was to keep the traces as short and as wide as possible. The current in the MOSFET drain and source traces are in the order of 50 A at 40% duty cycle, equating to an RMS current of approximately 20 A. For a current density of 10 A/mm^2, these traces require a cross sectional area of approximately 2 mm^2. During the design, it was found that traces of approximately max 10 mm wide could be fitted onto the PCB. These traces would then require a copper thickness of 0.2 mm.

The thickest readily available PCB material that could procured was 2 Oz, or approx 70 um. It was therefore decided that the PCB LV power PCB would be double sided, which would produce a combined thickness of 0.14 mm. This results in a trace current density of 14.3 A/mm^2, which is still acceptable.

The small traces leading to the transistor pins are required to be much smaller due to the close spacing of TO-220 transistor package. These traces were built up with solder on both sides to increase the cross sectional area.

Since the PCB is double sided, special care was taken in order to ensure the mounting screws of the transistors were accessible through the PCB. Otherwise installation would be difficult, and removal of the PCB to replace a faulty transistor would involve de-soldering of all the transistors on the PCB on both sides, which is nearly impossible.

The transistors were also spaced evenly to facilitate the mounting of the driver daughter boards. To ensure the maximum amount of copper around the transistors, it was decided to mount the drivers on separate boards (see chapter on driver design).

The interface of the LV PCB is the low voltage side of the transformer, which is mounted directly onto the PCB.

4.5.2 Mid Section (IGBT) PCB

The high voltage side of the transformer is mounted on the IGBT PCB. This PCB contains all six IGBT's.

The design philosophy of this PCB was similar to that of the Low Voltage PCB, although the traces were much smaller, since a maximum current of only 6.15 A is anticipated. For a current density of 10 A/mm^2, double-sided traces of approximately 4.25 mm wide were required.

Since voltages of +560 V and -560 V are present in this board, trace isolation is of importance. According to (IPC-2221, 1991) this board and the HV output board are classified as type B2, uncoated external conductors when used at elevations of less than 3050 meter. The minimum allowable trace isolation for this voltage is calculated as 2.8 mm. This was checked using the Design Rule Check function of EAGLE. Some traces on the boards however cannot be isolated to the minimum distance, for example transistor pins. Because of this, the boards were eventually coated with a conformal coating to increase their voltage withstand rating.

4.5.3 High Voltage (Output) PCB

The output PCB contains the inductor, output capacitors, voltage measurement transducers and relay. Connectors are also provided for both the mains and output. The same considerations as for the previous two PCB's apply.

The PCB trace for the main current flow was made much wider than required, so that the output PCB could be connected directly to the LV PCB to test the control and operation of the system without introducing large voltages.

The trace isolations were taken to be the same as the Mid section PCB above, and conformal coating was applied.

4.6 Chapter Conclusion

This chapter detailed the design of the power components of the converter.

From the proposed topology and practical considerations given in Chapter 3, the actual schematic of the power section was derived. The design of every component in this schematic was discussed in detail, including the heat sink and the mechanical mounting of the power devices. Finally the layout of the three power PCB's was discussed.

This chapter therefore concludes the discussion of the power components of the proposed topology, with the following chapters focusing on the control components of the converter, including the transistor driver and sensor designs.

5 Hardware Design: Drivers and Sensors

5.1 Chapter Introduction

This chapter details the design of the power transistor gate drivers and the selection of the current and voltage measurement sensors. The drivers form the interface between the power devices, discussed in the Chapter 4, and the digital controller that is discussed in the Chapter 6. The sensors are the interface by which the digital controller measures the current and voltages required by the control methodology.

The design of the IGBT and MOSFET drivers are presented separately, although the design procedure for the different devices is similar due to both types having insulated gates. The only major difference between the drivers for the IGBT's and MOSFET's is the placement of their associated power devices in the circuit. The MOSFET's are arranged in high-and-low pairs, which allow the use of a "flying-capacitor" driver arrangement. In contrast, the IGBT's are connected back-to-back in pairs that can swing up to 560 V above or below the neutral voltage. This configuration necessitates the use of isolated power supplies and gate signals to each pair.

The control system requires the battery voltage, inductor current, output voltage and mains voltage to be measured. All except the battery voltage measurement points are located on the high voltage side of transformer, and must therefore be galvanically isolated from the digital controller. Both the isolation requirements as well as the dynamic nature of the signals to be measured influence the selection of the sensors.

The layout of the IGBT and MOSFET Driver PCB's is shown Appendices A.6 and A.7 respectively.

5.2 IGBT Drivers

5.2.1 IGBT Connection

The need for controllable current flow in both directions on the high-voltage side of the converter necessitates the use of back-to-back IGBT transistors as switches. Whether the two transistors have either their collectors or emitters connected together does not influence the operation of the converter, but does have a large impact on the design of the drivers.

The two drivers must be independently switched and therefore require separate driver circuits. Each driver supplies one of the IGBT's with a positive voltage between their gate and emitter to switch them and, and then short the gate and emitter together to turn them off. Each of these drivers' ground is connected to the emitter of the corresponding transistor, and a positive power supply is required to supply them with power.

If the two emitters of the back-to-back IGBT's are connected together, the drivers share a common ground. A single power supply may therefore be used, and indeed a single integrated circuit may drive both of the transistors. Although the driver ground will still float between the maximum positive and negative emitter voltage values, the two circuits will float together, and a single isolated power supply may be provided. This greatly simplifies the design of both the IGBT driver circuit as well as the control power supply.

5.2.2 Driver Isolation

As mentioned in the section 5.2.1, the absolute voltage (with reference to earth) of the common connection of the two drivers depends on which transistor in the pair is switched on. The maximum voltages occur during reverse power flow when the batteries are charged. With the maximum battery charging voltage specified as 60 V, and the turns ratio of the transformer as $N_{PRI}/N_{SEC} = 9$, the maximum voltage that is expected is approximately 540 V. Since a centre-tapped transformer is used, the voltage at the common ground of the driver circuits will vary between -540 V to +540 V with respect to the neutral voltage. The fact that the common connection also swings to a large negative value, precludes the use of charge-pump or "flying capacitor" configurations.

It is therefore clear that the drivers need to be isolated from the control power supply and the digital controller. This isolation is discussed in detail in Chapter 6, since the digital signal isolation is performed on the DSP board.

The control power supply is also discussed in Chapter 8. It may however be mentioned here that the supply consists of a primary of a small power transformer that is fed with a half-bridge driver. The transformer then has multiple secondary windings that are used to feed each isolated driver and other supplies. The outputs of the secondary windings are square waves of approximately 50% duty cycle with an amplitude of 12 V, which are then individually rectified before being output to the individual driver boards.

5.2.3 Circuit Design

Figure 31 shows the schematic diagram of a single IGBT driver:

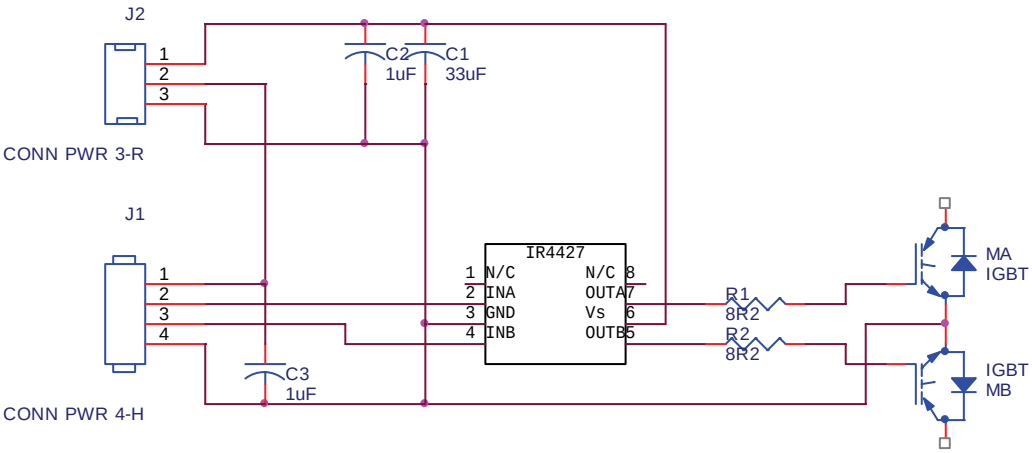

Figure 31: IGBT Driver Circuit

The circuit is designed around the IR4427 driver IC. It features two independent channels that can deliver 1.5A into and out of each transistor. Output voltages may range between 6 and 20 Volt. It features proprietary latch-immune circuitry and have matched propagation delays between channels.

5.2.3.1 Power Input

The control power supply provides 12 V gate drive and 5 V logic supplies to the driver. The power input is filtered by C1, C2 and C3, which perform both the functions of filtering and bypassing.

For the design of the capacitors it is assumed that the entire gate drive current is sourced from the bypass capacitors, which is the worst-case situation. From the datasheet it can be seen that the typical gate charge for a gate-emitter voltage of approximately 12 V is 130 nC.

To limit the capacitor voltage drop to less than 0.1% during each switch-on cycle, the required capacitance can be calculated as:

$$\begin{aligned} C &= \frac{\Delta Q}{\Delta V} \\ &= \frac{130E-9}{0.012} \\ &= 10.8uF \end{aligned} \qquad \textbf{(5-1)}$$

To compensate for any parasitic effects at high frequency, one 33 uF Tantalum and one 1 uF ceramic capacitor each have been selected.

5.2.3.2 Resistor Values

Resistors R1 and R2 limit the current into the gates to the maximum value. The output to the gate of the capacitor is approximately 12 V, if the voltage drop of the driver's output stage is neglected. Since the gate capacitor of the IGBT will be discharged when the transistor is switched off, the resistance of

the gate resistor can be calculated using the gate drive voltage and maximum driver current of 1.5 A:

$$R_{GATE} = \frac{V_{GATE}}{I_{DRIVER}} = 8\Omega \quad \textbf{(5-2)}$$

The gate resistor limits the rate at which the gate capacitor is charged and discharged. To determine the effect of the gate resistor on the switch-on and switch-off times of the transistor, the capacitance of the gate needs to be calculated.

The effective gate capacitance of the IGBT is calculated using the gate charge at 12 V.

$$C_{GATE} = \frac{Q_{GATE}}{V_{GATE}} = 10.8nF \quad \textbf{(5-3)}$$

The RC-time constant of the resistor and gate capacitor combination is given by:

$$\tau = R_{GATE}C_{GATE} = 86.4ns \quad \textbf{(5-4)}$$

Which is negligible in comparison with the switching period of 33 000 ns.

5.2.3.3 Resistor Power Dissipation

The gate resistor and gate capacitance form a first-order RC circuit. The instantaneous voltage across the resistor is given by:

$$V_R(t) = V_{SS}e^{\frac{-t}{R_{GATE}C_{GATE}}} \quad \textbf{(5-5)}$$

Where VSS is the supply voltage and it is assumed that this voltage does not change significantly during the switching operation.

The instantaneous power dissipation in the resistor is given by:

$$
\begin{aligned}
P_R(t) &= V_R(t)^2 \\
&= \left(V_{SS} e^{\frac{-t}{R_{GATE} C_{GATE}}} \right)^2 \\
&= V_{SS}^2 e^{\frac{-2t}{R_{GATE} C_{GATE}}}
\end{aligned}
\qquad \textbf{(5-6)}
$$

The energy dissipated during one switch-on of the transistor is the integral of the instantaneous power. Since the switching period is long with regards to the time constant, and the voltage across the resistor approaches zero asymptotically, the integration is taken from the time the driver output is turned on (t=0) to infinity:

$$
\begin{aligned}
E_R &= \int_0^\infty P_R(t) dt \\
&= \int_0^\infty V_{SS}^2 e^{\frac{-2t}{R_{GATE} C_{GATE}}} dt \\
&= \left. \frac{V_{SS}^2 e^{\frac{-2t}{R_{GATE} C_{GATE}}}}{\frac{-2}{R_{GATE} C_{GATE}}} \right|_0^\infty \\
&= \frac{V_{SS}^2}{\frac{2}{R_{GATE} C_{GATE}}} \\
&= 6.22 uJ
\end{aligned}
\qquad \textbf{(5-7)}
$$

Since the switch has to be both turned on and off during each switching cycle, and the switching frequency is 30 kHz, the average power dissipated by the resistor is:

$$
\begin{aligned}
P_{R,AVE} &= 2 F_S E_R \\
&= 0.375 W
\end{aligned}
\qquad \textbf{(5-8)}
$$

The closest standard resistor to the above specifications is a ½ Watt 8.2 Ohm resistor, which is selected for M1 and M2. Switch M3 turns on twice during each switch cycle, so that its gate resistor power dissipation is twice that of M1 and M2. For M3 two 15 Ohm ½ Watt resistors are used in parallel.

5.3 MOSFET Drivers

5.3.1 Circuit Design

The method used for the design of the MOSFET Low Voltage drivers is similar than that for the IGBT's, with the exception that the transistors do not share a common ground. The top driver's ground also only swings between zero and a positive value.

Although the top and bottom drivers function independently, charge pump IC's are available that combine the two drivers. This has the major advantage that the digital inputs to the top and the bottom drivers are at the same potential, so that additional isolation of the top input signal is not required. Figure 32 shows such a configuration designed around the IR2113 driver IC.

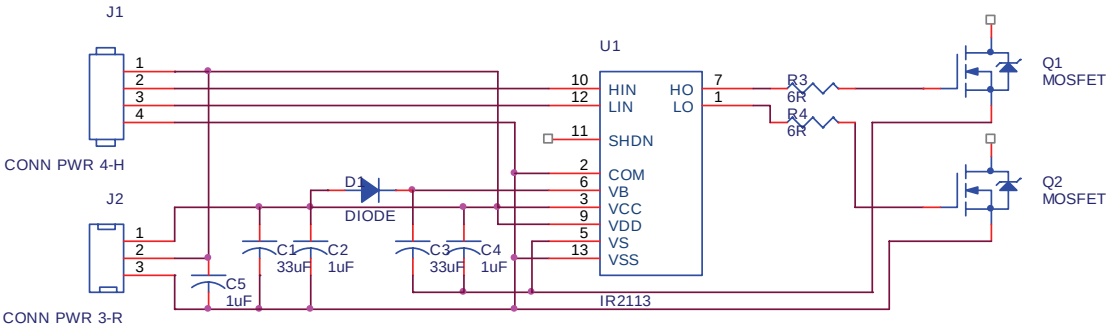

Figure 32: MOSFET Driver Circuit

The design of the bottom transistor's driver is identical to that of the IGBT's. For the top transistor, a so-called "flying capacitor" is utilised. The negative side of the flying capacitor was connected to the source of the top MOSFET, and the positive to the driver IC supply pin. The positive capacitor terminal was also connected via a diode to the bottom driver power supply. Thus, when the bottom transistor is on (and the top one off), the flying capacitor's negative terminal is at approximately 0 V, so that current flows through the diode to charge it. Once the capacitor is charged, it will provide a positive charge supply to the top driver IC with which to switch the transistor on.

The equations given in section 5.2 on IGBT driver design will be used to calculate the component values for the MOSFET drivers. The equations and derivations are not shown again.

5.3.1.1 Power Supply

The gate charge of each IRFB4710 is also approximately 130 nC. The total gate charge of the three transistors in parallel that make up a switch is 390 nC. Two 33 uF capacitors, the next standard size above three times 10.8 uF (the value calculated for the IGBT drivers, with identical transistor gate charge), are therefore used.

Since the top and bottom transistor banks are identical, the same value is also used for the charge pump capacitors.

5.3.1.2 Resistor Values

A power supply of 12 V is again used to supply the drivers. The IR2113 can supply +2 A and sink -2 A, so that a resistance of 6 Ohm is inserted between the IC and the transistor gate.

The time constant is now

$$\begin{aligned}\tau &= R_{GATE}C_{GATE} \\ &= 194.4\,ns\end{aligned} \qquad \textbf{(5-9)}$$

Which, although larger than that of the IGBT drivers, is still acceptable.

5.3.1.3 Resistor Power Dissipation

The energy dissipated during each switching on of the transistor is calculated as:

$$\begin{aligned}E_R &= \frac{V_{SS}^2}{\frac{2}{R_{GATE}C_{GATE}}} \\ &= 14\,uJ\end{aligned} \qquad \textbf{(5-10)}$$

This multiplied by the twice the switching frequency gives the power dissipated as 0.84 Watt. Two 12 Ohm, ½ Watt resistors are placed in parallel to dissipate this power.

5.4 Sensor Design

The control methodologies that are described in Chapter 7 require the following physical parameters to be measured:

- Battery Voltage (Range 0 – 60 V)
- Output Voltage (Range 0 – 400 V)
- Inductor Current (Range -20 – +20 A)
- Mains Supply Voltage (future implementation) (Range -400 - +400 V)

The inductor current and output and mains voltages are all measured on the high voltage side of the transformer and therefore require isolation. Thus, only transducers that incorporate signal isolation have been considered.

Sensors that utilise the Hall Effect to measure DC and AC electrical parameters have seen widespread use in power electronic designs and in industry. They do not suffer from many of the limitations of signal transformers, and were therefore selected.

5.4.1 Current Transducer Selection

The calculated current range of the inductor, as well as the maximum rate at which current can change within the inductor, determines the selection of the current transducer. Since the current in the inductor does not have large discontinuities, the reaction and response times of the current transducer is less important than the tracking accuracy.

The maximum rate of change possible in the inductor will occur if switch M3 is conducting, thereby applying the full output voltage over the inductor. It was calculated that the inductor current would average at a maximum of approx 6.15 A during forward operation, and that the current ripple amplitude would be 10%, or 0.615 A. It was also calculated that the time M3 is on during steady state operation is 3.33 us. Thus, the maximum rate of current change the sensor should track is di/dt = 0.18 A/us

The sensor should additionally have an accuracy that is at least that of the DSP. The DSP Analogue to Digital Converter accuracy (non-linearity) is given as +- 2 LSB (Least Significant Bits), or the value +-3. Since the resolution of the DSP ADC is 1024, this equates to approximately 0.3%.

The LAH 25-NP manufacture by LEM was selected to measure the inductor current. This sensor is a closed-loop Hall-Effect device that has a current range of +-25 A. It has a dynamic response of 200 A/us, which compares very favourably with the maximum circuit value calculated above of di/dt = 0.18 A/us. It is accurate to approx +-0.3%, which is almost exactly equivalent to the accuracy of the DSP ADC.

Since the dynamic response (di/dt) of the sensor is almost 1000 times the maximum expected current change rate, the propagation delay of the sensor has been neglected.

5.4.2 Voltage Transducer Selection

Since the voltage transducers are both connected to capacitors, their dynamic response can be slow. For a 250 VAC output the maximum value of the derivative of the 50 Hz output is 0.102 V/us.

The LV 25-P sensor from LEM was selected. The sensor uses a user-supplied resistor to generate a current that is proportional to the voltage to be measured, which is then measured via a Hall-effect sensor. The resistor must be selected so that the current through the sensor primary is 10mA when nominal voltage is applied to the resistor. This arrangement ensures that the sensor attains galvanic isolation, and can be used for wide voltage ranges. For approximately 10mA output at maximum 500 V input, a 47 kOhm, 5 W resistor is used for the measurement.

The accuracy of this sensor is slightly less than the current sensor and the DSP at approximately 0.8%, but it is still acceptable for this application.

5.4.3 Sensor Interfacing

Both the voltage and current sensors are supplied with +12 V and -12 V. This enables them to measure both positive and negative parameters. The sensors have to be supplied with bipolar supplies, even if only positive values are measured.

The sensor power supplies have to be tied to the DSP power supply. More specifically, the sensors and the DSP analogue must share a common ground that is free from interference in order to perform accurately and ensure galvanic isolation from the power circuits.

The outputs of the sensors are currents that are proportional to the current through the primary of the sensor. These currents are then passed through a resistor in order to generate a voltage that can be measured by the DSP ADC's.

The designs of the interfacing amplifiers to the DSP are discussed in Chapter 6.

5.5 Chapter Conclusion

This chapter detailed the design of the MOSFET and IGBT drivers, as well as the current and voltage measurement sensors. For the drivers, the selection of driver IC's as well as the circuit design was described.

For the sensors, the selections of the sensors were described in terms of the dynamic nature of the current and voltage signals that are to be measured.

The drivers and sensors form the interface between the power section that was described in Chapter 4 and the digital controller. The design of the digital controller is discussed in Chapter 6.

6 Hardware Design: Digital Controller and Power Supply

6.1 Chapter Introduction

The converter control system consists of two Printed Circuit Boards, namely the control power supply and the digital controller board. Since the operation of these two boards is closely linked, they are both discussed in this chapter.

The control power supply sources control power from either the mains grid or the batteries, and convert this to isolated power suitable for distribution to the DSP and driver boards.

The controller board is based on a Digital Signal Processor that performs all control functions in the system. It measures and scales the required circuit parameters by means of transducers and an analogue to digital converter, determines which mode the converter should operate in, determines the switching states of all power transistors, calculates the duty cycles of actively switched transistors, and outputs the Pulse Width Modulated switching signals to the transistor drivers. In addition to the DSP, several Integrated Circuits are included in the controller board in order to provide isolation and signal conditioning functions.

The diagram of Figure 33 shows the complete control system layout, including control power distribution and signal interconnections.

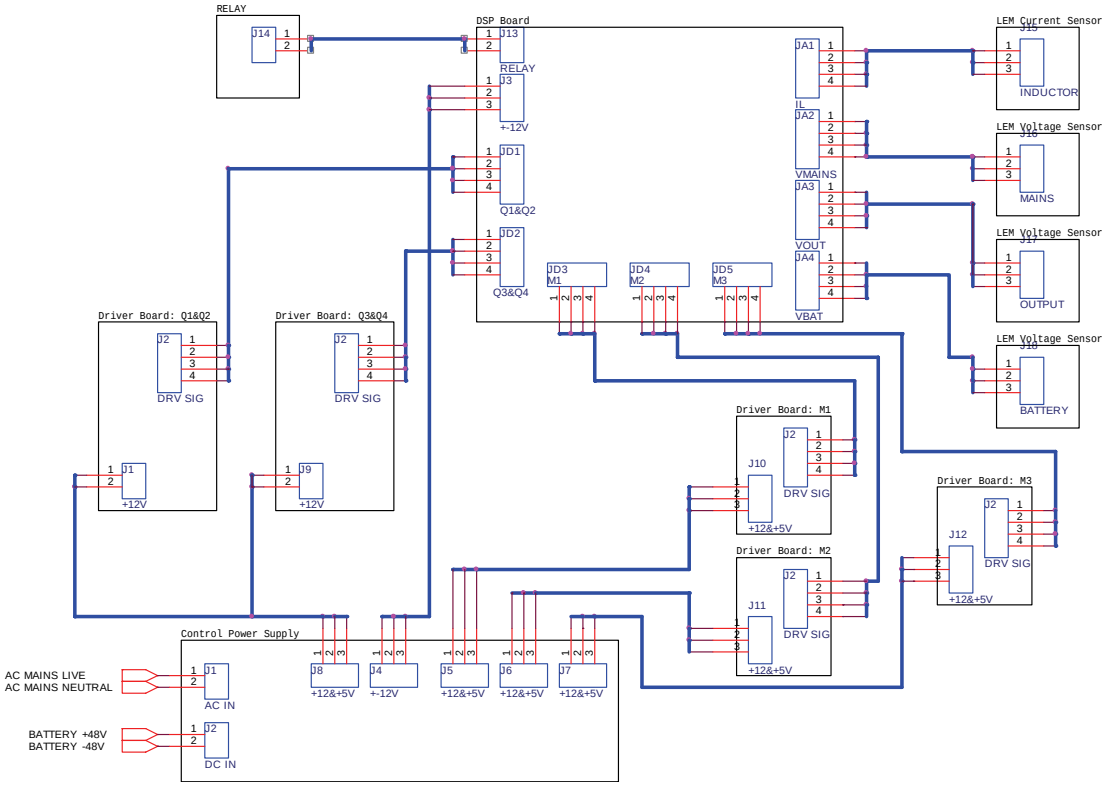

Figure 33: Control System Layout

The full schematic and PCB layout of the control power supply board is given as Appendices A.8 and A.9 respectively.

The design of the power supply shall be discussed first, followed by that of the DSP controller.

6.2 Control Power Supply Design

The design of the control power supply is a switching-mode converter design in its own right. Much of the work that has been discussed in previous chapters this report for the main bi-directional converter was also performed for the control power supply. The detail component and control design of this power supply is therefore not given here. Only the topology, operation and interface with the components of the main bi-directional converter are discussed. The author has drawn heavily on designs personally done on previous occasions for the design of this supply.

Figure 34 shows the power section of the control power supply. Drivers and control components are not shown.

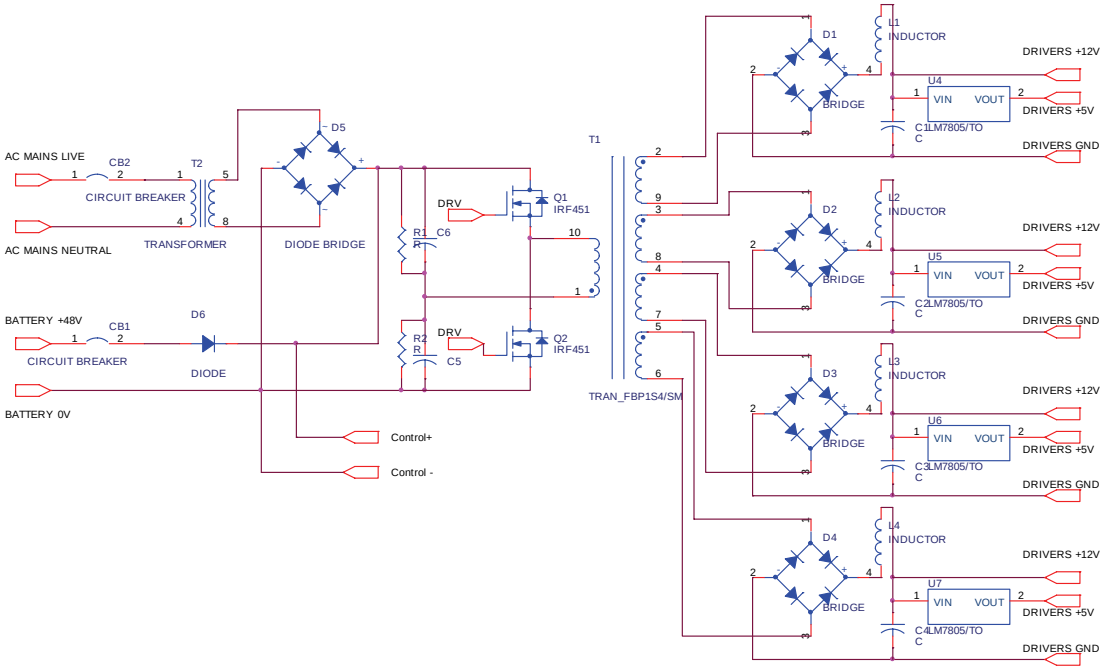

Figure 34: Control Power Supply Schematic

Note that only the 4 driver secondary windings, rectifiers and filters are shown. There is an additional +12 V & -12 V output that is not shown, due to limitations on the number of components a schematic may contain with the CAD software used.

6.2.1 Sourcing of Control Power

It is desirable that the converter control system is able to operate from both the batteries and the mains supply. This greatly increases the usefulness of the converter, since it can operate when any power source is available.

An typical example of when the converter is required to operate from mains supply alone is when flat storage batteries are to be charged. Similarly, when user equipment is to be operated without mains supply the converter has to operate from battery supply alone.

Since the batteries as well as the AC mains must act as power sources, there must be a single point where they can both feed power into the control voltage regulator. To minimise transients and the possibility of short periods without power, the two input capacitors of the half bridge converter is used to act as a buffer between the two supplies and the control voltage regulator. To keep the design of the circuit as simple as possible, the nominal voltage of the series capacitor combination is chosen the same as that of the batteries. This voltage is unregulated, and can have large variations in value (approx 36-60 V).

Since the battery voltage will always be lower than the SELV limit of 120 VDC, there is no safety requirement for the control circuits be galvanically isolated from the battery supply. A single diode with over current protection will suffice as connection from the batteries to the series capacitors. This diode will prevent the possibility of current flowing to the batteries from the AC mains through the control circuit.

The AC mains must however be isolated. This is most easily done via a small mains-frequency isolation transformer followed by a diode rectifier bridge. The rectifier bridge itself will prevent any reverse DC current flow into the transformer when operating from the batteries. Over current protection in the form of a thermal circuit breaker is again included to protect the system in case a fault occurs in the transformer or control circuit.

If the two circuit breakers in the schematic of Figure 34 are connected as a single double-pole circuit breaker, it may be used as a convenient position for switching the converter on and off.

6.2.2 Control Power Voltage Regulation and Distribution

The following devices require separate supplies from the control power supply:

Sink	Voltage (V)	Current (A)	Isolation from Batteries
MOSFET Drivers Q1-Q4	+12 & +5	0.2	No
IGBT Driver M1	+12 & +5	0.2	Yes
IGBT Driver M2	+12 & +5	0.2	Yes
IGBT Driver M3	+12 & +5	0.2	Yes
DSP, Digital & Analogue I/O Supply	+12 & -12	2 & 0.2	No

The output voltage of 12 V for each sink was selected primarily since it is compatible with both the measurement transducers that are used, as well as the transistor drivers. The 5 V output is provided to drive the driver side of the signal isolators, since these have an absolute maximum supply voltage of 7 V. The voltage and current sensors require both positive and negative supplies, hence the +-12 V. The input voltage can be in the range of approximately 36 – 60 VDC, which implies that the output voltages must be regulated.

The simplest method to construct such a power supply with multiple outputs is to use a single transformer with several secondary windings, some of which may be isolated (Mohan et al, 1995: 304). Since the winding turn counts are fixed, it is however not possible to regulate all of the outputs simultaneously by switching means. The output that is the most voltage sensitive is therefore chosen to be regulated.

In the present design the DSP supply voltage is actively regulated by the switching regulator. Since the driver circuits are not sensitive to voltage variations, small variations in their supply voltages due to winding resistance and other factors is accepted. It is not expected that the duty cycle will fluctuate considerably during operation of the power supply, other than with a change in input voltage. This was confirmed during the testing of the control power supply.

In order to prevent saturation of the transformer core, a half-bridge topology was selected. Since there are 6 windings in total (1 primary and 5 secondary windings), the amount of copper on the core should be kept to a minimum, thereby implying the use of full-bridge rectifiers on the secondary windings.

The output of each rectifier voltage is filtered using an inductor and capacitor (as for a step-down converter), and distributed to the points of consumption via cables.

The secondary windings that supply the driver boards have a 5 V linear regulator to supply the signal isolators. This voltage is conducted via the driver boards to the DSP board, in order to drive the driver-sides of the digital isolators.

6.2.3 Control Power Consumption

Four of the outputs from the control power supply are used to supply the transistor drivers with power. From the datasheets it can be seen that the total quiescent current consumption of the driver IC’s is less than 1mA. It is therefore assumed that the current consumption of the driver circuit consists only of the charging of the power transistor gates. It is also assumed that the driver IC uses supply power to charge the gate capacitors, and discharges them by shorting the gate and source / emitter of the transistors.

As mentioned in sections 5.2 and 5.3 on driver design, the gate charge of both the MOSFET’s and IGBT’s is approximately 130 nC. To calculate the average supply current for each driver, the gate charge is therefore multiplied by the

number of times the transistor is switched on and the number of gates in parallel. If it assumed that in the worst case every transistor is switched on during every switching cycle, the MOSFET driver should draw approximately 31 mA, and the IGBT's drivers approximately 8 mA for M1 and M2, and 16 mA for M3.

With this in mind, the control power supply is designed to deliver 200 mA from each of its first four secondary windings.

For the DSP board, the maximum current consumption of all the IC's and sensors is totalled, which equates to approximately 400 mA. The DSP supply is designed to supply 2 A.

6.2.4 Control Power Supply Control

Since the function of the control power supply is to supply the DSP board and drivers with a constant voltage, simple voltage mode control is utilised to regulate the output.

The control is based upon the LM3524 IC, and uses an IR2113 driver to switch the MOSFET's. The schematic of Figure 35 shows the design of the control system:

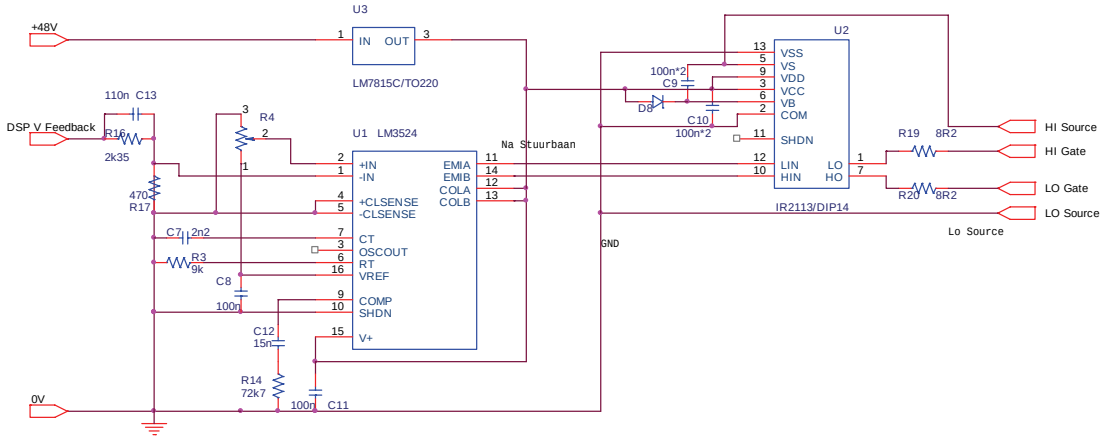

Figure 35: Control Power Supply Control

The LM3524 senses the DSP board output voltage and adjusts the output duty cycle as required. Compensation is performed by the external compensation networks.

The IR2113 implementation is almost identical to that of the MOSFET drivers of the bi-directional converter.

6.3 DSP Board Design

The schematic and PCB layout of the control board are shown in Appendices A.10 and A.11 respectively. The control board was designed around the

TMS320LF2403A DSP. The design of each of the sub-systems on the control board will be discussed in this section.

6.3.1 Microprocessor Selection

The control methodologies devised, together with the topology of the converter, determine the requirements for the microprocessor I/O count, speed of execution, etc. From the chapters on control and the topology discussion, the following set of minimum requirements can be set for the microprocessor system:

6.3.1.1 Analogue to Digital Conversion (ADC)

The following analogue measurements are required:

- Battery Voltage
- HV Output Voltage
- Inductor Current
- Mains Supply Voltage (AC Output Converter Only)

During simulation it was found that the command value is to be updated at the same period as the switching period, which therefore requires a maximum ADC conversion rate of 30 kHz.

To ensure accurate tracking, the resolution of the ADC should be as high as possible. There is however no reason for having a resolution that is higher than the accuracy of the current and voltage sensors. The most accurate sensor that has been selected is the LEM LAH 100-P current transducer, which has a specified accuracy of 0.25%. The error of this transducer is thus 1 part in 400. If it is required that the ADC discretization error is to be less than the transducer accuracy, a resolution of 9 bits (512 values) is sufficient.

6.3.1.2 Digital I/O

The following digital output signals are required:

- Gate drive pair Q1-Q4
- Gate drive pair Q2-Q3
- Gate drive M1a
- Gate drive M1b
- Gate drive M2a
- Gate drive M2b
- Gate drive M3a
- Gate drive M3b
- Mains Contactor (future implementation)
- Power supply indication LED
- Mode indication LED
- Fault Indication LED

If it is required that the rise time of the digital outputs should be less than 1% of the switching period, the required rise time is 0.3 us.

6.3.1.3 General Considerations

The design of the digital control board can be greatly simplified if a Digital Signal Processor (DSP) is used instead of a traditional microprocessor. DSP's typically have on-chip analogue-to-digital converters, as well as capture inputs, PWM outputs, etc. It is possible to implement the entire control system of this design on a single DSP chip.

The TMS320C24XX family of DSP's is optimised for power control systems. They are therefore well suited to this application. Based on the requirements above, the TMS320LF2403A DSP was selected. It is the smallest DSP to satisfy all I/O requirements and it exceeds the performance specifications.

6.3.2 Voltage Regulators

The control power supply supplies the DSP board with +12 V and -12 V supplies. As discussed below, it has been decided to keep the analogue and digital supplies separate by using individual linear regulators. They are however fed from the same 12 V source and share a common ground, and are therefore not electrically isolated from each other.

The internal logic and analogue circuits of the DSP operate at 3.3 V. According to the DSP datasheet, the power dissipated by the DSP and the peripherals is negligible, integrated circuit linear regulators are used to reduce the voltage to 3.3 V. An additional 5 V linear regulator is used to power the analogue input operational amplifiers, since the output of the selected amplifiers (LM358N) can only swing up to $V_{SUPPLY} - 1.5$ V.

Since the analogue circuits are extremely vulnerable to switching transients caused by the digital IO's, it was decided that the digital and analogue linear supplies shall be kept completely separate. There shall be only one point of interconnection between the analogue and digital circuit grounds, and this connection is made at the voltage regulators. This ensures that the analogue supply voltage will be free of switching spikes caused by digital logic operation.

The two analogue power supplies (3.3 V & 5 V) are both connected to the analogue ground net. The 3.3 V regulator supplies both the DSP ADC supply and reference voltages, while the 5 V regulator supplies the input operational amplifiers. The supplies are bypassed with suitable capacitors in close proximity to the DSP and the analogue IC's.

6.3.3 Digital I/O Design

6.3.3.1 Isolation Requirements

The major consideration in the design of digital I/O circuits is the decision of if, how and where the DSP signals and grounds need to be isolated or connected. In many designs, including the (TMS320C24x Reference Design Schematic), the decision is made to connect the digital ground directly to the power circuit ground. Although this method is simple and low cost, it has several disadvantages, of which the most important are:

- The large switching transients in the power circuit may cause voltage spikes of several volts, resulting in erroneous operation of and even damage to the DSP.
- Galvanic isolation between the high and low voltage circuits of the converter is not possible.

The second point is of great importance if the control circuit are to be fed from the low voltage side of the converter. If the high and low voltage sides are not galvanically isolated, the low voltage side may not be treated as a Safety Extra Low Voltage (SELV) system.

6.3.3.2 Methods of Isolation

Although several methods of isolation exist, the most common is that of providing isolation between the digital controller and the power transistor drive circuits.

This method has the advantage that only low-power binary signals need be transmitted, which is accomplished by the widespread use of devices like opto-couplers. The entire control system is then isolated from the high voltage potential, providing that devices measuring high-voltage parameters are also isolated.

Most of the commonly used opto-couplers have the drawback that their input current is more than what the DSP outputs can supply. The iCoupler family of isolators from Analogue Devices are however much more suited for direct connection to a TMS320 DSP. Specifically, the ADuM 140X range has input current of only +-10uA.

6.3.3.3 Isolation Implementation

If it were assumed that the PWM outputs of the DSP could provide 128 discrete pulse widths at 30kHz, the minimum pulse width would be

$$t_{\min} = \frac{1}{128 f_s} = 260ns \qquad \textbf{(6-1)}$$

The ADuM 140XARW (the slowest specification variant) has a propagation delay of max 100 ns and a pulse width distortion (i.e. the magnitude of the difference between the on and off propagation delays) of max 40 ns. Thus, the distortion of the pulse outputs would be approximately 15% at the lowest possible output (0.78%) and only 1.2% at 10% output. None of the inputs in the design has very short pulse widths. Based on these considerations, the ADuM140X family has been selected to isolate the digital I/O channels.

Only channels that are connected to the HV side of the converter require isolation in the interest of safety. However, even on the low voltage side transients can occur which may damage the DSP. Isolation IC's are much

more capable of handling these transients. The ADuM140X, for example, is capable of withstanding 560 VAC across the isolation barrier for a minimum lifetime period of 50 years.

In the interest of reliability, it has therefore been decided that all digital channels to and from the DSP be isolated. The only connection then between the DSP and outside voltages is through the voltage regulator (which is well filtered) and the analogue amplifiers (which are connected to isolated sensors).

6.3.3.4 Further Safety Considerations

In addition to isolation, a further safety concern can be identified with the digital outputs that are connected to power devices. Particular attention must be given to these outputs since they might be inadvertently activated during a processor error condition or during power up (perhaps before their function is set in the software initialization routine). This may lead to the possibility of dead short circuits (e.g. if both transistors in an arm of a bridge switch on) and other dangerous conditions.

The PWM outputs of the TMS320LF240X family all have internal pull-ups. Thus, inadvertent operation of the power devices will result if the PWM outputs are placed in their high impedance state.

To overcome this problem, pull-down resistors are used to ensure that all DSP outputs that are not actively switched high, is held in the low condition. The typical pull-up current value for PWM outputs is 16 uA. The reference schematics show typical external pull-down values of 10 kOhm, which results in a pull-down current of 330uA, which is more than adequate. The value of 10 kOhm was also chosen for the present design.

6.3.4 Analogue I/O Design

6.3.4.1 Isolation Considerations

As with digital I/O, analogue signals are susceptible to transients from switching. In fact, the low voltage analogue signals and measurements are much more affected by than their digital counterparts that have the same range (0 - 3.3 V), but can have only two possible values. For this reason, the analogue and digital circuits are powered by separate supplies, as previously discussed.

Since the analogue signals have to be isolated from the circuits they measure, transducers were selected that provide electrical isolation.

6.3.4.2 Buffering & Signal Conditioning

All analogue inputs of the DSP are first buffered through operational amplifiers. There are several reasons for this:

- Even though the transducers are isolated, transients could still occur on the signal cables that may damage the DSP.

- The voltage levels of the transducer outputs are usually not directly compatible with the DSP analogue inputs. Amplification or attenuation of the signal is therefore invariably required.
- Transducers may use one conductor and ground for the signal output, or differential signals. Both of these must be interfaced to the DSP.
- Transducers may have a current as an output, which then has to be converted to a voltage for measurement by the DSP.
- Transducers may provide either bi-polar or uni-polar outputs, while the DSP measures only positive values. In the case of bi-polar outputs, voltage translation is required.

It has been decided that the board will contain 4 differential and 4 absolute amplifiers. The amplifiers have the following features:

- All support either amplification or attenuation of signals.
- Provide an input signal filter, if required.
- Be able to measure voltages and currents.
- Shall be non-inverting.
- The differential amplifiers support the measurement of bipolar signals. That is, they will support voltage translation.

6.3.4.3 Absolute Amplifiers

The schematic of an absolute amplifier is shown in Figure 36.

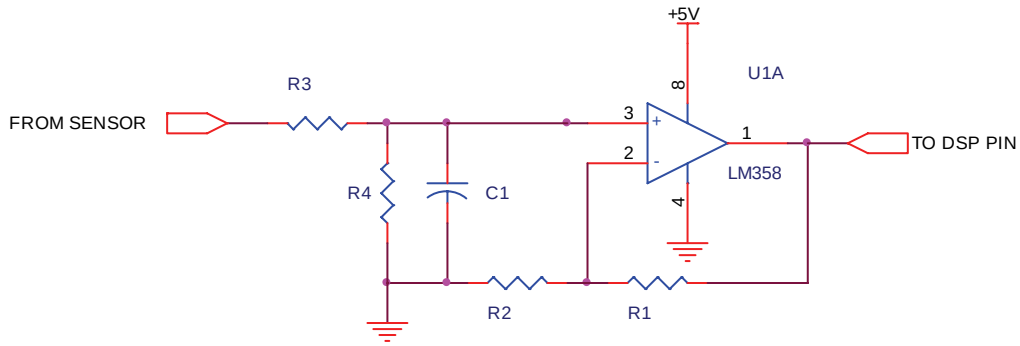

Figure 36: Absolute Amplifier

This amplifier is designed around one channel of a LM358 operational amplifier.

R3 and R4 form a series voltage divider. With these two resistors, the input signal can be attenuated by almost any factor. The attenuation factor is given by $A_{ATT}=R_4/(R_3+R_4)$. If required, C1 can be inserted to form a first order RC filter together with R_3 and R_4.

If a current is to be measured, R_3 can be replaced by a jumper. The current will then be converted to a voltage by R_4. Since the signal is connected directly to the op-amp non-inverting input, the input resistance of the amplifier is determined by R_3 and R_4 alone.

R_1 and R_2 form a feedback network. The fraction $R_2/(R_1+R_2)$ of the output voltage is fed back to the inverting input of the op-amp, so that the gain is given by $A_{AMP}= (R_1+R_2)/R_2$.

As can be seen, there is no direct current path between the input and the output, thereby providing effective signal buffering between the sensor and the DSP.

6.3.4.4 Differential Amplifiers

The schematic of a differential amplifier is shown in Figure 37:

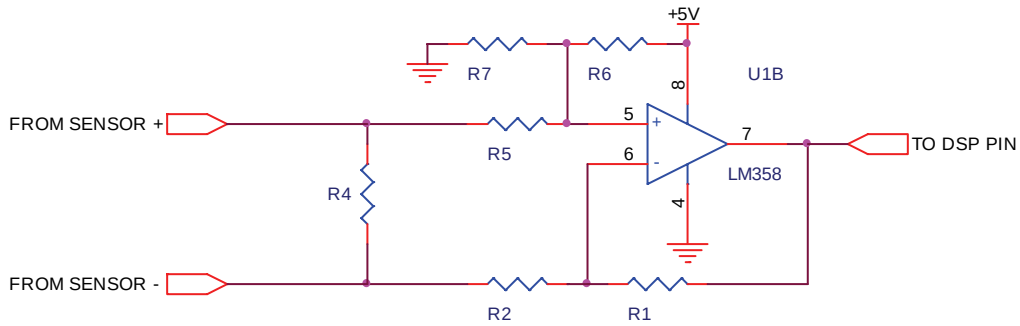

Figure 37: Differential Amplifier

This amplifier design is based on the sensor interface amplifier given in (Choudhury, 1999: 23). The amplifiers given in (Choudhury, 1999: 23) however have two major drawbacks, they are inverting and they need another negative power supply. The amplifier of Figure 37 has been designed to overcome these drawbacks, and is as far as can be ascertained is unique.

R_1, R_2 and R_4 fulfil the same functions as for the absolute amplifier, with the exception that R_4 is only intended for conversion of currents to voltages. R_3 is not required, since it will be shown that the amplifier can both amplify and attenuate signals.

In the calculations below, R_4 will be ignored. This can only be done if R_4 has a much lower value than the remaining resistors. Typical sensor output currents are in the range of 20 mA, which have to be converted to voltages in the 1.7V range. Thus a value for R_4 of 80 Ohm should be typical. The remaining resistors should have values in the 10 kOhm range.

Resistors R5, R6 and R7 form a network that adds an offset to the input voltage. This is done so that negative signals may be measured. For signals that swing symmetrically across the analogue ground, this offset must be 3.33/2 = 1.665 V.

The gain of the amplifier of Figure 37 is calculated as follows (ignoring R4):

Assume V_{SP} is the positive sensor voltage, V_{CC} the analogue supply voltage and V_+ the non-inverting op-amp input. Taking the sum of the currents entering the non-inverting terminal of the op-amp (terminal 5):

$$\frac{V_{SP}-V_+}{R_5}+\frac{V_{CC}-V_+}{R_6}=\frac{V_+}{R_7}$$
$$R_6R_7V_{SP}+R_5R_7V_{CC}=V_+\left(R_5R_6+R_6R_7+R_5R_7\right) \qquad \textbf{(6-2)}$$
$$V_+=\frac{R_6R_7V_{SP}+R_5R_7V_{CC}}{R_5R_6+R_6R_7+R_5R_7}$$

If the same is done for the inverting input:

$$\frac{V_{OUT}-V_-}{R_1}=\frac{V_--V_{SN}}{R_2}$$
$$V_{OUT}R_2-V_-R_2=V_-R_1-V_{SN}R_1 \qquad \textbf{(6-3)}$$
$$V_-R_1+V_-R_2=V_{OUT}R_2+V_{SN}R_1$$
$$V_-=\frac{V_{OUT}R_2+V_{SN}R_1}{R_1+R_2}$$

For an ideal op-amp, V_+ and V_- will be equal. Equating 6-2 and 6-3 yields:

$$\frac{V_{OUT}R_2+V_{SN}R_1}{R_1+R_2}=\frac{R_6R_7V_{SP}+R_5R_7V_{CC}}{R_5R_6+R_6R_7+R_5R_7}$$
$$V_{OUT}=\frac{R_6R_7V_{SP}+R_5R_7V_{CC}}{R_5R_6+R_6R_7+R_5R_7}\frac{\left(R_1+R_2\right)}{R_2}-\frac{V_{SN}R_1}{R_2} \qquad \textbf{(6-4)}$$
$$V_{OUT}=\frac{R_6V_{SP}+R_5V_{CC}}{R_6+\frac{R_5R_6}{R_7}+R_5}\frac{\left(R_1+R_2\right)}{R_2}-\frac{V_{SN}R_1}{R_2}$$
$$V_{OUT}=\frac{\left(R_1+R_2\right)}{R_6+\frac{R_5R_6}{R_7}+R_5}\frac{R_6V_{SP}+R_5V_{CC}}{R_2}-\frac{V_{SN}R_1}{R_2}$$

In the second last step, the first term has been divided by R_7/R_7. This was done so that V_{SP} and V_{CC} can have factors that are uniquely determined by a single resistor value, and will allow them to be independently chosen. This is the core principle driving this particular op-amp design.

If now the first factor of Equation 6-4 can be made equal to one, the resulting equation will be:

$$V_{OUT}=\frac{R_6V_{SP}+R_5V_{CC}}{R_2}-\frac{R_1V_{SN}}{R_2} \qquad \textbf{(6-5)}$$
$$=\frac{R_6V_{SP}}{R_2}+\frac{R_5V_{CC}}{R_2}-\frac{R_1V_{SN}}{R_2}$$

If R_6 is further chosen as the same value as R_1:

$$\begin{aligned} V_{OUT} &= \frac{R_1 V_{SP}}{R_2} - \frac{R_1 V_{SN}}{R_2} + \frac{R_5 V_{CC}}{R_2} \\ &= \frac{R_1 V_{DIFF}}{R_2} + \frac{R_5 V_{CC}}{R_2} \end{aligned} \qquad \textbf{(6-6)}$$

This is the desired amplifier gain equation. Equation 6-6 shows that the output is equal to the amplified difference between the input signals, plus a scaled value of the power supply voltage. The amplifier therefore performs both amplification and voltage translation functions, without inverting the output and without requiring an additional supply. Note that the input signal can be both amplified and attenuated, depending on whether R_1 is larger or smaller than R_2.

As mentioned above, for Equation 6-6 to hold, the following must be true (keeping in mind R_6=R_1):

$$\begin{aligned} \frac{(R_1 + R_2)}{R_6 + \frac{R_5 R_6}{R_7} + R_5} &= 1 \\ R_1 + R_2 &= R_6 + \tfrac{R_5 R_6}{R_7} + R_5 \\ \tfrac{R_1 R_5}{R_7} &= R_2 - R_5 \\ R_7 &= \frac{R_1 R_5}{R_2 - R_5} \end{aligned} \qquad \textbf{(6-7)}$$

Note that Equation 6-7 tends to infinity as R_5 approaches R_2's value. This is intuitively correct, since R_2 = R_5 would imply that the full supply voltage would be added (from the amplification equation), and that R_7 would then be an open circuit (infinite resistance). This situation would however never occur in practice, since the amplifier output would then be at the maximum output value continuously.

The design of implementations of this amplifier thus proceeds as follows:

- R_4 is chosen, if required, to convert the sensor's current signal to a voltage.
- The ratio of R_1/R_2 is then chosen to satisfy the amplification requirements, while the actual values are chosen to satisfy input resistance requirements.
- R_5 is chosen to add the required offset to the output.
- R_6 is chosen equal to R_1.
- R_7 is calculated with Equation 6-7.

6.3.4.5 Component Values

The three differential amplifiers utilised in the present design are all connected to LEM sensors (two voltage and one current sensor). All of these sensors have a secondary output current of +-25 mA. For a maximum voltage at the amplifier input of 1.65 V, R_4 = 66 Ohm. The closest standard value is 68 Ohm.

R_1 is chosen to equal to R_2 as 10 kOhm. This is a 150 times the value of R_4, so that the input resistance of the amplifier may be neglected. The amplifiers will therefore have gains of one.

If an offset value of 1.65 is to be added to the input signal, R_5 should have a value of R_5 = 1.65V*10k/5V = 3.3 kOhm.

With the formula given, R_7 is calculated as 5 kOhm.

6.3.5 DSP Board Layout

The DSP board has been designed on the standard 100x160mm Eurocard format. The size is the smallest area in which the layout could be fitted, and coincides with the maximum area allowed by the standard EAGLE Layout editor.

To minimise the effects of induction, all tracks conducting digital signals were kept to the minimum length. It was however also a requirement to keep the analogue and digital signals physically separated, so that a compromise between length and separation was required. The board layout shows the digital signals to the left of the board, while all analogue signals were kept to the right.

As far as possible, all signals traces were kept on the top layer, and power supply traces on the bottom layer. Due to the layout of the DSP pins, this was however not always possible. Some signals must be routed to headers, which require them to pass with via's down to the bottom layer, before routing to the header pins.

Since the board is a prototype, it has been designed to be hand-soldered. Maximum use was therefore made of through-hole components. However, the DSP and the isolators are not available in through-hole packages. These were attached to the PCB by very carefully hand soldering the pins and subsequent removal of excess solder with the aid of solder wick.

Dual op-amps were chosen for the analogue amplifiers to increase component density, but without unnecessarily increasing the complexity of the board layout. The original layout was designed with quad op-amps, but was later changed to dual op-amps due to the layout complexity.

Jumpers were added to all the isolators, so that every isolator could either be powered by the board or field device it was connected to (as in the case of the drivers), or it can be powered by the internal I/O and communication power supply (as in the case of indication LED's that require no isolation).

A single point of connection is supplied between the digital and analogue grounds, as discussed previously. This was done through a jumper, firstly to make the connection obvious, but secondly also to enable the digital and analogue grounds to have different net names in the CAD layout software. This greatly simplified the layout of the respective grounds.

6.4 Chapter Conclusion

The design of both the control power supply as well as the digital controller board were discussed in this chapter.

The control power supply was designed to provide 5 isolated supplies to the driver boards and the controller board. This was achieved by using a single half-bridge driver to drive a transformer with 5 secondary windings. Only the output to the DSP board was actively regulated, since the driver boards are not voltage sensitive.

The digital controller board is designed around a DSP that implements all functions required to control the proposed converter. The only external elements required were digital isolators and analogue amplifiers.

An analogue amplifier circuit was developed for the DSP board that both scales and adds an offset to the analogue signals from the sensors.

This chapter concluded the hardware design section of this thesis. Chapters 7-9 discuss the development of the control methodologies, the DSP software as well as the converter simulation.

7 Converter Control Methodology and Compensation Equations

7.1 Chapter Introduction

The primary goal of this chapter is to determine the compensation difference equations that the digital controller of Chapter 6 has to apply in order to control the proposed converter. A secondary goal is to describe the method that was developed for determining the transfer functions of switch-mode converters through inspection.

Sections 7.2 to 7.4 of this chapter describe the design of the compensation equations. When the proposed converter is supplying power to user equipment, the converter output voltage must be a regulated sine wave of fixed amplitude and frequency. The output current must be adjusted so that this voltage reference is accurately tracked.

The literature study of Chapter 2 showed that bi-directional converters require current mode control for at least some of their operating modes. The current mode control literature sources discussed the advantages of the Average Current Mode Control (ACMC) method, and its suitability for the proposed converter was mentioned.

With the above considerations in mind, it was decided that the proposed converter would always be controlled by an inner current loop and an outer voltage loop. The inner current mode loop will use a modified version of the ACMC method.

Section 7.5 of this chapter describe the method for determining transfer functions. The calculation of the transfer functions of the loops is a lengthy and complicated procedure. However, no mention is made in the references of Chapter 2 to the calculation of the functions. This led the author to develop a method whereby the transfer functions of switch mode converter may be obtained by inspection alone.

In order to provide continuity with Chapters 6 and 8, the design of the control loops are discussed first without consideration how the transfer functions are calculated. Once both the current and voltage loops have been compensated, the developed method for determining the transfer functions is described.

7.2 Control Loop Design Methodology

7.2.1 Voltage and Current Control Loops

It is mentioned in Section 7.1 that the proposed converter is controlled by an inert current control loop and an outer voltage control loop. Average current mode control is used for the inner loop.

Figure 38 shows this arrangement for the converter operating in the reverse mode. Note that the equivalent circuit is shown for the converter in reverse mode, as described in section 7.2.3.

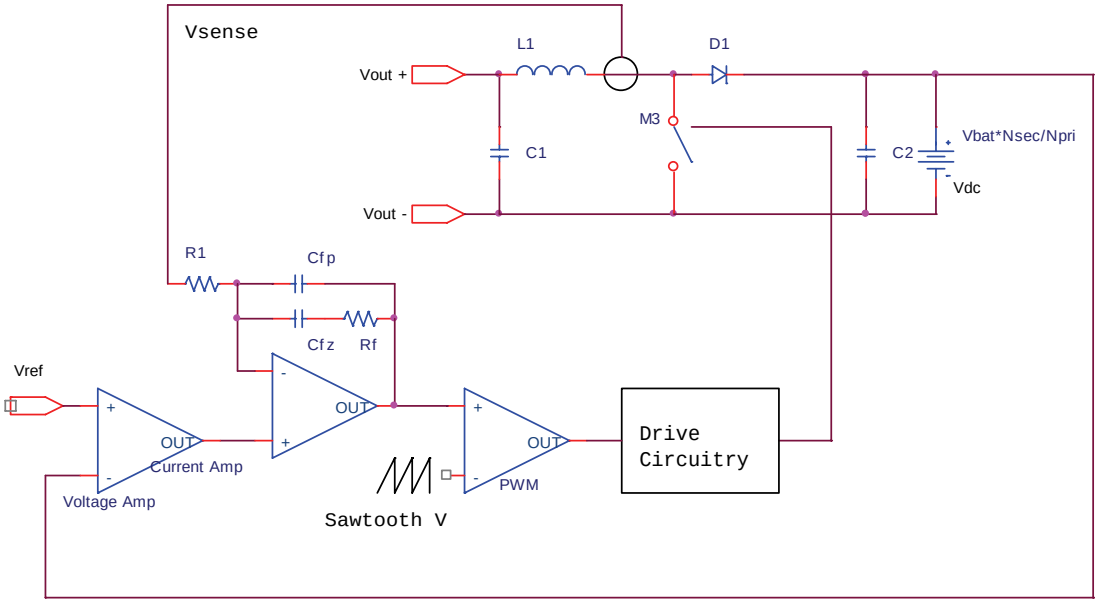

Figure 38: Voltage and Current Control Loops

Figure 38 shows the control loops in terms of analogue components. The entire control loop design procedure is performed using continuous transfer functions and analogue components. Only in the very last step is the final compensation transfer function digitized into a difference equation.

When the converter is supplying power to the user load, the command value for the external voltage loop will be the reference sinusoid. The digital controller will calculate this sinusoidal reference using its internal clock and a lookup table. In Figure 38 this reference is applied to terminal V_{ref}.

The voltage amplifier will calculate the voltage error, which is the difference between the reference and actual voltages. This error signal is compensated by the voltage loop compensator (not shown in Figure 38). The voltage error is fed to the current amplifier as a current reference.

The current amplifier determines the current error, which is the difference between the current reference and the actual current. This error signal is compensated by the current loop compensator, which is shown as an RC-network in Figure 38.

The output of the current amplifier is compared with a saw-tooth or triangle waveform to determine the actual switch duty cycle. The switch duty cycle directly determines the increase or decrease of the inductor current.

The overall function of the current and voltage loops is therefore to ensure that the output voltage tracks the reference voltage accurately.

7.2.2 Control Loop Design Procedure

Experience has shown that the design of a control loop for a switch-mode converter always consist of the following steps:

- Simplification of the power circuit into a basic equivalent circuit.
- Calculation of the small-signal transfer function of the equivalent circuit.
- Identification of additional loop gains (e.g. measurement and output gains).
- Plotting the open-loop frequency response of the system on a Bode plot.
- Application of the frequency response method to design a compensator to shape the frequency response to the desired specification.
- Evaluation of the closed-loop response to verify the stability and dynamic response of the system.
- Digitizing the compensator transfer function to yield the difference equations for implementation on a digital controller.

Except for the circuit simplification, the above steps have to be performed for both the current and voltage loops. The current loop is inside the voltage loop, so that it must be calculated first. The compensated current loop is then used as the un-compensated system for the voltage loop.

The equivalent circuit obtained through simplification is valid for both control loops, and is discussed in section 7.2.3. Thereafter the current and voltage loops are designed using the above steps.

7.2.3 Circuit Simplifications for Transfer Function Determination

When determining the voltage and current mode transfer functions of the converter it is not necessary to consider the full topology of Figure 21 in Chapter 3.

Firstly, the switching frequency of the converter (30 kHz) is many times the output frequency (50 / 60 Hz). The output voltage therefore changes relatively slowly when compared to the switching transients. In order to calculate the transfer functions, it may therefore be assumed that the output of the converter is a DC voltage about some steady state value. The compensation equations are then designed for this quasi-DC steady state. It must be ensured that the overall loop response is still fast enough that AC outputs can be accurately attained.

Furthermore, it will be shown that for a specific power flow direction, the positive and negative voltage output modes are identical, since the equations are not dependent on output polarity (except for the negative sign). Thus, only two modes need to be considered, that of forward power flow and that of negative power flow. The calculations can be performed for either positive or

negative outputs. They are however only considered for positive output voltages in the interest of simplicity.

Lastly, the topology itself can be significantly simplified for the purposes of the control system design. Consider for example the converter operating in reverse power flow mode. As noted in Chapter 2, the operation of the converter in the reverse mode is similar to that of a conventional step-up (boost) converter. This can be seen by inspecting the converter topology, with the battery (output for this mode) on the right hand side:

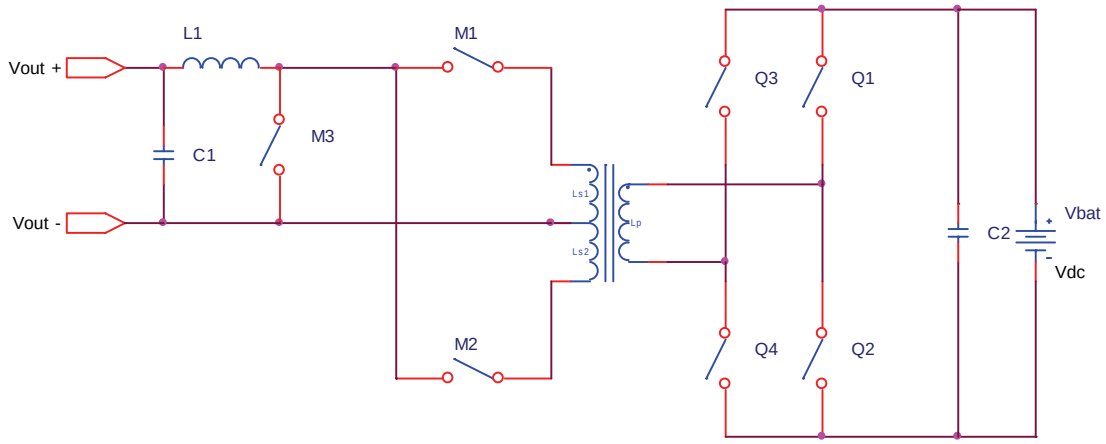

Figure 39: Converter in Reverse Mode

If the switches are assumed as ideal, and synchronism of the switches is maintained, then M_1, M_2 can be omitted, and only M_3 retained. Q_1-Q_4 can also be eliminated from the circuit, since they act as a rectifier bridge. If an ideal transformer is also assumed, it may also be removed if by multiplying the battery voltage with N_{high}/N_{low} (the transformer turns ratio). The final simplified circuit for the reverse mode is shown in Figure 40.

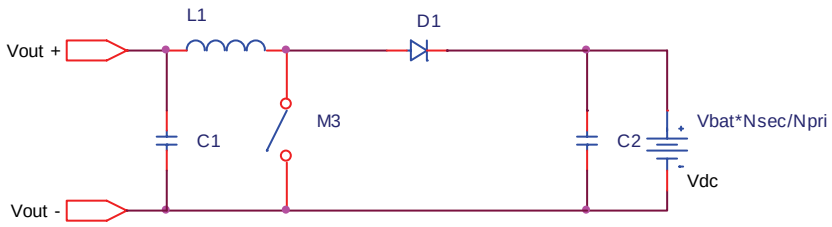

Figure 40: Equivalent Circuit, Reverse Mode

Noted that switches M_1 and M_2 and $Q_1 – Q_4$ were replaced by the single diode D_1 in Figure 40.

Thus, the converter topology can be simplified to that of a basic step-up converter during the reverse power flow mode. The procedure is similar during forward power flow mode, and the converter may be simplified to a basic step-down converter.

7.3 Current Control Loop

The current control loop is designed using the procedure of section 7.2.2.

As mentioned at the end of section 7.5.4, the current loop transfer functions for the forward and reverse modes of the converter are identical. This greatly simplifies the design of the control system, since the same compensation can be used for forward and reverse modes.

The current loop transfer function is calculated in section 7.5.4 as (Equation 7-28):

$$\frac{\tilde{i}_L}{\tilde{d}} = V_{bat}\frac{N_{\sec}}{N_{pri}}\frac{1}{sL + R_L} \qquad \textbf{(7-1)}$$

Equation 7-1 shows that the system has a single pole at R_L/sL. The system will therefore always be stable, since a single pole can only affect a maximum phase shift of 90 degrees.

7.3.1 Additional Gains

In addition to the power section transfer function of Eq. 7-1, there are additional gains present in the feedback loop. The design of a compensator requires all gains that are present between the output and the input of the compensator to be considered. For the present loop, the additional gains are the modulation (PWM) gain and the measurement gain.

7.3.1.1 PWM Gain

The output of the compensator is a duty cycle command between 0 and 1. However, in the DSP, this is an integer value. This integer value (as loaded into the PWM compare register) is compared to a triangular waveform in the PWM output peripheral. Since the output would be on continuously (100% duty cycle) when the compare value is equal to the half the amplitude of the triangular wave, this action has the effect of dividing the output by half the triangle wave amplitude N_{TRI}. Thus

$$A_{PWM} = \frac{1}{0.5\hat{N}_{TRI}} \qquad \textbf{(7-2)}$$

As discussed in section 8.2.3.1, the amplitude of the triangle waveform is $N_{TRI,MAX}$=666. The PWM Gain is therefore A_{PWM} = 1/333.

7.3.1.2 Measurement Gain

The inductor current value is not used directly in the control equation, it is measured by a transducer, sampled by the ADC, scaled, etc. Each of these components and operations introduce a gain in the control loop.

The inductor current is measured by means of a closed loop hall-effect current transducer. The transducer produces a secondary current that is directly proportional to current through its primary. Full scale is 25 mA output for 25 A input. The current / current conversion ratio is designated as N_{Trans}. Since the microprocessor Analogue to Digital Converters (ADC's) measure voltage, the secondary transducer current is passed through a measurement resistor. Thus, the value measured by microprocessor is given by:

$$V_{SENSE} = R_{Meas} N_{Trans} V_{DC} \qquad \textbf{(7-3)}$$

For the TMS320F240X DSP's, this value has to be equal or less than the microprocessor supply voltage. The digital value sampled by the ADC is given by:

$$V_{SENSE} = 1023 \times \frac{V_{SENSE} - V_{REFLO}}{V_{REFHI} - V_{REFLO}} \qquad \textbf{(7-4)}$$

where V_{REFHI} and V_{REFLO} are the high and low analogue reference values respectively. For the present application, V_{REFLO} is connected to the analogue ground, and V_{REFHI} to a 3.3 V regulator.

The TMS320LF240X DSP's are 16 bit processors, and it has been decided to represent the parameter measurements as 16-bit integers. It should be noted that the 10-bit measured ADC value is left justified by zero padding, which has the effect of multiplying the result by 2^6 = 64, and placed into a 16-bit result register. The value of the register is thus between 0 and 65535.

Since some measurements may be negative, a midpoint voltage offset is added to most of the measurements. Thus, although the ADC resolution is 10 bits, only half of that (9 bits) are used for the actual measurement, since the MSB is used as a sign bit. To convert the 16 bit result register from a uni-polar to a bipolar representation, the value 32767 is simply subtracted from it.

The overall result is that a +25 A measurement will correspond to a integer value of 32767. This gives and overall measurement gain of:

$$\begin{aligned} A_{Measure} &= 32767 / 25 \\ &= 1310.68 \end{aligned} \qquad \textbf{(7-5)}$$

$R_{Measure}$ is therefore chosen so that a 25 A inductor current (25 mA transducer output) produces 1.65 V at the ADC.

7.3.2 Current Loop Response

Using the transfer function of Equation 7-1, the gains of Equations 7-2 and 7-5, and the power section component values calculated in Chapter 4, the open-loop Bode Plot of the current control system is as follows:

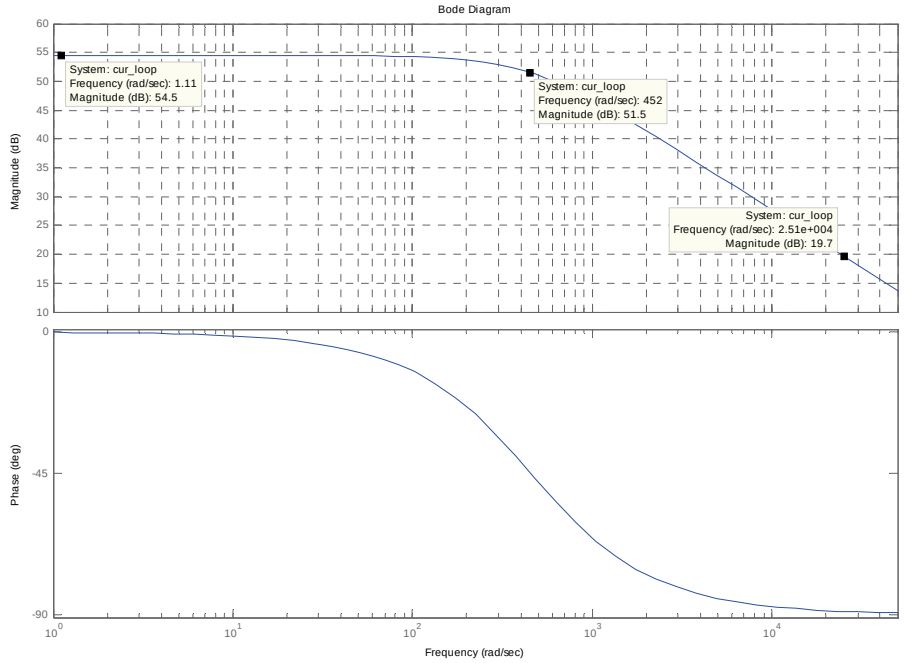

Figure 41: AC Output Converter, Open Loop Current Response

7.3.3 Compensator Design

In order to accurately track the 15th current harmonic which may be encountered (as discussed in section 4.4.1), the crossover frequency of the converter is chosen to be 5 times 15th harmonic frequency of 750 Hz. Thus the crossover frequency should be 3750 Hz, which is rounded to 4000 Hz. This is equal to 25.1 krad/s.

The Bode plot of Figure 41 shows that the current loop has almost exactly 20 db of gain at the desired crossover frequency. This can easily be attenuated by inserting a pole and a zero in the loop that are exactly one decade apart. The pole must be below the zero. In the decade between the zero and pole an additional 20 db per decade will be subtracted from the plot. This delivers the desired result of 20 db attenuation at frequencies above the zero.

The pole and zero combination will add a negative phase shift to the response. To prevent the phase margin from becoming too small, the pole should be placed relatively low. If it is placed too low however, the low frequency gain of the system will be attenuated, leading to reduced tracking ability. As a trade off, the pole has been chosen at the power section pole (454 rad/s), and the zero one decade above (4540 rad/s). The transfer function of the compensator is:

$$G_c(s) = \frac{s + 4540}{10s + 4540} \qquad \textbf{(7-6)}$$

The Bode plot of the current loop compensator of Equation 7-6 is shown in Figure 42.

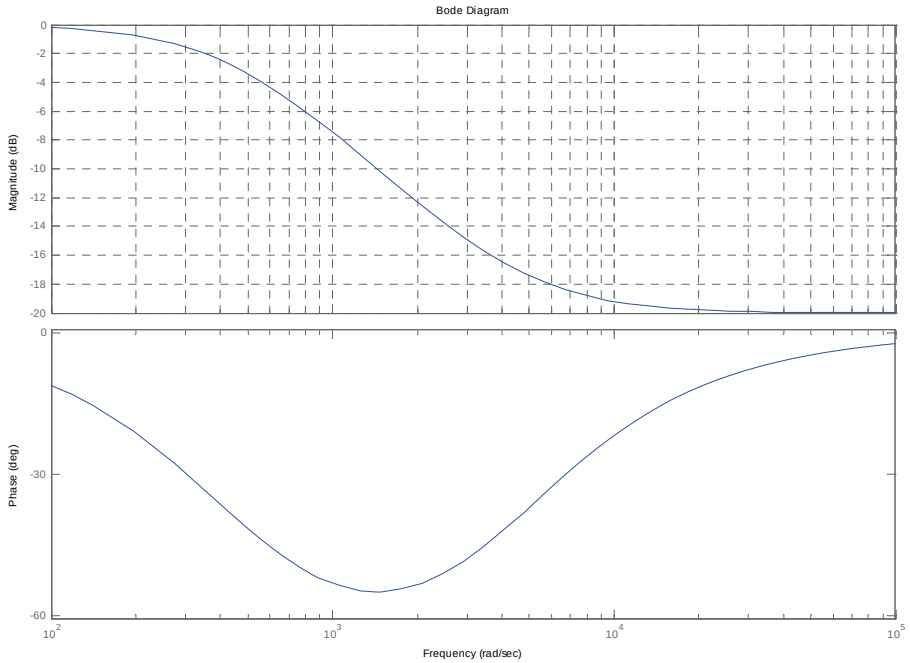

Figure 42: AC Output Converter, Current Loop Compensator

The loop response of the system and the compensator is shown in Figure 43.

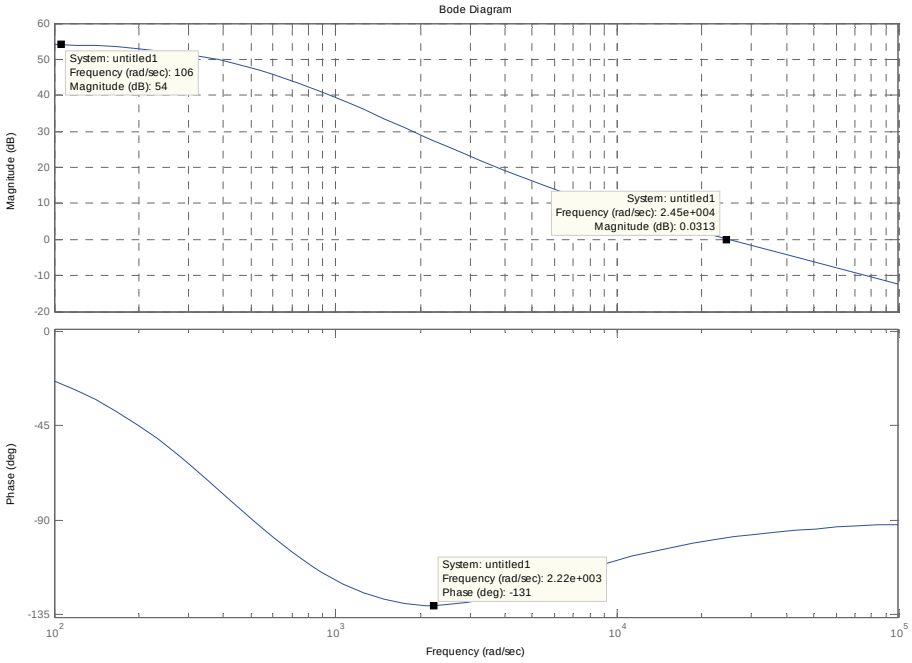

Figure 43: AC Output Converter, Compensated Current Loop

Note that the crossover frequency is almost exactly at the design value. The low frequency gain has not been significantly attenuated, and the phase margin is almost 60 degrees.

7.3.4 Compensator Digitization

The compensator was digitized using Matlab software, resulting in:

$$G_z = \frac{0.1 - 0.08513z^{-1}}{1 - 0.9851z^{-1}} \qquad \textbf{(7-7)}$$

This yields the following difference equation:

$$\begin{aligned} &\frac{0.1 - 0.08513z^{-1}}{1 - 0.9851z^{-1}} = \frac{u(k)}{e(k)} \\ &u(k) - 0.9851u(k-1) = 0.1(e(k)) - 0.08513(r(k-1) - c(k-1)) \\ &u(k) = 0.1(e(k)) - 0.08513(e(k-1)) + 0.9851u(k-1) \end{aligned} \qquad \textbf{(7-8)}$$

Equation 7-8 is the final difference equation that is directly implemented by the digital controller to control the current loop.

7.4 Voltage Mode Control

7.4.1 Additional Gain

The voltage control loop has only a measurement gain. It has no PWM gain, since the output of the voltage loop is taken directly in software as the input to the current control loop.

The calculation of the voltage measurement gain is identical to that of the current measurement gain given in section 7.3.1.2. The overall result is that a +500 V measurement will correspond to a integer value of 32767. This gives and overall measurement gain of:

$$\begin{aligned} A_{Measure} &= 32767/500 \\ &= 65.53 \end{aligned} \qquad \textbf{(7-9)}$$

$R_{Measure}$ is therefore chosen so that a 500 V output voltage (25 mA transducer output) produces 1.65 V at the ADC.

7.4.2 Frequency Response

When the converter is supplying a load, and not connected to mains, the impedance of the output capacitor (and its series resistance) in parallel with the assumed load resistor is

$$\begin{aligned} \frac{1}{Z_{C+R}} &= \frac{1}{R_{LOAD}} + \frac{1}{\frac{1}{sC} + R_C} \\ Z_{C+R} = G_O(s) &= \frac{R_{LOAD}\left(\frac{1}{sC} + R_C\right)}{R_{LOAD} + \frac{1}{sC} + R_C} \\ &= \frac{sCR_C + R_{LOAD}}{sC\left(R_C + R_{LOAD}\right) + 1} \end{aligned} \qquad \textbf{(7-10)}$$

The system for the outer voltage loop is the compensated inner current loop transfer function multiplied by the output impedance, that is $G_{OUT}(s) = G_I(s)*G_O(s)$. The open-loop Bode plot of this combination system is shown in Figure 44.

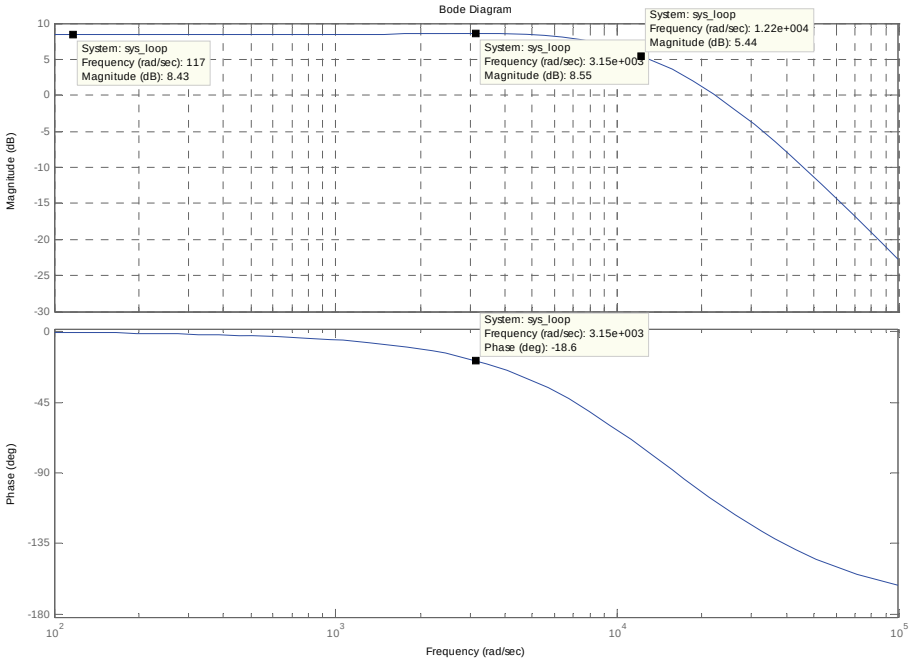

Figure 44: AC Output Converter, Open Loop Voltage Response

7.4.3 Compensator Design

The gain of the system in Figure 44 at low frequencies is low, only 8.4 dB, or 2.63. In order to again have a steady state error of 0.5%, a proportional factor is included in the compensator with value K = 200/2.63 = 76, which is 37.6 dB.

To ensure accurate voltage tracking, the crossover frequency is chosen to be 10 times the sinusoid reference frequency of 50 Hz. This is equal to 500 Hz or 3142 rad/s. From the bode plot in Figure 44 it can be seen that the gain at this frequency is 8.55 dB plus the 37.6 dB from the proportional factor, giving a total gain of 46.25 dB. This gain will be attenuated to 0 dB at the crossover frequency with a lag compensator of the form:

$$G_C = K\frac{1+T_{lag}s}{1+\beta T_{lag}s} \qquad \textbf{(7-11)}$$

Since the gain of the loop is essentially constant over a very wide frequency range, it must be ensured that the zero of the lag compensator is not placed before the pole of the power section. If this is not done, the lag compensator will result on a flat gain of 0dB over a large frequency range, thereby not crossing over cleanly. The corner frequency (ω_l) of the lag compensator zero is selected at the dominant pole of the power section, namely 12.2 krad/s. This corner frequency corresponds to the zero of the lag compensator (given by $\omega_l = \frac{1}{T}$), so

$$T = \frac{1}{\omega_l} = \frac{1}{12.2krad/s} = 82us \qquad \textbf{(7-12)}$$

To attenuate the system at crossover frequency to 0 dB, β must have a value of

$$\begin{aligned} -46.25 &= -20\log_{10}\beta \\ 2.3125 &= \log_{10}\beta \\ \therefore \beta &= 205 \end{aligned} \qquad \textbf{(7-13)}$$

However, since the zero is now located above the crossover frequency, the full 46.25dB attenuation is not affected. By trial and error, β = 610 has been selected as the optimal value. This gives a crossover frequency of 5000 rad/s. The simulation of Chapter 9 has proven this value effective in providing a fast rise time without excessive overshoot.

The transfer function of the lag compensator is therefore

$$G_{lead}(s) = \frac{1+0.000082s}{1+0.050s} \qquad \textbf{(7-14)}$$

The Bode plot of the compensated voltage loop is given in Figure 45.

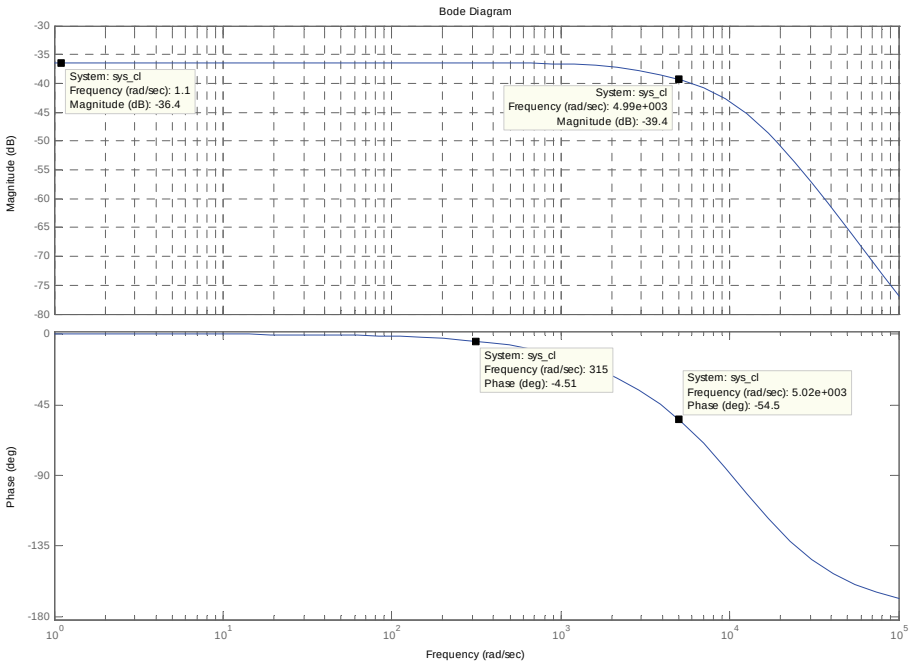

Figure 45: AC Output Converter, Closed Loop Voltage Response

Note in Figure 45 that the overall gain of the system is not 0 dB as expected, but -36.4 dB. This is due to the measurement gain of approximately 65 (Equation 7-9) in the feedback path. This attenuation is required since the reference sinusoid value is not given in Volt, but as a scaled integer that has the same scale factor as the measurement. Thus, with reference to physical voltage, the Bode plot of Figure 45 needs to be multiplied with 36.4 dB.

The converter exhibits an excellent phase margin of 125.5 degrees, indicating that almost no oscillatory behaviour will be present. At 50 Hz (314 rad/s) a phase shift of ϕ = -4.5 degrees is expected between the input and output. This translates to a time difference of $t = \phi/\omega$ = 14.3 ms. This delay was shown in the simulation results of Chapter 9.

7.4.4 Compensator Digitization

The voltage mode compensator was again digitized using Matlab resulting in:

$$G_z = \frac{0.1246 - 0.0745z^{-1}}{1 - 0.9993z^{-1}} \qquad \textbf{(7-15)}$$

This yields the difference equation that was implemented on the DSP:

$$\frac{0.1246 - 0.0745z^{-1}}{1 - 0.9993z^{-1}} = \frac{u(k)}{e(k)}$$
$$u(k) = 0.1246(e(k)) - 0.0745(e(k-1)) + 0.9993u(k-1) \qquad \textbf{(7-16)}$$

7.5 Determining Transfer Functions Through Inspection

7.5.1 Introduction

The formal derivation of a converter transfer function is a lengthy procedure. An example of such a derivation for the voltage transfer function of the converter in forward mode is given in the Appendix A.13 for reference.

The Application Notes written by Mr. Lloyd Dixon from Unitrode that were reviewed in Chapter 2 never contained any mention of how the converter transfer functions were derived. This led the author to develop a method for determining transfer functions based on intuitive inspection, which saves a significant amount of design effort.

This method was used to determine the transfer function of the proposed converter for the compensator designs given in sections 7.3 and 7.4. The remainder of this chapter details the method.

7.5.2 Time Varying Components

The transfer function of a converter is normally determined for the small signal response of the converter. The steady state (not time varying) response is generally not used in the design of the control system, except that the gain must be high enough to ensure the output approximates the reference value.

Since all components in a power electronics design are normally operated in their linear ranges (except transistors, which are only used as on/off switches), and the properties of the components do not change rapidly with time (changes occur several orders of magnitude slower than the switching period), most converters are classified as Linear Time Invariant (LTI). This implies that the principle of superposition can be applied.

Superposition allows the division of signals into components. For this analysis, the division of all variables into steady state values and perturbations is the most useful. For example, the instantaneous inductor current and duty cycle may be given as:

$$\begin{aligned} i_0 &= I_0 + \tilde{i}_0 \\ d &= D + \tilde{d} \end{aligned} \qquad \textbf{(7-17)}$$

Where I_0 and D are the steady state inductor current and switch duty cycles respectively, and the perturbation components are indicated by "~".

7.5.3 Impedance of Components

In general, the voltage and current relationship of any LTI component can be written as:

$$V = IZ \qquad \textbf{(7-18)}$$

Since time-varying components are applied to the impedance, Z may be complex. The voltage and current of Equation 7-18 can be written in terms of perturbations as in Equation 7-17:

$$\begin{aligned} V_{DC} + \tilde{v} &= \left(I_{DC} + \tilde{i}\right)Z \\ &\textit{thus} \\ \tilde{v} &= Z\tilde{i} \end{aligned} \qquad \textbf{(7-19)}$$

Equation 7-19 shows that superposition may be used to relate the perturbation components to each other through the complex impedance.

For inductors, a series resistance is normally modelled with the inductance. The impedance of an inductor is therefore given by:

$$Z_L(s) = sL + R_L \qquad \textbf{(7-20)}$$

If a series resistance is also assumed for a capacitor, the impedance is given by:

$$Z_C(s) = \frac{1}{sC} + R_C \qquad \textbf{(7-21)}$$

7.5.4 Effect of Changes in Duty Cycle

Consider a basic step-down (buck) regulator. The average voltage (over one switch cycle) applied to the non-output side of the inductor is given by:

$$V_{L,IN} = DV_{IN} \qquad \textbf{(7-22)}$$

Using superposition, the effect of changes in the duty cycle is:

$$\begin{aligned} V_{L,IN} + \tilde{v}_{L,IN} &= \left(D + \tilde{d}\right)V_{IN} \\ &\textit{thus} \\ \tilde{v}_{L,IN} &= \tilde{d}V_{IN} \end{aligned} \qquad \textbf{(7-23)}$$

Where it is assumed that the input voltage is constant or slowly changing. Equation 7-23 seems intuitive, since an additional fraction of the input voltage is added to the average inductor input voltage with an increase in duty cycle.

If it is assumed that the average output voltage of the converter changes slower than the inductor current (due to the assumed large output capacitor, or connectivity to mains supply) the change in the voltage over the inductor is due only to the change on the non-output side, so that Equation 7-23 may be written as:

$$\tilde{v}_L = \tilde{d}V_{IN} \qquad \textbf{(7-24)}$$

Thus, using the perturbation equation of 7-19 and the impedance of the inductor (Equation 7-20), the change in the inductor current can be related to the duty cycle:

$$\begin{aligned} \tilde{v} &= Z\tilde{i}_L \\ \tilde{d}V_{IN} &= (sL + R_L)\tilde{i}_L \\ &\textit{thus} \\ \frac{\tilde{i}_L}{\tilde{d}} &= \frac{V_{IN}}{sL + R_L} \end{aligned} \qquad \textbf{(7-25)}$$

Equation 7-25 is the required transfer function of the inner current loop of a current mode controlled step-down converter. This transfer function is valid for all current mode converters where the output current is the inductor current.

For a step-up (boost) converter, the switch causes V_{OUT} to be "taken away" from the inductor. The average value at the non-output side would then be

$$V_{L,OUT} = (1 - D)V_{OUT} \qquad \textbf{(7-26)}$$

Resulting in:

$$\begin{aligned} V_{L,OUT} + \tilde{v}_{L,OUT} &= \left(1 - \left(D + \tilde{d}\right)\right)V_{OUT} \\ &\textit{thus} \\ \tilde{v}_{L,OUT} &= -\tilde{d}V_{OUT} \end{aligned} \qquad \textbf{(7-27)}$$

This is the negative of the equation for the step-down converter. The negative indicates that the current will be towards V_{OUT}, whereas it was away from V_{IN} for the step-down converter.

The current loop transfer function for the step-up converter becomes:

$$\frac{\tilde{i}_L}{\tilde{d}} = -\frac{V_{OUT}}{sL + R_L} \qquad \textbf{(7-28)}$$

It should be noted that the transfer function of the input current of a step-up converter (Equation 7-28) and the output current of a step-down converter (7-25) are identical, with the only difference being the negative sign. This result enabled the design of the current and voltage control loops of sections 7.3 and 7.4.

7.5.5 Output Current Not Inductor Current

Several converter topologies exist where the output current is not the inductor current. Examples are the output current of a step-up (boost) converter, or if the input current of a step-down converter is to be controlled.

The most significant implication is that when the output current of the converter is not the inductor current, the inductor current is "taken away" from the output when the switch is on. Thus the period that the inductor current is applied to the output is shortened by the increase in duty cycle. Even though the inductor current builds up during this period, the average output current decreases.

The total average inductor current, and not only the change in inductor current, is therefore subtracted from the output with an increase in duty cycle. This can be mathematically shown by writing the output current in terms of components:

$$\begin{aligned} I_O + \tilde{i}_O &= \left(1-\left(D+\tilde{d}\right)\right)\left(I_L + \tilde{i}_L\right) \\ &= (1-D)I_L - \tilde{d}I_L + (1-D)\tilde{i}_L \\ &\textit{thus} \\ \tilde{i}_O &= (1-D)\tilde{i}_L - \tilde{d}I_L \end{aligned} \qquad \textbf{(7-29)}$$

Cross products of perturbation components were removed in Equation 7-29. If the expression for the perturbation in inductor current (Equation 7-25) is now combined with Equation 7-29, the required transfer function is obtained:

$$\begin{aligned} \tilde{i}_O &= (1-D)\tilde{d}\,\frac{V_{IN}}{sL+R_L} - \tilde{d}I_L \\ \frac{\tilde{i}}{\tilde{d}} &= \frac{(1-D)V_{IN}}{sL+R_L} - I_L \\ &= \frac{V_{OUT}}{sL+R_L} - I_L \end{aligned} \qquad \textbf{(7-30)}$$

In the last step it was recognised that the steady state output and input voltages are related through the factor 1/(1-D) for a step-up converter.

Equation 7-30 contains a term that subtracts the inductor current with a positive increase in duty cycle. This causes the output to "go the wrong way", and is the cause of the Right Hand Plane Zero referred to in section 2.2 of the literate study of Chapter 2.

7.5.6 Voltage Transfer Function

Once the current loop transfer function is known, the voltage transfer function can be calculated. This transfer function gives the voltage mode response without the inclusion of an inner current loop, and is shown for completeness. It will be performed for a step-down converter, but the calculation for a step-up converter is similar, with the substitution of the correct current transfer function.

Using the impedance relationship (Equation 7-19) and the current transfer function (Equation 7-25), the change in output voltage of a buck converter may be given as:

$$\tilde{v}_{OUT} = Z_{C+R}\tilde{i}_L$$
$$\textit{where} \qquad \textbf{(7-31)}$$
$$\tilde{i} = \tilde{d}\,\frac{V_{IN}}{sL + R_L}$$

Z_{C+R} is the equivalent resistance of the capacitor (and its series resistance) in parallel with the assumed load resistor. Thus

$$\frac{1}{Z_{C+R}} = \frac{1}{R_{LOAD}} + \frac{1}{\frac{1}{sC} + R_C}$$
$$Z_{C+R} = \frac{R_{LOAD}\left(\frac{1}{sC} + R_C\right)}{R_{LOAD} + \frac{1}{sC} + R_C} \qquad \textbf{(7-32)}$$

However, in the preceding discussions the capacitor resistance, $R_{C,}$ has always been omitted in order to bring the examples in line with Mr. Dixon's application notes. Similarly neglecting R_C from Equation 7-32, the capacitor and load combined impedance is taken as:

$$\frac{1}{Z_{C+R}} = \frac{1}{R_{LOAD}} + \frac{1}{\frac{1}{sC}}$$
$$Z_{C+R} = \frac{R_{LOAD}\left(\frac{1}{sC}\right)}{R_{LOAD} + \frac{1}{sC}} \qquad \textbf{(7-33)}$$

Substitution of Equation 7-33 into 7-31 gives:

$$\tilde{v}_{OUT} = \frac{R_{LOAD}\left(\frac{1}{sC}\right)}{R_{LOAD} + \frac{1}{sC}}\,\tilde{d}\,\frac{V_{IN}}{sL + R_L}$$
$$\frac{\tilde{v}_{OUT}}{\tilde{d}} = V_{IN}\,\frac{1}{\left(sC + \frac{1}{R_{LOAD}}\right)\left(sL + R_L\right)}$$
$$= V_{IN}\,\frac{1}{s^2LC + \frac{sL}{R_{LOAD}} + sCR_L + \frac{R_L}{R_{LOAD}}} \qquad \textbf{(7-34)}$$
$$= V_{IN}\,\frac{1}{LC\left(s^2 + s\left(\frac{1}{CR_{LOAD}} + \frac{R_L}{L}\right) + \frac{R_L}{LCR_{LOAD}}\right)}$$

Equation 7-34 is almost identical to that derived in Appendix A.13 for the original forward mode control method, if the capacitor resistance is neglected

from that equation. The above derivation is many times shorter than the formal derivation. There is a slight discrepancy regarding the final term in the denominator, which is due to cross products of R_c and R_L being removed in the voltage transfer function calculation.

7.5.7 General Method

From the preceding paragraphs, the following general method may be described to find the transfer function of any converter:

- Assume that the voltage at the non-switch side of the inductor changes slowly compared to the inductor current. This is valid since output is normally capacitor buffered, or connected to mains.
- Determine the magnitude of the voltage change applied to the non-output side of the inductor when the switch is turned on (include the effect of transformers, if applicable). E.g. V_{IN} is applied when a buck regulator switch is turned on, so that that the change is taken as + V_{IN}. However, V_{IN} is taken away when a boost regulator's switch is turned on, so that the change is - V_{IN}, with the minus indicating the current will be towards V_{IN}.
- Divide this by the (complex) inductor impedance to get the change in inductor current.
- If the inductor is not in the output path, subtract the magnitude of the current that is taken away from the output when the switch is turned on (include the effect of transformers, if applicable). Otherwise leave it as is.

This method will give the simplified current transfer function of the converter. To obtain the voltage transfer function, multiply the current transfer function with the complex impedance of the output network.

This method can be extended to include the effects of capacitor resistance, although this will not be shown.

7.6 Chapter Conclusion

This chapter described the calculation of the compensation difference equations that are used in the digital controller software of Chapter 8 to control the converter voltage and current loops.

The compensation equation for the current control loop was calculated first, since it is located inside the voltage loop. The compensated current loop was then taken as the uncompensated system for the outer voltage loop.

The chapter closed with a method that was developed to determine the transfer functions of switch mode converters by inspection alone. This method was applied in the control loop designs of the present chapter. The method significantly reduces the amount of effort in calculating transfer functions.

8 DSP Configuration and Software

8.1 Chapter Introduction

This chapter describes the design of the software for the Digital Signal Processor (DSP) that forms the basis of the converter control system.

The selection of the DSP and the design of the digital controller board is described in Chapter 6. The control methodology and compensation equations that must be implemented in the DSP are described in Chapter 7.

The software has two basic functions, firstly to initialize the on-chip peripherals, and secondly to execute the control code. The on-chip peripherals are typically only configured following a power-on or reset. The control thereafter executes continuously while the converter is in operation.

The control code implements the voltage and current feedback loops designed in Chapter 7. These loops require the actual values to be sampled and scaled, the new duty cycles calculated with compensation equations and the PWM output duty cycle to be updated.

The control code is also responsible for the generation of the sine wave reference signal, which the converter output voltage must track.

8.2 DSP Control Implementation

8.2.1 DSP Peripherals

The TMS320LF2403A DSP was selected since the entire control system of the converter can be implemented using the on-chip peripherals. For the purposes of the present converter, the most important peripherals are Event Manager A and the Analogue to Digital Converter (ADC). These integrated modules greatly reduce the overhead on the CPU, and enables the user code to execute much faster than would otherwise be the case.

When correctly configured, the on-chip Event Manager A (EVA) can handle the entire PWM generation operation, with the only input from the CPU being the duty cycle and operational mode settings (i.e. forward/reverse mode, positive/negative voltage). The EVA module of the DSP contains two 16-bit General Purpose Timers (GPT1, GPT2), one comparator per timer (T1CMPR & T2CMPR) and 3 dedicated PWM Comparators (CMPR1 – CMPR3). The three comparators drive 6 PWM output pins (PWM1 – PWM6). The ADC can sequentially sample up to 16 sequential samples from any of its 8 input channels. Each sample has an accuracy of 10 bits.

GPT1 generates a 30 kHz symmetrical triangle waveform generates the forward mode PWM signals for Q1 – Q4, and the reverse mode switching signals for M1 and M2. GPT2 generates a 60 kHz symmetrical triangle

waveform of half the amplitude of that of GPT1's, which is used to switch M3 during the reverse power flow mode.

The on-chip Analogue to Digital Converter (ADC) and associated sequencer can handle all sampling operations. GPT1's period interrupt starts the ADC sequence.

8.2.2 DSP Sampling and Switching Schemes

The on-chip peripherals handle the sampling and the PWM output operations. The methods in which these peripherals operate are discussed in the following sections.

8.2.2.1 Data Acquisition

A state sequencer controls the sampling sequence of the on-chip ADC of the DSP. The state sequencer is capable of sequencing 16 A-to-D conversions, while each conversion may be from any of the 8 input channels. The channel and sequence assignments that were made for the present converter are shown in Table 8.1.

Table 8.1: Channel and Sequence assignments for the converter

Channel Sequence (State)	ADC Channel	Variable Measured
0	0	Inductor Current
1	1	Battery Voltage
2	2	DC Link Voltage
3	3	Mains Voltage

To obtain a value for the average inductor current, it is sampled halfway through the switch on- period. Since the inductor current increases and decreases linearly with time, the half-way value will be the average. This eliminates the need for a separate averaging amplifier. In addition, since it is sampled as far away as possible from switching transients, the measurement is noise immune. Furthermore, the current will always build up when the switch is on, and will therefore always be continuous, even though the inductor current may be discontinuous when the switch is turned off. If the inductor current is discontinuous, the measured value will not be the average value. The simulation has however shown that this is insignificant and it was not considered further. Correct sampling timing is ensured by starting the ADC conversion cycle when a GPT1 period interrupt occurs.

Since the measurement of the inductor current is time-sensitive (the value must be sampled exactly in the middle of the switching cycle), it is measured first, immediately when the sequence starts. The voltages are sequentially measured after the current, since they are not significantly time-sensitive.

Originally it was intended that the ADC sample the values every tenth cycle. As discussed in the simulation of Chapter in section 9.3.1, this proved to be completely inadequate. The ADC must sample the values at every switching cycle, or 30 kHz. The ADC is started every time Timer 1 has a period match,

as this match will always occur be in the middle of a switch's on time. The ADC takes approximately 60 clock cycles to finish the conversions.

The sequence busy flag SEQ1_BSY is monitored continuously by the main program loop. Once the ADC has been started and the measurements process completes the values are scaled, the control calculations are performed and duty cycles updated.

8.2.2.2 Forward Mode Switching

During forward mode, the low voltage switch pairs (Q1-Q4 and Q2-Q3) are switched alternately at duty cycles of less than 50% each. Either the forward or negative transistor making up half of M1, M2 and M3 are switched on permanently in this mode, so that the freewheeling diode of the remaining transistors rectify the square wave to either a positive or a negative voltage.

Table 8.2 gives the high voltage transistors that have to be switched on to produce a positive or negative output voltage. This switching is done much slower than the switching period, since the switching only occurs when the output polarity changes:

Table 8.2: High Voltage Transistors, Switching Polarity

High Voltage Transistor	Output Polarity
M1A, M2A, M3A Permanently On	Positive
M1B, M2B, M3B Permanently On	Negative

Thus, only Q1-4 and Q2-3 should switched at the switching frequency. GPT1 is used to generate a symmetrical triangle waveform of positive amplitude. GPT1 is configured as a continuous up/down counter. Two compare values are then used to switch Q1-Q4 and Q2-Q3. If the maximum triangle amplitude is taken to be A, then the two compare values are given by A*(1-D) and A*D.

Since D < 50% under all conditions, A*(1-D) will always be the higher and A*D always the lower compare value. If A(t) is the instantaneous saw-tooth (timer) value, the correct switching pattern will be obtained if:

- Q1-Q4 is on when A(t) > A*(1-D)
- Q2-Q3 is on when A(t) < A*D

Figure 46 graphically shows this switching scheme for a duty cycle D = 25% and A = 1. Red indicates the time that Q1-Q4 is switched on, and Green Q2-Q3:

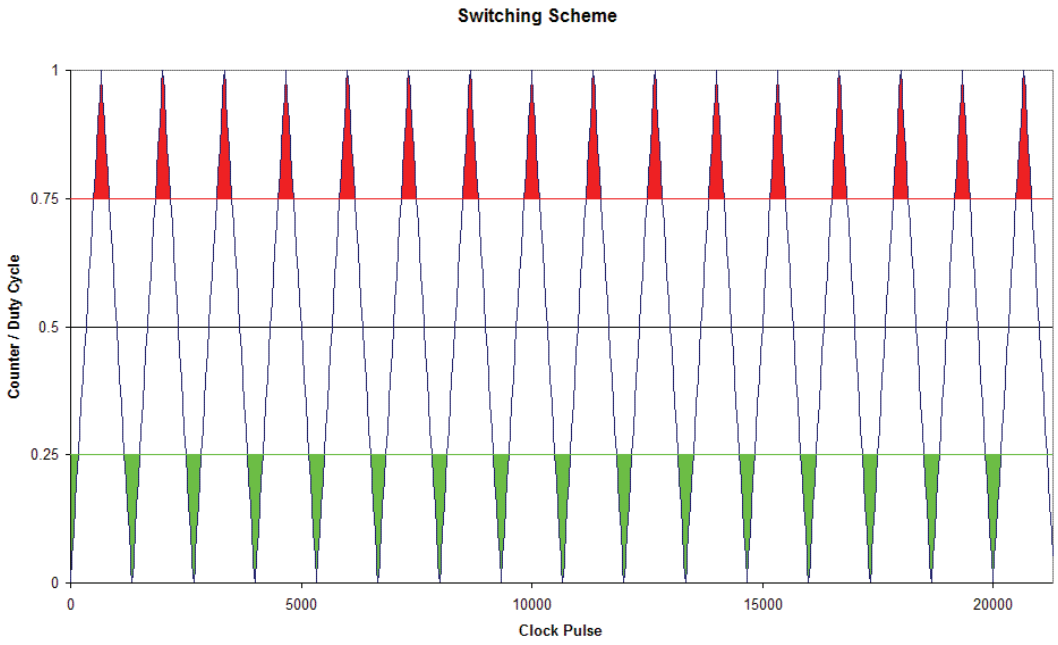

Figure 46: Forward Switching Scheme

A symmetrical triangle waveform is used since this gives a definite point exactly in the centre of the switching period (i.e. the GPT1 period interrupt), which is used to measure the inductor current and voltages by the ADC, as far away as possible from all switching transients.

The PWM pairs however share a comparator. A PWM pair therefore cannot drive Q1-Q4 and Q2-Q3, since Q1-Q4 and Q2-Q3 require different compare values. The DSP board has provision to connect PWM5 (comparator CMP3) as well as T1PWM to the same isolator IC to drive Q1-Q4 and Q2-Q3. This ensures that two independent comparators are available to generate this switching scheme.

8.2.2.3 Reverse Mode Switching

In reverse mode, M3 is switched on for a duty cycle D<50%, at twice the frequency of M1 or M2. Since M3 is switched during both half cycles (i.e. it is switched before M1 or M2 is switched on), a duty cycle of D_{M3} = 50% will actually result in M3 being turned on continuously. Q1 – Q4 are not switched at all during the reverse mode. Their anti-parallel diodes are used as a static full bridge rectifier.

For this mode, GPT1 is configured as for the forward mode, with the exception that switches M1 and M2 are now switched instead of Q1-4 and Q2-3. The values A*(0.5+D) for the larger value, and A*(0.5-D) for the smaller value, are loaded into the compare registers (CMP1 and CMP2) to ensure that the inductor current increases with increasing duty cycle.

GPT2 generates a triangle waveform that is twice the frequency of GPT1 and in phase. This triangle waveform is used to switch M3. The duty cycle value is

loaded in GPT1 and GPT2 compare registers, and the outputs configured so that M3 is on whenever M1 or M2 is not on.

Figure 47 again shows this switching scheme graphically for a duty cycle of D = 25% and A = 1. Red indicates M1 on, Green indicates M2, with blue indicating M3:

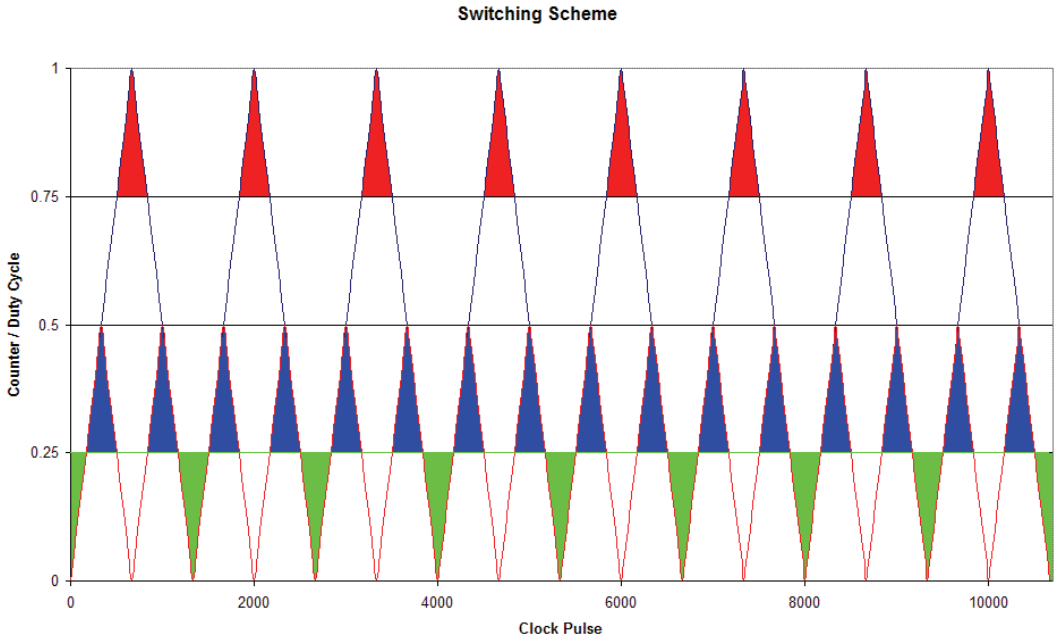

Figure 47: Reverse Switching Scheme

This switching scheme has one drawback however, the possibility might exist that M3 has turned off before M1 or M2 has switched on. To prevent the possibility of the inductor not having a current path, M1 and M2 are actually switched at 50% duty cycle, not at the duty cycle shown in Figure 47. This is possible since no voltage is applied to the transformer when M3 is on.

8.2.3 DSP PWM Configuration

This section describes the actual DSP configuration for implementing the PWM switching schemes described in the previous section.

8.2.3.1 Timer 1 Configuration

To generate switching signals for both low voltage pairs using a single timer, GPT1 is configured to the continuous up/down mode. In this mode the counting direction of GPT1 changes only at the period value (T1PR) and 0000h. GPT1 changes from up to down counting at T1PR, and from down to up counting at 0000h. This generates the equivalent of a symmetrical triangle waveform to which duty cycle values can be compared.

The switching frequency is specified as 30 kHz, giving a switching period of 33 us. The CPU internal clock is used for EVA, with a frequency of 40 MHz (period 25 ns).

In order to have the highest possible resolution in PWM output, the period (T1PR) must be as large as possible. This can be recognised from the fact that the counter increments/decrements once for each clock pulse, so that the slope of the resulting waveform is either 1 or -1. The resolution of the PWM output and the period is therefore equal in magnitude.

The clock prescaler of GPT1 is set to the lowest value (1), so that the CPU clock is directly applied to the timer. Thus, a period of 33.3 us is equal to 1333 clock pulses. Since the counter counts up and down during a single period, the period register has to have a value of approximately 1332/2 = 666. The value 667 is not chosen since it is not divisible by two, and GPT2 needs to run at twice the frequency (half the period) of GPT1.

8.2.3.2 Timer 2 Configuration

The PWM signals for M3 are generated with GPT2. It is set up and started in exactly the same way as GPT1, with the exception that the period register T2PR is half of T1PR, that is T2PR = 333. This will generate an in-phase waveform of half the amplitude and double the frequency of GPT1. GPT2 is started using GPT1, so that they are in phase.

8.2.3.3 PWM Outputs Configuration

Although there are 6 PWM output pins available on EVA, they operate in pairs and each pair shares a compare register. The converter however requires four independent outputs. Table 8.3 shows the pin assignments.

Table 8.3: DSP Pin Assignments for the Proposed Converter

SIGNAL	DEVICE
PWM1	M1A Gate Drive
PWM2	M1B Gate Drive
PWM3	M2A Gate Drive
PWM4	M2B Gate Drive
PWM5	Q1 & Q4 Comm.Drv.
T1PWM	Q2 & Q3 Comm.Drv
T2PWM & PWM6	M3A Gate Drive
T2PWM & /PWM6	M3B Gate Drive

The pair of switches Q1-Q4 or Q2-Q3 are always switched on simultaneously, so they are assigned the same output pin of the DSP.

A PWM output pin can be ACTIVE either when the counter value is equal or larger than the concerned compare register, or smaller or equal. That is A(t) >= CMPRx or A(t) <= CMPRx. Thus, for the top compare value (A*(1-D), used to drive Q1-Q4 during forward mode) the output pins need to be high when the pin is active. PWM5 is therefore configured as Active High. The reverse is true for Q2-Q3 during forward mode, the pins need to be low when the compare is active, so that T1PWM is configured as active low.

GPT2 must drive both M3A and M3B, but has only one output pin. An additional output pin (PWM 6) is therefore used to control M3A/B. During the

forward mode, either M3A or M3B is on, while the other is off. Since switching between these two transistors occur relatively slowly (every time the output polarity changes) the PWM6 pin is software switched to select between them. The T2PWM output is forced high during the forward mode. In the reverse mode, either M3A or M3B is switched off (diode only conducts), while the other is switched at double the switching frequency. Again, the switching between M3A and M3B occurs slowly.

This methodology can be implemented using a NOT and two AND gates. T2PWM is AND'ed separately with PWM6 and NOT PWM6 respectively. When PWM6 is low, M3A is selected. When PWM6 is high, M3B is selected. In this way, T2PWM is multiplexed to switch both transistors M3A and M3B. For the prototype a TI SN74LVC1G18 1-of-2 Non-Inverting De-multiplexer mounted on a small daughterboard was used.

Table 8.4 summarizes the switching conditions (pin actions and compare values) for the possible converter modes:

Table 8.4: Summary of switching conditions for converter modes

Mode	**Pin or**	**FWD**	**FWD**	**REV**	**REV**
Polarity	**Compare**	**POS V**	**NEG V**	**POS V**	**NEG V**
Q1,Q4 Pin	PWM5	AH	AH	FL	FL
Q1,Q4 Compare	CMPR3	A*(1-D)	A*(1-D)	--	--
Q2,Q3 Pin	T1PWM	AL	AL	FL	FL
Q2,Q3 Compare	T1CMPR	A*D	A*D	--	--
M1A Pin	PWM1	FH	FL	FL	AH
M1B Pin	PWM2	FL	FH	AH	FL
M1 Compare	CMPR1	--	--	A*(0.5)	A*(0.5)
M2A Pin	PWM3	FH	FL	FL	AL
M2B Pin	PWM4	FL	FH	AL	FL
M2 Compare	CMPR2	--	--	A*(0.5)	A*(0.5)
M3A/B Select Pin	PWM6	FL	FH	FH	FL
M3A/B Strobe Pin	T2PWM	FH	FH	AH	AH
M3 Compare	T2CMP	--	--	A*(0.5-D)	A*(0.5-D)

Where

- AH = Active High
- AL = Active Low
- FH = Forced High
- FL = Forced Low
- -- = Don't Care

To simplify the DSP program, the following values are always written to the compare registers:

- A*(1-D) to CMPR1
- A*D to T1CMPR
- A*(0.5) to CMPR2 and CMPR3
- A*(0.5-D) to T2CMP.

The output pin action control bits then completely control the direction and polarity of the converter.

Through an ordering oversight, IR4426 drivers were ordered for the IGBT's, instead of IR4427. The IR4426 is inverting, so that the actual values in the DSP program for PWM 1 – PWM4 and T2PWM are the inverse of the above table.

8.3 AC Output Control

8.3.1 Voltage Reference

To ensure that the voltage is an approximate sine wave, a reference is required for the voltage loop to track. Several methods exist of generating sine wave references, including Infinite Impulse Response Filters, floating point functions and trigonometric algorithms.

Speed of execution is of primary concern for the present program. The nature of the converter requires that a large number of calculations are performed during every switch cycle. Thus, a sine wave reference generator has to be selected that uses the least number of CPU instructions.

Using a lookup table requires only a single instruction, and it has therefore been selected. The sine wave values are generated by the DSP at switch-on or reset and placed into an array. The value required at a specific interval is then simply indexed through a counter. For the sine generator to comprise a single cycle, one complete sine wave has to be generated and stored in the array.

If the sine reference were updated every switching cycle (30 kHz) with an output frequency of 50 Hz, the sine wave array will comprise 600 entries. However, the 'LF2403A has only 544 words of Dual Access RAM and 512 words of Single Access RAM. Using 600 words for the sine wave array is therefore not practical.

Since the positive half of the sine wave is symmetrical around a the 90 degrees phase line, and the negative half symmetrical around 270 degrees phase line, each of these require only the first 90 degrees to be calculated. The remainder of the values can be obtained by simply indexing the array from the other side. Furthermore, the positive and negative halves are symmetrical around the time axis. Thus, only the first 90 degrees of the sine wave needs to be calculated, the remainder can be obtained through indexing variations.

For the present program, the first 150 values are calculated using the floating point sine function of the TMS320C2000 real time library. The execution time is irrelevant because this is done only after power-on or reset, before the outputs are enabled. When a new voltage reference value is required, it is determined in which quadrant the indexing counter is in, and the correct value returned through indexing either from the front or the rear of the array, and

inverting the value for the negative half cycle. This does however slightly increase the number of instructions required.

8.3.2 Compensating Equations

Current mode control is also used for the AC output converter. As was previously described, the current and voltage transfer functions of the AC output converter is identical for the forward and reverse modes, and not dependent on polarity. Thus, single voltage and current compensating equations are used for all modes of operation of the converter.

Once the voltage reference is generated, it is compared with the measured value and a new current command is generated using the voltage compensating equation. The command current is capped between a positive and negative maximum value.

The command current is then compared to the measured current and the current compensating equation is used to generate the command duty cycle, which is loaded into the compare registers. Care must be taken to reverse the error calculation for positive and negative current outputs, since a positive error must result in an increased duty cycle error when the inductor current is forward, while a negative error must result in an increased duty cycle with reverse inductor current.

The calculated duty cycle is capped between 0 and 50%. A negative duty cycle is not meaningful, as the mode and direction control bits will handle the direction and polarity of the converter.

8.3.3 Mode and Direction

The functions of the polarity and direction bits as well as their influence on the action control registers are described in section 8.2.3.3. It is however not always trivial to determine which mode the converter is in or should go to next.

After several iterations a scheme was implemented where the voltage command polarity, the current command direction and the actual inductor current direction was used to determine the mode of the converter. In addition to the four modes that can be identified using the polarity and direction bits, four additional modes were defined in which the inductor current is allowed to decay to zero before a mode change is made.

The additional four modes are identical to their corresponding normal modes in terms of polarity and direction bits, with the exception that the duty cycle is forced to zero. As is discussed in the simulation results in section 9.3.5, it was found that the duty cycle needs to be inverted when a mode change occurs. The additional modes therefore do not disturb the duty cycle variable, but merely command a zero duty cycle. Once the inductor current has decayed, the previous duty cycle is recalled and inverted. This methodology was proved through simulation.

8.4 DSP Software

8.4.1 Control Code Algorithm

The algorithm used for the actual control code that implements the voltage and current control loops and determines the switching states is given below. Please refer to Appendix B.4 for a complete code listing.

After the DSP CPU has been reset, the control algorithm executes as follows:

- Initialise all system and peripheral devices.
- Calculate sine reference lookup array.
- Start the timers and enable interrupts.
- Repeat in an infinite loop:
    - While waiting for ADC to finish
        - Store previous cycle's values
        - Calculated new sine wave reference vale
    - Wait for the ADC to finish
    - Read and scale all the measured values
    - Calculate Current Reference
        - Calculate difference between sine reference and measured value.
        - Use error in compensation equation to calculate new current reference.
        - Cap current reference to positive and negative maximums.
    - Calculate Duty Cycle
        - Calculate difference between command and measured value, correct polarity if required.
        - Use error in compensation equation to calculate new duty cycle.
        - Cap duty cycle between 0 and 50%
    - Determine Mode and Direction
        - Force inductor current measurement to zero if small.
        - Use current and voltage command as well as current measurement to determine polarity and direction.
        - Set MASK bit if inductor current is to decay as soon as possible.
    - Test for Mode Change
        - If true, invert duty cycle if voltage and current are not crossing over together.
    - Update Values
        - If MASK is set output 0% duty cycle, otherwise output true duty cycle.
        - Update PWM control bits with mode & polarity information
        - Update comparators with new duty cycles

The following comments may be made regarding the algorithm:

8.4.1.1 Timer Interrupts

Timer 1 generates an interrupt when the period compare match is made. The interrupt starts the ADC via hardware, while the Interrupt Service Routine (ISR) for GPT1 increments the sine reference counter. Timer 2 interrupts are disabled.

8.4.1.2 ADC Interrupts

ADC interrupts are disabled. The conversion busy flag is constantly monitored. Once the flag is cleared (conversion finished) the main control program is executed.

8.4.1.3 Control History

The z-transform of the forward mode transfer function requires that the current and last value of the reference, measured and command output values be stored. For the mode change detected, the previous cycle's Positive and Forward bits are also stored.

8.4.2 Code Execution Period

The version of Texas Instrument's Code Composer Studio available to the author did however not support time profiling of code. The code execution time was therefore checked through hardware. For this purpose an output bit was toggled each time the main program was completed. This bit was compared to the PWM outputs to gauge the execution time of the program.

As is shown in section 11.3.2, the DSP program could not execute at a rate of 30 kHz. In fact, the code executed at just above 15 kHz. After several attempts of code optimization, it became clear that the program could not retain its functionality and execute at 30 kHz.

Several options were investigated, including rewriting the code intensive portions of the program in Assembler. As a quick test, it was decided to re-digitize the compensation equations at 15 kHz, using Matlab, which is a trivial task. The equations are the only sections of the program that are sampling rate sensitive. It was found that this lower speed did not affect the operation of the converter largely, and sufficient time was not available for an Assembler rewrite.

It was therefore decided to leave the program as is (apart from the compensation equations) and accept the lower sample frequency of 15 kHz for the tests.

To ensure that the main program execution is started exactly every second switching period, an additional bit is toggled in the GPT1 Interrupt Service Routine. The main program checks this bit before executing.

8.5 Chapter Conclusion

This chapter described the design of the software that implements the control methodologies developed in Chapter 7.

The configuration of the on-chip peripherals are discussed in detail, since they are instrumental in implementing the control methodologies.

The actual control code algorithm are also discussed, as well as the execution speed of the control code.

This chapter concludes the actual design of the converter. The software developed in this chapter is used in both the simulation described in Chapter 9, as well as in the prototype converter that was tested in Chapter 11.

9 Converter Simulation

9.1 Introduction

The aim of simulating the converter is to verify the operation of the power and control components before they are committed to hardware. This identifies potential problems early on in the design cycle, and greatly reduces the amount of hardware faultfinding and software debugging needed on the physical prototype.

Although it is customary to separately simulate the power and control components, a more realistic and much more meaningful simulation can be made if the power and control components are simulated simultaneously in the same model. For this purpose, a simultaneous simulation was developed using Simplorer from ANSOFT. Simplorer has the ability to simulate both hardware models as well as software models in C and VHDL. The simulation method uses a single VHDL model block in which the entire control system is contained.

This chapter discusses the simultaneous simulation method, as well as the results of the simulation. Several of the problems identified in the original design are highlighted. The final results validate the operation of the proposed converter topology.

In addition to verifying the operation of the converter, the simulation results also served as reference for the results of the prototype tests.

9.2 Simulation Models

9.2.1 Power Component Models

For the power electronic components, the circuit was redrawn in Simplorer using system-level simulation models. The individual components have already been selected and qualified for use in the converter, so that system-level, as opposed to device level, models were used.

To reduce the circuit complexity, the transistors that make up a single switch were grouped and represented by a single transistor whose parameter values reflect the combination.

Furthermore non-ideal values for all the components were included to render the simulation as realistic as possible. The values estimated however failed to show the large ringing effect observed during physical converter testing.

The Simplorer schematic with the purely resistive load case is shown in Appendix A.12.

9.2.2 Control Model

It is customary to design the control system using continuous transfer functions, and then digitize the final compensation equations (as in Chapter 7). Consequently, the control system is also usually modelled in simulations using continuous models (i.e. transfer functions, ramp voltage generators and comparators). It is however considerably more useful to model the system in a high-level software language, since the simulation therefore also acts as software functionality verification. This also greatly simplifies the circuit complexity. The control system was therefore modelled using a single VHDL-AMS model. Although this model is a single component on the schematic sheet, it embodies the entire control system.

Simplorer has the ability to model both C and VHDL languages. Conceptually it would seem advantageous to model the control system in C, since the code could then be ported directly to the DSP. However both the DSP and Simplorer have significant amounts of initialisation and other non-control code, which prevents direct portability. It was therefore decided to model the control system in VHDL-AMS, as this was the simplest method and would focus on the functionality of the control methodology, and not on implementation specific details.

VHDL with Analogue and Mixed Signal (AMS) extension was selected so that the control model could directly interface with the power component models using real values. (VHDL Reference Manual, 1997) and (VHDL Mini Reference, -) were used as general VHDL Language References. (Randewijk and Mouton, 2006) and (Knorr and Devarajan, -) were used as references for the AMS extensions.

The VHDL code listing is given in Appendix B.5. The following sections describe the VHDL code.

9.2.3 VHDL Code

The VHDL code simulates both the DSP software as well as the DSP hardware. Although, for the sake of simplicity, the distinction was not made in the modularization of the code (i.e. hardware and software simulation code was not contained in independent functions, procedures or models). However, the different code sections were however kept separate in one entity.

9.2.3.1 DSP Hardware Model VHDL Code

The TMS320LF2403 has a multi-channel ADC as well as several PWM generators built in. In this simulation it was only necessary to simulate them at a system-level, that is, their functionality and not their structure.

The VHDL entity declaration specified the connections of the model with the power components. The ports defined consisted of the four Analogue inputs, eight PWM outputs and the clock signal. In addition, four analogue (type real) test outputs were provided that enables the monitoring of signal and variable values within the VHDL model during simulation. This was done since

Simplorer does not support real-time debugging of the VHDL code. The four outputs were used for the following signals:

Test1: Voltage Reference
Test2: Current Reference
Test3: Duty Cycle Reference
Test4: Converter State (A variable used to display the polarity and power flow direction of converter)

The input clock was set to 40 MHz, the same as for the DSP.

The ADC was simulated by multiplying the input values with factors to represent the gains of the analogue amplifiers and the ADC. Counters were used to determine the moment at which the ADC would start the conversion, and the model input ports were read at that instant.

The PWM generators were simulated using counters that count continuously up and down. Compare registers were created with which these counters were compared to. Furthermore, a register containing the mode of each output (i.e. Forced High, Forced Low, Active High and Active Low) was implemented to mimic the operation of the ‘2403 output pins.

9.2.3.2 Software VHDL Code

In order to verify as much as possible of the control code for functionality, it is desirable to have the structure of the VHDL code identical to the software for the DSP. This is not always possible, since the focus in the simulation is to make fault finding as easy as possible, while the focus for the DSP software is to ensure fast code execution. The structure of the VHDL and C programs therefore differ somewhat, but their functionality is identical.

The design of the DSP software was an iterative process, with both the implementation details of the DSP (as discussed in Chapter 8) as well as simulation results driving the software design

9.3 Software Problems Identified Through Simulation

The simulation of the converter provided the first realistic evaluation of the converter and control operation, and several problems with initial design decisions were found. The following paragraphs describe the most important problems encountered and their solutions.

9.3.1 Sampling Period

Initially it was planned that the ADC would only measure the actual values at a rate of 3 kHz, or 10 times slower than the switching frequency. The simulation showed that this would be impossible, since the inductor current could increase from zero to its maximum value during this time. This can be explained by recalling that the current ripple is 5% (originally 10%), meaning

that in 10 switching periods (recall that the converter is switched twice per switching period) the maximum output current could be reached.

This required much quicker sampling of the actual values. The final version of the simulation sampled the values at the switching period, which is every second transistor switching interval. This improved the dynamic response greatly, but also required that that the main program code finishes before the next interrupt is generated. This was unfortunately not the case, and the sampling had to be performed every second switching cycle, as discussed in section 8.4.2.

9.3.2 Inductor Size

The inductor was originally sized to produce a 10% current ripple. As discussed above, this could result in the inductor current changing by its maximum anticipated value in only 5 switching cycles. The simulation showed that the DSP would not be able to control this rapidly changing current effectively.

The inductor size was consequently doubled to produce a 5% ripple current, which the simulation proved the DSP could control. The new inductor value was at the limit of the selected core's capability.

9.3.3 Output Capacitors

The converter was originally designed with output capacitors of 1.6 uC. This value was calculated from harmonic distortion considerations. The simulation showed that the output voltage changed very rapidly with this value, up to the point that it became difficult to control the output voltage without causing significant voltage oscillations. Even the doubling of the inductance value did not result in satisfactory voltage oscillations.

To alleviate this, the capacitor's size was increased to 3.2 uC, which significantly reduced the voltage oscillations and made the converter controllable.

9.3.4 Mode Control

A simple method of determining the converter polarity and direction was considered based on the measured output voltage and the command current direction. The simulation showed that this resulted in situations where a mode change is made without regard to the inductor current, leading to open-circuiting of the inductor and associated large voltage spikes. These spikes would have undoubtedly destroyed the transistors of the real system.

A new methodology was adopted whereby the inductor current is also taken into account. For the cases when a mode change is required, but the change would result in no freewheeling path for the inductor current, four additional modes were introduced. These additional modes have the same polarity and direction as the current mode of the converter, but force the duty cycle to zero

to let the inductor current decay to zero. Once the inductor current has decayed to a safe value (chosen as 150 mA) the mode change is made.

9.3.5 Duty Cycle Continuity

The simulation showed that the slower duty cycle change associated with the current compensation equation caused significant current and voltage spikes when a mode change occurs. This occurs when a high duty cycle is commanded during one mode (e.g. a reverse mode with a low output voltage where the inductor current changes slowly), but in the next mode (e.g. a forward mode) the inductor current would change rapidly with the same duty cycle. While the duty cycle is ramped down from the high to the low value, significant current and voltage spikes developed.

Initially it was attempted to address this problem by forcing the duty cycle to zero each time a mode change occurred. This alleviated the problem in some instances (specifically when the duty cycle was high before the mode change), but not visa-versa.

It was realised that the duty cycle for the new mode should be matched to that of the previous mode during a mode change, so that the current will not experience significant spikes. This is much more easily accomplished than it at first appears.

Firstly consider the fact that a mode change between the forward and reverse modes occur every time either the current or the voltage crosses through zero. The only exception to this rule is when the current and voltage cross over at exactly the same time. Secondly, since the inductor current must be continuous, either M1/M2 or M3 must always be on. Thus, the sum of the duty cycles of M1/M2 and M3 must be 0.5.

Consequently, when either the voltage or the current crosses through zero, the duty cycle must be instantaneously inverted. That is, $D_{after} = 0.5 - D_{before}$. This ensures that the waveform applied to the inductor during the new mode is identical to before the mode change. Thus, all that is required is to detect a mode change between forward and reverse modes, make sure that both voltage and current are not crossing over together, and invert he duty cycle if this is not the case.

For the modes that apply zero duty cycle to force the inductor current to decay to zero, the above method does not hold true, since the duty cycle will then always be set to 50% (the maximum value) when the next mode change occurs. To address this, a mask bit was introduced so that the stored duty cycle during these modes are not changed, but only a zero valued output is given to the power section. When a mode change occurs, the previously stored duty cycle is inverted and applied.

The above method was successfully implemented in the simulation.

9.3.6 Current Error Calculation

When the output voltage is negative, it was found that the controller would command zero duty cycle continuously. The problem was traced to calculation of the current error. When a negative current is commanded, a negative current error means the duty cycle should be increased, since the actual inductor current is too small in the reverse direction. This is exactly the opposite of the positive mode.

The first attempt was to take the absolute value of the current error. This however resulted in the duty cycle increasing for both positive and negative current errors. The final solution was to invert the current error when a negative current is commanded, while capping the duty cycle between 0% and 50%.

9.4 Simulation Load Cases

In order to provide a realistic simulation of the converter, three load cases were simulated. These load cases represent unity, lagging and leading power factors.

- A purely resistive load of 52.8 Ohm. This gives and RMS output of 1000 W.
- An inductive load consisting of the 52.8 Ohm resistor in series with a 117 mH inductor. This results in a lagging Power Factor of approximately 0.7.
- A capacitive load consisting of the 52.8 Ohm resistor in parallel with a 60 uC capacitor. This results in a leading Power Factor of approximately 0.7.

In all cases the simulation was run for 25 ms, or 1.25 50 Hz cycles.

For the resistive load the reference sine wave was started at an arbitrary phase angle of 150 degrees. For the inductive and capacitive loads the sine wave phase angle at t = 0 is 0 degrees.

9.5 Simulation Results

For all simulation results, the following channel assignments were made:

- Yellow: Internal DSP reference sine wave. Scaled to read in Volt.
- Light Grey: Output Voltage
- Blue: Internal DSP current command, scaled to read in Amps x 10.
- Cyan: Inductor current scaled by a factor of 10.
- Green: Internal DSP duty cycle, scaled to read between 0 and 100 for duty cycles between 0 and 0.5.

- Red: Internal DSP Mode Variable. Used to indicate the mode the DSP is in (see VHDL in Appendix B.5).

9.5.1 Resistive Load

Figure 48 shows the output of the converter closely tracking the reference sine wave once the initial transients have dissipated.

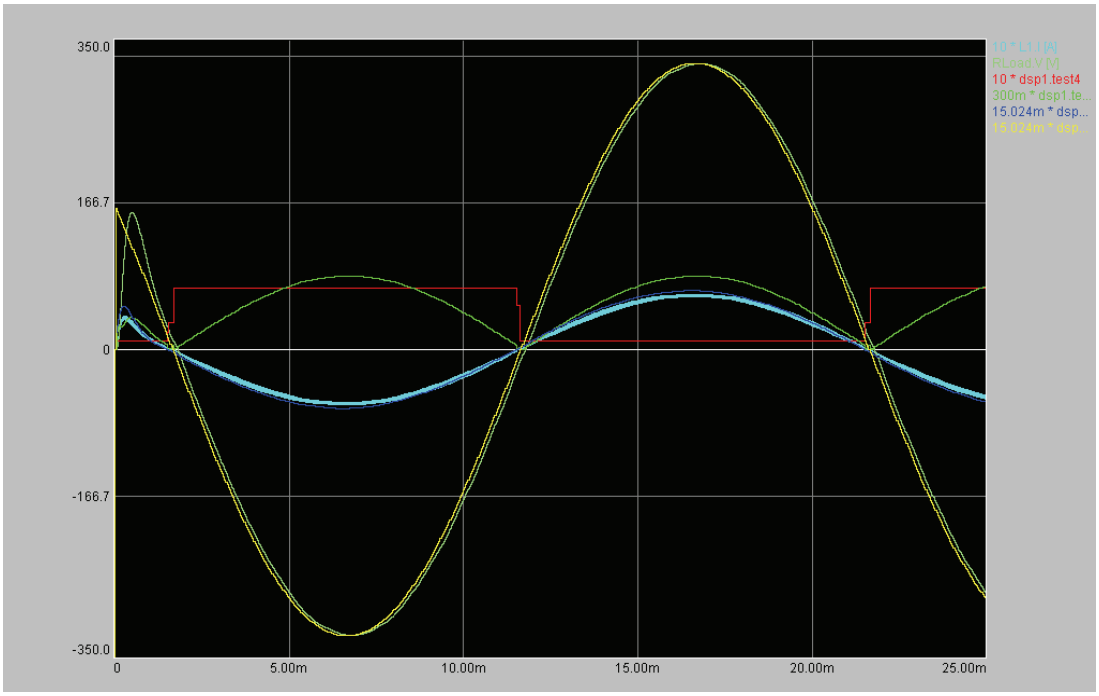

Figure 48: Resistive Load Simulation, Output

A slight phase lag of approximately 13.8 us is evident, which agrees very well with the value of 14.3 us previously calculated from the closed loop converter response (section 7.4.3). Since the load is purely resistive, the output voltage and current are in phase. The peak output voltage is within 0.5 V of the reference voltage peak.

Figure 49 shows a magnified view of the initial transients of Figure 48.

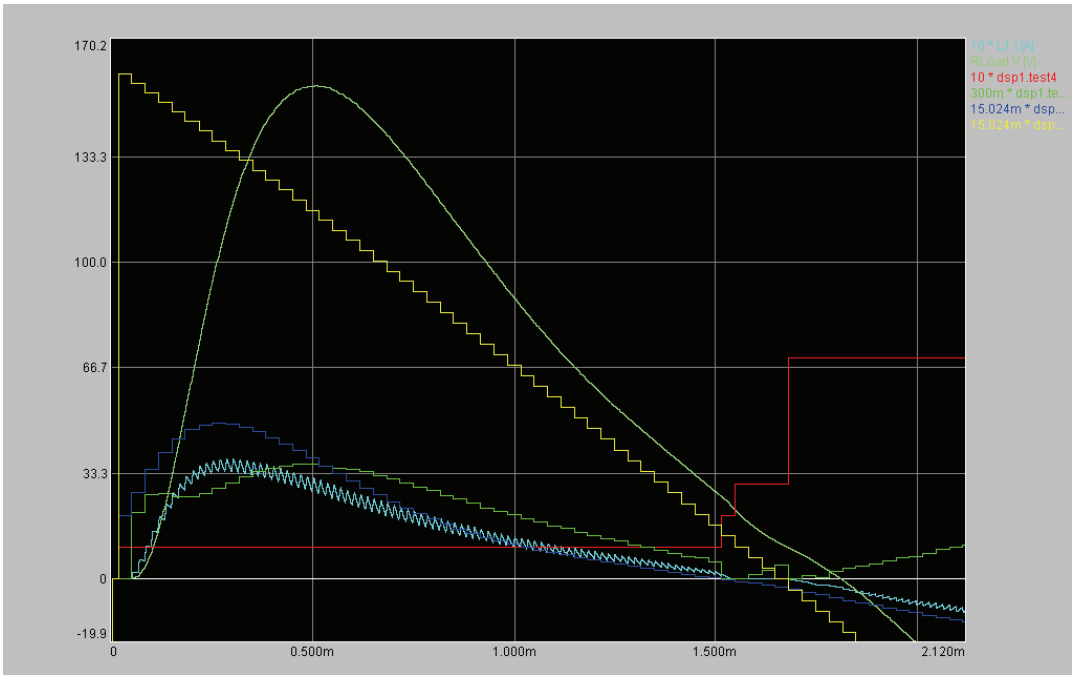

Figure 49: Resistive Load Simulation, Initial Transients

The converter output settles down after a period of only approximately 1 ms. Almost no oscillatory behaviour is visible, as was predicted by the flat closed loop system response Bode plot.

9.5.2 Inductive Load

The inductive load simulation results of Figure 50 shows the large current phase lag as well as the reduced current magnitude due to the series inductor. When the inductor current and output voltage are of opposite magnitude, the converter is in reverse mode and regenerating energy back into the batteries.

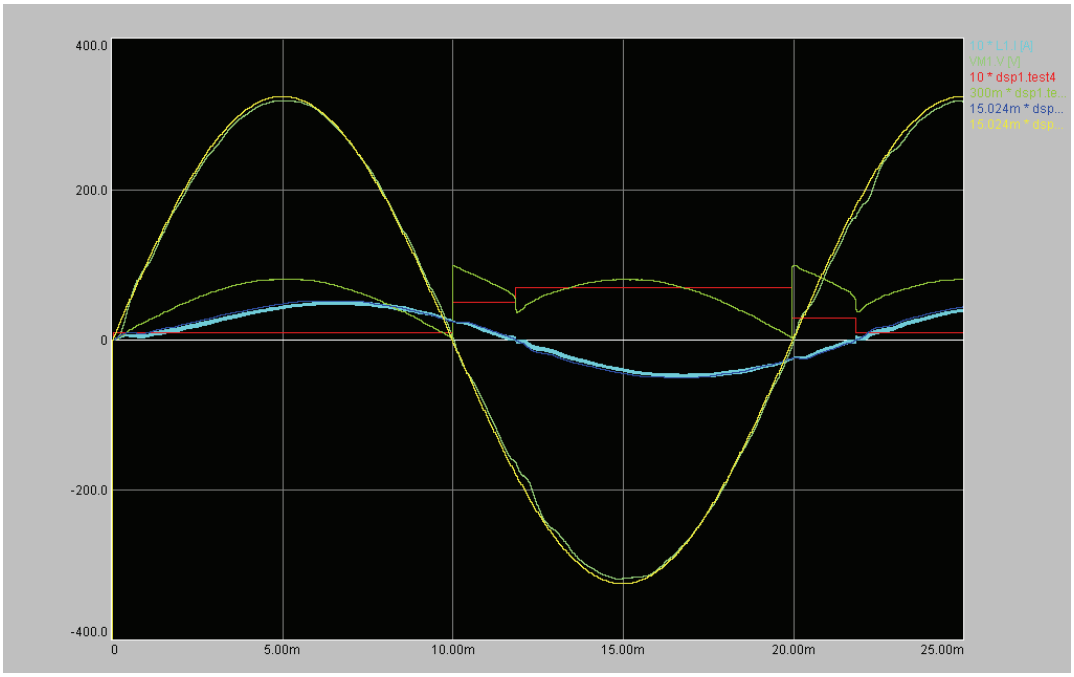

Figure 50: Inductive Load Simulation, Output

The initial transients dissipate within 0.5 ms, and it should be noted that the output voltage peak is slightly lower than the reference peak. Some distortion is evident during the zero current crossover, as shown in Figure 51:

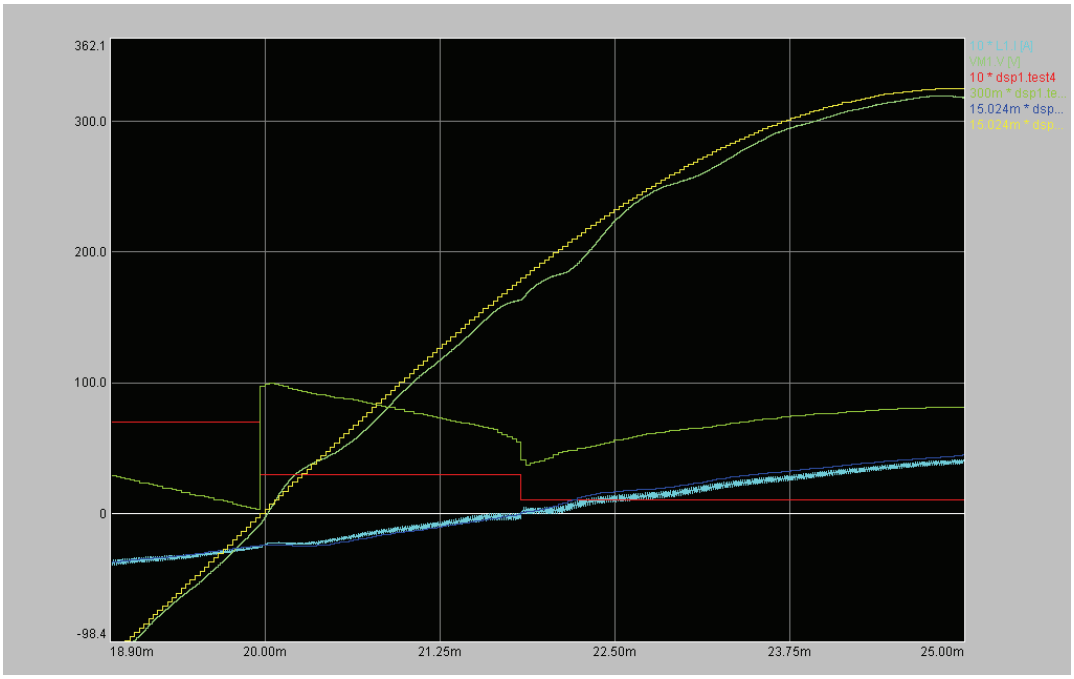

Figure 51: Inductive Load Simulation, Crossover Transients

Note that the duty cycle inversion at the mode changes (voltage and current) in Figure 51 results in a continuous command current and almost continuous inductor current.

The transient at the zero voltage crossing is caused by the reduction in gain at low output voltages. Since the output voltage is low, even a large duty cycle cannot force a significant change in inductor current for a reverse mode. Since this gain changes slowly it was not included in the small signal model, but it does have an effect at mains frequencies.

The transient at the zero current crossing is due to the inductor current becoming discontinuous. The inductor current cannot change direction before it has not completely died down. Thus, during this time the average inductor current is not equal to the command current, and output voltage distortion occurs. Since the inductor acts as a high-pass filter, the voltage distortions are more visible than for the resistive and capacitive loads.

9.5.3 Capacitive Load

Figure 52 shows the inductor current as leading the voltage reference, as is expected from a capacitive load. In order to charge the output capacitor, maximum current (12.5 A) is commanded for the first few milliseconds. Note the larger inductor current due to the decreased load impedance (due to the parallel capacitor), and that the output voltage is larger than the reference (as opposed to smaller with the inductor).

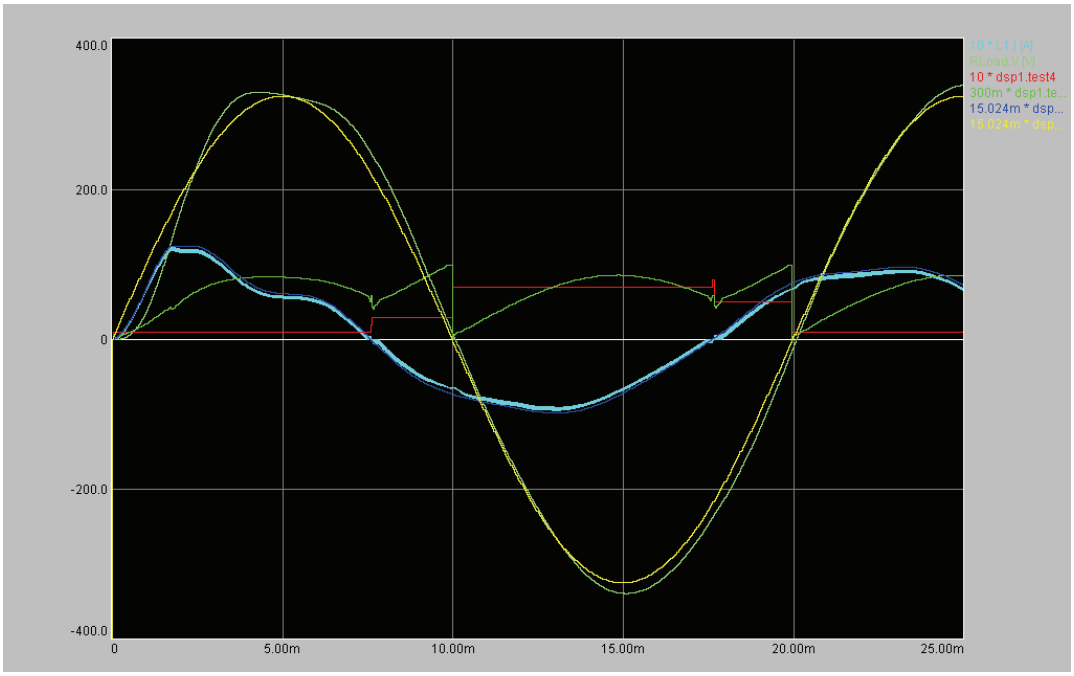

Figure 52: Capacitive Load Simulation, Output

The output with a capacitive load is slightly more oscillatory than the other load cases, but still acceptable. The crossover transients are much smaller than for the inductive case, since the load capacitor attenuates high frequency disturbances and smooth the output waveform.

Figure 53 shows a magnified view of the voltage and current crossovers.

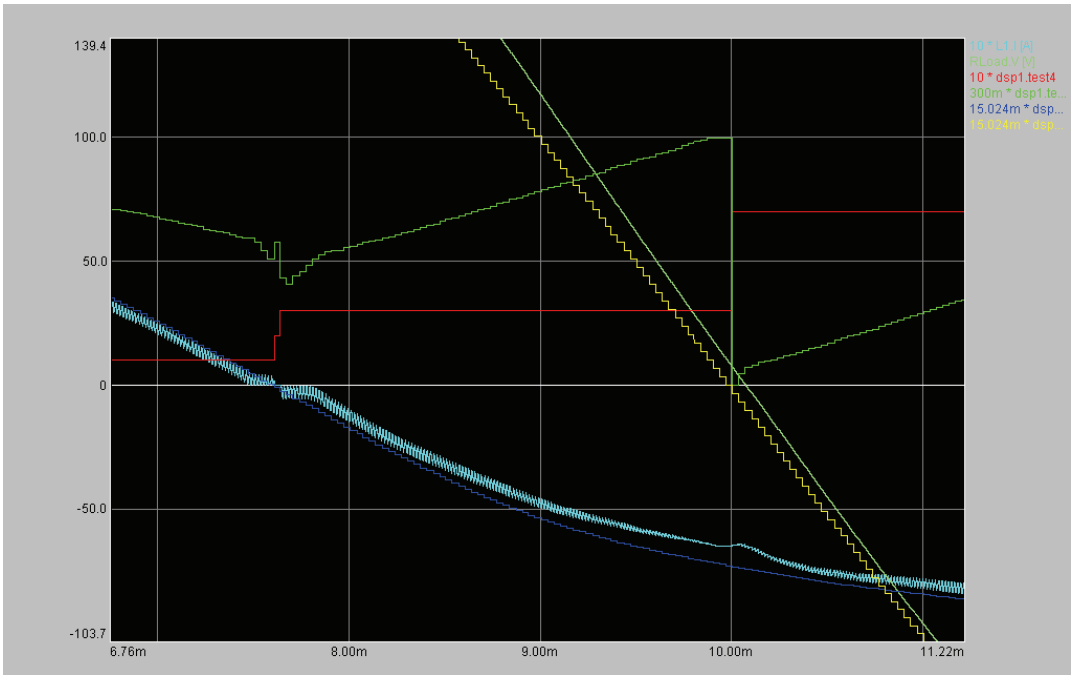

Figure 53: Capacitive Load Simulation, Crossover Transients

The transients in the inductor current in Figure 53 can again be attributed to discontinuous inductor current (at t = 7.5 ms) and low current loop gain at low output voltages (at t = 10 ms).

Note that just before t = 10 ms the converter is in reverse mode (voltage and current polarities different) and full duty cycle is commanded by the DSP, but the inductor current remains unchanged. After t = 10 ms the converter is in forward mode (voltage and current same polarity) and a small duty cycle command causes the inductor current to rapidly decrease. This clearly shows the low current loop gain effect at low output voltages.

9.6 Simulation Conclusion

The converter was simulated with realistic values and load cases, and has proved to operate as intended.

Overall the simulation was an excellent method to validate the power section design, as well as the control methodologies and software. Several serious problems with the original designs were identified through the simulation, and solutions to these problems could easily be tested in the simulation.

The fact that the verified and proven VHDL code could be converted to C and directly ported to the DSP greatly reduced the amount of debugging required on the DSP. The risk of damage to the converter components through erroneous controller operation was also greatly reduced.

The process of simulating the power and control components in a single simulation does have the drawback of being very resource intensive. The time

step for the simulation needs to be at most half of the clock input period for Simplorer to compile the simulation. With a clock period of 25us (40MHz clock), running the simulation for only a couple of milliseconds takes several hours.

In hindsight more effort could have been done to select realistic values for the transformer winding inductances. This would have highlighted the ringing effect observed during prototype converter testing early on in the development cycle.

10 Physical Implementation and Commissioning

10.1 Chapter Introduction

This chapter briefly describes the physical construction of the prototype converter. It also presents photographs of the completed converter.

It only covers aspect of the construction not previously described in the chapters in Chapters 4 to 6 on hardware design.

10.2 Enclosure, Mounting and Cabling

10.2.1 External Connectors and Circuit Breakers

The converter has external connectors for the mains voltage, the output and the battery connection. For the two high voltage connections (mains and output) standard IEC three pin sockets were used. A male socket was used for the mains connection and a female one for the output, in order to prevent accidental contact with live pins. Each socket was wired to the High Voltage PCB through a 15 A magnetic circuit breaker and both earth connections were connected to a stud on the heat sink.

The battery connection consists of M5 bolts that are fixed through the non-conducting Polycarbonate end plate of the heat sink. The bolts are internally wired to the Low Voltage PCB through a 50 A magnetic circuit breaker, while the external threads of the bolts provide means for connecting the batteries.

All the circuit breakers were mounted in the lower part of the heat sink top cover.

10.2.2 Power PCB's

In order to provide easy access to power transistors during construction and during maintenance, all the transistors were mounted on a removable aluminium plate of 4 mm thickness. The Low Voltage and Mid Section PCB's were mounted onto the plate. The plate was bolted to the heat sink and thermally bonded with conducting paste, but could be removed to access individual transistors.

The high-voltage PCB was directly mounted to the heat sink using the mounting rails of the heat sink.

10.2.3 Driver PCB's

The drivers were inserted onto the pins of the transistors protruding through the Low Voltage and Mid Section PCB's. No additional mechanical support was provided.

10.2.4 DSP and Control Power PCB's, Cabling

The DSP and Control Power PCB's were mounted upside down in the heat sink top cover. This was done so that all their connectors point downward towards the power PCB's, thereby greatly simplifying the cabling within the converter.

The interconnection cables were made of sufficient length to enable the top cover to be removed and placed alongside the heat sink, in order to facilitate ease of testing and maintenance.

The control transformer was mounted to the top end plate of the heat sink, next to the High Voltage PCB.

10.3 Converter Prototype Photographs

Figure 54 shows the completed converter prototype. Note the external connections for the battery, mains grid and user equipment.

Figure 54: Converter External Connections

Figure 55 shows the internal layout of the converter, as well as the interconnections between the various Printed Circuit Boards. It was found that the manufacture of the wiring harnesses was much more labour intensive than anticipated, and future designs will attempt to reduce the number of interconnecting cables.

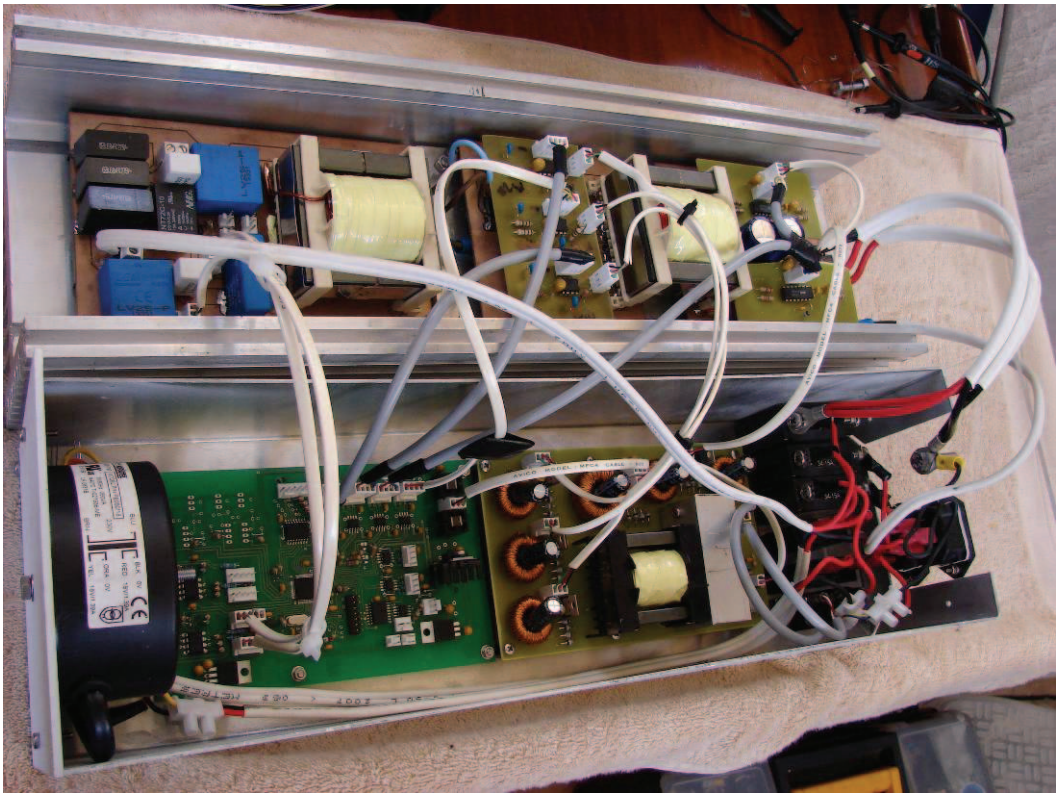

Figure 55: Converter Internal Layout

11 Measurements and Results

11.1 Chapter Introduction

This chapter reports the results of measurements made with the converter in an experimental setup.

The experimental and measurement setup is briefly discussed. Thereafter measurements are shown that verifies the correct operation of the various sub-systems of the converter (e.g. power supply, DSP controller).

Once the correct operation of sub-systems were verified, the converter was operated in DC output mode. This verified the operation of the converter in all four quadrants, namely positive and negative output voltages with positive and negative power flow. A ringing effect was discovered during these tests, which impacted significantly on the operation of the converter. However, the DC operation of the converter was proven. The DC efficiency of the converter in the forward mode is also reported.

Lastly, the results of measurements with the converter operating in closed-loop AC mode are reported. These results confirm that the converter is capably of feeding AC loads of any power factor.

11.2 Experimental and Measurement Setup

11.2.1 Equipment Used

In the interest of safety, and to test the converter in a controlled method that would prevent damage, the converter was not connected to the mains supply or batteries. A regulated and overload protected power supply was used as input source. This power supply is rated at 30 V and 20 A output, which limits the maximum input power to the converter to 600 W.

Measurements were conducted using a 40 MHz, 100 MS/s Digital Storage Oscilloscope. In some instances an analogue oscilloscope was more suited for the specific measurements. A 60 MHz dual trace Cathode Ray Oscilloscope was therefore used. Both 10x and 100x probes were used for voltage measurements, all with a bandwidth of at least 60 Mhz. Current was measured by an AEMS K100 current probe.

Two digital multimeters were used for all DC measurements.

11.2.2 Forward Mode DC Test Setup

The 20 A power supply was connected to the battery terminals of the converter. Six 100 W, 250 V globes were used as load. The globes act as resistors, and provided an almost ideal load that could be tested at a range of voltages. Removal and insertion of individual globes enabled variation of the

load power, and their incandescence gave visual feedback of the power delivered.

Two multimeters were used to measure the voltage and current, while the input voltage and current were measured by the power supply's digital meters.

11.2.3 Reverse Mode DC Test Setup

The 20 A power supply was connected to the High Voltage terminals of the converter. To simulate the batteries, a 0.66 Ohm high power resistor was placed across the converter's battery terminals. This low resistance was required since the power supply has a maximum output of 30 V and the main transformer divides the voltage by a factor of approximately 9. The boost action of the converter can boost the supply voltage by a factor of 2-3 if required, resulting in a maximum low voltage output of approximately 10 V.

Multimeters were again used to measure the load voltage and current.

11.2.4 AC Test Setup

The most realistic AC load case would be an inductive load, for example an electric motor. However, the use of a motor complicates reduced load testing considerably. It was also not possible to procure inductors of the large values required to impart a significant phase shift that will prove the bi-directional operation of the converter.

It was therefore decided to construct a capacitive load consisting of resistors and capacitors. Almost all single-phase AC motors use a capacitor to impart phase shift in an auxiliary winding for starting and / or running. As a result AC capacitors of large size and high voltage rating are therefore relatively common. When these capacitors are combined with a resistive load, a combined load with a significant leading power factor could be created. For the experiment a 40 uC, 250 VAC capacitor was procured and placed in series and parallel with the load resistors.

For the load resistors, the globe assembly of the DC load tests was used.

11.3 Measurements: Sub-System Tests

This section details the measurements made in order to verify the correct functioning of the individual sub-systems of the converter.

11.3.1 Control Power Supply

The control power supply performed very well throughout the tests, although more than one failure of the linear 12 V regulator was experienced. This would indicate that the part is overstressed, and warrants redesign in future converters. Otherwise it provided a clean and regulated output to the DSP board and isolated supplies to the driver boards and transducers.

Figure 56 show one of the transistor gate drive signals (Ch.2) together with the power supply transformer centre tap voltage (Ch.1).

The gate drive signal shown is a 12 V pulse with a frequency of approximately 28.5 kHz. In the figures shown the duty cycle of the transistor is approx 30%, for an overall combined duty cycle for both transistors of 60%.

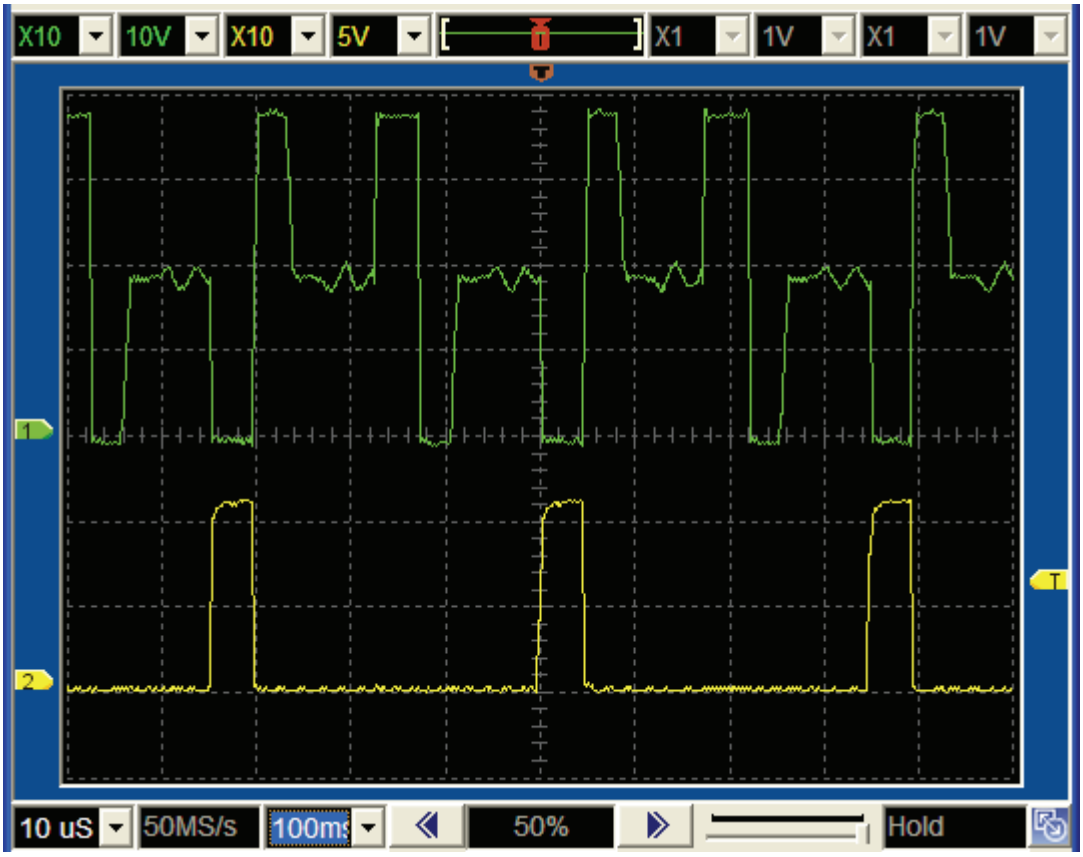

Figure 56: Power Supply, Transformer Tap (Ch.1) and Gate Drive (Ch.2)

The transformer tap voltage waveform shown Figure 56 shows that the input voltage to the control power supply is approximately 38 V. The duty cycle did not change appreciably during operation, except with a change in input voltage. Thus, the function of the half bridge converter is therefore to ensure a constant voltage on the outputs regardless of the input voltage, which can fluctuate significantly with the battery voltage.

Figure 57 again shows one of the transistor gate drive signals, (Ch.2) together with the output of one of the transformer secondary windings (Ch.1).

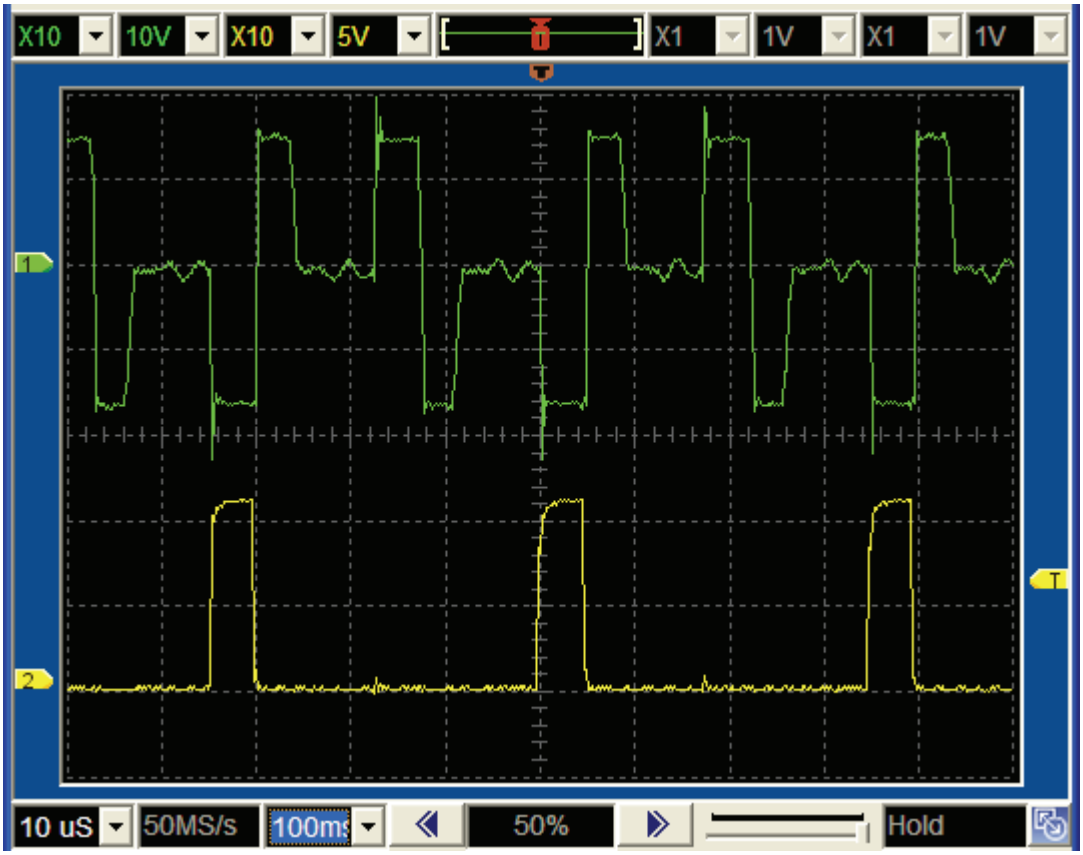

Figure 57: Power Supply, Secondary Winding (Ch.1) and Gate Drive (Ch.2)

The unloaded output voltage on the non-controlled rectifiers was approximately 0.6 V lower than on the controlled rectifier. This was due the fact that the uncontrolled rectifiers are full bridge, and have one more semiconductor junction in the current path than the controlled rectifier. This was not foreseen during development, but does not affect the operation of the power supply or the drivers.

When a load is applied to the regulated output, the converter controller increases the duty cycle to compensate, leading to an increase in the voltage of the unregulated secondary outputs. The average output of these secondary outputs was approximately 15 V, while the DSP board -12 V was -12.10 V. This secondary winding voltage can be seen as the square wave of Ch.2 in Figure 57.

11.3.2 DSP and Drivers

The DSP clock output was measured as 40 MHz with a 10 MHz input crystal frequency.

For the forward mode, MOSFET's Q1-Q4 are actively switched. Figure 58 shows the gate drive signals of the two MOSFET transistor combinations (Q1 and Q2), as measured at their gates.

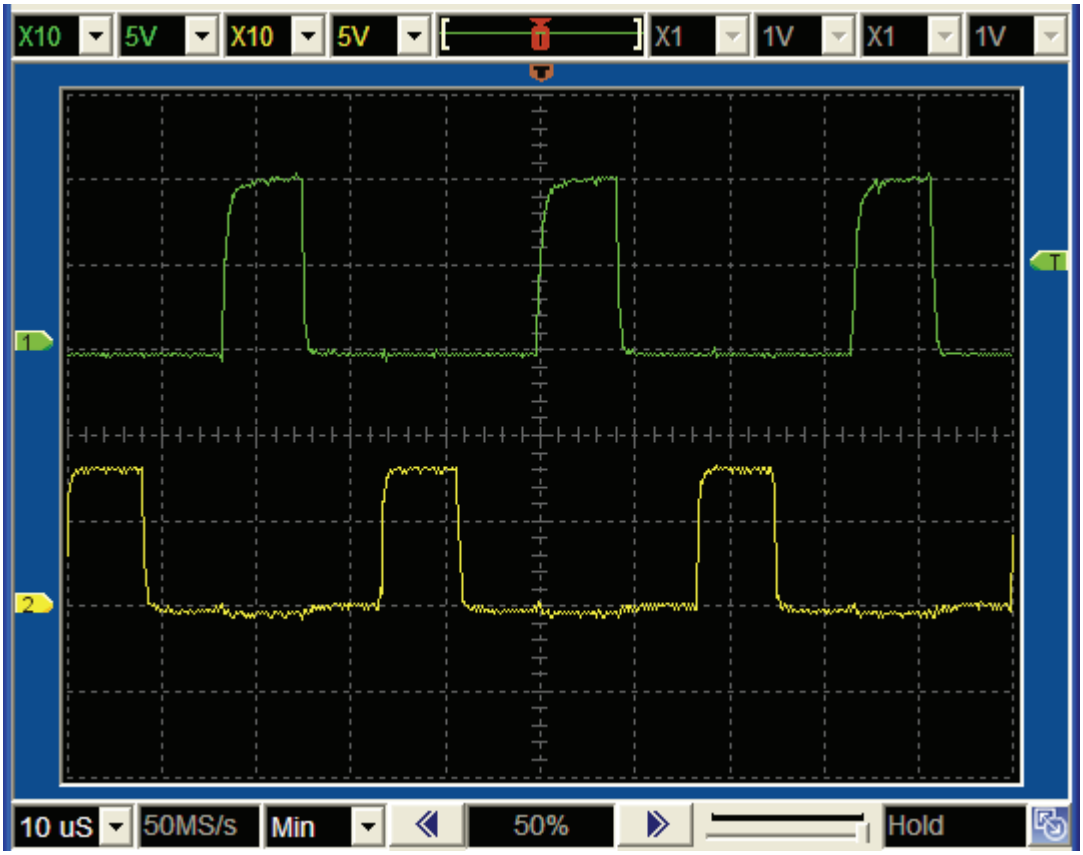

Figure 58: DSP, Gate Drive, Q1 (Ch.1) and Q2 (Ch.2)

Figure 58 shows the drive signal of Q2 on Ch.1 and Q1 on Ch.2. Both these waveforms have a frequency of 33 kHz (the switching frequency), and are exactly out of phase as expected. The amplitude of Q2's gate drive is a approximately 10 V, while for Q1 it is approximately 8 V. The 2 V difference is due to two diode voltage drops, one from being charged from the "flying capacitor" which is fed through a diode, and the other from the MOSFET body diodes that conduct to ground the source of Q1.

For the reverse mode, M1A/B and M2A/B are switched at 50% duty cycle and out of phase, as shown in Figure 59. The signals are again measured at the IGBT gates.

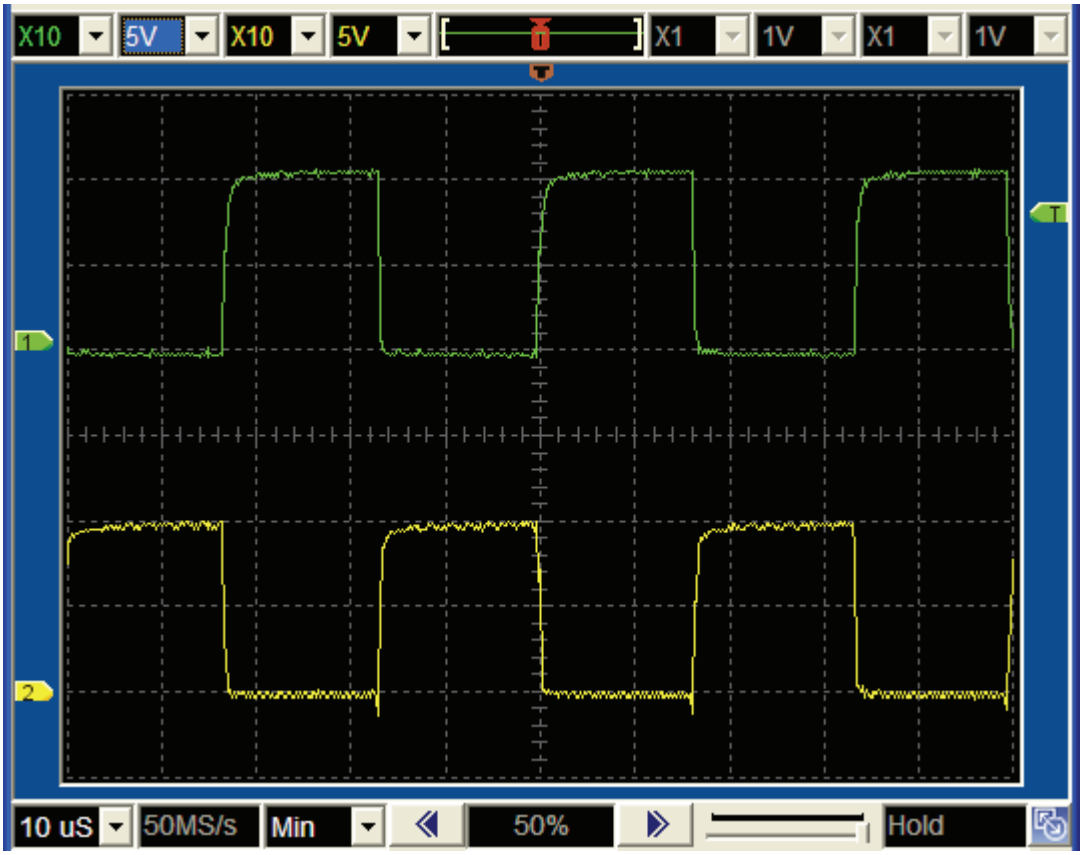

Figure 59: DSP, Gate Drive, M1 (Ch.1) and M2 (Ch.2)

In contrast with the MOSFET gate drive signals, the IGBT's waveforms are of identical amplitude, since they are fed from almost identical power supplies, which is however isolated. Note the rounded edges of the waveforms at the top of their rising edges. This clearly shows the charging of the gate capacitors through the driver resistors. Again, both waveforms have a frequency of 30 kHz, and are exactly out of phase, since during the reverse mode both M1A/B and M2A/B are switched at 50% duty cycle.

M3A/B is switched at twice the frequency of M1/M2, so that the switching of M1/M2 occurs exactly halfway during the on-period of M3. This is shown in Figure 60 where M1 is Ch.1 and M3 is Ch.2.

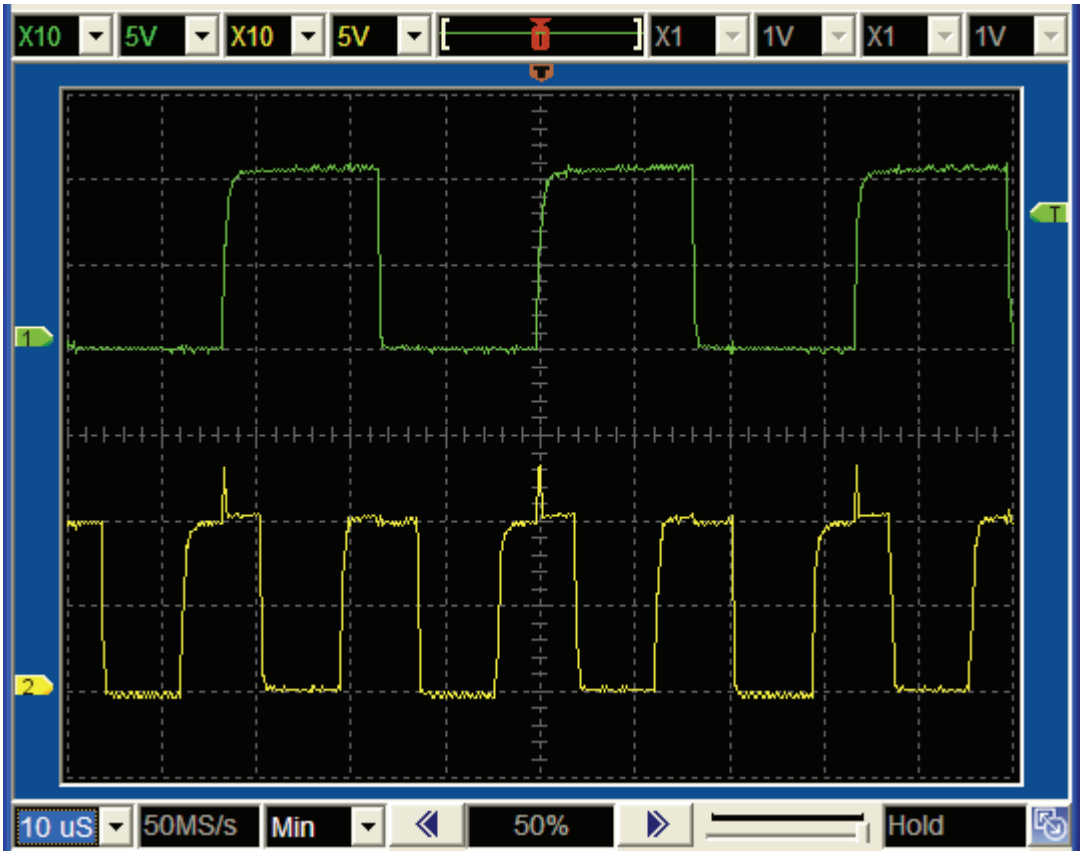

Figure 60: DSP, Gate Drive, M1 (Ch.1) and M3 (Ch.2)

Lastly, as mentioned in the section on DSP design, an output bit is toggled each time the main program finishes execution, which can then be compared to one of the PWM outputs in order to determine the execution time of the program. The software toggle bit (Ch.1) and Q2's PWM output (Ch.2) is shown in Figure 61.

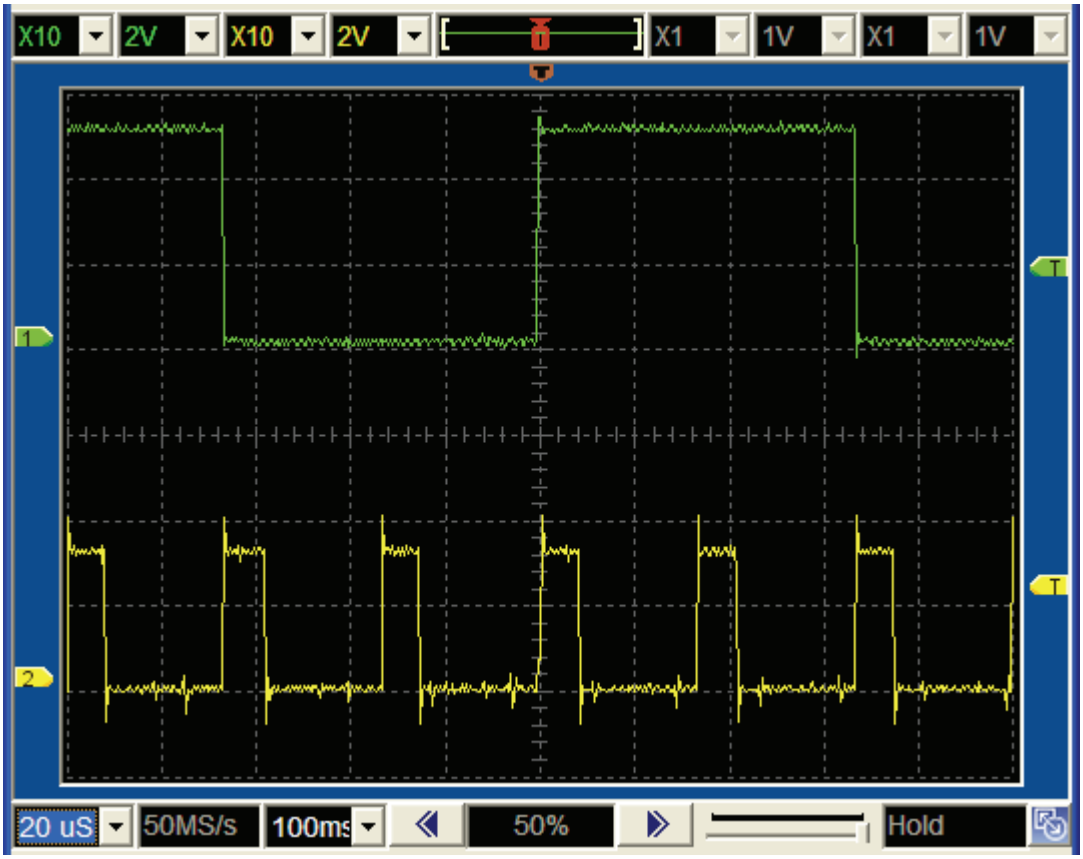

Figure 61: DSP, Execution Time (Ch.1) and PWM Output (Ch.2)

As mentioned in Chapter 8, it can be seen in Figure 61 that the code executes in slightly less than two switching periods, that is, slightly faster than 15 kHz. Since the bit is toggled at each code execution, each change in the Ch.1 trace signifies the completion of one execution.

11.3.3 Transducers and Analogue Circuits

The transducers and analogue circuitry were tested by applying DC voltages and currents to the particular transducers, as applicable, and monitoring the digitized value in the DSP using the JTAG interface.

It was found that that all transducers had some DC offset in the result registers. Slight variations were recorded between channels. The offsets were probably the result of the design of the differential op-amps, where the input impedance of the amps is finite, as well as resistor tolerances. Due to availability issues, some of the resistors used were of 5% tolerance. The measurement slope (i.e. the increase in counts per unit input quantity change) of all measurements were found to be within 10%. The offsets were easily compensated for by taking measurements at zero input, and subtracting the measurement from the result register.

Once it became apparent that full output voltage and current would not be reachable due to the ringing effect (section 11.4.1.1), and that large transients were present in the system, it was decided to boost the resolution of the measurements at the expense of range. The output resistor of the voltage

transducers were doubled in size to 120 Ohm, while the current transducer resistor was quadrupled to 270 Ohm. At the same time the measured values were divided by 2 and 4 respectively by shifting the result register to the right. These changes necessitated recalibration of the measured values.

11.4 Results: DC Tests

This section presents the results of measurements made with the converter operating in both forward and negative DC output modes, with both positive and negative output voltages.

11.4.1 Forward Mode

11.4.1.1 Positive Output Voltage

Figure 62 shows the transformer-side inductor voltage (Ch.1) as well as the inductor current (Ch.2). The converter is operating in the forward mode with a positive output at a duty cycle of approximately 50%. The inductor transformer-side voltage has a nominal value of approximately 200 VDC, for an output voltage of approximately 100 VDC (not shown). The inductor (and output) current is 1.2 A.

Figure 62: Fwd. Mode, Pos. Output, Inductor Voltage (Ch.1) and Current (Ch.2)

The most distinctive feature of the waveform of Figure 62 is the large ringing transient of the voltage at the transformer side of the inductor. For low secondary winding voltages (up to 100 V), the amplitude of the ringing is almost exactly twice the steady state value of the transformer output voltage. For secondary winding voltages between 100 V and 200 V the ringing amplitude is approximately constant. Above 200 V the Transient Voltage Suppressors added between the IGBT's outputs and the inductor clamp the maximum ringing peak at approximately 300 V. The ringing behaviour does not depend on the output voltage polarity.

With the exception of the ringing effect, the waveform is as expected. It shows that switches M1 to M3 rectifies the transformer output voltage and presents a positive square wave to the inductor. Note that the inductor current and voltage is of the same polarity, thereby indicating that the converter is indeed operating in the forward mode.

Figure 63 shows the converter again operating in the forward mode, but now with the maximum input voltage as supplied by the power supply (31.2 V) and an overall duty cycle of 90%. This represents the maximum power at which the converter operated. The nominal inductor voltage is approximately 305 V at 90% duty cycle with an average inductor current of 1.8 A. This equates to a power transfer of approximately 500 W.

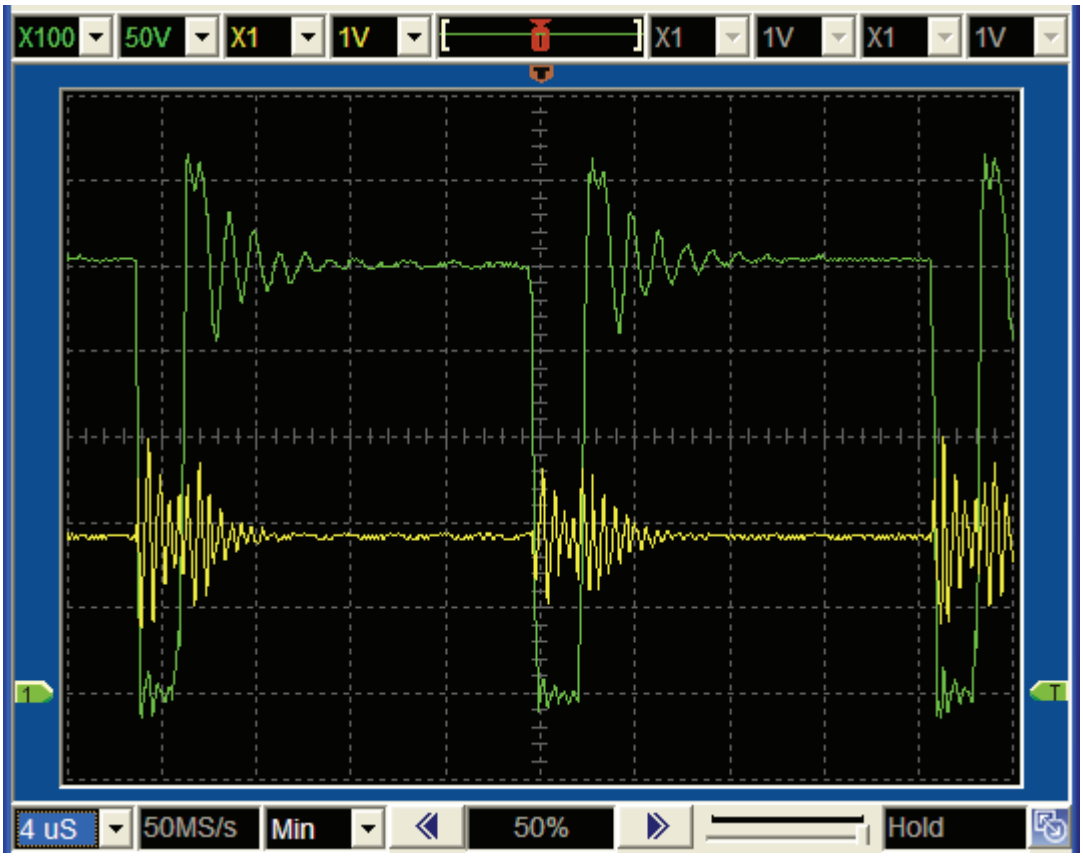

Figure 63: Fwd. Mode, Pos. Output, Maximum Power. Inductor Voltage (Ch.1) and Current (Ch.2)

Note that the two consecutive inductor voltage pulses are not exactly equal in Figure 63. The two pulse amplitudes are slightly different, and closer inspection indicates that the ringing frequencies are also slightly different. This is in detail for the reverse mode measurements, since the effect is more pronounced during the reverse mode.

Figure 64 again shows the inductor voltage at the transformer side (Top Traces), as well as the inductor current (Bottom Trace). However, the inductor voltage is now sensed with a high-bandwidth (-1 dB at 200 kHz) Hall-effect current transducer and an analogue oscilloscope. This combination provided a much higher resolution image that was possible with the AEMS probe and digital oscilloscope. The vertical scale for voltage is 10 V/div and 0.5 A / div for current.

Figure 64 shows that the large inductor voltage ringing causes a relatively large current ring.

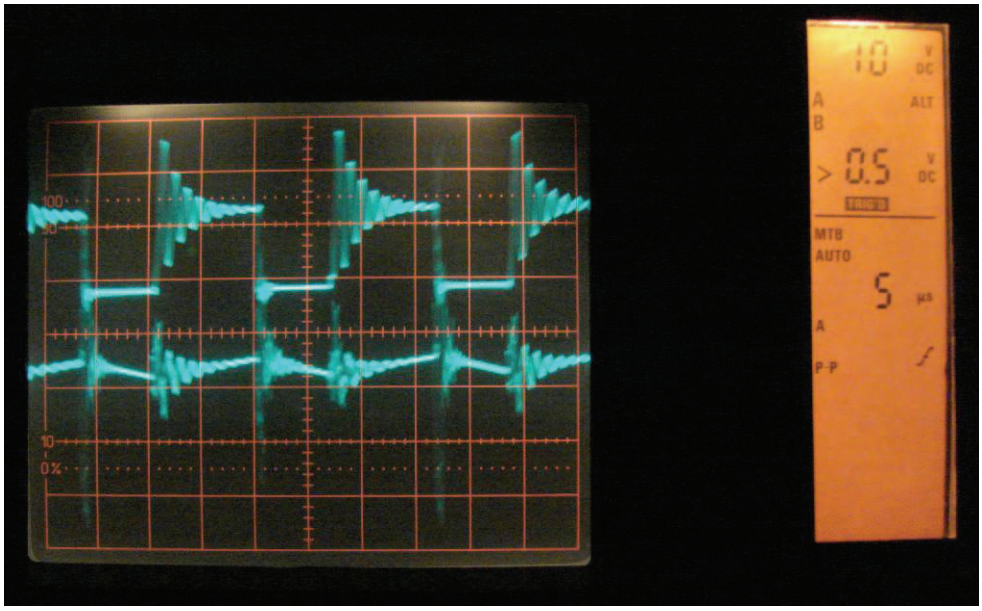

Figure 64: Fwd Mode, Inductor Voltage (Ch.1) and Current (Ch.2)

Unfortunately, the current ringing is most pronounced on the upward slope, which is where the DSP samples the inductor current. It is therefore expected that the current loop will show some distortion, probably in the form of high frequency noise, when in closed loop mode.

11.4.1.2 Negative Output Voltage

Figure 65 shows the converter during the forward mode with a negative output, obtained by turning on M1/2/3B instead of M1/2/3A. M1 to M3 again rectify the transformer output voltage to present a negative voltage to the inductor.

The nominal inductor voltage (Ch.1) is -200 V and the inductor current (Ch.2) is -1.2 A. This figure is almost the exact inverse of Figure 62, showing that the converter operation is identical for forward and reverse operating modes.

Note that the inductor voltage and current are both negative in Figure 65, again indicating that the converter is indeed operating in the forward mode.

Figure 65: Fwd Mode, Neg. Output, Inductor Voltage (Ch.1) and Current (Ch.2)

As for the forward mode, Figure 65 shows the ringing effect. If a single pulse of Figure 65 is magnified and measured with an analogue oscilloscope, the ringing effect can be more clearly seen, as in Figure 66.

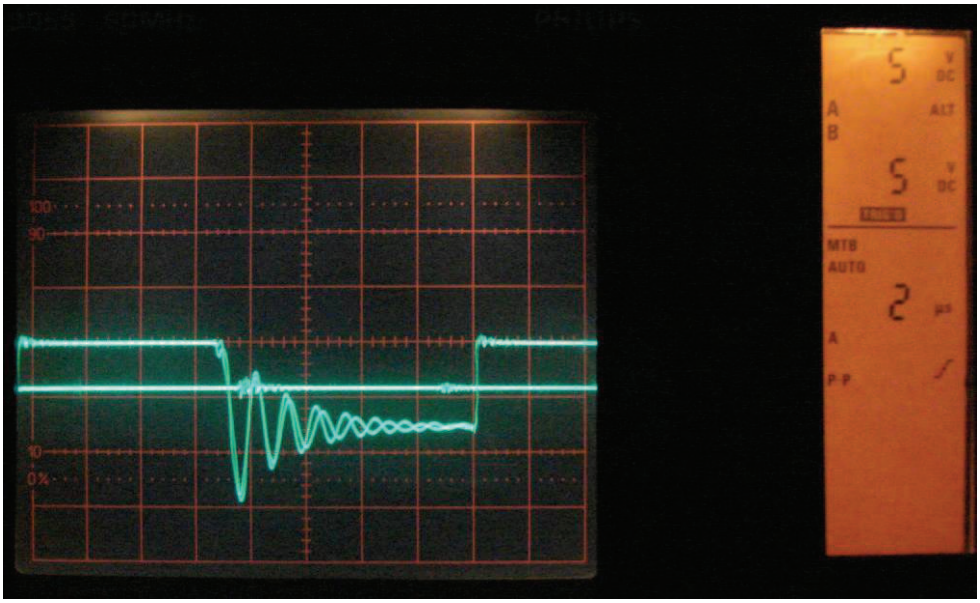

Figure 66: Fwd Mode, Neg. Output, Inductor (Ch.1) and Output (Ch.2) Voltages, Ringing Effect

An analogue oscilloscope has to be used for Figure 68 since a digital oscilloscope only stores the last waveform that was captured, thus showing only one pulse. By taking a photograph of the display of an analogue oscilloscope, the two consecutive pulses that make up a complete switching cycle can effectively be overlaid, thereby clearly showing the differences between the consecutive pulses.

Figure 68 shows that consecutive pulses contain two decaying sinusoidal oscillations that have slightly different oscillation amplitudes and frequencies. This is not due to random effects, since both waveforms represent stable steady-state signals. Since there are exactly two different waveforms, it is deduced that the differences between the two secondary windings are responsible for the waveforms.

This might imply that the ringing effect is caused by the coupling of the transformer secondary windings with the inductor. The different ringing frequencies and amplitudes may correspond to the two secondary windings having slightly different inductances. The transformer secondary winding inductance was not considered in the design of the converter.

In an attempt was made to reduce the ringing amplitude, a simple RCD snubber was placed between the inductor input and ground. This consisted of a full bridge fast diode rectifier that feeds a parallel combination capacitor and resistor. The intent was for the rectified pulses to be absorbed by the capacitor, which is then discharged through the resistors. Several capacitor sizes between 0.01 and 0.47 uF were experimentally tested, with resistors dissipating between 5 and 15 W. These attempts had little success in attenuating the ringing effect.

11.4.1.3 Low-Voltage Waveforms

Figure 67 shows the transformer primary winding (battery side) voltage. The figure shows that a +18 V and -18 V is alternately applied to the transformer primary at a frequency of 30 kHz. This corresponds to the full bridge operation of MOSFET's Q1 to Q4 with an 18 V input voltage.

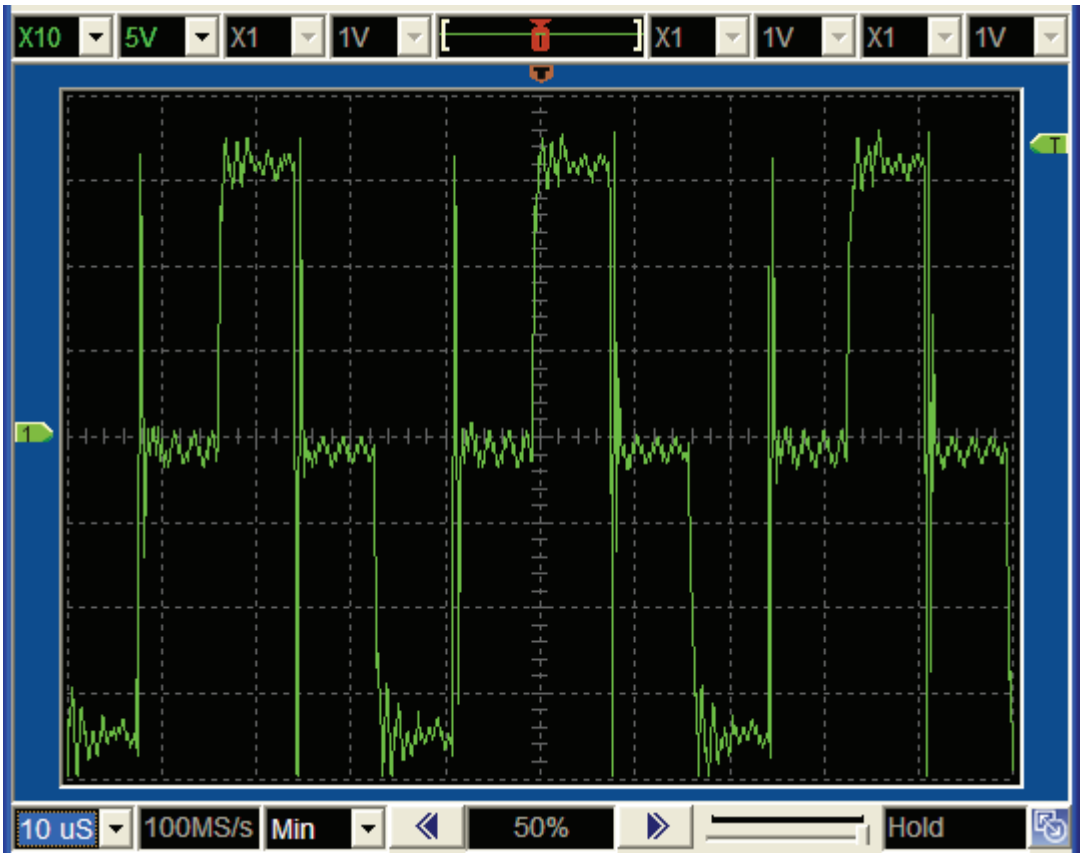

Figure 67: Fwd. Mode, Input Voltage (Ch.1)

The ringing is also present here since it is conducted through the transformer, although it is not as prevalent. This may be due to the voltage ratio of the transformer, as well as the damping effect of the capacitors.

On the other hand, the capacitors and the transformer primary may contribute to the oscillations. The ringing effect therefore warrants further investigation.

11.4.2 Reverse Mode

11.4.2.1 Positive Voltage

Figure 68 shows the transformer-side inductor voltage (Ch.1) as well as the inductor current (Ch.2). The converter is operating in the reverse mode with a positive output at a duty cycle of approximately 50%. The inductor transformer-side voltage has a nominal value of approximately 500 V, for an equipment-side input voltage of approximately 25 V (not shown). The inductor (and input) current is -1.4A.

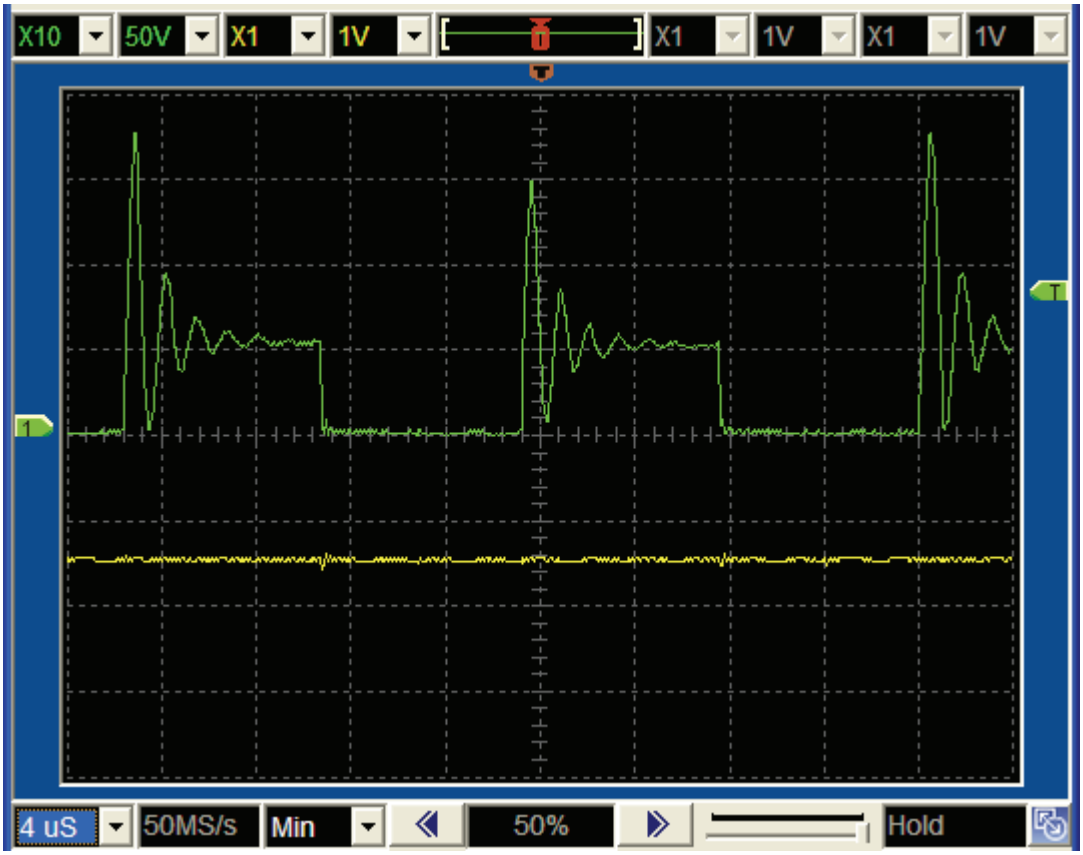

Figure 68: Rev. Mode, Pos. Input, Inductor Voltage (Ch.1) and Current (Ch.2)

During the reverse mode current is built up in the inductor via switch M3. Once M3 is switched off, the inductor current is forced through M1 or M2 into the transformer secondary winding, even though the secondary winding voltage is greater than the input voltage. Figure 68 shows this voltage boost effect, since the steady state square wave amplitude is approximately 2 times the input voltage.

The ringing effect can again be seen, and is in fact even more pronounced than for the forward mode. Note that the maximum oscillation peak is now almost 2.5 times the steady state value. Also note that consecutive peaks have different amplitudes, while every second peak has the same amplitude. This may again point to the difference in secondary winding inductance leading to different oscillations.

Note that the inductor voltage and current now have different polarities, indicating that the power flow is in the reverse direction.

11.4.2.2 Negative Voltage

Figure 69 shows the operation of the converter for a negative input voltage. The channel assignments and magnitudes of the voltages and currents are similar to those in Figure 68.

As in Figure 68, the waveforms of Figure 69 are again of different polarities, as is expected for reverse power flow.

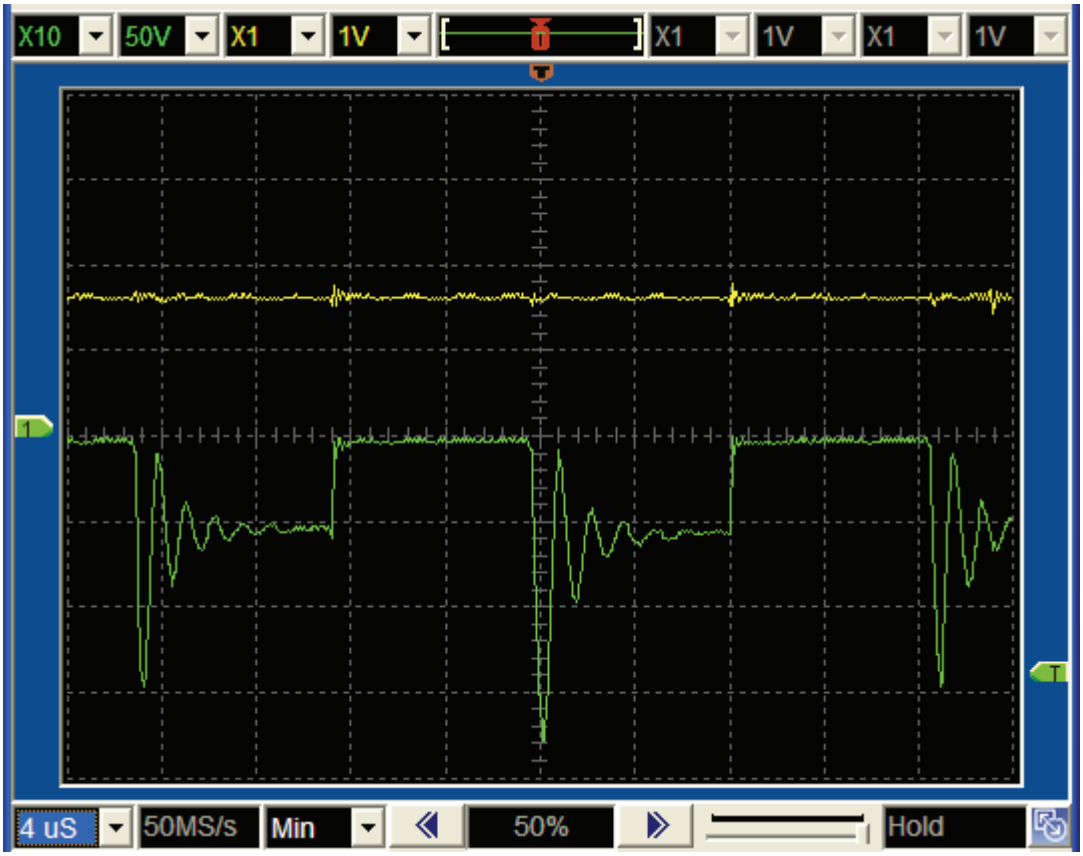

Figure 69: Rev. Mode, Neg. Input, Inductor Voltage (Ch.1) and Current (Ch.2)

For both positive and negative input voltages, the body diodes of Q1 to Q4 (who are all switched off) rectifies the transformer output voltage and presents a positive DC output to the batteries. Figure 70 shows the transformer primary voltage before rectification.

The transformer divides the voltage waveform of Figure 69 (50 V nominal) by a factor of nine. Figure 70 therefore shows an approximate square waveform with a nominal voltage of 5.6 V. Note that the ringing effect can be seen on the output waveform peaks.

Note the large oscillations in Figure 70 when M3 is switched on and the output drops to zero volt. This again indicates that the transformer secondary windings have significant inductance. Also not the gradual rise in voltage when M1 and M2 commutate (halfway between pulses). This may also be due to the secondary winding inductances.

Figure 70: Reverse Mode, Rectifier Input Voltage (Ch.1)

11.5 Results: DC Converter Efficiency

The efficiency of the converter was experimentally determined for the forward DC output mode with positive output polarity. The results are tabulated in Table 11.1 for input power values of in the range of approximately 50 W to 500 W:

Table 11.1: Converter Efficiency

Input			Output			Efficiency
Voltage (V)	Current (A)	Power (W)	Voltage (V)	Current (A)	Power (W)	Ratio (%)
7.3	7	51.1	51	0.84	42.84	83.84
11.8	9.1	107.38	84	1.05	88.2	82.14
15.1	10.5	158.55	110	1.23	135.3	85.34
18.3	11.8	215.94	133	1.37	182.21	84.38
22	13.2	290.4	162	1.52	246.24	84.79
27.3	15.1	412.23	202	1.71	345.42	83.79
31.2	16.6	517.92	232	1.84	426.88	82.42

The efficiency is relatively constant over the given input power range, varying from 82.42% to 85.34%. The efficiency peaks at approximately 160 W input power, and then declines as the input power is increased.

The efficiency is slightly less than was expected, but still acceptable.

11.6 Results: AC Tests

The preceding sections proved that the converter is able to operate in four quadrants, which is a prerequisite for AC converter operation.

This section details the measurements made with the converter operating in AC output mode. Three load cases are discussed, that of a purely resistive load, a series resistive and capacitive load, and lastly a parallel resistive and capacitive load.

11.6.1 Resistive Load

Figure 71 shows the output voltage (Ch.1) and current (Ch.2) of the converter when feeding a purely resistive load consisting of six 100W globes at an output frequency of 50 Hz. The output voltage has a peak amplitude of 35 V, with a peak current of approximately 1 A.

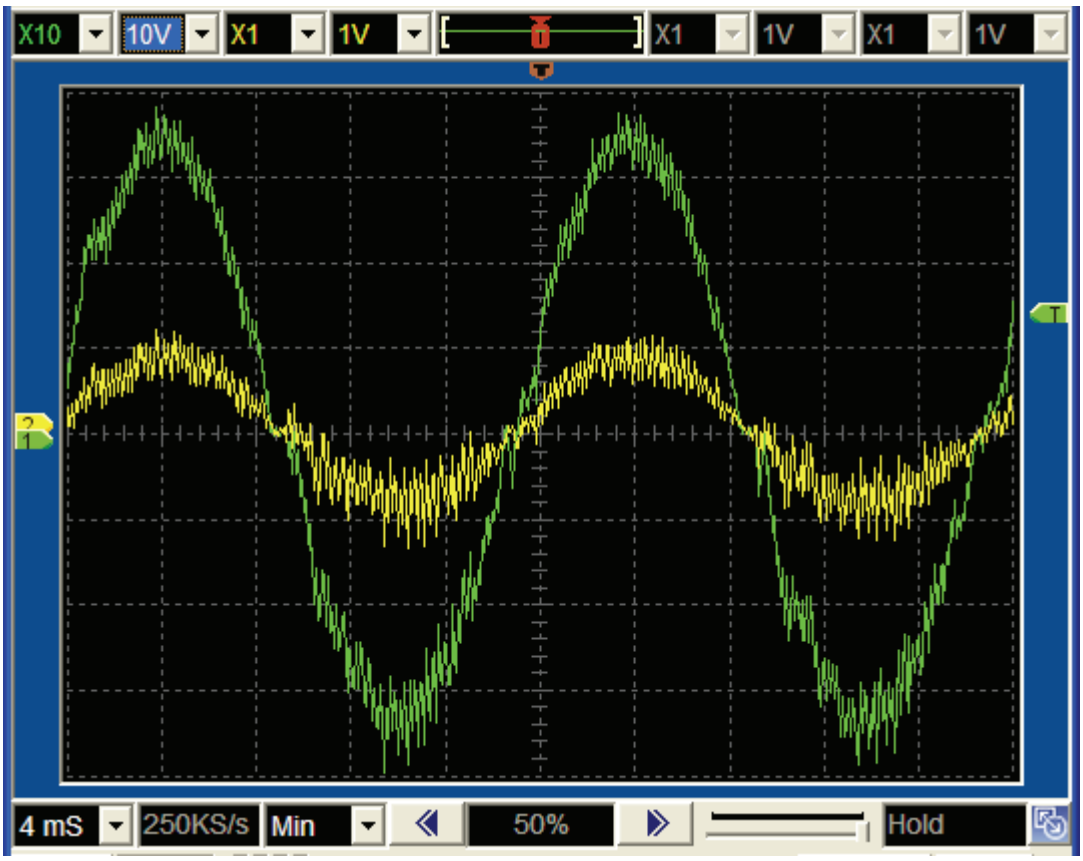

Figure 71: AC Output, Resistive Load, Output Voltage (Ch.1) and Current (Ch.2)

Both waveforms in Figure 71 show a significant amount of high-frequency noise. This is most likely due to the ringing effect seen previously introducing high frequency variations in the voltage and especially the current measurements. The effect of ringing on the measured results were discussed in Figure 64 of section 11.4.1.1. The lower sampling frequency of 15 kHz could possibly also influence the amplitude of the distortion.

Figure 71 sows that the voltage and current waveforms are in phase, as can be expected of resistive load. Note that both the average output voltage and current tracks the command value with relative precision, with some distortion evident at the zero crossings.

11.6.2 Resistors and Capacitors in Series

Figure 72 shows the output voltage (Ch.1) and current (Ch.2) of the converter when feeding a series combination of resistive (six 100W globes) and capacitive (40 uF) loads. The output voltage has a frequency of 50 Hz and a peak amplitude of 38 V. The peak current amplitude is approximately 0.5 A.

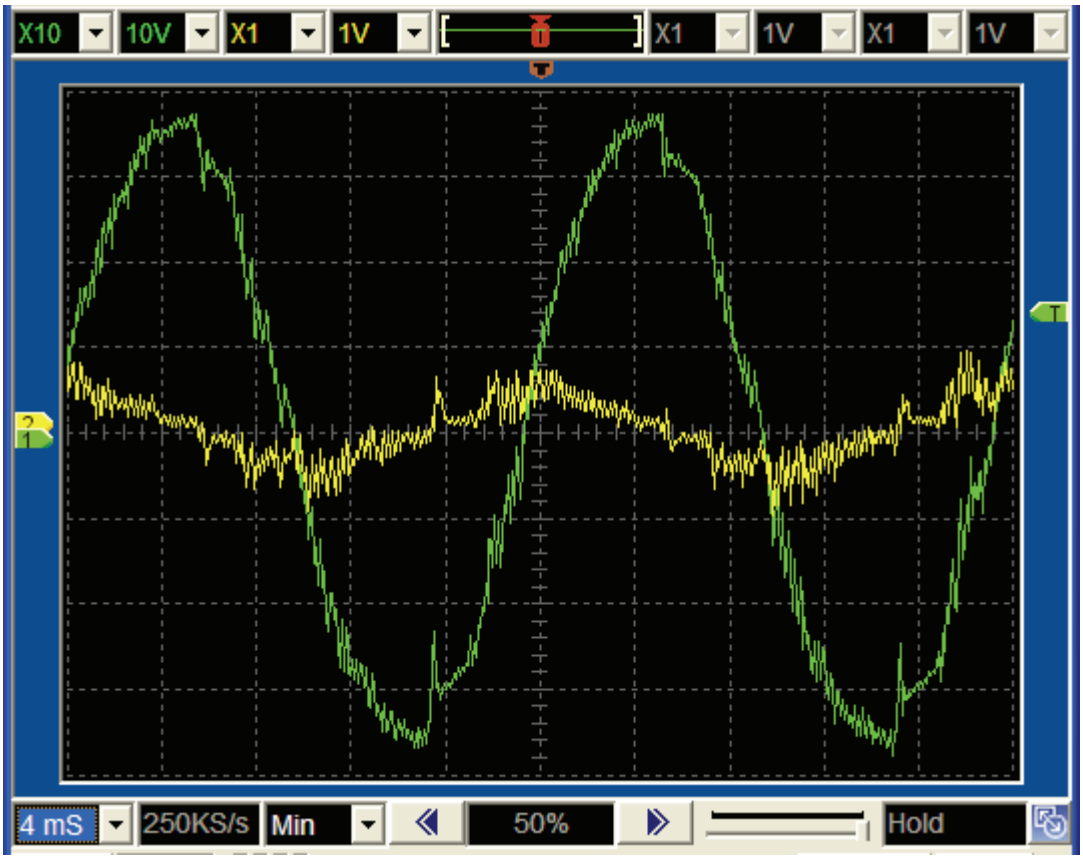

Figure 72: AC Output, Resistors and Capacitors in Series, Output Voltage (Ch.1) and Current (Ch.2)

The most significant feature of Figure 72 is the fact that the current waveform leads the voltage waveform by almost 90 degrees. This is exactly as expected for a series RL load with a high capacitance value.

Figure 72 therefore proves that the converter is able to operate in all four quadrants at 50 Hz, and as such is able to supply a load at any power factor.

Note the current waveforms in Figure 72 around the zero voltage and current crossings. The distortion is most pronounced when the current crosses through zero, and is most likely caused by the converter waiting for the inductor current to decay to zero before effecting a mode change. This result was anticipated during the simulation and is discussed in section 9.5.2.

Current waveform distortion can also be noticed around zero voltage crossings. This is caused by the reduction in gain of the inner current loop in the reverse mode for low output voltages, as was seen in the simulation.

It should be noted that the switch mode power supply used as input to the battery side experienced oscillations of its output when the converter was driven to high power levels with this load. This is caused by the converter regenerating a relatively large amount of energy back to the low voltage side during each output period. The power supply cannot except reverse currents, and the low voltage capacitors' voltage will rise if the reverse current is significant. This causes the power supply to reduce its output, by which time the converter is again in forward mode and drawing current from the supply and the capacitors, causing the low voltage potential to fall. With batteries, this will not occur, although a significant ripple current may be introduced through four quadrant converter operation.

11.6.3 Resistors and Capacitors in Parallel

Figure 73 shows the output voltage (Ch.1) and current (Ch.2) of the converter when feeding a parallel combination of resistive (six 100W globes) and capacitive (40 uF) loads. The output voltage has a frequency of 50 Hz and a peak amplitude of 38 V. The peak current amplitude of approximately 1 A.

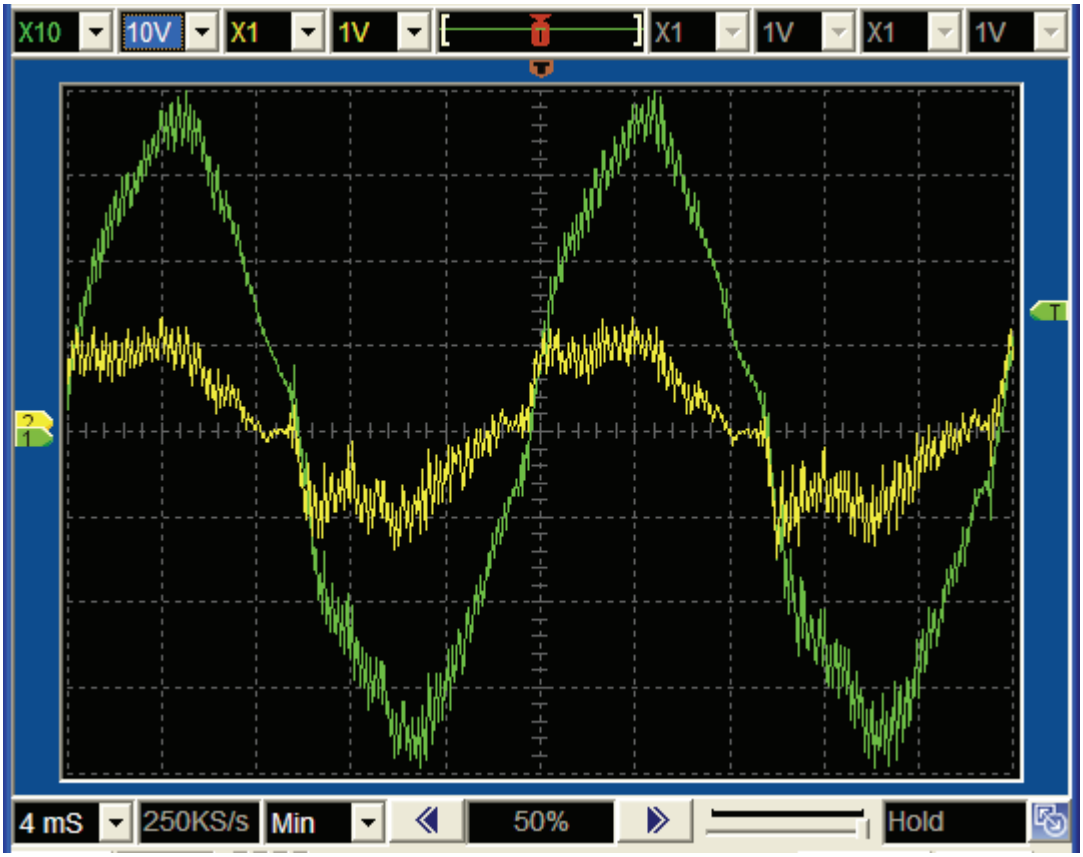

Figure 73: AC Output, Resistors and Capacitor in Parallel, Output Voltage (Ch.1) and Current (Ch.2)

The waveforms of Figure 73 are however not symmetrical about their peak values, as for the preceding waveforms. This is due to the charging and discharging of the capacitor. Note the sharp rise in inductor current after the voltage waveform crosses the x-axis. This is evident for both positive and negative outputs, and indicates the high current required to charge the capacitor to the commanded voltage.

When the output voltage magnitude is decreasing, the inductor voltage is gradually reduced to augment the discharging of the capacitor via the globe resistances. Some distortion is again evident when the inductor current crosses the zero axis. This is due to the reduction in reverse gain at low output voltages, as predicted in section by the converter simulation .

11.7 Results Conclusion

The tests and measurements confirmed that the converter is capable of bidirectional and bipolar, DC and AC operation. The operation of both the power topology as well as the DSP-based control system was therefore demonstrated.

However, the ringing effect of the converter inductor voltage is a cause of concern. It was shown that the amplitude of the ringing can easily exceed the

waveform steady state value. Unfortunately, the ringing occurs in the section of the converter that is already subjected to extremely high voltages. With the ringing effect, this may cause the IGBT's of the Mid Section to be exposed to voltages exceeding 2000 V, which is clearly unacceptable.

It also causes several other undesirable effects, for example causing relatively large errors in the measurements of values and spikes on signal lines. This introduces a significant amount of high-frequency noise on the closed-loop outputs of the converter.

12 Conclusions and Recommendations

12.1 Chapter Introduction

The objective of this project was to develop a direct conversion, bi-directional, low voltage DC to high voltage AC converter, for use in a household renewable energy system.

This chapter will evaluate the success of the project in achieving this objective by considering the sub-objectives, or deliverables, that were defined in Chapter 1. For each deliverable the following points are discussed:

- The degree to which the project was successful in achieving the deliverable.
- Successes and achievements attained in the process of reaching the deliverable.
- Elements of the design that can be considered as unsuccessful to some degree.
- Recommendations for future work.

12.2 Deliverable 1: Development of a Suitable Converter Topology

The project was mostly successful in the development of a suitable topology that conforms to the requirements identified in Chapter 1. The topology was developed from basic step-up and step-down converters that were combined to form a bi-directional DC-DC converter. This bi-directional converter was further generalized into a bi-polar output converter, and then the final high-voltage output topology. The final topology contained a full-bridge inverter / rectifier at the low-voltage side, a high-frequency transformer, a half bridge rectifier inverter and a LC filter on the high voltage side.

The proposed topology was successful in:

- Providing high voltage positive and negative output voltages from a low voltage DC bus.
- Delivering positive and negative power flows for both positive and negative output voltages.
- Being able to rapidly switch between voltages and power flow directions.
- Providing a controllable voltage output that can accurately track a sine wave reference.
- Performing all of the above with a single conversion with no intermediate DC bus.

The proposed topology did however display a ringing effect in the inductor voltage and current during operation. This effect was not anticipated in the design or simulation stages, and is significant in that it prevents the converter

from operating at full design power. The ringing also affected the DSP measurements and therefore the accuracy of the control loops.

It is suspected that the ringing is caused by the inductive coupling of the two transformer secondary windings and the inductor itself. Observations that support this suspicion include the fact that two distinct ringing frequencies and amplitudes were experimentally observed, and that the ringing amplitude was linearly proportional to the transformer secondary voltage. It should be noted that the transformer secondary windings contain a large amount of turns, and may therefore have a significant leakage inductance. This leakage inductance was not considered in the design or simulation.

The ringing effect will need to be addressed before development of this type of converter can be continued. Several options may be explored for reducing the ringing effect, which includes:

- Designing transformer secondary windings with low leakage inductance.
- Using only a single secondary winding.
- Using capacitors or other circuit elements to dampen the ringing. This was unsuccessfully attempted during the measurements of this project, but can be revisited.
- Investigate the influence of the low-voltage capacitors on the ringing.
- Placing the inductor on the low-voltage side of the transformer. This was attempted previously by the author without a large degree of success, but the concept could be revisited.

12.3 Deliverable 2: Development of Suitable Control Methodologies

The project was fully successful in the development of control methodologies and compensation means for both voltage and current mode control loops.

The following successes were achieved in the development of the control methodologies:

- A new method was developed for determining the transfer functions of common power electronic converter by inspection alone, thereby saving a significant amount of work in the design of converter control systems. The method considers the effect of duty cycle changes and load impedances on the time-varying values of circuit parameters. e
- The above method was successfully applied to calculate the transfer functions of the converter in both voltage and current mode.
- All additional gains (modulation, measurement) were correctly identified and included in the transfer functions.
- The frequency response of the transfer functions were analysed with the aid of Bode plots, and suitable compensators designed.

- Compensation equations for the control loops were designed using the frequency response method. The final compensated closed loop responses conformed to the requirements identified in Chapter 1.
- The compensation equations were digitized with Matlab and successfully implemented in the DSP.
- The converter was successfully operated in closed loop mode. This was demonstrated by the operation of the converter in AC output mode during the experimental tests.

The control methodologies and compensation means that were developed performed very well, although other parts of the system design did impact somewhat negatively on their operation. The ringing effect described under Deliverable 1 introduced significant fluctuations in the DSP measurements, thereby degrading the accuracy of the control loops. The selected DSP was also not capable of executing the compensation interrupt routine at the design rate of 30 kHz, and a lower rate of 15 kHz had to be adopted. This also negatively impacted on the accuracy of the loops.

As is discussed in relation with the DSP design in section 12.6, rewriting of the compensation code in Assembler, as opposed to in C, might solve the latter issue.

12.4 Deliverable 3: Combined Hardware and Software Simulation

The simultaneous simulation of the converter hardware and software was fully successful, and proved an invaluable aid in the development and debugging of the control software.

The following successes were achieved through simulation of the converter:

- The entire control systems was modelled as a single VHDL simulation element. The VHDL simulation element contained functional models of both the DSP hardware as well as the DSP software.
- The control system was simulated together with models of power section components.
- The operation of the converter was proven and numerous enhancement opportunities were identified through the simulation.
- The overall development time was significantly shortened.

The simultaneous simulation of both the converter hardware and software was an original initiative of the author, once he became aware of the VHDL capabilities of Ansoft's Simplorer. As far as could be ascertained this is not a widely known method, and its application has the capability of greatly reducing the effort and risk associated with power electronic converter design.

The only negative aspect of the converter simulation was that it was not used to identify the ringing effect earlier in the development cycle. The failure of the simulation to show the ringing effect is due to unrealistic values that were

assumed for the transformer secondary winding leakage inductances. Future projects should take greater care that parameter values used in such simulations are based on realistic calculations, or preferably even measurements.

12.5 Deliverable 4: Design and Construct Prototype Converter Power Section

The proposed topology was successfully prototyped using commercially available components and manufactured Printed Circuit Boards. The power section consisted of three power PCB's, as well as the transistor drivers and sensors.

The following elements were successfully completed during the design and construction of the power section converter:

- Identification and sourcing of suitable components.
- Schematic design of all PCB's.
- Board layouts of all PCB's.
- Manufacture and assembly of all PCB's.
- Mechanical construction of converter housing and mounting of PCB's.
- Commissioning of power section PCB's.

With some minor changes the manufacturability, maintainability and cost of the boards could be substantially improved.

12.6 Deliverable 5: Design and Construct Prototype Converter Control Section

A digital control system for the proposed topology was successfully designed and prototyped. The control section consisted of a DSP board based on the Texas Instruments TMS320LF2403A DSP, as well as a multiple output isolated power supply.

The following elements were successfully completed during the design and manufacture of the control system for the proposed converter:

- Identification and sourcing of suitable components.
- Schematic design of DSP and power supply PCB's.
- Board layouts of DSP and power supply PCB's.
- Manufacture, assembly and commissioning of DSP and power supply PCB's.
- Development of DSP software.
- Programming of the DSP via a JTAG interface.
- Debugging of DSP Software.

The control power supply provided clean power to the drivers and DSP board. A failure of the linear regulator that powers the power supply switching regulator was observed. The voltage input to this component should be reduced in future designs by a switch mode pre-regulator.

The digital control system of the proposed converter allowed the implementation of several algorithms that would have been difficult or impossible to construct using analogue electronics. Examples are the determination of the mode of the converter, duty cycle masking to enable the inductor current to decay and duty cycle inversion after a mode change.

The computationally intensive sections of the DSP code needs to be rewritten in assembler to ensure the fastest execution time possible. The calculation of the current and duty cycle commands are examples of such sections that would greatly benefit from hand-written assembler code.

Although the digital control system performed well, several features may be added in future for a commercial system. The control system may be expanded to allow the converter to automatically connect and disconnect from the mains supply. For automatic disconnection, some method to determine when the mains voltage is unhealthy is required. This will probably be implemented by comparing the mains input with a reference sinusoid of variable amplitude and frequency, in order to detect anomalies and initiate disconnect. This sinusoid would also be helpful in determining the command current during the charging mode.

For automatic connection, a method will be required to drift the converter output voltage amplitude and frequency so that it is of the same magnitude and phase as the mains input. To prevent damage to user equipment, the mains disconnect contactor can only be closed when the two sinusoidal voltage waveforms are synchronised.

Better communication of converter status and events with the user could also be implemented, for example low battery voltage warning, fault indication and overload indication. An indication of the mode (charging or inverting) would also be useful.

Since the DSP board was designed to be hand-soldered, through-hole components was specifically used for many of the PCB's. Space can be saved in future systems by the greater use of surface mount components.

12.7 Deliverable 6: Demonstrate 4 –Quadrant DC Operation of Converter

It was demonstrated that the converter successfully generated both positive and negative DC output voltages that were software controllable. Furthermore, the converter supported both positive and negative power flows for positive and negative output voltages. Thus, the converter was shown to successfully operate in four quadrants under DC conditions.

The converter was however not able to reach full design power due to ringing effect described in section 12.2.

12.8 Deliverable 7: Demonstrate AC Operation of Converter

It was demonstrated that the converter successfully generated a controllable sinusoidal AC voltage output with both resistive and capacitive loads. The AC output operation of the converter successfully used closed loop control of both the voltage and current.

Of particular importance was the demonstration of operation with a capacitive load that required regeneration within a single output waveform period. This proved that the converter is capable of rapidly reversing power flow direction in order to control the output voltage.

This final test of the converter verified that all sub-systems of the designed prototype performed substantially according to design.

Some distortion was however present in the output waveform. This distortion is accredited to the ringing effect and the reduced DSP code execution frequency, as described in sections 12.2 and 12.3.

12.9 Concluding Remarks

The successful achievement of the deliverables defined for this project indicates that the proposed converter is indeed capable of meeting the requirements for use in the household renewable energy system defined in Chapter 1.

With the completion of the further work recommended in this chapter, it will be possible to use the proposed converter as the central component of a system that interfaces several DC generation and storage devices with AC user devices and the mains grid. This arrangement will ensure maximum renewable resource utilization.

The direct conversion topology developed for this converter has the potential to increase the efficiency and lower the cost of the DC-AC interface in a household system. The proposed converter may therefore positively impact on the uptake of renewable technologies.

The extensive simultaneous simulation of hardware and software significantly reduced the development effort of the converter. This method can be applied in the design of future converters in order to verify the correct functioning of both hardware and software. This will increase productivity, reduce development time and reduce the project risk.

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14 Appendix A

14.1 Appendix A.1: Transformer Core Selection Table

Transformer Core Type	PM 50/39	PM 62/49	PM 74/59	PM 87/70	ETD 44/22/15	ETD 49/25/16	ETD 54/28/19	ETD 59/31/22
Pmax.trans @ 100kHz (W)	1742	2999	5036	0	1708	2645	3998	6692
Pmax.trans @ 50kHz (W)	871	1499.5	2518	0	854	1322.5	1999	3346
Pmax.trans @ 30kHz (W)	522.6	899.7	1510.8	0	512.4	793.5	1199.4	2007.6
Ae (mm^2)	370	570	790	910	173	211	280	368
An (mm^2)	154	270	442	657	210	269	315	365
Switching Frequency (Hz)	30000	30000	30000	30000	30000	30000	30000	30000
Steady State Duty Cycle (D)	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Max. Magnetic Flux Density Change (T)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Primary Winding Voltage (V)	60	60	60	60	60	60	60	60
Primary Turns	**6.76**	**4.39**	**3.16**	**2.75**	**14.45**	**11.85**	**8.93**	**6.79**
Module Power Capability (W)	2000.00	2000.00	2000.00	2000.00	2000.00	2000.00	2000.00	2000.00
Min Battery Voltage (V)	46.80	46.80	46.80	46.80	46.80	46.80	46.80	46.80
Primary RMS Current (A)	42.74	42.74	42.74	42.74	42.74	42.74	42.74	42.74
Allowable Current Denesity (A/mm^2)	6.00	6.00	6.00	6.00	6.00	6.00	6.00	6.00
Primary Conductor Area (mm^2)	7.12	7.12	7.12	7.12	7.12	7.12	7.12	7.12
Turns Ratio	0.1152	0.1152	0.1152	0.1152	0.1152	0.1152	0.1152	0.1152
Secondary Turns (per winding)	**58.65**	**38.07**	**27.47**	**23.85**	**125.44**	**102.85**	**77.50**	**58.97**
Output Voltage (V)	230.00	230.00	230.00	230.00	230.00	230.00	230.00	230.00
Steady State Duty Cycle	0.75	0.75	0.75	0.75	0.75	0.75	0.75	0.75
Secondary RMS Current (A)	6.52	6.52	6.52	6.52	6.52	6.52	6.52	6.52
Secondary Conductor Area (mm^2)	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
Number of Primary Windings	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Number of Secondary Windings	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
Fill Factor	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
Total Window Area Required	351.26	228.01	164.51	142.82	751.25	615.95	464.17	353.17

14.2 Appendix A.2: Inductor Core Selection Table

u0 1.25664E-06

Ferrite Material		N27	N27	N27	N27	N27	N27	N27	N27
Specific Core		ETD29/16/10	ETD34/17/11	ETD39/20/13	ETD44/22/15	ETD49/25/16	ETD54/28/19	ETD59/31/22	
Core Data	le [mm]	70.4	78.6	92.2	103	114	127	139	
Core Data	Ae [mm^2]	76	97.1	125	173	211	280	368	
Core Data	AN [mm^2]	97	122	178	210	269.4	315.6	365.6	
Core Data	ue	1470	1540	1500	1560	1590	1510	1500	
Core Data	ui	2000	2000	2000	2000	2000	2000	2000	
Calculated	Re	501454.89	418285.42	391308.95	303708.30	270405.43	239033.56	200385.30	
Calculated (Should match Core Date)	AL	1.994E-06	2.391E-06	2.556E-06	3.293E-06	3.698E-06	4.184E-06	4.990E-06	
Chosen Inductance	L [H]	3.520E-03	3.520E-03	3.520E-03	3.520E-03	3.520E-03	3.520E-03	3.520E-03	3.520E-03
Chosen Peak Current Value	I [A]	6.45	6.45	6.45	6.45	6.45	6.45	6.45	6.45
Approximate Average Current	I [A]	6.15	6.15	6.15	6.15	6.15	6.15	6.15	6.15
Chosen Current Density	J [A/mm^2]	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0
Calculated Copper Area Required	Awire [mm^2]	0.879	0.879	0.879	0.879	0.879	0.879	0.879	0.879
Calculated Wire Diameter Required	d [mm]	1.058	1.058	1.058	1.058	1.058	1.058	1.058	1.058
Chosen Wire Diameter	d [mm]	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Chosen Copper Fill Factor (for Litz wire fCU~=0.3)	fCU	0.55	0.55	0.55	0.55	0.55	0.55	0.55	0.55
Calculated Copper Area for chosen Wire Diameter	Awire [mm^2]	0.79	0.79	0.79	0.79	0.79	0.79	0.79	0.79
Calculated Maximum Numer of Turns Possible	Nmax [turns]	67.93	85.43	124.65	147.06	188.66	221.01	256.02	
Choose Number of Turns	N [turns]	67	85	50	147	188	221	150	
Calculated Inductance Factor Required	AL	7.841E-07	4.872E-07	1.408E-06	1.629E-07	9.959E-08	7.207E-08	1.564E-07	
Calculated Effective Permeability Required	ue	578.02	313.83	826.44	77.18	42.82	26.01	47.02	
Calculted Maximum Flux Density	Bmax [T]	4.459	2.751	3.633	0.893	0.572	0.367	0.411	
Core Data	Bsat @ 100C [T]	0.410	0.410	0.410	0.410	0.410	0.410	0.410	0.410
Calculated Airgap Required	s [mm]	0.09	0.21	0.07	1.28	2.61	4.82	2.89	
Calculated Airgap Length as a percentage of le	%	0.12%	0.27%	0.07%	1.25%	2.29%	3.79%	2.08%	
Chosen Airgap	s [mm]	2.00	2.00	1.70	2.00	2.00	2.00	2.89	
Calculated Effective Permeability	ue	34.59	38.54	52.80	50.21	55.42	61.55	46.97	
Calculted Maximum Flux Density	Bmax [T]	0.267	0.338	0.232	0.581	0.741	0.868	0.411	
Calculated Inductance Factor	AL	4.693E-08	5.983E-08	8.996E-08	1.060E-07	1.289E-07	1.705E-07	1.563E-07	
Calculated Inductance	L [H]	2.107E-04	4.323E-04	2.249E-04	2.290E-03	4.556E-03	8.328E-03	3.516E-03	

14.3 Appendix A.3: Schematic and Layout: Low Voltage Board

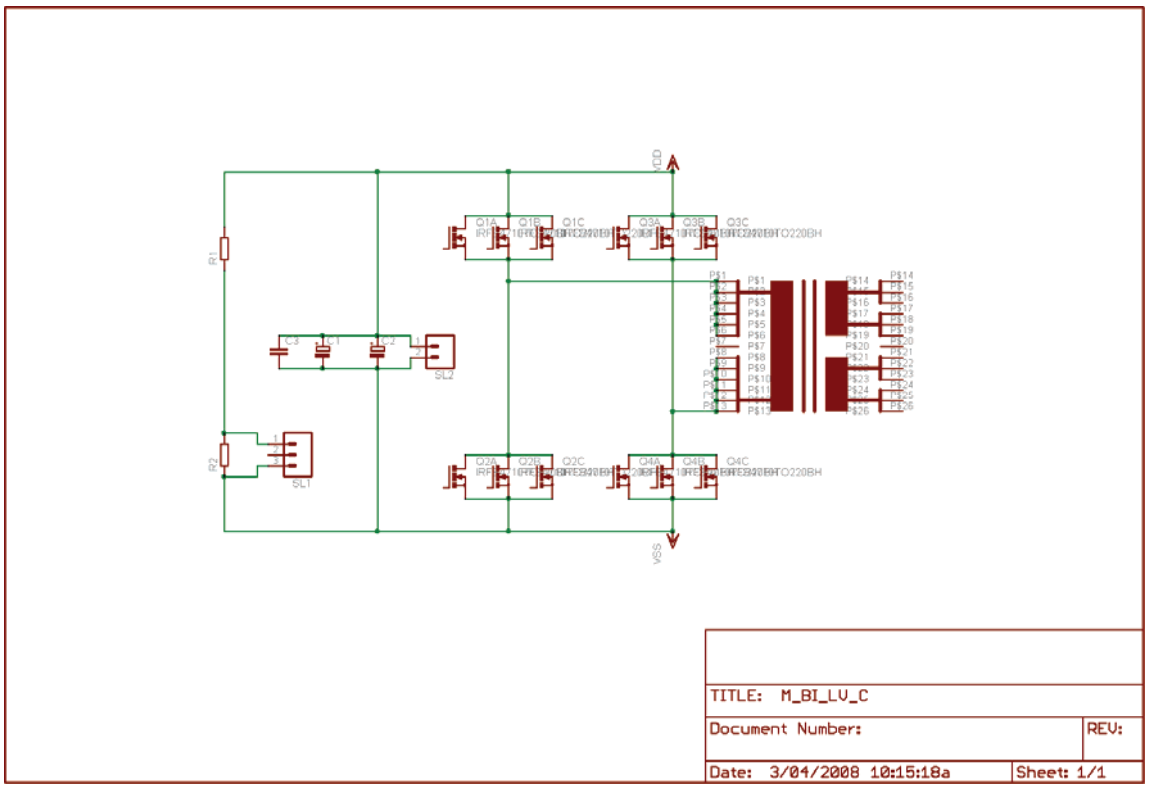

Figure 74: Low Voltage Board Schematic

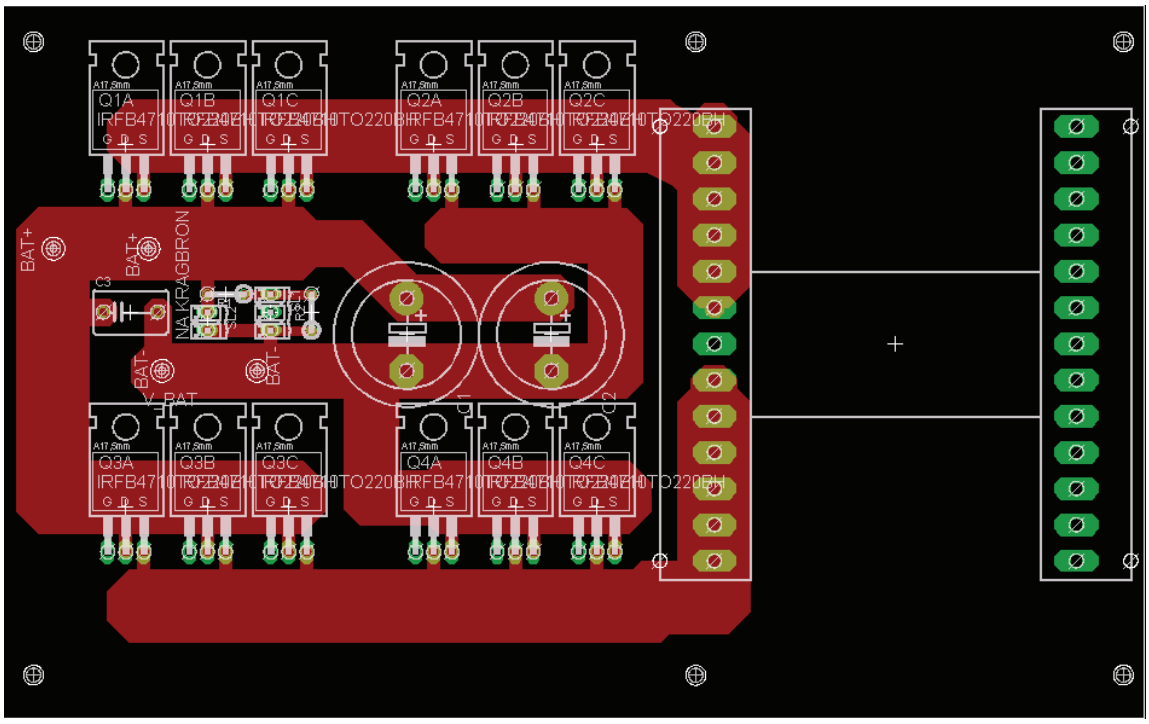

Figure 75: Low Voltage Board Layout

14.4 Appendix A.4: Schematic and Layout: Mid Section Board

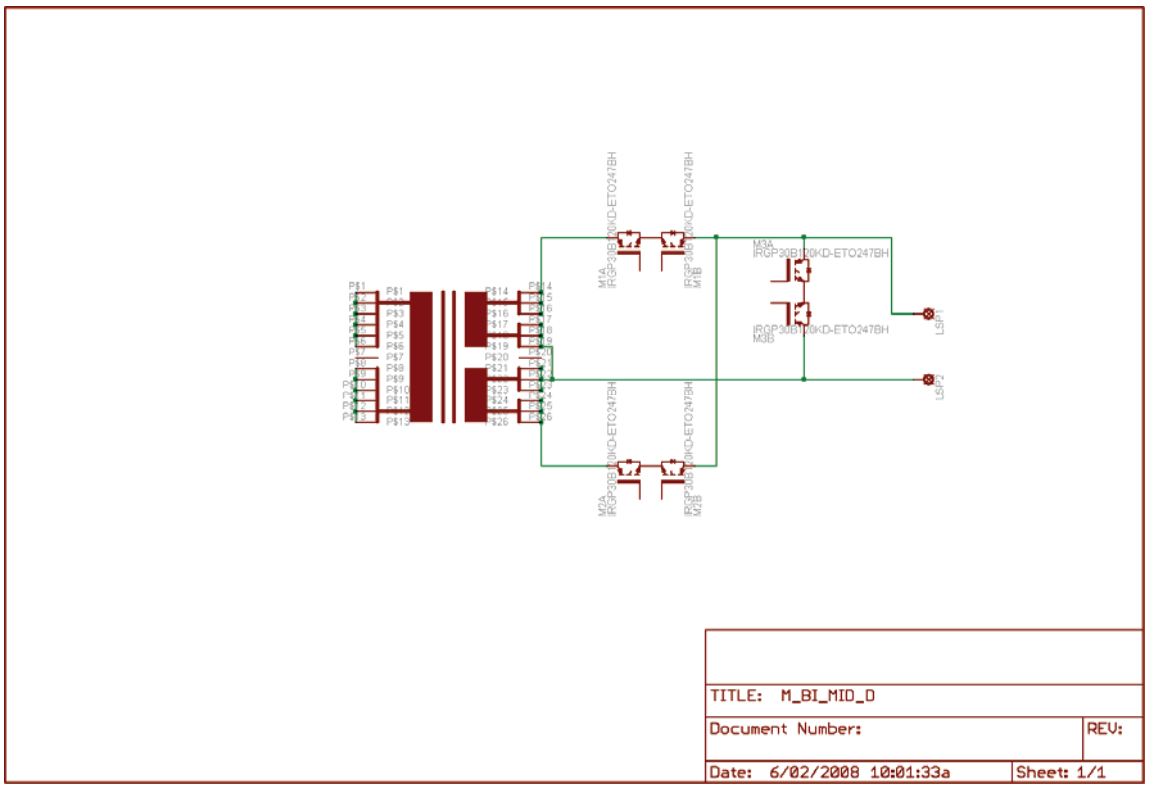

Figure 76: Mid Section Board Schematic

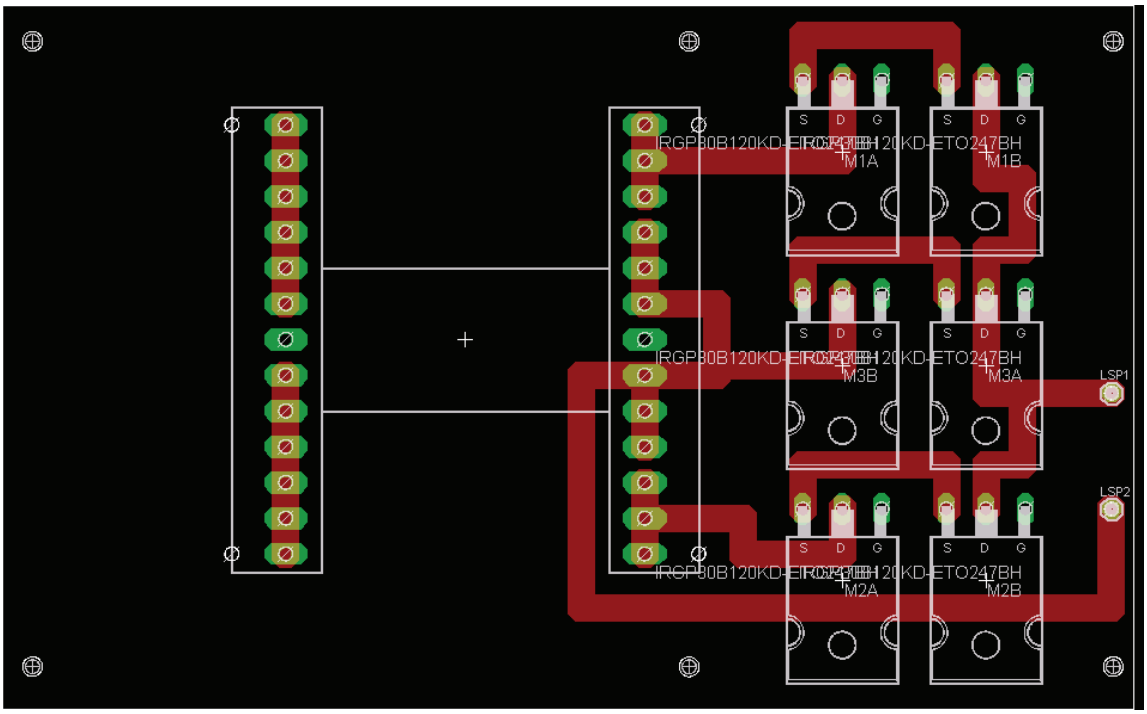

Figure 77: Mid Section Board Layout

14.5 Appendix A.5: Schematic and Layout: High Voltage Board

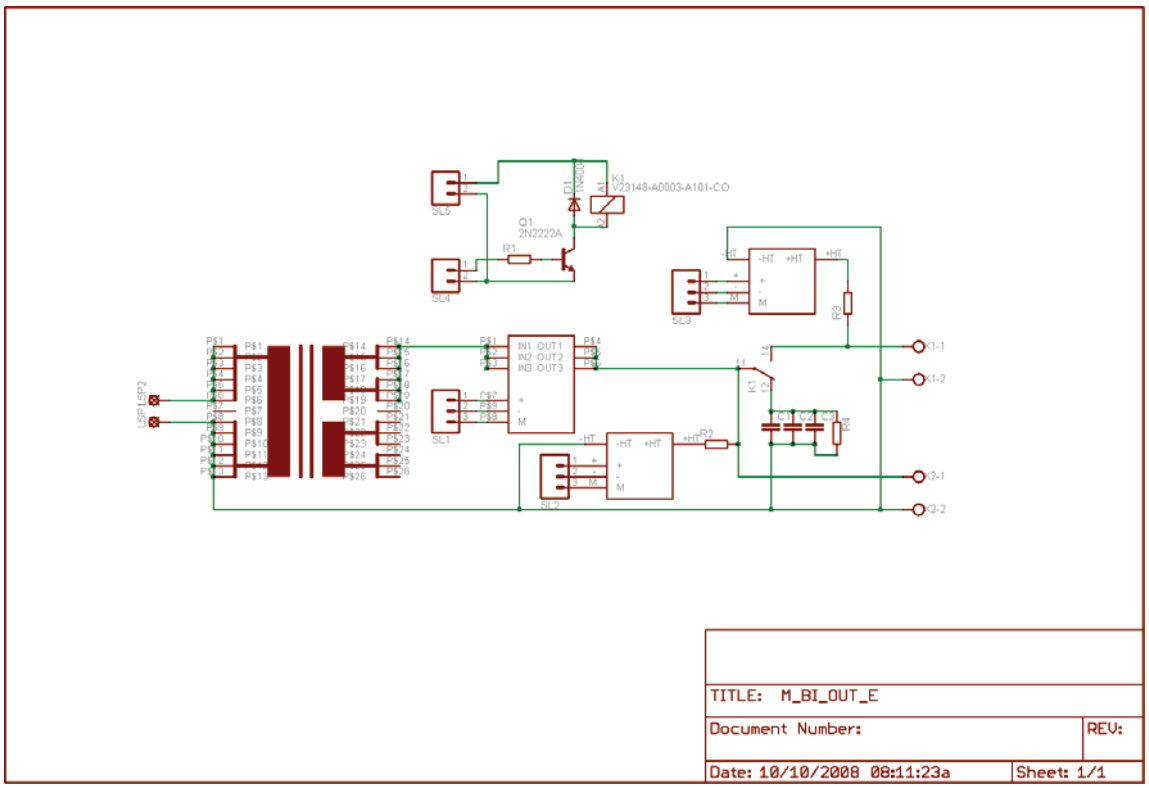

Figure 78: High Voltage Board Schematic

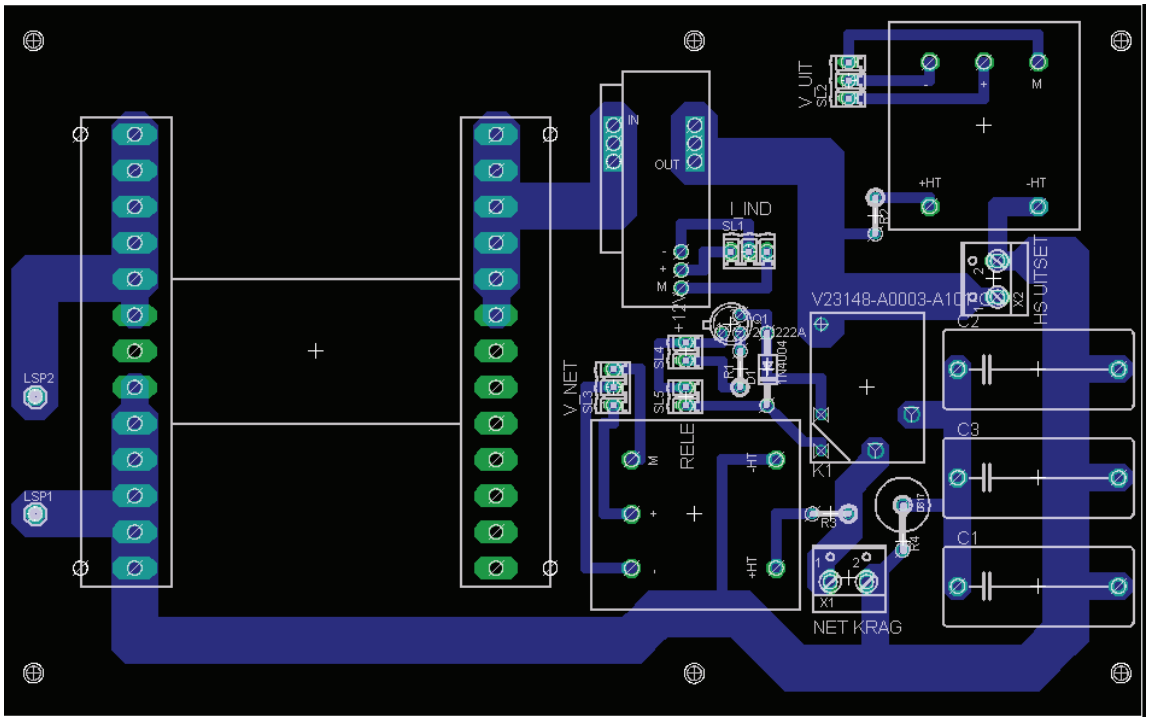

Figure 79: High Voltage Board Layout

14.6 Appendix A.6: Schematic and Layout: IGBT Drivers

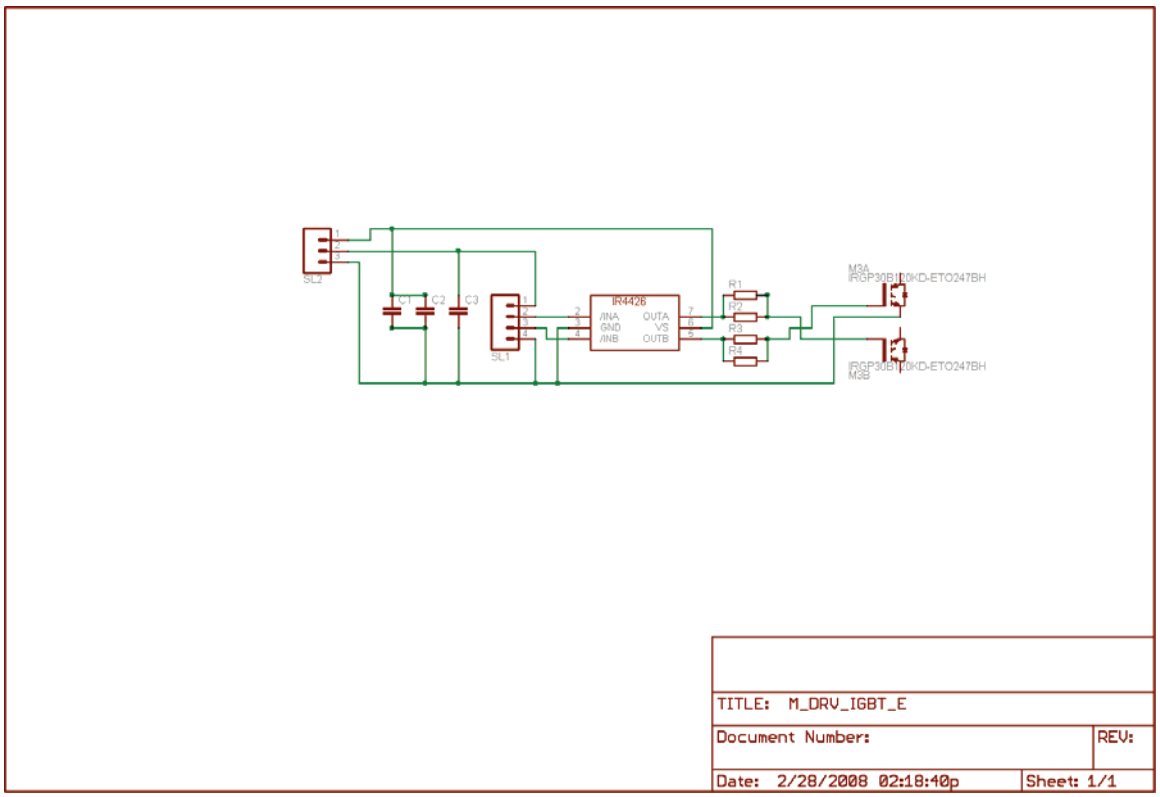

Figure 80: IGBT Driver Board Schematic

Figure 81: IGBT Driver Board Layout

14.7 Appendix A.7: Schematic and Layout: MOSFET Drivers

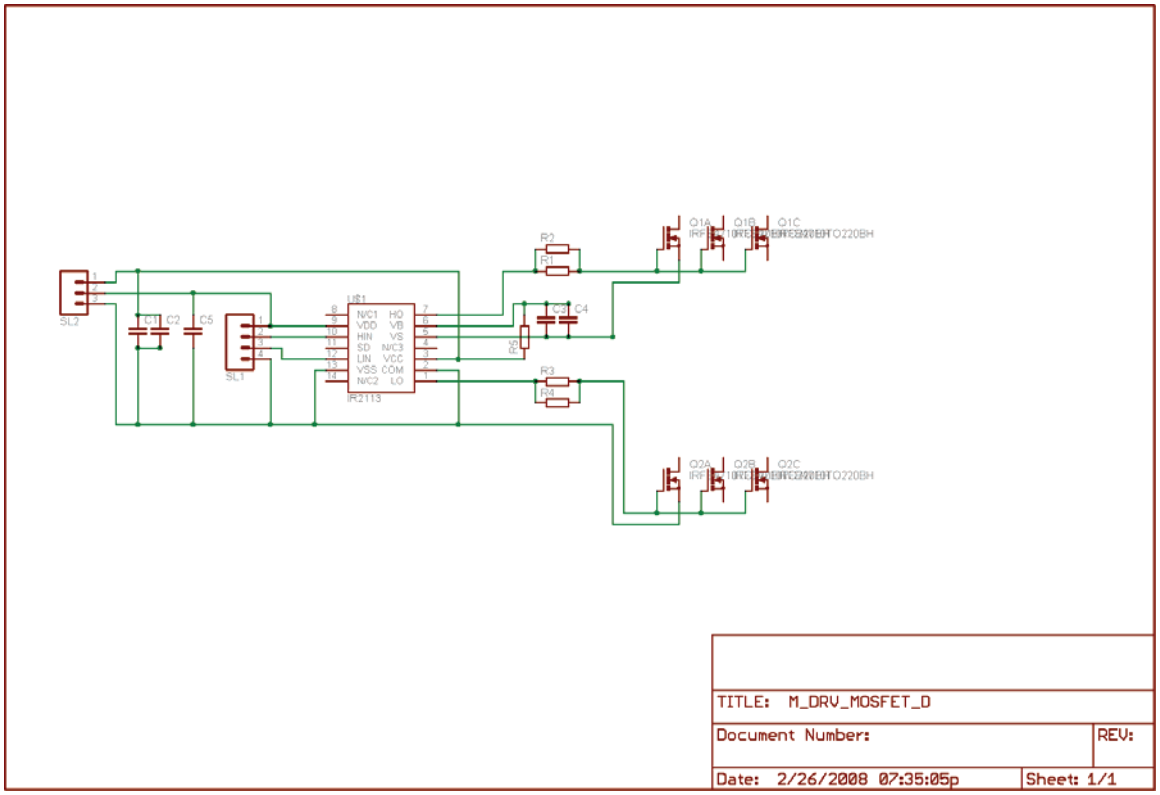

Figure 82: MOSFET Driver Board Schematic

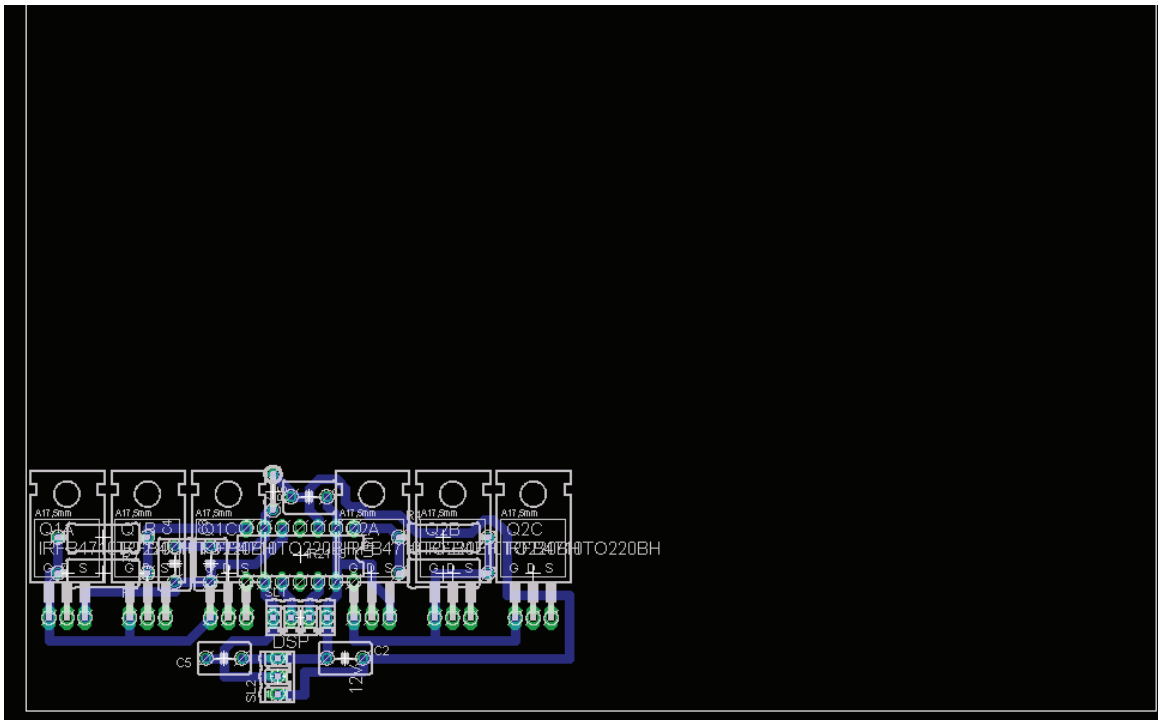

Figure 83: MOSFET Driver Board Layout

14.8 Appendix A.8: Schematic: Control Power Supply Board

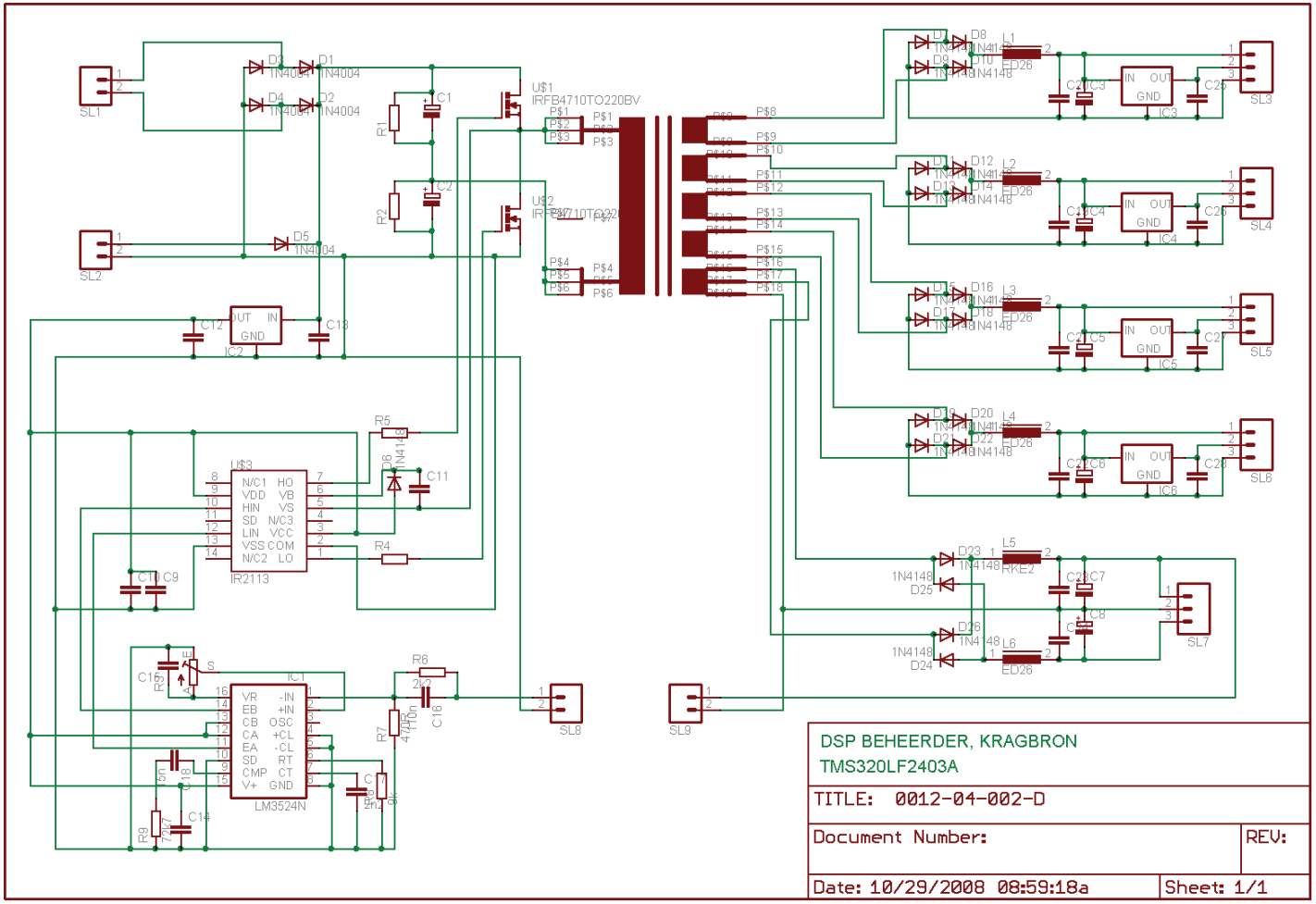

Figure 84: Control Power Supply Schematic

14.9 Appendix A.9: Layout: Control Power Supply Board

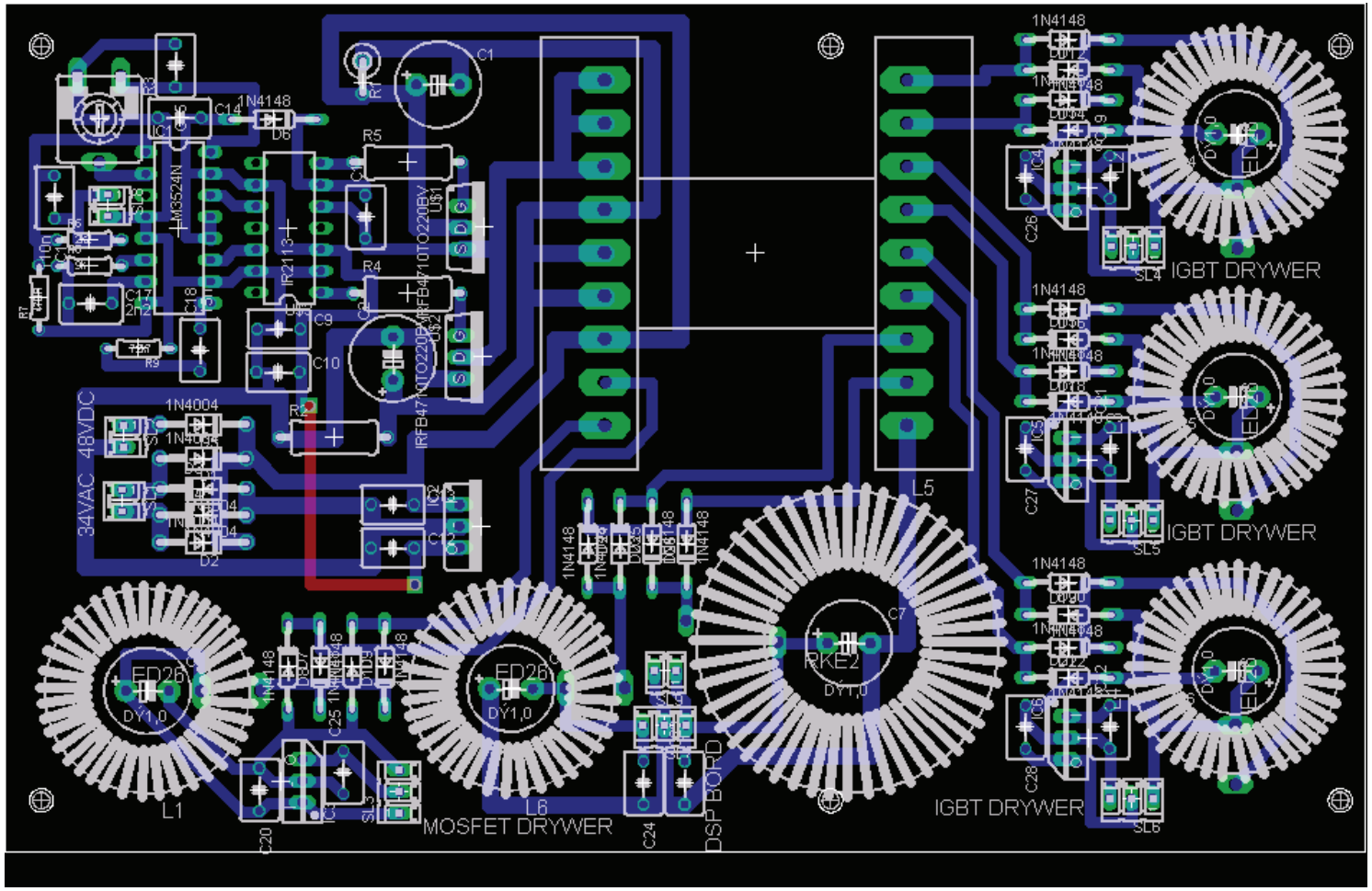

Figure 85: Control Power Supply Layout

14.10 Appendix A.10: Schematic: DSP Control Board

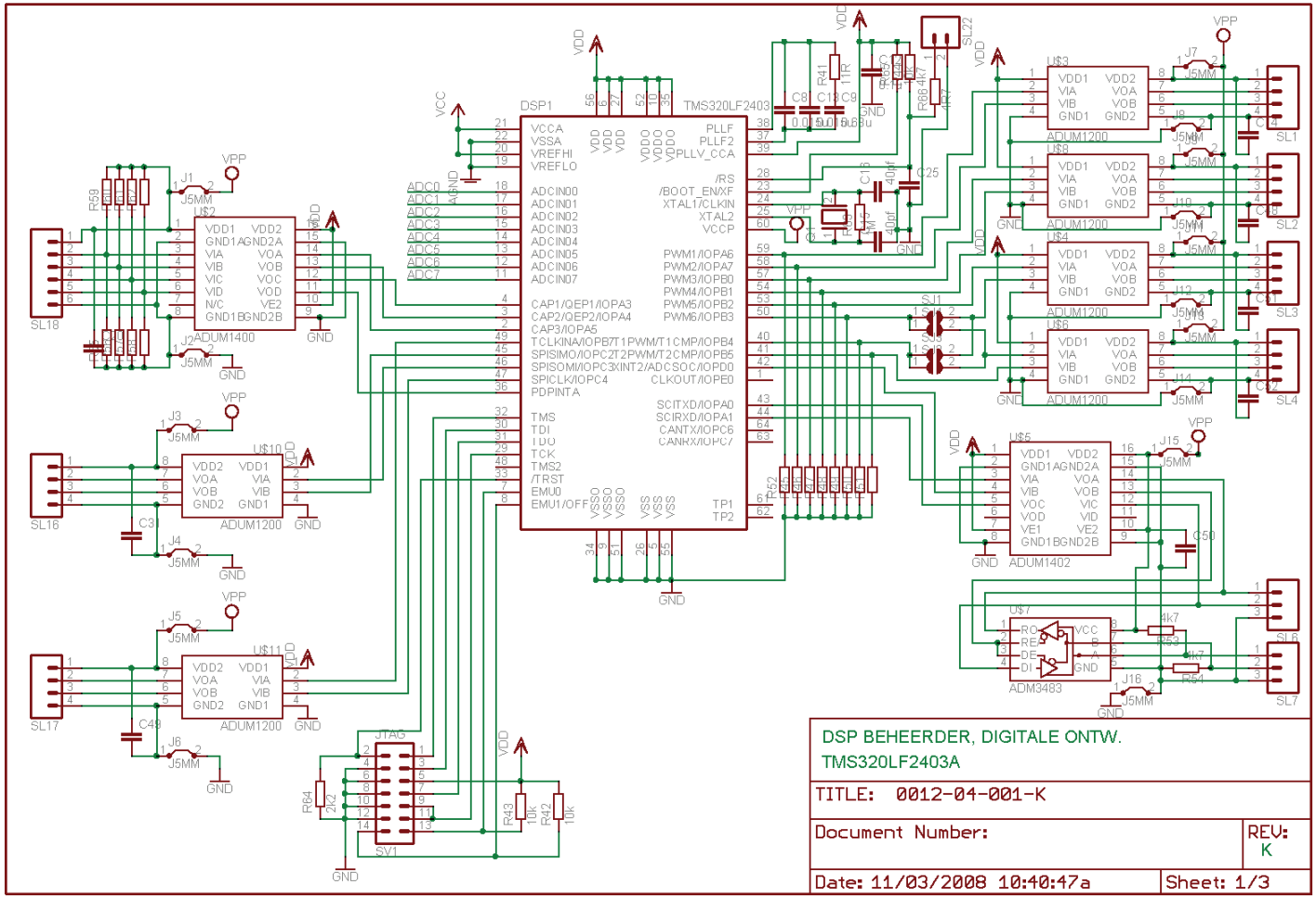

Figure 86: DSP Controller Schematic Sheet 1

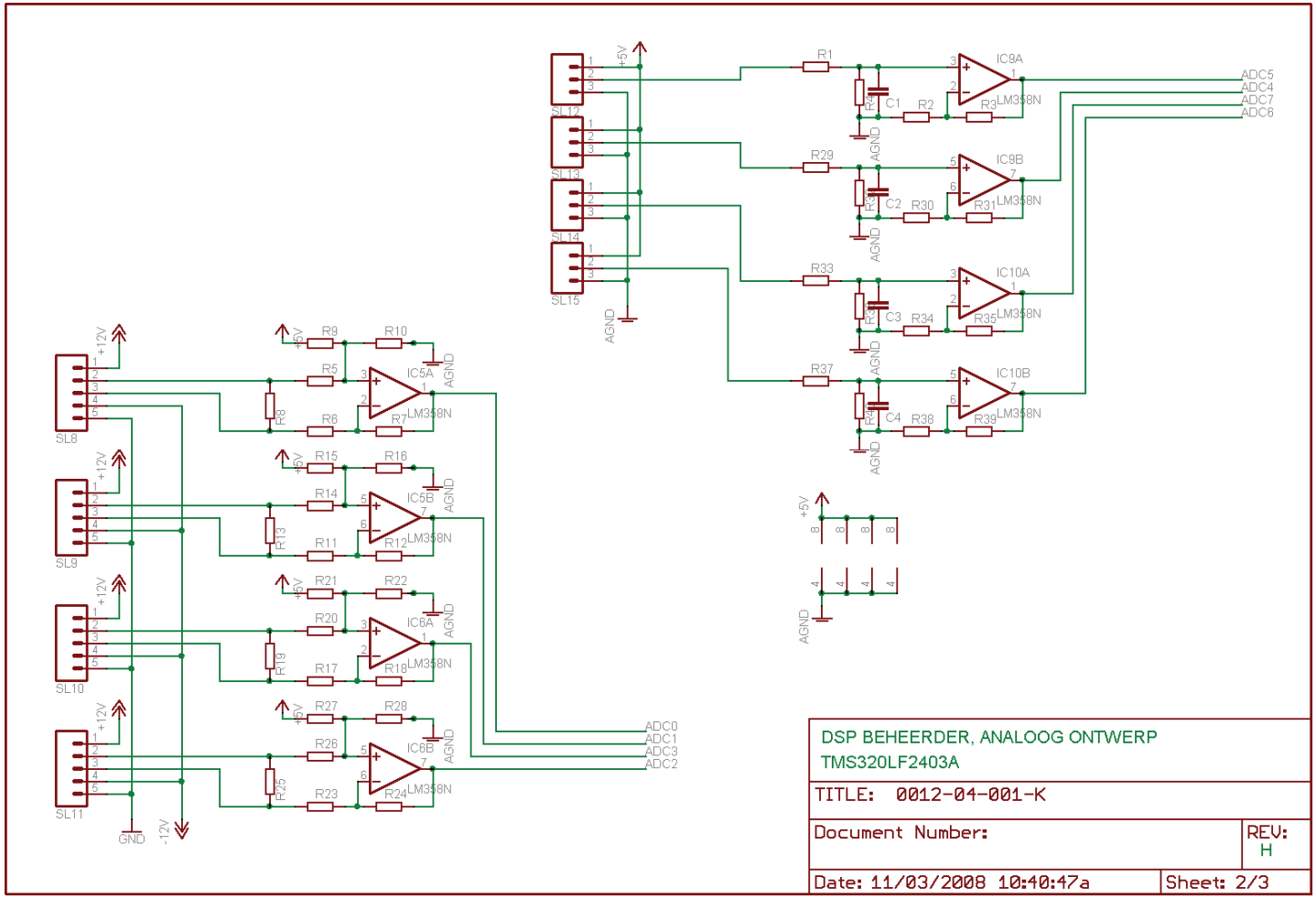

Figure 87: DSP Controller Schematic Sheet 2

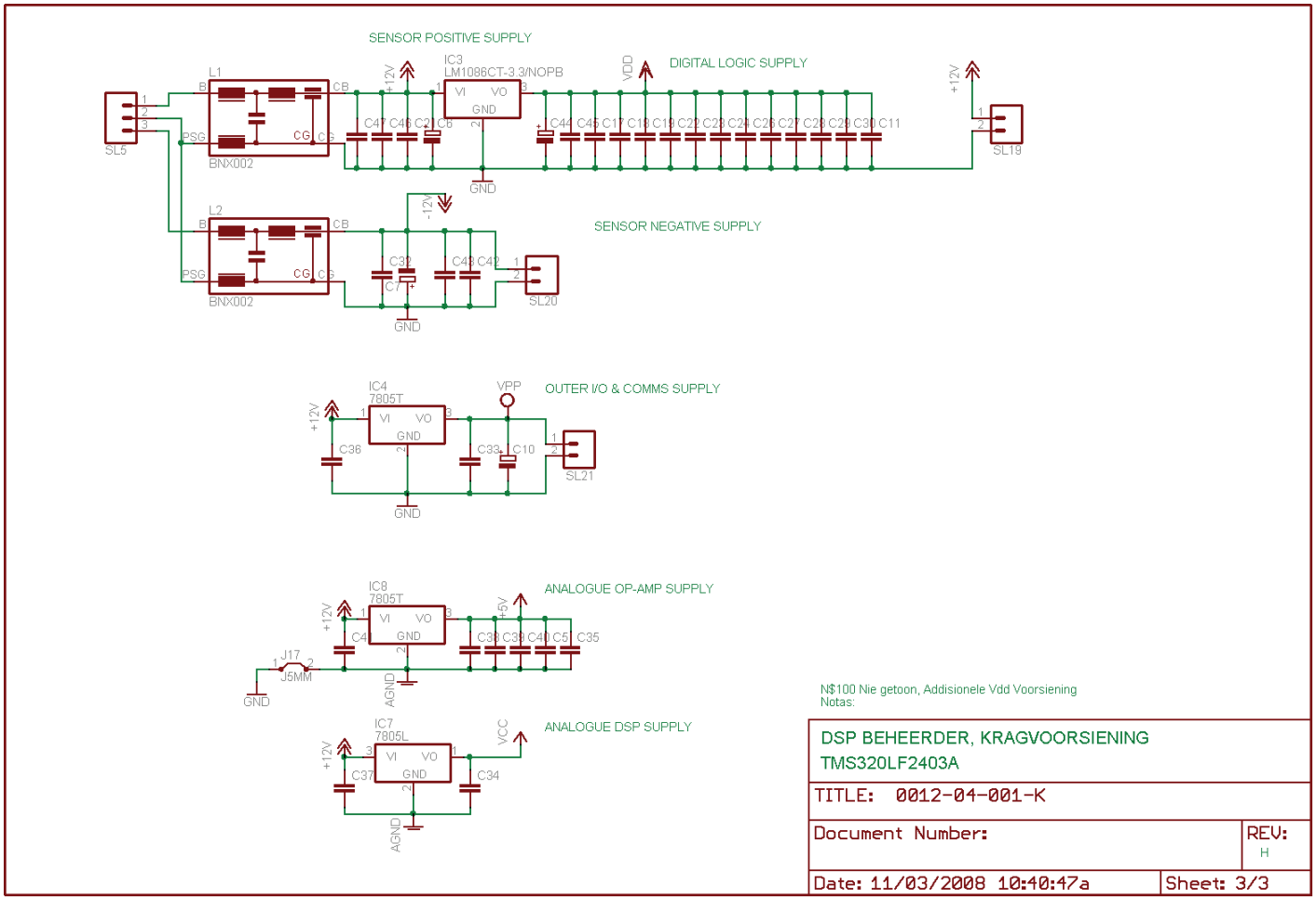

Figure 88: DSP Controller Schematic Sheet 3

14.11 Appendix A.11: Layout: DSP Control Board

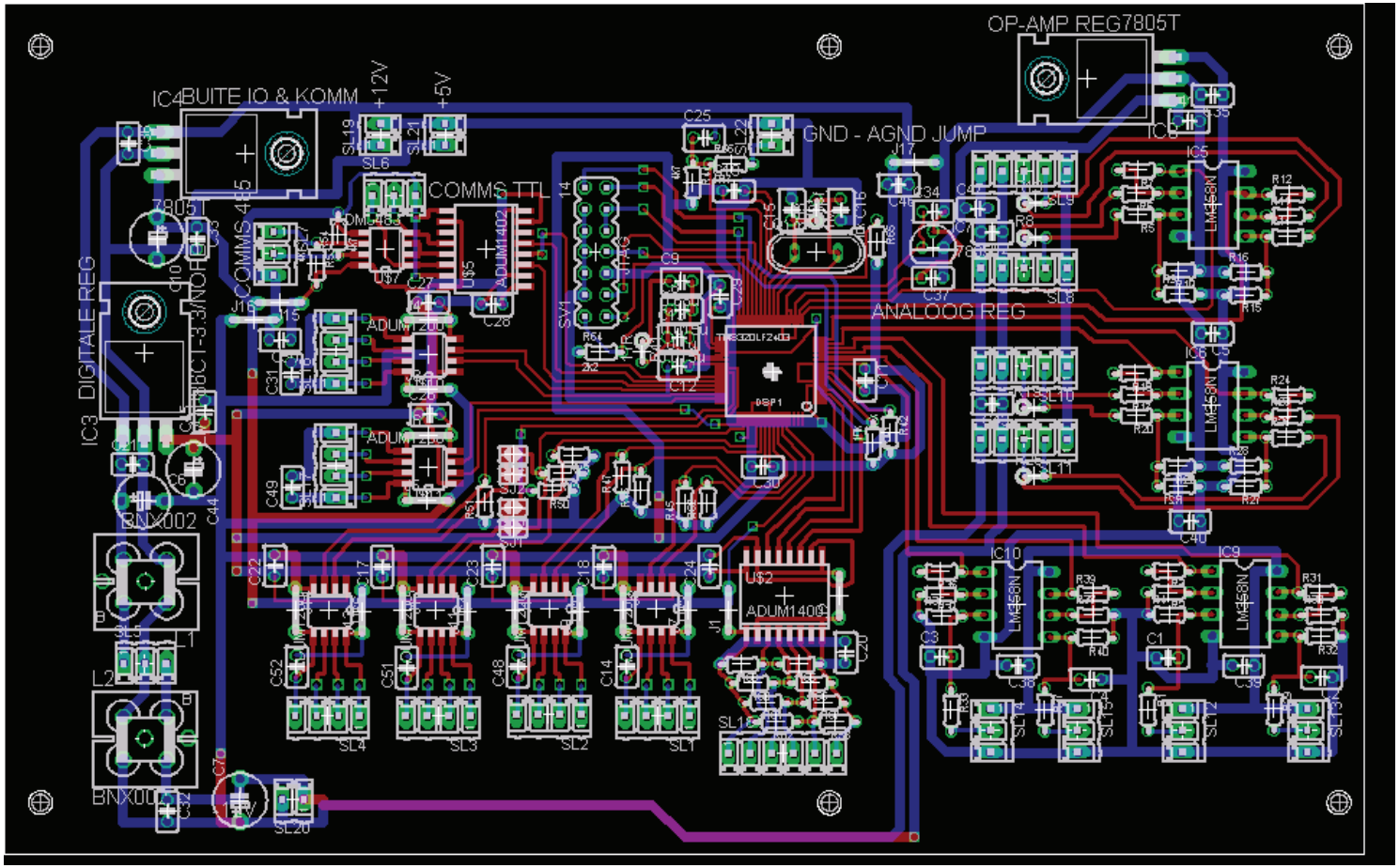

Figure 89: DSP Controller Layout

14.12 Appendix A.12: Simplorer Schematic

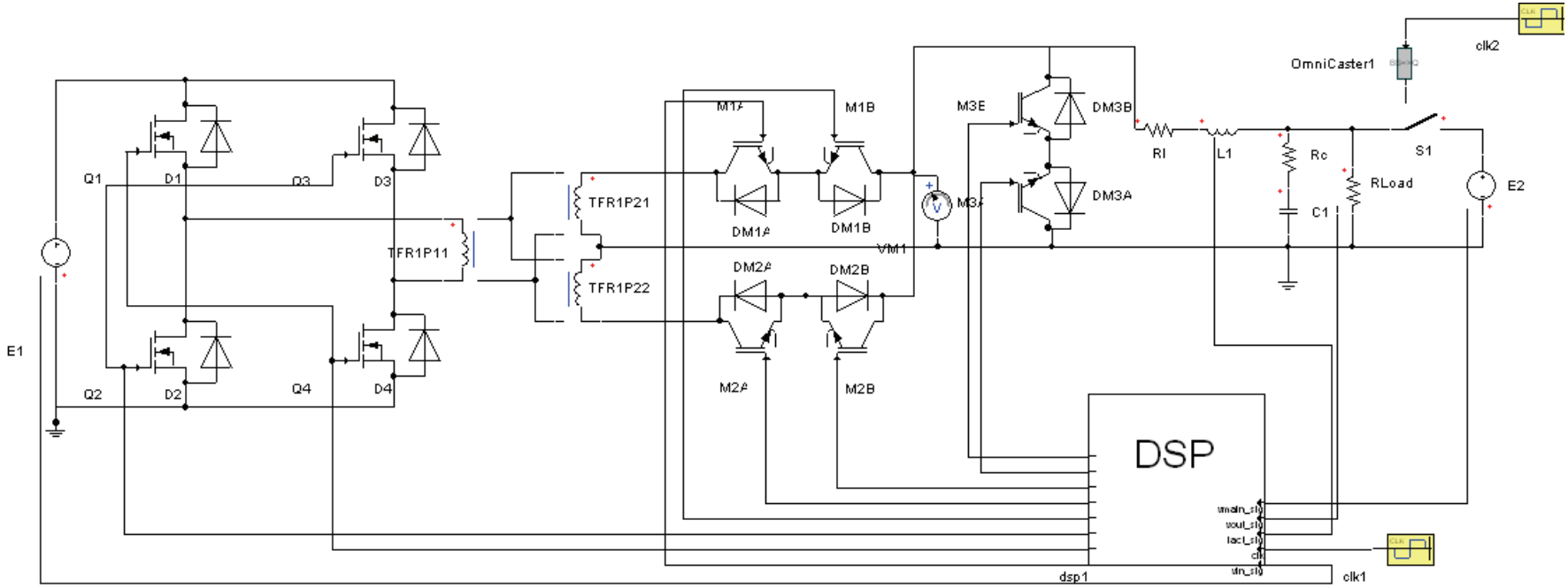

Figure 90: Simplorer Simulation Schematic

14.13 Appendix A.13: Derivation of Forward Mode Transfer Function

14.13.1 Introduction

This appendix contains calculations that were performed for an earlier draft of this thesis. They are included for reference only. As such, they have not been edited for clarity, reference conformity or numbering.

The forward mode control system can only be designed once the transfer function of the converter is known. This is calculated by first constructing state-space equations for the converter for all possible switch states, and then averaging the state equations by means of the duty cycle. Once the transfer function of the converter is known, the compensating network may be designed.

14.13.2 A.13.1 Forward Mode: State Space Representation

The first step in deriving the state-space representation is to identify the state variables. The state variables are chosen as the inductor current (hereafter referred to as x_1) and the output capacitor potential (x_2). For the forward mode, the converter can be in one of 3 states:

- M_1 on and M_2 off
- M_1 off and M_2 on
- Both M_1 and M_2 off

In terms of our state variables, the first two states are identical, since the switches and secondary windings are identical. The three states can be reduced to only two:

- M_1 or M_2 on
- Both M_1 and M_2 off

The schematics for the two states can be redrawn as:

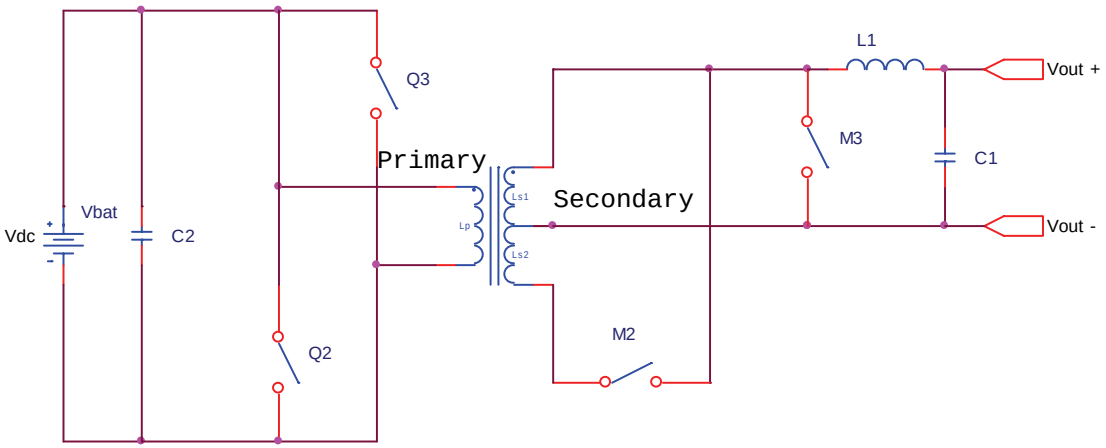

Figure 91: Forward Mode, M_1 or M_2 On (M_1 on shown)

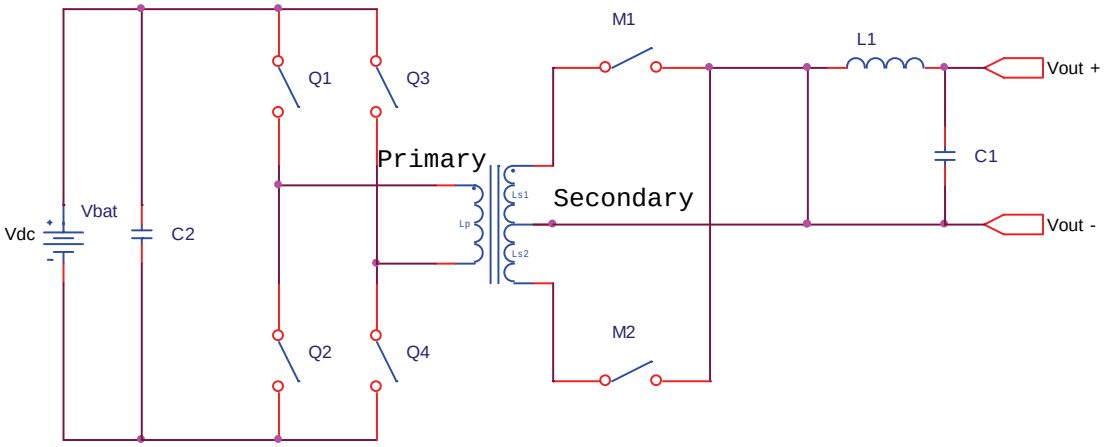

Figure 92: Forward Mode, M_1 & M_2 Off

Since Q_1-Q_4 and Q_2-Q_3 are switched synchronously with M_1 and M_2, it is not necessary to consider them further, as long it is assumed that the correct voltage is applied to the primary winding at the correct instant. If the transformer is assumed to be ideal, the secondary winding voltages are given by:

$$V_{\text{sec}} = \frac{N_{\text{sec}}}{N_{pri}} V_{bat}$$

The state-variable description will first be determined for each of these two states, and then averaged over half of a switching period.

14.13.2.1 State 1: M_1 or M_2 On

In this state, one of the switches is on for the time period $D*T_s$. The converter schematic diagram can be redrawn for this particular state (with M_1 on):

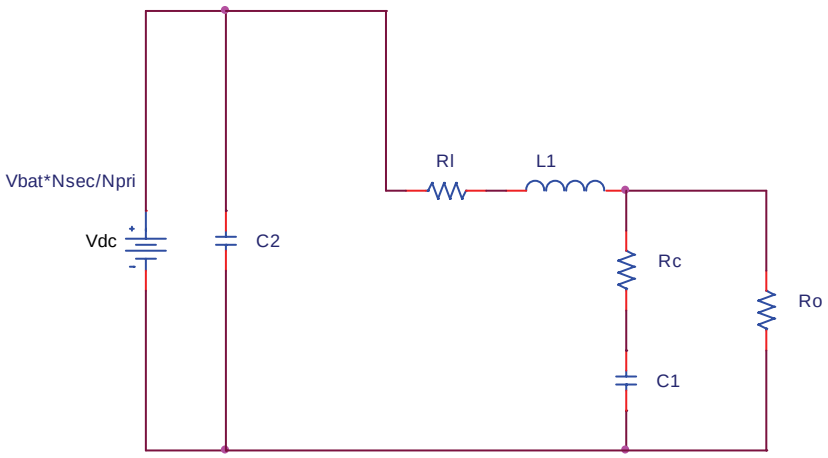

Figure 93: Forward Mode, M_1 or M_2 On

The resistances of the inductor (R_L) and the output capacitor (R_C) are shown in the circuit. It is assumed that the load is resistive, and is represented by R_O. M_2 & M_3 is not switched during the positive forward mode, so they have been removed. The battery, together with the input filter capacitor, is seen as an ideal voltage source. All switches are assumed to be ideal.

With M_1 is switched on, V_{bat} is applied to the left hand side of the inductor. Applying Kirchoff's loop rule to the loop formed by the battery, M1, L1 and C1 results in the following equation:

$$V_{bat}\frac{N_{\sec}}{N_{pri}} = L\dot{x}_1 + R_L x_1 + x_2 + R_C C\dot{x}_2$$

and for the right hand loop:

$$x_2 + R_C C\dot{x}_2 = R_O\left(x_1 + C\dot{x}_2\right)$$

or

$$\dot{x}_2 = \frac{R_O}{C(R_C + R_O)}x_1 - \frac{1}{C(R_C + R_O)}x_1$$

This equation for the second state variable can be substituted into the first to give

$$\dot{x}_1 = -\frac{1}{L}\left[\frac{R_O R_L + R_L R_C + R_O R_C}{\left(R_C + R_O\right)}\right]x_1 - \frac{1}{L}\left[\frac{R_O}{\left(R_C + R_O\right)}\right]x_2 + \frac{N_{\sec}V_{bat}}{N_{pri}L}$$

The output voltage can be written as

$$
\begin{aligned}
V_O &= R_O\left(x_1 - C\dot{x}_2\right) \\
&= R_O\left(x_1 - \frac{R_O}{R_O + R_C}x_1 + \frac{1}{R_O + R_C}x_2\right) \\
&= \frac{R_O R_C}{(R_C + R_O)}x_1 + \frac{R_O}{(R_C + R_O)}x_2
\end{aligned}
$$

The preceding three equations can now be written in standard state-space matrix notation:

$$
\begin{aligned}
\dot{x} &= A_1 x + B_1 V_d \quad for(D * T_S) \\
V_O &= C_1 x \quad for(D * T_S)
\end{aligned}
$$

where

$$
A_1 = \begin{bmatrix} -\frac{1}{L}\left(\frac{R_O R_L + R_L R_C + R_O R_C}{(R_C + R_O)}\right) & -\frac{1}{L}\left(\frac{R_O}{(R_C + R_O)}\right) \\ \frac{R_O}{C(R_C + R_O)} & -\frac{1}{C(R_C + R_O)} \end{bmatrix}
$$

$$
B_1 = \begin{bmatrix} \frac{N_{sec}}{N_{pri}L} \\ 0 \end{bmatrix}
$$

$$
C_1 = \begin{bmatrix} \frac{R_O R_C}{R_C + R_O} & \frac{R_O}{R_C + R_O} \end{bmatrix}
$$

14.13.2.2 State 2: M_1 and M_2 off

In this state the input is disconnected from the output and the inductor current flows through M_3's diode to ground. The schematic of the converter in this state is:

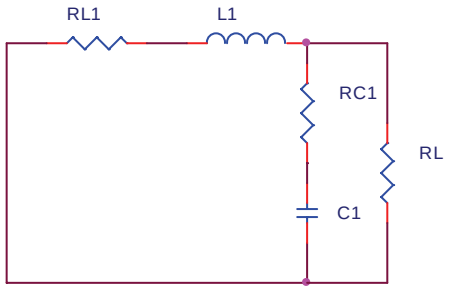

Figure 94: Forward Mode, M_1 & M_2 Off

Since only the input to the circuit is different in this state, it is clear that the A and C matrices for this state is identical to the A and C matrices for the previous state. It should also be recognised that, since the input is now zero,

the B matrix should only contain zeros. Thus, for this state, the state-space representation is:

$$\dot{x} = A_2 x + B_2 V_d \quad for\ (0.5 - D)T_S$$
$$V_O = C_2 x \quad for(0.5 - D)T_S$$

where the A, B en C matrices have the following values:

$$A_2 = A_1$$
$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$
$$C_2 = C_1$$

14.13.3 A.13.2 Forward Mode: Averaging the State-Space Representation

The complete converter state-space representation can be obtained by time-averaging the two states. The duty cycle specifies the time the converter is in each state. This can be stated mathematically:

$$\dot{x} = \begin{cases} A_1 x + B_1 V_d & for(D * T_S) \\ A_2 x + B_2 V_d & for(0.5 - D)T_S \end{cases}$$

and

$$v_0 = \begin{cases} C_1 x & for(D * T_S) \\ C_2 x & for(0.5 - D)T_S \end{cases}$$

where

$$A_1 = A_2 = \begin{bmatrix} -\frac{1}{L}\left(\frac{R_O R_L + R_L R_C + R_O R_C}{(R_C + R_O)}\right) & -\frac{1}{L}\left(\frac{R_O}{(R_C + R_O)}\right) \\ \frac{R_O}{C(R_C + R_O)} & -\frac{1}{C(R_C + R_O)} \end{bmatrix}$$
$$B_1 = \begin{bmatrix} \frac{N_{\text{sec}}}{N_{pri} L} \\ 0 \end{bmatrix}$$
$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$
$$C_1 = C_2 = \begin{bmatrix} \frac{R_O R_C}{R_C + R_O} & \frac{R_O}{R_C + R_O} \end{bmatrix}$$

If the state-space representations are now time-averaged over half of a switching period, then

$$\dot{x} = [A_1 D + A_2(0.5 - D)]x + [B_1 D + B_2(0.5 - D)]V_{bat}$$
$$v_0 = [C_1 D + C_2(0.5 - D)]x$$

To linearize the system, it is split into AC and DC components. Small AC perturbations (indicated by ~) are introduced into the steady-state DC components.

$$x = X + \tilde{x}$$
$$v_0 = V_0 + \tilde{v}_0$$
$$d = D + \tilde{d}$$

If these compound values are substituted into the time-averaged state-space representation, the following is obtained (product terms of ~x and ~d are ignored, and by definition of steady state the derivative of X is zero):

$$\dot{\tilde{x}} = AX + BV_d + A\tilde{x} + [(A_1 - A_2)X + (B_1 - B_2)V_{bat}]\tilde{d}$$

with

$$A = A_1 D + A_2(0.5 - D)$$
$$B = B_1 D + B_2(0.5 - D)$$

Since $A_1 = A_2$, and because the derivative of the steady state values $AX + BV_{bat}$ is zero, the representation becomes

$$\dot{\tilde{x}} = A\tilde{x} + (B_1 - B_2)V_{bat}]d$$

By time-averaging the output voltage, and applying the same reasoning as above, it can be shown that:

$$\tilde{v}_0 = C\tilde{x}$$

To obtain the transfer function of the converter, the above two equations can be Laplace-transformed:

$$\tilde{x}(s) = (sI - A)^{-1}(B_1 - B_2)V_{bat}\tilde{d}(s)$$
$$\tilde{v}_0 = C\tilde{x}(s)$$
or
$$\frac{\tilde{v}_0(s)}{\tilde{d}(s)} = C(sI - A)^{-1}(B_1 - B_2)V_d$$

The values of the A, B and C matrices may now be substituted

$$\frac{\tilde{v}_0(s)}{\tilde{d}(s)} = \begin{bmatrix} \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} s - \frac{1}{L}\left(\frac{Rr_L + r_c r_L + r_C R}{R+r_C}\right) & -\frac{1}{L}\left(\frac{R}{R+r_C}\right) \\ \frac{R}{C(R+r_C)} & s - \frac{1}{C(R+r_C)} \end{bmatrix}^{-1} \begin{bmatrix} \frac{N_{sec}}{N_{pri}}\frac{1}{L} \\ 0 \end{bmatrix} V_{bat}$$

which, after simplification, is the desired result:

$$\frac{\tilde{v}_0(s)}{\tilde{d}(s)} = V_{bat}\frac{N_{\sec}}{N_{pri}}\left[\frac{1 + sr_c C}{LC\left(s^2 + s\left(\frac{1}{RC} + \frac{r_c + r_L}{L}\right) + \frac{1}{LC}\right)}\right]$$

This equation relates the change in output voltage for a change in duty cycle.

14.13.4 A.13.3 Forward Voltage Mode Compensation

14.13.4.1 Additional Gains

The additional gains are calculated exactly the same way as for the forward mode. This time, the inductor current is measured, and the measurement gain is given as:

$$A_{Measure} = 32767/500$$
$$= 65.534$$

The switching frequency is unchanged, so that the PWM gain is the same at 1/333.

The total additional gain is thus given by:

$$A_{LOOP} = 65.534/333$$
$$= 0.1968$$

14.13.4.2 Forward Mode: Lead & Lag Compensation

To design the lead and lag compensation networks, a Bode plot of the system frequency response is required. Since the transfer function has already been calculated, and all the component values have already been chosen, the Bode plot can easily be generated using Matlab.

The method followed is based on undergraduate work done previously by the author as well as [5.3].

In order to be as accurate as possible, the resistances of the inductor and DC link capacitor were measured on actual components with a RACAL-DANA 9343 LCR Bridge. The values measured at 10kHz were:

R_c = 0.036 Ohm
R_l = 1.6 Ohm

The Bode plot is shown below, while the Matlab code used to generate it can be found in the Appendix H.

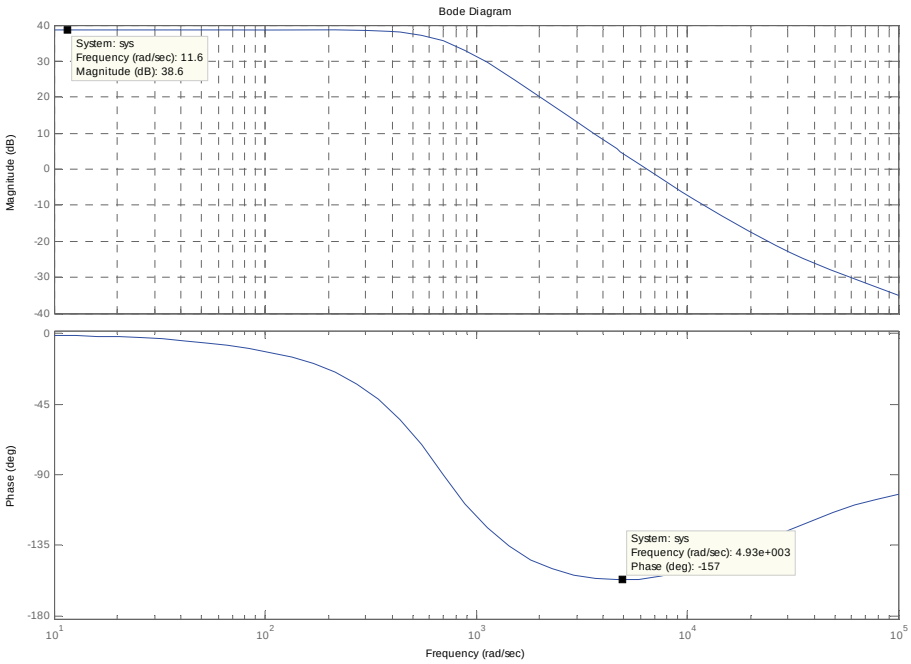

Figure 95: Converter Forward Response, Uncompensated

From the above figure it can be seen that the minimum phase margin is only 23 degrees at approximately 4900 rad/s, which will be too low when the lag compensation is introduced. A lead compensator is therefore required to improve the phase margin.

A lead-lag compensator has the standard form:

$$G_C = K\frac{1+T_{lead}s}{1+\alpha T_{lead}s}\frac{1+T_{lag}s}{1+\beta T_{lag}s}$$

Where $0<\alpha<1$ and $\beta>1$. First consider the steady state error.

In order to have an error of less than E_{steady} =0.5%, the overall gain of the compensator and the converter should be:

$$E_{steady} = \frac{1}{1+A_{LOOP}}$$

$$A_{LOOP} = \frac{1}{E} - 1$$

$$= 199$$

Choose A_{LOOP} as 200. The converter transfer function with additional gains have a total gain of 85 (Approximately 38.6dB) at zero frequency. Thus K should be 200/85 = 2.344.

Now consider the lead compensation factor. Assume that the lead compensator should increase the phase margin by $\phi_m = 45°$. Since the lead compensator will be implemented in software, the choice is arbitrary.

The required attenuation factor can be calculated from

$$\alpha = \frac{1-\sin\phi_m}{1+\sin\phi_m}$$
$$= 0.172$$

By recognising that the frequency of maximum phase shift is the geometric mean of the two corner frequencies of the lead compensator, the lower corner period T can be calculated as:

$$T = \frac{1}{\sqrt{\alpha}\omega_m}$$
$$= 0.514ms$$

The transfer function of the lead compensator is thus:

$$G_{LEAD} = \frac{1+0.000514s}{1+0.000088s}$$

The Bode plot of the lead compensated system is shown below.

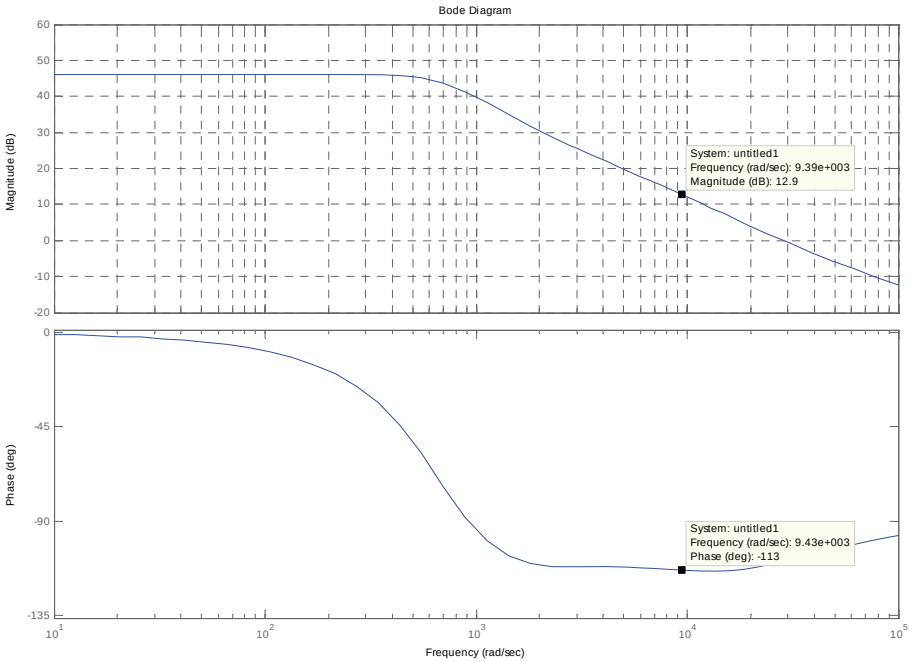

Figure 96: Forward Converter Response, Lead Comp.

To ensure that the system responds quickly to transients, such as load changes, the crossover frequency is selected one decade below the switching frequency. From the lead compensated Bode plot it can be seen that the new phase margin, at the chosen crossover frequency of 1500Hz (9424 rad/sec), has improved to 67°, which is adequate.

To reduce the crossover frequency to the chosen value of 1500Hz, the lag compensation factor is considered (equation above).

The corner frequency (ω_l) of the lag compensator is selected to be one decade below the crossover frequency (ω_c). This low corner frequency has been chosen so that the phase margin is improved by placing the compensator zero well before the converter minimum phase frequency. This corner frequency corresponds to the zero of the lag compensator (given by $\omega_l = \frac{1}{T}$), so

$$T = \frac{1}{\omega_l} = \frac{1}{0.1 \cdot \omega_c} = \frac{1}{0.1 \cdot 2\pi(1500)} = 1.06ms$$

From the Bode plot it can be seen that the system gain at the crossover frequency is still 12.9dB. To attenuate the system to 0dB, β must have a value of

$$\begin{aligned} -12.9 &= -20\log_{10}\beta \\ 0.645 &= \log_{10}\beta \\ \therefore \beta &= 4.415 \end{aligned}$$

The transfer function of the lag compensator is therefore

$$G_{lead}(s) = \frac{1 + 0.00106s}{1 + 0.00468s}$$

The Bode plot of the compensated system is given below:

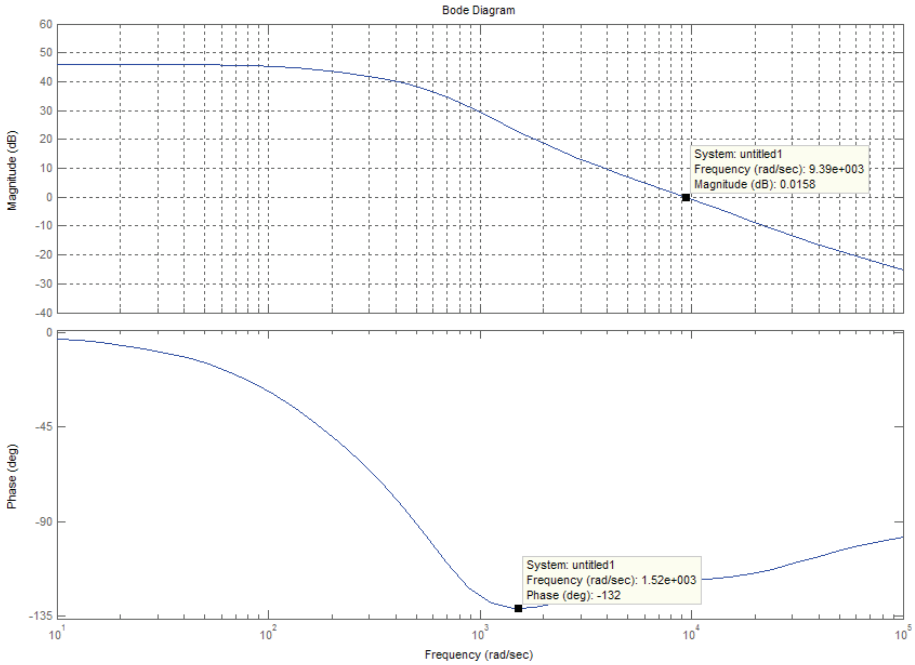

Figure 97: Forward Converter Response, Lead & Lag Comp.

The compensated system has a phase margin of 48°, which is greater than the recommended 45°.

The closed loop response of the system with compensator is shown below:

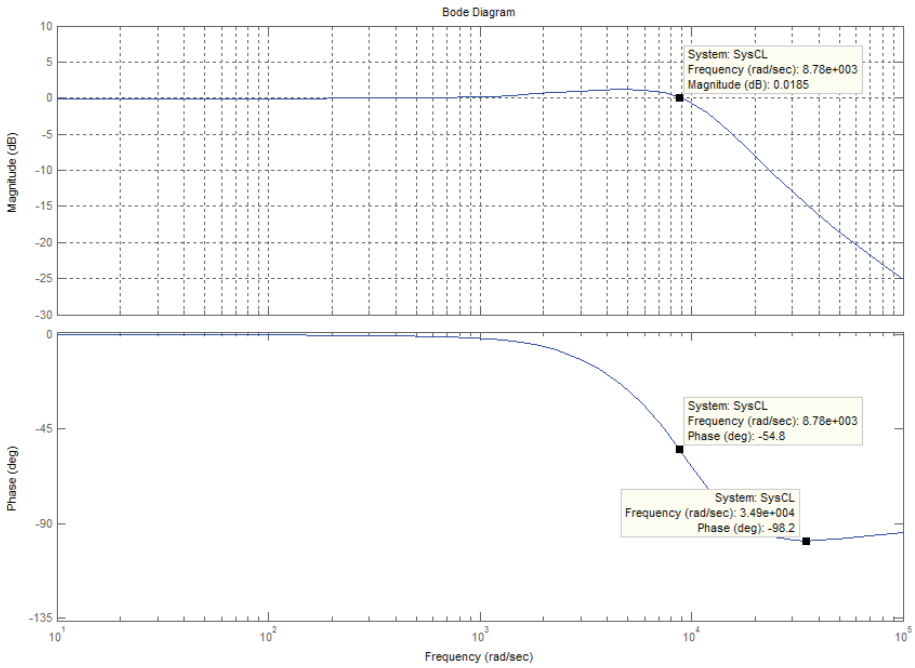

Figure 98: Forward Converter Response: Closed Loop

It can be seen that the converter will accurately track reference voltage references up to about 10kHz, and will not show any instabilities due to the wide phase margin.

14.13.4.3 Compensator Digitisation

In order to implement the compensation on a microprocessor, it needs to be converted to digital form. The Matlab function "c2d" was used to perform the z-transform. The sampling frequency need not be the same as the switching frequency. To reduce the computational load on the DSP, a sampling frequency of $1/10^{th}$ the switching frequency was selected. This is equal to f_{SAMPLE} = 10/30kHz = 333us. The result is:

$$G_z = \frac{3.101 - 5.196z^{-1} + 2.251z^{-2}}{1 - 0.9554z^{-1} + 0.02192z^{-2}}$$

The difference equation can be obtained by equating the above transfer function to the ration of the controller output to the controller input:

$$\frac{3.101 - 5.196z^{-1} + 2.251z^{-2}}{1 - 0.9554z^{-1} + 0.02192z^{-2}} = \frac{u(k)}{e(k)} = \frac{u(k)}{r(k) - c(k)}$$

$$u(k) - 0.9554u(k-1) + 0.02192u(k-2) = 3.101(r(k) - c(k)) - 5.196(r(k-1) - c(k-1)) + 2.251(r(k-2) - c(k-2))$$

$$u(k) = 3.101(r(k) - c(k)) - 5.196(r(k-1) - c(k-1)) + 2.251(r(k-2) - c(k-2)) + 0.9554u(k-1) - 0.02192u(k-2)$$

Which can be directly implemented in the microprocessor.

15 Appendix B: Software Code

Contents

15.1 Appendix B.1: Matlab Code: Forward Mode Response and Compensation

```
%Matlab Code to generate un-compensated and compensated Bode plots
%of the converter in the forward mode, as well as digitise compensator.

L = 0.001760;          %Inductance Value
C = 0.0012;            %Capacitance Value
rl = 1.6;              %Inductor Resistance
rc = 0.036;            %Capacitor Resistance
vbat = 48;             %Battery Voltage
nsec = 9;              %Secondary Winding Turns
npri = 1;              %Primary Winding Turns
R = 52.8125;           %Load Resistance for 2kW output
A = tf(0.1968);        %PWM and Measurement Gain

num = vbat*nsec/npri*[rc*C 1];                  %Numerator
den = L*C*[1 (1/(R*C) + (rc + rl)/L) 1/(L*C)];  %Denumerator
sys1 = tf(num,den);                             %Converter Transfer Function
sys = A*sys1

num_lead = [0.000514 1];       %Numerator
den_lead = [0.000088 1];       %Denumerator
lead = tf(num_lead,den_lead)   %Compensator Transfer Function

num_lag = [0.00106 1];         %Numerator
den_lag = [0.00468 1];         %Denumerator
lag = tf(num_lag,den_lag)      %Compensator Transfer Function

K = tf(2.344);                 %Compensator Gain

comp = K*lead*lag              %Complete Lead/Lag Compensator Transfer Function

bode(sys,{10,100000});         %Bode plot of open loop system
grid on;
figure;
bode(K*sys*lead,{10,100000});  %Bode plot of lead compensated open loop system
grid on;
figure;
bode(K*sys*lead*lag,{10,100000});   %Bode plot of lead & lag compensated open loop
system
grid on;

SysCL = comp*sys/(1+comp*sys);
figure;
bode(SysCL,{10,100000});       %Bode plot of lead & lag compensated closed loop system
grid on;

Comp_Digital = c2d(comp,(0.00033),'zoh')    %Digitisation of Compesnator
```

15.2 Appendix B.2: Matlab Code: Reverse Mode Response and Compensation

```
%Matlab Code to generate un-compensated and compensated Bode plots
%of the converter in the reverse mode.

L = 0.001760;              %Inductance Value
rl = 1.6;                  %Inductor Resistance
nsec = 9;                  %Secondary Winding Turns
npri = 1;                  %Primary Winding Turns
Vout = 325;                %DC link voltage
A = tf(1.968);             %PWM and Measurement Gain

Io = 0.1;
num = [(-Io*L) (Vout + Io*rl)];
den = [L rl];
sys1 = A*tf(nsec/npri)*tf(num,den);     %System Transfer Function for I = 0.1A

Io = 1;
num = [(-Io*L) (Vout + Io*rl)];
den = [L rl];
sys2 = A*tf(nsec/npri)*tf(num,den);     %System Transfer Function for I = 1A

Io = 5;
num = [(-Io*L) (Vout + Io*rl)];
den = [L rl];
sys3 = A*tf(nsec/npri)*tf(num,den);     %System Transfer Function for I = 0.5A

Io = 15;
num = [(-Io*L) (Vout + Io*rl)];
den = [L rl];
sys4 = A*tf(nsec/npri)*tf(num,den)      %System Transfer Function for I = 15A

K = tf(0.05177);                        %Compensator Gain

cnum = [0.002 1];
cden = [0.077 1];
comp = K*tf(cnum,cden)*tf(1);           %Compensator Transfer Function

%bode(sys1,sys2,sys3,sys4);             %System Bode Plots
%bode(sys4*K)                           %System and Compensator Gain Bode Plots
%bode(sys1*comp,sys2*comp,sys3*comp,sys4*comp); %System and Compensator Bode
Plots

cl1 = sys1*comp/(1+sys1*comp);
cl2 = sys2*comp/(1+sys2*comp);
cl3 = sys3*comp/(1+sys3*comp);
cl4 = sys4*comp/(1+sys4*comp);
bode(cl1,cl2,cl3,cl4);                  %System and Compensator Closed Loop Bode Plots

Comp_Digital = c2d(comp,(0.00033),'zoh')  %Digitisation of Compensator
```

15.3 Appendix B.3: Matlab Code: AC Output Response and Compensation

```
%Matlab Code to generate un-compensated and compensated Bode plots
%of the converter in AC Output mode for both current and voltage loops.

L = 0.003520;              %Inductance Value
rl = 1.6;                  %Inductor Resistance
C = 3.2E-6;                %Capacitance Value
rc = 0.036;                %Capacitor Resistance
Rl = 26.45;                %AC Load Resistance
nsec = 9;                  %Secondary Winding Turns
npri = 1;                  %Primary Winding Turns
Vbat = 48;                 %BAttery voltage
AMC = tf(655.34);          %Current Measurement Gain
AMV = tf(65.534);          %Voltage Measurement Gain
APWM = tf(1/333);          %PWM Gain
ATRF = tf(Vbat*nsec/npri); %Battery and Transformer Gain

num = [1];
den = [L rl];
sys_cur = tf(num,den);
cur_loop = APWM*ATRF*sys_cur*AMC;          %Current Loop Transfer
Function

cnum = [454];              %Pole at 454 rad/s
cden = [1 454];
comp_cur1 = tf(cnum,cden);                 %Current Compensator Transfer
Function 1

cnum = [1 4540];           %Zerp at 4540 rad/s
cden = [4540];
comp_cur2 = tf(cnum,cden);                 %Current Compensator Transfer
Function 2
comp_cur = comp_cur1*comp_cur2             %Current Compensator Transfer
Function

sys_cur_cl = comp_cur*APWM*ATRF*sys_cur/(1 +
comp_cur*APWM*ATRF*sys_cur*AMC); %Current Closed Loop Response

num = [C*rc Rl];           %Output Section
den = [C*(rc + Rl) 1];
sys_out = tf(num,den);     %Output Impedance Transfer Function

sys_loop = sys_cur_cl*sys_out*AMV;  %Voltage Loop Transfer Function

cnum = [0.000082 1];       %Voltage Loop Lag Compensator
cden = [0.050 1];
comp = 76*tf(cnum,cden)
```

```
sys_cl = comp*sys_cur_cl*sys_out/(1 + comp*sys_cur_cl*sys_out*AMV);%Closed Loop System Response

%bode(cur_loop, {1, 50000});          %Plot Current Loop
%grid on;
%figure;
%bode(comp_cur);                      %Plot Current Compensator
%grid on;
%figure;
%bode(cur_loop*comp_cur);             %Plot Compensated Current Loop
%grid on;
%figure;
%bode(sys_cur_cl);                    %Plot Closed Current Loop Response
%grid on;

figure;
bode(sys_loop);                       %Plot Voltage Loop
grid on;
%figure;
%bode(comp);                          %Plot Voltage Compensator
figure;
bode(sys_loop*comp);                  %Plot Compensated Voltage Loop

figure;
bode(sys_cl);                         %Plot Closed Voltage Loop
grid on;
c2d(comp_cur, 0.000033,'zoh')         %Digitize Current Compensator
c2d(comp,0.000033,'zoh')              %Digitize Voltage Compensator
```

15.4 Appendix B.4: DSP Code Listing

15.4.1 Main Program

```
/*********************************************************/
/*
  Name                : ASMSC.c
  Descrption   : Bi-directional converter control
  Author              : AN Schutte
  Date                : 2008-11-25
  Revision            : 1
*/
/*********************************************************/

/*
  Control of a bi-directional converter, AC Output.
  Generate sawtooths for switching on T1 and T2.
  Monitor Inductor Current on ADCIN0
  Monitor Battery Voltage on ADCIN1
  Monitor Output Voltage on ADCIN2
  Monitor Mains Supply Voltage on ADCIN3
*/

/*** Load Address Definitions ***/
#include       "EVA24XX.h"
#include       "DIO24XX.h"
#include       "SYS24XX.h"
#include       "ADC24XX.h"
#include       "COM24XX.h"
#include       "math.h"

/*** Constant Definitions ***/
/*XXX*/

/*** Global Variable Definitions ***/
signed int g_iSin_cntr;              /*Counter to generate sine wave reference */
signed int g_iSin_table[151];
signed int g_iI_Max;
unsigned int g_iToggle = 0;

/***************************** SUB ROUTINES *************************/

void generate_sine(signed int *p_iTable, signed int p_iAmpl, signed int p_iPer_quart)
{int l_iIndex;
 for (l_iIndex = 0;l_iIndex <= p_iPer_quart; l_iIndex++)
 {
       p_iTable[l_iIndex] = p_iAmpl*sin(1.5708*l_iIndex/(p_iPer_quart));
 }
}

void generate_const(signed int *p_iTable, signed int p_iAmpl, signed int p_iPer_quart)
{int l_iIndex;
 for (l_iIndex = 0;l_iIndex <= p_iPer_quart; l_iIndex++)
 {
       p_iTable[l_iIndex] = p_iAmpl;
 }
}


void set_mode(short int p_iMode, short int p_iPol, int p_iD, int p_iPer)
{
       /*ACTRA = *ACTRA & 0xF000;    /* Reset PWM1-6 bits (0-11) */
       /*GPTCONA = *GPTCONA & 0xFFF0;/* Reset T1PWM Action bits (0&1) */

       if (p_iMode && p_iPol)        /* Forward Mode, Positive Polarity */
       {
              *ACTRA = 0x02CC;              /* Set
PWM1=FH,PWM2=FL,PWM3=FH,PWM4=FL,PWM5=AH,PWM6=FL */
              *GPTCONA = (*GPTCONA & 0xFFF0) | 0x0001;/* T1PWM=AL,T2PWM=FH */
       }
       else if (p_iMode && !p_iPol)/* Forward Mode, Negative Polarity */
       {
           *ACTRA = 0x0E33;          /* Set
PWM1=FL,PWM2=FH,PWM3=FL,PWM4=FH,PWM5=AH,PWM6=FH */
```

```
                *GPTCONA = (*GPTCONA & 0xFFF0) | 0x0001;/* T1PWM=AL,T2PWM=FH */
        }
        else if (!p_iMode && p_iPol)/* Reverse Mode, Positive Polarity */
        {
            *ACTRA = 0x0CB7;          /* Set
PWM1=FL,PWM2=AH,PWM3=FL,PWM4=AL,PWM5=FL,PWM6=FH */
                *GPTCONA = (*GPTCONA & 0xFFF0) | 0x0004;/* T1PWM=FL,T2PWM=AH */
        }
        else                                        /* Reverse Mode, Any Polarity */
        {
                *ACTRA = 0x00ED;              /* Set
PWM1=AH,PWM2=FL,PWM3=AL,PWM4=FL,PWM5=FL,PWM6=FL */
                *GPTCONA = (*GPTCONA & 0xFFF0) | 0x0004;/* T1PWM=FL,T2PWM=AH */
        }

        *CMPR3 = 666 - p_iD;
        *T1CMPR = p_iD;

        *CMPR1 = 325;
        *CMPR2 = 325;
        *T2CMPR = 333 - p_iD;
}


/***************************** MAIN ROUTINE *************************/
void main(void)
{
/* Variable Definitions */
 short int l_iFwd = 0, l_iPos = 0, l_iMask;  /* Mode flags, 0 = REV & NEG */
 short int l_iFwd_prev, l_iPos_prev;         /* Previous Cycle Mode flags, 0 = REV &
NEG */
 signed int l_iD, l_iD_prev;                         /* Duty Cycles */
 signed int l_iVbat = 0;                             /* Bat. voltage -100 to 100V = -
32768 to 32768 */
 signed int l_iVout = 0;                             /* HV Cap voltage -500 to 500V = -
32768 to 32768 */
 signed int l_iIout = 0;                             /* Output current -25 to 25A = -
32768 to 32768 */
 signed int l_iVmain = 0;                            /* Mains voltage -500 to 500V = -
32768 to 32768 */
 signed int l_iIbat = 0;                                     /* Battery Current -200 to
200A = -32768 to 32768 */
 signed int l_iVout_prev, l_iIout_prev;              /* Previous Cycle Output Values */
 signed int l_iVcmd = 0, l_iIcmd = 0;        /* Reference Values */
 signed int l_iVcmd_prev, l_iIcmd_prev;      /* Previous Referene Values */

 signed int l_iIerror = 0, l_iIerror_prev = 0; /* Current Error Values */
 signed int l_iVerror = 0, l_iVerror_prev = 0; /* Voltage Error Values */

 int l_iRef_mode = 3;                         /* Change via JTAG for commissioning */
 int l_iRef_val = 166;                       /* Change via JTAG for commissioning */
 int x;                                                              /* General
Purpose Variable */

/* Do Initialisations */
 init_SYS();
 init_DIO();
 init_Timers();
 init_ADC();

/*** Other setup ***/
 /* Generate Reference Sine Array */
 x = 0;               /* Dummy instruction for breakpoint position */
 g_iI_Max = 770;
 generate_sine(g_iSin_table, 7573, 150); /* Always generate this one */
 if (l_iRef_mode == 1) generate_sine(g_iSin_table, 10816, 150);
 if (l_iRef_mode == 2) generate_sine(g_iSin_table, 5408, 150);
 if (l_iRef_mode == 3) generate_sine(g_iSin_table, 2704, 150);
 if (l_iRef_mode == 4) generate_sine(g_iSin_table, l_iRef_val, 150);


/*** Setup Interrupts ***/
 init_SYS_INT();
 init_EVA_INT();

/*** Enable global interrupts ***/
 asm(" CLRC INTM");                 /* enable global interrupts */
```

```
/*** Proceed with main routine ***/
for ( ; ; )                                          /* endless loop, wait for
interrupt */
 {
    if ((ADCCTRL2 & INT_FLAG_SEQ1) && g_iToggle)     /* Test for ADC event and every
second switch period*/
    {
        ADCCTRL2 |= INT_FLAG_SEQ1;    /* Reset timer 2 interrupt flag */

            /* Do as much as possible while waiting for ADC */
               /* Store Previous' cycle's values */
            l_iVcmd_prev = l_iVcmd;
               l_iIcmd_prev = l_iIcmd;
               l_iVout_prev = l_iVout;
               l_iIout_prev = l_iIout;
               l_iD_prev = l_iD;
               l_iFwd_prev = l_iFwd;
               l_iPos_prev = l_iPos;


               /*Calculate Voltage Reference */
               if (g_iSin_cntr >= (600)) g_iSin_cntr = 0;
               if (g_iSin_cntr <= (150)) l_iVcmd = g_iSin_table[g_iSin_cntr];
               else if (g_iSin_cntr <= (300)) l_iVcmd = g_iSin_table[300 -
g_iSin_cntr];
               else if (g_iSin_cntr <= (450)) l_iVcmd = -g_iSin_table[g_iSin_cntr -
300];
               else if (g_iSin_cntr <= (600)) l_iVcmd = -g_iSin_table[600 -
g_iSin_cntr];


               /* Commissioning */
               if (l_iRef_mode == 5) l_iVcmd = l_iRef_val;


               /* Wait for measurement to finish */
               x = 0;
       while (ADCCTRL2 & SEQ1_BSY)
       {
               x++;
       }


       /* Scale newly measured values */
       l_iIout = (RESULT0 >> 2) - 9552;
       l_iVbat = (RESULT1 >> 3) - 4095;
           l_iVout = (RESULT2 >> 1) - 18592;
           l_iVmain =(RESULT3 >> 1) - 18835;
               /*l_iIbat = l_iIout*9*l_iVbat/l_iVout;       /* Compute steady state
battery current */


               /* Calculate Current Reference */
               l_iVerror = l_iVcmd - l_iVout;
               l_iVerror_prev = l_iVcmd_prev - l_iVout_prev;
               l_iIcmd = (0.1246*l_iVerror - 0.02439*l_iVerror_prev +
0.9987*l_iIcmd_prev);
               if (l_iIcmd > g_iI_Max)       l_iIcmd = g_iI_Max;
               else if (l_iIcmd < -g_iI_Max) l_iIcmd = -g_iI_Max;


       /* Commissioning */
               if (l_iRef_mode == 6) l_iIcmd = l_iRef_val;


               /* Calculate Duty Cycle */
               if (l_iIcmd >= 0) l_iIerror = l_iIcmd - l_iIout;
               else l_iIerror = l_iIout - l_iIcmd;

               if (l_iIcmd_prev >= 0) l_iIerror_prev = l_iIcmd_prev - l_iIout_prev;
               else l_iIerror_prev = l_iIout_prev - l_iIcmd_prev;

               l_iD = (0.1*l_iIerror - 0.07048*l_iIerror_prev + 0.9705*l_iD_prev);
               if (l_iD > 300)       l_iD = 300;
               else if (l_iD < 0) l_iD = 0;
```

```
		/* Force small (<150 mA) inductor currents to zero */
		if ((l_iIout > -100) && (l_iIout < 100)) l_iIout = 0;


		/* Determine Direction and Polarity */
		l_iMask = 0;
		if ((l_iVcmd >= 0) && (l_iIout >= 0) && (l_iIcmd >= 0))
		{
			l_iPos = 1;
			l_iFwd = 1;
		}
		else if ((l_iVcmd >= 0) && (l_iIout > 0) && (l_iIcmd < 0))
		{
			l_iPos = 1;
			l_iFwd = 1;
			l_iMask = 1;
		}
		else if ((l_iVcmd >= 0) && (l_iIout <= 0) && (l_iIcmd < 0))
		{
			l_iPos = 1;
			l_iFwd = 0;
		}
		else if ((l_iVcmd >= 0) && (l_iIout < 0) && (l_iIcmd >= 0))
		{
			l_iPos = 1;
			l_iFwd = 0;
			l_iMask = 1;
		}
		else if ((l_iVcmd < 0) && (l_iIout >= 0) && (l_iIcmd >= 0))
		{
			l_iPos = 0;
			l_iFwd = 0;
		}
		else if ((l_iVcmd < 0) && (l_iIout > 0) && (l_iIcmd < 0))
		{
			l_iPos = 0;
			l_iFwd = 0;
			l_iMask = 1;
		}
		else if ((l_iVcmd < 0) && (l_iIout <= 0) && (l_iIcmd <= 0))
		{
			l_iPos = 0;
			l_iFwd = 1;
		}
		else if ((l_iVcmd < 0) && (l_iIout < 0) && (l_iIcmd >= 0))
		{
			l_iPos = 0;
			l_iFwd = 1;
			l_iMask = 1;
		}


		/* Test for mode change and invert duty cycle if so */
		if ((l_iFwd && !l_iFwd_prev) || (!l_iFwd && l_iFwd_prev))
		{
			if ((l_iVcmd < 300) && (l_iVcmd > -300) && (l_iIout < 300) &&
(l_iIout > -300)) l_iD = 0;
			else l_iD = 333 - l_iD;
		}


		/* Commissioning */
		if (l_iRef_mode == 7)
		{
			l_iD = l_iRef_val;
			l_iFwd = 1;
			l_iPos = 1;
			l_iMask = 0;
		}
		else if (l_iRef_mode == 8)
		{
			l_iD = l_iRef_val;
			l_iFwd = 1;
			l_iPos = 0;
			l_iMask = 0;
		}
```

```
                else if (l_iRef_mode == 9)
                {
                        l_iD = l_iRef_val;
                        l_iFwd = 0;
                        l_iPos = 1;
                        l_iMask = 0;
                }

                else if (l_iRef_mode == 10)
                {
                        l_iD = l_iRef_val;
                        l_iFwd = 0;
                        l_iPos = 0;
                        l_iMask = 0;
                }
                x = 0;          /* Dummy instruction for Breakpoint */
                /*** Toggle the IOPC0 pin ***/
        *PCDATDIR = *PCDATDIR ^ 0x0008;    /* Reset the IOPC3 bit to toggle the pin */

                /* Test for Duty Cycle Masking and set mode and duty cycle */
                if (l_iMask) set_mode(l_iFwd,l_iPos, 0, 666);
                else set_mode(l_iFwd, l_iPos, l_iD, 666);


    }
 }
}
/* end of main() */


/********************** INTERRUPT SERVICE ROUTINES ********************/

interrupt void timer1_isr(void)
{

     *EVAIFRA = *EVAIFRA & 0x0080;      /* clear T1PINT flag */
     g_iSin_cntr ++;

         g_iToggle = g_iToggle ^ 0x0001;

/*** Toggle the IOPC0 pin ***/
/*      *PCDATDIR = *PCDATDIR ^ 0x0008;    /* Reset the IOPC3 bit to toggle the pin */
}
```

15.4.2 Interrupt Vector Table

```
;***************************************************************
* Filename: cvectors.asm                                       *
*                                                              *
* Author: David M. Alter, Texas Instruments Inc.               *
*                                                              *
* Last Modified: 03/14/01                                      *
*                                                              *
* Description: Interrupt vector table for '240x DSP core       *
* for use with C language programs.                            *
*                                                              *
;***************************************************************

         .ref _c_int0, _timer1_isr

        .sect    "vectors"
rset:   B       _c_int0         ;00h reset
int1:   B       int1            ;02h INT1
int2:   B       _timer1_isr     ;04h INT2
int3:   B       int3                 ;06h INT3
int4:   B       int4            ;08h INT4
int5:   B       int5            ;0Ah INT5
int6:   B       int6            ;0Ch INT6
int7:   B       int7            ;0Eh reserved
int8:   B       int8            ;10h INT8  (software)
int9:   B       int9            ;12h INT9  (software)
int10:  B       int10           ;14h INT10 (software)
int11:  B       int11           ;16h INT11 (software)
int12:  B       int12           ;18h INT12 (software)
int13:  B       int13           ;1Ah INT13 (software)
int14:  B       int14           ;1Ch INT14 (software)
int15:  B       int15           ;1Eh INT15 (software)
int16:  B       int16           ;20h INT16 (software)
int17:  B       int17           ;22h TRAP
int18:  B       int18           ;24h NMI
int19:  B       int19           ;26h reserved
int20:  B       int20           ;28h INT20 (software)
int21:  B       int21           ;2Ah INT21 (software)
int22:  B       int22           ;2Ch INT22 (software)
int23:  B       int23           ;2Eh INT23 (software)
int24:  B       int24           ;30h INT24 (software)
int25:  B       int25           ;32h INT25 (software)
int26:  B       int26           ;34h INT26 (software)
int27:  B       int27           ;36h INT27 (software)
int28:  B       int28           ;38h INT28 (software)
int29:  B       int29           ;3Ah INT29 (software)
int30:  B       int30           ;3Ch INT30 (software)
int31:  B       int31           ;3Eh INT31 (software)
```

15.4.3 Digital I/O Initialization

```
/*********************************************************/
/*
  Name                : DIO24XX.h
  Descrption   : Header file for Digital Inputs / Outputs
  Author              : AN Schutte
  Date                : 2008-11-01
  Revision            : 2
*/
/*********************************************************/

/* I/0 Multiplex control register A. Selects primary or secondary function */
#define MCRA         (volatile unsigned int *)0x7090   /* I/O mux control reg A */
#define MCRB         (volatile unsigned int *)0x7092   /* I/O mux control reg B */
#define MCRC         (volatile unsigned int *)0x7094   /* I/O mux control reg C */

/* Data and direction registers for input/ output ports */
#define PADATDIR     (volatile unsigned int *)0x7098   /* I/O port A data & dir reg */
#define PBDATDIR     (volatile unsigned int *)0x709A   /* I/O port B data & dir reg */
#define PCDATDIR     (volatile unsigned int *)0x709C   /* I/O port C data & dir reg */
#define PDDATDIR     (volatile unsigned int *)0x709E   /* I/O port D data & dir reg */
#define PEDATDIR     (volatile unsigned int *)0x7095   /* I/O port E data & dir reg */
#define PFDATDIR     (volatile unsigned int *)0x7096   /* I/O port F data & dir reg */

/* External interrupt configuration registers */
#define XINT1CR      (volatile unsigned int *)0x7070   /* Ext interrupt 1 config reg
*/
#define XINT2CR      (volatile unsigned int *)0x7071   /* Ext interrupt 2 config reg
*/


/* Initialisation Function(s) */
void init_DIO(void);

/* End of DIO24XX.h */


/*********************************************************/
/*
  Name                : DIO24XX.c
  Description  : Subroutines to initialise the digital I/O
  Author              : AN Schutte
  Date                : 2008-11-24
  Revision            : 2
*/
/*********************************************************/

#include "DIO24XX.h"

/*      Initialise EVA General Purpose Timer Control.
        Use Config Sheet to calculate register values */

void init_DIO(void)
{
 *MCRA = 0x3FC3;                    /* group A pins */
/*
 bit 15        0:      0=IOPB7,     1=TCLKINA
 bit 14        0:      0=IOPB6,     1=TDIRA
 bit 13        1:      0=IOPB5,     1=T2PWM/T2CMP
 bit 12        1:      0=IOPB4,     1=T1PWM/T1CMP
 bit 11        1:      0=IOPB3,     1=PWM6
 bit 10        1:      0=IOPB2,     1=PWM5
 bit 9         1:      0=IOPB1,     1=PWM4
 bit 8         1:      0=IOPB0,     1=PWM3
 bit 7         1:      0=IOPA7,     1=PWM2
 bit 6         1:      0=IOPA6,     1=PWM1
 bit 5         0:      0=IOPA5,     1=CAP3
 bit 4         0:      0=IOPA4,     1=CAP2/QEP2
 bit 3         0:      0=IOPA3,     1=CAP1/QEP1
 bit 2         0:      0=IOPA2,     1=XINT1
 bit 1         1:      0=IOPA1,     1=SCIRXD
 bit 0         1:      0=IOPA0,     1=SCITXD
*/
```

```
 *MCRB = 0xFE00;                    /* group B pins */
/*
 bit 15        1:      0=reserved,  1=TMS2 (always write as 1)
 bit 14        1:      0=reserved,  1=TMS  (always write as 1)
 bit 13        1:      0=reserved,  1=TD0  (always write as 1)
 bit 12        1:      0=reserved,  1=TDI  (always write as 1)
 bit 11        1:      0=reserved,  1=TCK  (always write as 1)
 bit 10        1:      0=reserved,  1=EMU1 (always write as 1)
 bit 9         1:      0=reserved,  1=EMU0 (always write as 1)
 bit 8         0:      0=IOPD0,     1=XINT2/ADCSOC
 bit 7         0:      0=IOPC7,     1=CANRX
 bit 6         0:      0=IOPC6,     1=CANTX
 bit 5         0:      0=IOPC5,     1=SPISTE
 bit 4         0:      0=IOPC4,     1=SPICLK
 bit 3         0:      0=IOPC3,     1=SPISOMI
 bit 2         0:      0=IOPC2,     1=SPISIMO
 bit 1         0:      0=IOPC1,     1=BIO*
 bit 0         0:      0=IOPC0,     1=W/R*
*/

 *MCRC = 0x0001;                    /* group C pins */
/*
 bit 15        0:      reserved
 bit 14        0:      0=IOPF6,     1=IOPF6
 bit 13        0:      0=IOPF5,     1=TCLKINB
 bit 12        0:      0=IOPF4,     1=TDIRB
 bit 11        0:      0=IOPF3,     1=T4PWM/T4CMP
 bit 10        0:      0=IOPF2,     1=T3PWM/T3CMP
 bit 9         0:      0=IOPF1,     1=CAP6
 bit 8         0:      0=IOPF0,     1=CAP5/QEP4
 bit 7         0:      0=IOPE7,     1=CAP4/QEP3
 bit 6         0:      0=IOPE6,     1=PWM12
 bit 5         0:      0=IOPE5,     1=PWM11
 bit 4         0:      0=IOPE4,     1=PWM10
 bit 3         0:      0=IOPE3,     1=PWM9
 bit 2         0:      0=IOPE2,     1=PWM8
 bit 1         0:      0=IOPE1,     1=PWM7
 bit 0         1:      0=IOPE0,     1=CLKOUT
*/


/*** Configure IOPC0 pin as an output ***/

 *PADATDIR = 0x0000;
/*
 bit 15        0:      IOPA7DIR 0=IN, 1=OUT
 bit 14        0:      IOPA6DIR 0=IN, 1=OUT
 bit 13        0:      IOPA5DIR 0=IN, 1=OUT
 bit 12        0:      IOPA4DIR 0=IN, 1=OUT
 bit 11        0:      IOPA3DIR 0=IN, 1=OUT
 bit 10        0:      IOPA2DIR 0=IN, 1=OUT
 bit 9         0:      IOPA1DIR 0=IN, 1=OUT
 bit 8         0:      IOPA0DIR 0=IN, 1=OUT
*/

 *PBDATDIR = 0x8800;
/*
 bit 15        1:      IOPB7DIR 0=IN, 1=OUT
 bit 14        0:      IOPB6DIR 0=IN, 1=OUT
 bit 13        0:      IOPB5DIR 0=IN, 1=OUT
 bit 12        0:      IOPB4DIR 0=IN, 1=OUT
 bit 11        0:      IOPB3DIR 0=IN, 1=OUT
 bit 10        0:      IOPB2DIR 0=IN, 1=OUT
 bit 9         0:      IOPB1DIR 0=IN, 1=OUT
 bit 8         0:      IOPB0DIR 0=IN, 1=OUT
*/

 *PCDATDIR = 0x1D00;
/*
 bit 15        0:      IOPC7DIR 0=IN, 1=OUT
 bit 14        0:      IOPC6DIR 0=IN, 1=OUT
 bit 13        0:      IOPC5DIR 0=IN, 1=OUT
 bit 12        1:      IOPC4DIR 0=IN, 1=OUT
 bit 11        1:      IOPC3DIR 0=IN, 1=OUT
 bit 10        1:      IOPC2DIR 0=IN, 1=OUT
 bit 9         0:      IOPC1DIR 0=IN, 1=OUT
 bit 8         1:      IOPC0DIR 0=IN, 1=OUT
```

```
*/

 *PDDATDIR = 0x0100;
/*
 bit 15        0:      IOPD7DIR 0=IN, 1=OUT
 bit 14        0:      IOPD6DIR 0=IN, 1=OUT
 bit 13        0:      IOPD5DIR 0=IN, 1=OUT
 bit 12        0:      IOPD4DIR 0=IN, 1=OUT
 bit 11        0:      IOPD3DIR 0=IN, 1=OUT
 bit 10        0:      IOPD2DIR 0=IN, 1=OUT
 bit 9         0:      IOPD1DIR 0=IN, 1=OUT
 bit 8         1:      IOPD0DIR 0=IN, 1=OUT
*/

 *PEDATDIR =   0;
/*
 bit 15        0:      IOPE7DIR 0=IN, 1=OUT
 bit 14        0:      IOPE6DIR 0=IN, 1=OUT
 bit 13        0:      IOPE5DIR 0=IN, 1=OUT
 bit 12        0:      IOPE4DIR 0=IN, 1=OUT
 bit 11        0:      IOPE3DIR 0=IN, 1=OUT
 bit 10        0:      IOPE2DIR 0=IN, 1=OUT
 bit 9         0:      IOPE1DIR 0=IN, 1=OUT
 bit 8         0:      IOPE0DIR 0=IN, 1=OUT
*/

 *PFDATDIR =   0;
/*
 bit 15        Reserved
 bit 14        0:      IOPB6DIR 0=IN, 1=OUT
 bit 13        0:      IOPB5DIR 0=IN, 1=OUT
 bit 12        0:      IOPB4DIR 0=IN, 1=OUT
 bit 11        0:      IOPB3DIR 0=IN, 1=OUT
 bit 10        0:      IOPB2DIR 0=IN, 1=OUT
 bit 9         0:      IOPB1DIR 0=IN, 1=OUT
 bit 8         0:      IOPB0DIR 0=IN, 1=OUT
*/
}

/* End of DIO24XX.h */
```

15.4.4 Event Manager A Intitialization

```
/*********************************************************/
/*
  Name                : EVA24XX.h
  Descrption   : Header file for Event Manager A
  Author              : AN Schutte
  Date                : 2008-11-01
  Revision            : 2
*/
/*********************************************************/

/* Timers */
#define GPTCONA      (volatile unsigned int *)0x7400   /* GP timer control reg A */

#define T1CNT        (volatile unsigned int *)0x7401   /* GP timer 1 counter reg */
#define T1CMPR       (volatile unsigned int *)0x7402   /* GP timer 1 compare reg */
#define T1PR         (volatile unsigned int *)0x7403   /* GP timer 1 period reg  */
#define T1CON        (volatile unsigned int *)0x7404   /* GP timer 1 control reg */

#define T2CNT        (volatile unsigned int *)0x7405   /* GP timer 2 counter reg */
#define T2CMPR       (volatile unsigned int *)0x7406   /* GP timer 2 compare reg */
#define T2PR         (volatile unsigned int *)0x7407   /* GP timer 2 period reg */
#define T2CON        (volatile unsigned int *)0x7408   /* GP timer 2 control reg */

/* Compare */
#define COMCONA      (volatile unsigned int *)0x7411   /* Compare control reg A */
#define ACTRA        (volatile unsigned int *)0x7413   /* Compare action control reg A
*/
#define DBTCONA      (volatile unsigned int *)0x7415   /* Dead-band timer control reg
A */
#define CMPR1        (volatile unsigned int *)0x7417   /* compare reg 1 */
#define CMPR2        (volatile unsigned int *)0x7418   /* compare reg 2 */
#define CMPR3        (volatile unsigned int *)0x7419   /* compare reg 3 */


/* Capture / QEP */
#define CAPCONA      (volatile unsigned int *)0x7420   /* Capture control reg A */
#define CAPFIFOA     (volatile unsigned int *)0x7422   /* Capture FIFO status reg A */
#define CAP1FIFO     (volatile unsigned int *)0x7423   /* Capture Channel 1 FIFO top
*/
#define CAP2FIFO     (volatile unsigned int *)0x7424   /* Capture Channel 2 FIFO top
*/
#define CAP3FIFO     (volatile unsigned int *)0x7425   /* Capture Channel 3 FIFO top
*/
#define CAP1FBOT     (volatile unsigned int *)0x7427   /* Bottom reg of capture FIFO
stack 1 */
#define CAP2FBOT     (volatile unsigned int *)0x7428   /* Bottom reg of capture FIFO
stack 2 */
#define CAP3FBOT     (volatile unsigned int *)0x7429   /* Bottom reg of capture FIFO
stack 3 */


/* Interrupts */
#define EVAIMRA      (volatile unsigned int *)0x742C   /* EVA interrupt mask reg A */
#define EVAIMRB      (volatile unsigned int *)0x742D   /* EVA interrupt mask reg B */
#define EVAIMRC      (volatile unsigned int *)0x742E   /* EVA interrupt mask reg C */
#define EVAIFRA      (volatile unsigned int *)0x742F   /* EVA interrupt flag reg A */
#define EVAIFRB      (volatile unsigned int *)0x7430   /* EVA interrupt flag reg B */
#define EVAIFRC      (volatile unsigned int *)0x7431   /* EVA interrupt flag reg C */

/* Individual Bits */
#define T1PWM 0x1000
#define T2PWM 0x2000

/* Initialisation Function(s) */
void init_GPTA(void);
void init_GPT1(void);
void init_GPT2(void);
void init_COMCONA(void);
void init_ACTRA(void);
void init_DBTCONA(void);
void init_EVA_INT(void);

/* #define T1PINT_FLAG 0x0080 */
```

```
/* End of eva.h */



/*********************************************************/
/*
  Name                : EVA24XX.c
  Descrption   : Subroutines to initialise the peripherals of EVA
  Author              : AN Schutte
  Date                : 2008-11-01
  Revision            : 1
*/
/*********************************************************/

#include "EVA24XX.h"

void init_Timers(void)
{

/*** Setup timers 1 and 2, and the PWM configuration ***/
 *T1CON = 0x0000;                    /* disable timer 1 */
 *T2CON = 0x0000;                    /* disable timer 2 */

 *GPTCONA = 0x0140;                  /* configure GPTCONA */
/*
 bit 15        0:      reserved
 bit 14        0:      T2STAT, read-only
 bit 13        0:      T1STAT, read-only
 bit 12-11     00:     reserved
 bit 10-9      00:     T2TOADC, 00 = no timer2 event starts ADC
 bit 8-7       10:     T1TOADC, 10 = start ADC with T1 at period
 bit 6         1:      TCOMPOE, 1 = Enable compare outputs
 bit 5-4       00:     reserved
 bit 3-2       00:     T2PIN, 00 = forced low XXXX
 bit 1-0       00:     T1PIN, 00 = forced low XXXX
*/

/* Timer 1: Generate PWM waveform for Q1-Q4, M1, M2 */
/* Symmetric PWM, 30KHz carrier frequency */
 *T1CNT = 0x0000;                    /* clear timer counter */
 *T1PR = 666;                              /* set timer period */
 *DBTCONA = 0x0000;                  /* deadband units off */
 *CMPR1 = 0;                                /* set intital PWM1 duty cycle */
 *CMPR2 = 0;                                /* set intital PWM1 duty cycle */
 *CMPR3 = 0;                                /* set intital PWM1 duty cycle */

 *ACTRA = 0x0000;                    /* All PWM pins forced low */
/*
 bit 15        0:      space vector dir is CCW (don't care)
 bit 14-12     000:    basic space vector is 000 (dont' care)
 bit 11-10     00:     PWM6/IOPB3 pin forced low
 bit 9-8       00:     PWM5/IOPB2 pin forced low
 bit 7-6       00:     PWM4/IOPB1 pin forced low
 bit 5-4       00:     PWM3/IOPB0 pin forced low
 bit 3-2       00:     PWM2/IOPA7 pin forced low
 bit 1-0       00:     PWM1/IOPA6 pin forced low
*/

 *COMCONA = 0xCA00;                          /* configure COMCON register */
/*
 bit 15        1:      1 = enable compare operation
 bit 14-13     10:     10 = reload CMPRx immediately
 bit 12        0:      0 = space vector disabled
 bit 11-10     10:     10 = reload ACTR immediately
 bit 9         1:      1 = enable PWM pins
 bit 8-0       0's:    reserved
*/

/* Timer 2: Generate PWM waveform for M3 */
/* Symmetric PWM, 60KHz carrier frequency, sunchronize with T1 */
 *T2CNT = 0x0000;                     /* clear timer counter */
 *T2PR = 333;                               /* set timer period */

 *T2CON = 0x88CA;                    /* configure T2CON register */
/*
```

```
 bit 15-14     10:     operation not affected by emulator suspend
 bit 13        0:      reserved
 bit 12-11     01:     10 = continous-up count mode
 bit 10-8      000:    000 = x/1 prescaler
 bit 7         1:      T2SWT1, 2 = start with T1 TENABLE bit
 bit 6         1:      TENABLE, 1 = enable timer (not used)
 bit 5-4       00:     00 = CPUCLK is clock source
 bit 3-2       10:     10 = reload compare reg immediately
 bit 1         1:      1 = enable timer compare
 bit 0         0:      SELT1PR, 0 = use own period register
*/

/* Timer 2 is also started with Timer 1's enable bit */
 *T1CON = 0x884A;                  /* configure T1CON register */
/*
 bit 15-14     10:     operation not affected by emulator suspend
 bit 13        0:      reserved
 bit 12-11     01:     01 = continous-up/down count mode
 bit 10-8      000:    000 = x/1 prescaler
 bit 7         0:      reserved in T1CON
 bit 6         1:      TENABLE, 1 = enable timer
 bit 5-4       00:     00 = CPUCLK is clock source
 bit 3-2       10:     10 = reload compare reg immediately
 bit 1         1:      1 = enable timer compare
 bit 0         0:      reserved in T1CON
*/

}


/* Initialise Interrupt Masking Registers */

void init_EVA_INT(void)
{
 /*** Setup the event manager interrupts ***/
 *EVAIFRA = 0xFFFF;                  /* clear all EVA group A interrupts */
 *EVAIFRB = 0xFFFF;                  /* clear all EVA group B interrupts */
 *EVAIFRC = 0xFFFF;                  /* clear all EVA group C interrupts */
 *EVAIMRA = 0x0080;                  /* enable desired EVA group A interrupts */
 *EVAIMRB = 0x0000;                  /* enable desired EVA group B interrupts */
 *EVAIMRC = 0x0000;                  /* enable desired EVA group C interrupts */
}
```

15.4.5 System Initialization

```
/*********************************************************/
/*
  Name                : SYS24XX.h
  Descrption   : Header file for hardware initialisation
  Author              : AN Schutte
  Date                : 2008-11-01
  Revision            : 1
*/
/*********************************************************/

/* Core registers */
#define IMR          (volatile unsigned int *)0x0004   /* Interrupt mask reg */
#define GREG         (volatile unsigned int *)0x0005   /* Global memory allocation reg
*/
#define IFR          (volatile unsigned int *)0x0006   /* Interrupt flag reg */

/* System configuration and interrupt registers */
#define PIRQR0       (volatile unsigned int *)0x7010   /* Peripheral interrupt request
reg 0 */
#define PIRQR1       (volatile unsigned int *)0x7011   /* Peripheral interrupt request
reg 1 */
#define PIRQR2       (volatile unsigned int *)0x7012   /* Peripheral interrupt request
reg 2 */
#define PIACKR0      (volatile unsigned int *)0x7014   /* Peripheral interrupt
acknowledge reg 0 */
#define PIACKR1      (volatile unsigned int *)0x7015   /* Peripheral interrupt
acknowledge reg 1 */
#define PIACKR2      (volatile unsigned int *)0x7016   /* Peripheral interrupt
acknowledge reg 2 */
#define SCSR1        (volatile unsigned int *)0x7018   /* System control & status reg
1 */
#define SCSR2        (volatile unsigned int *)0x7019   /* System control & status reg
2 */
#define DINR         (volatile unsigned int *)0x701C   /* Device identification reg */
#define PIVR         (volatile unsigned int *)0x701E   /* Peripheral interrupt vector
reg */

/* Watchdog timer (WD) registers */
#define WDCNTR       (volatile unsigned int *)0x7023   /* WD counter reg */
#define WDKEY        (volatile unsigned int *)0x7025   /* WD reset key reg */
#define WDCR         (volatile unsigned int *)0x7029   /* WD timer control reg */

/* I/O space mapped registers */
#define FCMR portFF0F                                  /* Flash control mode register
*/
ioport unsigned int portFF0F;                          /* C2xx compiler specific
keyword */
#define WSGR portFFFF                                  /* Wait-state generator reg */
ioport unsigned int portFFFF;                          /* C2xx compiler specific
keyword */

/* Module Enable Bits in SCSR1 */
#define ADC_CLKEN    0x0080
#define SCI_CLKEN    0x0040
#define SPI_CLKEN    0x0020
#define CAN_CLKEN    0x0010
#define EVB_CLKEN    0x0008
#define EVA_CLKEN    0x0004

/* Wait State Bits */
#define PSWSB0 0x0001
#define PSWSB1 0x0002
#define PSWSB2 0x0004
#define DSWSB0 0x0008
#define DSWSB1 0x0010
#define DSWSB2 0x0020
#define IOWSB0 0x0048
#define IOWSB1 0x0080
#define IOWSB2 0x0100

void init_SYS(void);
void init_SYS_INT(void);
```

```
/* End of SYS24XX.h */


/*********************************************************/
/*
  Name                : SYS24XX.c
  Descrption   : Functions for set-up of phase locked loop and to enable features
  Author              : AN Schutte
  Date                : 2008-11-01
  Revision            : 1
*/
/*********************************************************/
/* Derived from code supplied by Spectrum Digital */

#include "SYS24XX.h"

void init_SYS()
{
/*** Configure the System Control and Status registers ***/
    *SCSR1 = 0x00FD;
/*
 bit 15        0:      reserved
 bit 14        0:      CLKOUT = CPUCLK
 bit 13-12     00:     IDLE1 selected for low-power mode
 bit 11-9      000:    PLL x4 mode
 bit 8         0:      reserved
 bit 7         1:      1 = enable ADC module clock
 bit 6         1:      1 = enable SCI module clock
 bit 5         1:      1 = enable SPI module clock
 bit 4         1:      1 = enable CAN module clock
 bit 3         1:      1 = enable EVB module clock
 bit 2         1:      1 = enable EVA module clock
 bit 1         0:      reserved
 bit 0         1:      clear the ILLADR bit
*/

    *SCSR2 = (*SCSR2 | 0x000B) & 0x000F;
/*
 bit 15-6      0's:    reserved
 bit 5         0:      do NOT clear the WD OVERRIDE bit
 bit 4         0:      XMIF_HI-Z, Zero on all but '2407. 0=normal mode, 1=Hi-Z'd
 bit 3         1:      disable the boot ROM, enable the FLASH
 bit 2     no change   MP/MC* bit reflects state of MP/MC* pin
 bit 1-0      11:      11 = SARAM mapped to prog and data
*/

/*** Disable the watchdog timer ***/
    *WDCR  = 0x00E8;
/*
 bits 15-8     0's:     reserved
 bit 7         1:       clear WD flag
 bit 6         1:       disable the dog
 bit 5-3       101:     must be written as 101
 bit 2-0       000:     WDCLK divider = 1
*/

/*** Setup external memory interface for LF2407 EVM ***/
    WSGR = 0x0040;
/*
 bit 15-11     0's:    reserved
 bit 10-9      00:     bus visibility off
 bit 8-6       001:    1 wait-state for I/O space
 bit 5-3       000:    0 wait-state for data space
 bit 2-0       000:    0 wait state for program space
*/
}

void init_SYS_INT()
{
/*** Setup the core interrupts ***/
    *IMR = 0x0000;                      /* clear the IMR register */
    *IFR = 0x003F;                      /* clear any pending core interrupts */
    *IMR = 0x0002;                      /* enable desired core interrupts */
}
/* End of SYS24XX.c */
```

15.4.6 Analogue to Digital Converter Initialization

```
/*********************************************************/
/*
  Name                : ADC24XX.h
  Descrption   : Header file for analog-to-digital conversion
  Author              : AN Schutte
  Date                : 2008-11-01
  Revision            : 2
*/
/*********************************************************/

#define ADCCTRL1      *(volatile unsigned int *) 0x70A0
#define ADCCTRL2      *(volatile unsigned int *) 0x70A1
#define MAX_CONV      *(volatile unsigned int *) 0x70A2
#define CHSELSEQ1     *(volatile unsigned int *) 0x70A3
#define CHSELSEQ2     *(volatile unsigned int *) 0x70A4
#define CHSELSEQ3     *(volatile unsigned int *) 0x70A5
#define CHSELSEQ4     *(volatile unsigned int *) 0x70A6
#define AUTO_SEQ_SR   *(volatile unsigned int *) 0x70A7

#define RESULT0       *(volatile unsigned int *) 0x70A8
#define RESULT1       *(volatile unsigned int *) 0x70A9
#define RESULT2       *(volatile unsigned int *) 0x70AA
#define RESULT3       *(volatile unsigned int *) 0x70AB
#define RESULT4       *(volatile unsigned int *) 0x70AC
#define RESULT5       *(volatile unsigned int *) 0x70AD
#define RESULT6       *(volatile unsigned int *) 0x70AE
#define RESULT7       *(volatile unsigned int *) 0x70AF
#define RESULT8       *(volatile unsigned int *) 0x70B0
#define RESULT9       *(volatile unsigned int *) 0x70B1
#define RESULT10      *(volatile unsigned int *) 0x70B2
#define RESULT11      *(volatile unsigned int *) 0x70B3
#define RESULT12      *(volatile unsigned int *) 0x70B4
#define RESULT13      *(volatile unsigned int *) 0x70B5
#define RESULT14      *(volatile unsigned int *) 0x70B6
#define RESULT15      *(volatile unsigned int *) 0x70B7

#define CALIBRATION   *(volatile unsigned int *)0x70B8

/* Individual bits of ADCCTRL1 */
#define  ADC_RESVD          0x8000
#define  ADC_RESET          0x4000
#define  ADC_SOFT              0x2000
#define  ADC_FREE              0x1000
#define  ADC_ACQ_PS3    0x0800
#define  ADC_ACQ_PS2    0x0400
#define  ADC_ACQ_PS1    0x0200
#define  ADC_ACQ_PS0    0x0100
#define  ADC_CPS           0x0080
#define  ADC_CONT_RUN   0x0040
#define  ADC_INT_PRI    0x0020
#define  ADC_SEQ_CASC   0x0010
#define  ADC_CAL_ENA    0x0008
#define  ADC_BRG_ENA    0x0004
#define  ADC_HI_LO             0x0002
#define  ADC_FTEST_ENA  0x0001

/* Individual bits of ADCTRL2 */
#define RST_SEQ1            0x4000
#define STRT_CAL               0x4000
#define SOC_SEQ1            0x2000
#define SEQ1_BSY            0x1000
#define INT_FLAG_SEQ1     0x0200
#define EVA_SOC_SEQ1      0x0100

#define ADC_SIZE    16

/* Initialisation Function(s) */
void init_ADC(void);

/* End of ADC24XX.h */
```

```
/*********************************************************/
/*
  Name                : ADC24XX.c
  Descrption   : Subroutines to initialise the ADC
  Author              : AN Schutte
  Date                : 2007-02-26
  Revision            : 0
*/
/*********************************************************/

#include "ADC24XX.h"

void init_ADC(void)
{
  /* Non Cascade for 4 measurements. */
  /* Will affect RESULT0 to RESULT3 only */

  ADCCTRL1 = 0x0000;   /*Reset Regsiters */
  ADCCTRL2 = 0x0000;

  ADCCTRL1 = (ADC_SOFT);

  CHSELSEQ1 = 0x3210; /* 4 measurements on Channels 0 - 5 */
  CHSELSEQ2 = 0xFFFF;
  CHSELSEQ3 = 0xFFFF;
  CHSELSEQ4 = 0xFFFF;
  MAX_CONV  = 0x0003; /* 8 measurements */

  /* Reset sequence at zero and EVA to start conversion */

  ADCCTRL2 = (RST_SEQ1 | EVA_SOC_SEQ1);
}
```

15.5 Appendix B.5: Simplorer VHDL Code Listing

```
---------- VHDLAMS MODEL DSP ----------
LIBRARY ieee;
LIBRARY std;
USE        std.ALL;
USE        ieee.ALL;
USE ieee.math_real;

---------- ENTITY DECLARATION DSP ----------
ENTITY   DSP IS
            PORT(
                        clk                                                                 : IN        BIT;
                        QUANTITY Q14, Q23, M1A, M1B, M2A, M2B, M3A, M3B : OUT        REAL;
                        QUANTITY Iact_Sig, Vin_Sig, Vout_Sig, Vmain_Sig  : IN        REAL;
                        QUANTITY Test1, Test2, Test3, Test4                  : OUT  REAL
              );
END ENTITY DSP;


-- ARCHITECTURE DECLARATION arch_DSP ----------
ARCHITECTURE arch_DSP OF DSP IS
            TYPE PWM_MODE IS (AH, AL, FH, FL);
            TYPE PWM_MODE_REG IS ARRAY (0 TO 7) OF PWM_MODE;
            TYPE PWM_CMP_REG IS ARRAY (0 TO 7) OF INTEGER;
            TYPE CONT_ARR IS ARRAY (0 TO 2) OF INTEGER;

            SIGNAL PWM_OUT                                  : REAL_VECTOR (0 TO 7);
            SIGNAL Test_Sig1, Test_Sig2          : INTEGER;
            SIGNAL Test_Sig3, Test_Sig4          : INTEGER;

FUNCTION calc_iref(MEAS_V: IN INTEGER) RETURN INTEGER IS
BEGIN
            IF (MEAS_V >= 3780) THEN RETURN 0;                                          --Battery
Voltage > 56.8V. I = 0
            END IF;
            IF ((MEAS_V >= 3594) AND (MEAS_V < 3780)) THEN RETURN 333;      --Battery  Voltage  >  54V.  I
= 0.5
            END IF;
            IF ((MEAS_V >= 3461) AND (MEAS_V < 3594)) THEN RETURN 2000;     --Battery  Voltage  >  52V.  I
= 3
            END IF;
            IF ((MEAS_V >= 3195) AND (MEAS_V < 3461)) THEN RETURN 6656;     --Battery  Voltage  >  48V.  I
= 10
            END IF;
            IF ((MEAS_V >= 2662) AND (MEAS_V < 3195)) THEN RETURN 9984;     --Battery  Voltage  >  40V.  I
= 15
            END IF;
            IF (MEAS_V < 2662) THEN RETURN 665;                                         --Battery
Voltage < 40V. I = 1
END IF;
END FUNCTION;

FUNCTION calc_vref_AC(AMPL,CNTR,PER: IN INTEGER) RETURN INTEGER IS
BEGIN
            IF PER = 0 THEN
                        RETURN AMPL;
            ELSE
                        RETURN   INTEGER(REAL(AMPL)*SIN(REAL(CNTR)*6.283185/real(PER)));  --Calculate
Sine Wave Reference.
            END IF;
END FUNCTION;

FUNCTION calc_iref_AC(REF,MEAS,REF_PREV,MEAS_PREV,CMD_PREV,MAX_I: IN INTEGER) RETURN
INTEGER IS
   VARIABLE CUR : LONG INTEGER;                                          --Temporary Current Command Value
BEGIN

            -- Goed .5mH 3.2uC CUR := INTEGER(2.0*REAL((REF - MEAS))) -
INTEGER(1.8008*REAL(REF_PREV - MEAS_PREV)) + INTEGER(0.9000*REAL(CMD_PREV));
            --Perfek 3.5mH 10-20uC CUR := INTEGER(5.0*REAL((REF - MEAS))) -
INTEGER(4.0*REAL(REF_PREV - MEAS_PREV)) + INTEGER(0.8000*REAL(CMD_PREV));
            --Te vinnig CUR := INTEGER(0.3501*REAL((REF - MEAS))) - INTEGER(0.08513*REAL(REF_PREV
- MEAS_PREV)) + INTEGER(0.9981*REAL(CMD_PREV));
```

```
		--Te Stadig CUR := INTEGER(0.08309*REAL((REF - MEAS))) - INTEGER(0.04966*REAL(REF_PREV - MEAS_PREV)) + INTEGER(0.9996*REAL(CMD_PREV));
		CUR := INTEGER(0.1246*REAL((REF - MEAS))) - INTEGER(0.0745*REAL(REF_PREV - MEAS_PREV)) + INTEGER(0.9993*REAL(CMD_PREV));


		IF CUR > MAX_I THEN --Cap current command value between +Max_I and -Max_I.
			CUR := MAX_I;
		ELSIF CUR < -MAX_I THEN
			CUR := -MAX_I;
		END IF;
		RETURN CUR;
END FUNCTION;

FUNCTION calc_DC_AC(REF,MEAS,REF_PREV,MEAS_PREV,CMD_PREV,MAX_D: IN INTEGER) RETURN INTEGER IS
  VARIABLE DC, ERROR, ERROR_PREV : INTEGER; --Temporary Duty Cycle and Error Values
BEGIN
		IF REF >= 0 THEN --If reference is positive
			ERROR := REF - MEAS; --Error is not inverted
		ELSE
			ERROR := MEAS - REF; --Error is inverted
		END IF;
		IF REF_PREV >= 0 THEN --If previous reference is positive
			ERROR_PREV := REF_PREV - MEAS_PREV; --Previous error is not inverted
		ELSE
			ERROR_PREV := MEAS_PREV - REF_PREV; --Error is inverted
		END IF;

		--Werk goed 3.5uH, 3.2uC DC := (ERROR)/10 - INTEGER(0.08364*REAL(ERROR_PREV)) + INTEGER(0.9836*REAL(CMD_PREV));
		DC := (ERROR)/10 - INTEGER(0.08513*REAL(ERROR_PREV)) + INTEGER(0.9851*REAL(CMD_PREV));

		IF DC < 0 THEN --Only positive duty cycles allowed, mode bits will take care of direction
			DC := 0; --  -DC;
		END IF;
		IF DC > MAX_D THEN --Cap control value to maximum duty cycle.
			DC := MAX_D;
		END IF;
		RETURN DC;
END FUNCTION;

PROCEDURE set_mode(dir, pol: IN BOOLEAN; dc, max_dc: IN INTEGER; modes: OUT PWM_MODE_REG; comps: OUT PWM_CMP_REG) IS
BEGIN
--Q13, Q24, M1A, M1B, M2A, M2B, M3A, M3B
		: OUT	STD_LOGIC;
		IF (dir AND pol) THEN --Forward, Positive
			modes(0) := AH;
			modes(1) := AL;
			modes(2) := FH;
			modes(3) := FL;
			modes(4) := FH;
			modes(5) := FL;
			modes(6) := FH;
			modes(7) := FL;

			comps(0) := max_dc - dc;
			comps(1) := dc;
		END IF;
--Q13, Q24, M1A, M1B, M2A, M2B, M3A, M3B
		: OUT	STD_LOGIC;
		IF (dir AND NOT(pol)) THEN --Forward, Negative
			modes(0) := AH;
			modes(1) := AL;
			modes(2) := FL;
			modes(3) := FH;
			modes(4) := FL;
			modes(5) := FH;
			modes(6) := FL;
			modes(7) := FH;
```

```
                comps(0) := max_dc - dc;
                comps(1) := dc;
        END IF;
                                                --Q13, Q24, M1A, M1B, M2A, M2B, M3A, M3B
        : OUT   STD_LOGIC;
        IF (NOT(dir) AND pol) THEN              --Reverse, Positive
                modes(0) := FL;
                modes(1) := FL;
                modes(2) := FL;
                modes(3) := AH;
                modes(4) := FL;
                modes(5) := AL;
                modes(6) := FL;
                modes(7) := AH;

                comps(3) := max_dc/2;
                comps(5) := max_dc/2;
                comps(7) := max_dc/2 - dc;
        END IF;
                                                --Q13, Q24, M1A, M1B, M2A, M2B, M3A, M3B
        : OUT   STD_LOGIC;
        IF (NOT(dir) AND NOT(pol)) THEN         --Reverse, Negative
                modes(0) := FL;
                modes(1) := FL;
                modes(2) := AH;
                modes(3) := FL;
                modes(4) := AL;
                modes(5) := FL;
                modes(6) := AH;
                modes(7) := FL;

                comps(2) := max_dc/2;
                comps(4) := max_dc/2;
                comps(6) := max_dc/2 - dc;
        END IF;
END PROCEDURE;

BEGIN
        PROCESS (clk) IS
                VARIABLE PWM1_CNTR, PWM1_PER   : INTEGER := 0;       --PWM    Counter    register
and period
                VARIABLE PWM2_CNTR, PWM2_PER   : INTEGER := 0;       --PWM    Counter    register
and period
                VARIABLE  PWM1_DIR,  PWM2_DIR,  ADC_INT:  STD_LOGIC  :=  '0';--PWM  Counter
Direction bit 1 = up, ADC Interrupt
                VARIABLE ADC_CNTR, ADC_PER                : INTEGER := 0;       --ADC    Counter
register and period
                VARIABLE IOUT, VBAT, VOUT, VMAIN          : INTEGER := 0;       --Measured    and
Scaled Parameters
                VARIABLE ICMD, VCMD, IBAT                 : INTEGER := 0;       --Command
Values
                VARIABLE VOUT_PREV, ICMD_PREV, VCMD_PREV          : INTEGER := 0;--Previous
Cycle Values
                VARIABLE IOUT_PREV, D_PREV                : INTEGER := 0;       --Previous Cycle
Values
                VARIABLE SIN_CNTR, SIN_PER                : INTEGER := 0;       --Sine         wave
reference counter and period. 250
                --VARIABLE SIN_AMPL, SIN_MAX_MEAS          : INTEGER := 0;       --Mains        input
sine wave parameters
                VARIABLE D                                : INTEGER := 0;       --Duty Cycle
                VARIABLE FWD, POS, MASK             : BOOLEAN;                  --Mode       status
bits
                VARIABLE FWD_PREV, POS_PREV               : BOOLEAN;                  --
Previous Cycle Values
                VARIABLE PWM_CNTRL                        : PWM_MODE_REG;             --
PWM Register
                VARIABLE PWM_CMP                          : PWM_CMP_REG;  --Compare
Register
                VARIABLE TEST_STATE                       : INTEGER := 0;       --Mode reporting
variable
        BEGIN
                IF clk'EVENT AND clk = '1' THEN
                        PWM1_PER := 666;
                        PWM2_PER := 333;
```

```
                        ADC_PER := 1;                                   --
Sample on every switching cycle
                        ADC_CNTR := ADC_PER - 1;                        --Sample on the
very first cycle
                        SIN_PER := 600;                                 --Sine period =
600/30kHz = 50Hz

                        --Implement PWM1 Timer, Continuously Up/Down Counting
                        IF PWM1_DIR = '1' THEN                          --Count Up
                                PWM1_CNTR := PWM1_CNTR + 1;
                        ELSIF PWM1_DIR = '0' THEN                       --Count Down
                                PWM1_CNTR := PWM1_CNTR - 1;
                        ELSE
                                PWM1_CNTR := 0;                         --Error, Reset
                        END IF;
                        IF (PWM1_CNTR <= 0) THEN                        --Lower     Limit
Reached
                                PWM1_CNTR := 0;
                                PWM1_DIR := '1';
                        END IF;
                        IF (PWM1_CNTR >= PWM1_PER) THEN                 --Upper     Limit
Reached
                                PWM1_CNTR := PWM1_PER;
                                PWM1_DIR := '0';
                        END IF;

                        --Implement PWM1 Timer, Continuously Up/Down Counting
                        IF PWM2_DIR = '1' THEN                          --Count Up
                                PWM2_CNTR := PWM2_CNTR + 1;
                        ELSIF PWM2_DIR = '0' THEN                       --Count Down
                                PWM2_CNTR := PWM2_CNTR - 1;
                        ELSE
                                PWM2_CNTR := 0;                         --Error, Reset
                        END IF;
                        IF (PWM2_CNTR <= 0) THEN                        --Lower     Limit
Reached
                                PWM2_CNTR := 0;
                                PWM2_DIR := '1';
                        END IF;
                        IF (PWM2_CNTR >= PWM2_PER) THEN                 --Upper     Limit
Reached
                                PWM2_CNTR := PWM2_PER;
                                PWM2_DIR := '0';
                        END IF;

                        --Implement ADC Timer, Continuously Up Counting
                        ADC_INT := '0';                                 --Reset Interrupt
                        IF PWM1_CNTR = PWM1_PER THEN                    --Count Up
                                ADC_CNTR := ADC_CNTR + 1;
                        END IF;
                        --IF PWM1_CNTR = 0 THEN                         --Count Up
                        --      ADC_CNTR := ADC_CNTR + 1;
                        --END IF;
                        IF (ADC_CNTR >= ADC_PER) THEN                   --Upper     Limit
Reached
                                ADC_CNTR := 0;
                                ADC_INT := '1';                         --Set Interrupt
                        END IF;

                        --Implement Sine Reference Timer, Continuously Up Counting
                        IF PWM1_CNTR = PWM1_PER THEN                    --
Count Up
                                SIN_CNTR := SIN_CNTR + 1;
                        END IF;
                        IF (SIN_CNTR >= SIN_PER) THEN                   --
Upper Limit Reached
                                SIN_CNTR := 0;
                        --      SIN_AMPL := SIN_MAX_MEAS;
                        --      SIN_MAX_MEAS := 0;
                        END IF;

                        --Generate PWM signals
                        PWM1_LOOP: FOR INDEX IN 0 TO 5 LOOP
```

```
                                    IF ((PWM_CNTRL(INDEX) = FH) OR ((PWM1_CNTR >=
PWM_CMP(INDEX)) AND (PWM_CNTRL(INDEX) = AH)) OR ((PWM1_CNTR < PWM_CMP(INDEX)) AND
(PWM_CNTRL(INDEX) = AL))) THEN
                                        PWM_OUT(INDEX) <= 10.0;
                                    ELSIF ((PWM_CNTRL(INDEX) = FL) OR ((PWM1_CNTR <
PWM_CMP(INDEX)) AND (PWM_CNTRL(INDEX) = AH)) OR ((PWM1_CNTR >= PWM_CMP(INDEX)) AND
(PWM_CNTRL(INDEX) = AL))) THEN
                                        PWM_OUT(INDEX) <= 0.0;
                                    END IF;
                                END LOOP PWM1_LOOP;

                                PWM2_LOOP: FOR INDEX IN 6 TO 7 LOOP
                                    IF ((PWM_CNTRL(INDEX) = FH) OR ((PWM2_CNTR >=
PWM_CMP(INDEX)) AND (PWM_CNTRL(INDEX) = AH)) OR ((PWM2_CNTR < PWM_CMP(INDEX)) AND
(PWM_CNTRL(INDEX) = AL))) THEN
                                        PWM_OUT(INDEX) <= 10.0;
                                    ELSIF ((PWM_CNTRL(INDEX) = FL) OR ((PWM2_CNTR <
PWM_CMP(INDEX)) AND (PWM_CNTRL(INDEX) = AH)) OR ((PWM2_CNTR >= PWM_CMP(INDEX)) AND
(PWM_CNTRL(INDEX) = AL))) THEN
                                        PWM_OUT(INDEX) <= 0.0;
                                    END IF;
                                END LOOP PWM2_LOOP;

                                --Test Signals
                                Test_Sig1 <= VCMD;
                                Test_Sig2 <= ICMD;
                                Test_Sig3 <= D;
                                Test_Sig4 <= TEST_STATE;

                                --Main Program
                                IF ADC_INT = '1' THEN                                   --
Only performed every time the ADC has finished
                                    --Store Previous Cycle Values
                                    VCMD_PREV := VCMD;
                                    VOUT_PREV := VOUT;
                                    ICMD_PREV := ICMD;
                                    IOUT_PREV := IOUT;
                                    D_PREV := D;
                                    FWD_PREV := FWD;
                                    POS_PREV := POS;

                                    --Measure and Calculate Values
                                    IOUT := INTEGER(Iact_Sig*(512.0/50.0)*65.0);        --50A   =   512
After ADC. Scaled by 65 to equal 33280.
                                    VBAT := INTEGER(Vin_Sig*(-512.0/100.0)*13.0);    --100V   =   512
After ADC. Scaled by 13 to equal 6656.
                                    VOUT := INTEGER(Vout_Sig*(512.0/500.0)*65.0);    --500V   =   512
After ADC. Scaled by 65 to equal 33280.
                                    VMAIN :=INTEGER(Vmain_Sig*(-512.0/500.0)*65.0);             --
500V = 512 After ADC. Scaled by 65 to equal 33280.

                                    IBAT := IOUT*9*VBAT/325;--VOUT;                         --
Compute steady state battery current
                                    --IF VMAIN > SIN_MAX_MEAS THEN                         --
Capture Mains Sine Wave Amplitude
                                    --          SIN_MAX_MEAS := VMAIN;
                                    --ELSIF -VMAIN > SIN_MAX_MEAS THEN
                                    --          SIN_MAX_MEAS := -VMAIN;
                                    --END IF;

                                    --FWD := TRUE;                                         --
Commissioning Values
                                    --POS := FALSE;                                        --
Commissioning Values
                                    --D := 167;
            --Commissioning Values

                                    --IF SIN_AMPL <= 19800 THEN
            --Is Mains Sine Wave OK?
                                        VCMD   :=   calc_vref_AC(21632,   SIN_CNTR,   SIN_PER);
            --No, Start Inverting
                                        ICMD                                            :=
calc_iref_AC(VCMD,VOUT,VCMD_PREV,VOUT_PREV,ICMD_PREV,8320);          --Max current =
8320 = 12.5A
```

```
                                        --ELSE
                        --Yes, Start Charging
                                        --          ICMD := VMAIN/SIN_AMPL*calc_iref(VBAT);
                --Power factor of 1 (constant ratio of mains voltage)
                                        --END IF;
                                        D                                                       :=
calc_DC_AC(ICMD,IOUT,ICMD_PREV,IOUT_PREV,D_PREV,PWM1_PER/2);            --Calculate Duty
Cycle

                                        --Force small inductor current to zero
                                        IF ((IOUT > -100) AND (IOUT < 100)) THEN
                --If inductor current is less than 150mA
                                                IOUT := 0;
                        --Force measured value to zero
                                        END IF;

                                        --Determine Mode of converter
                                        MASK := FALSE;
                                        IF ((VCMD >= 0) AND (IOUT >= 0) AND (ICMD >= 0)) THEN
                                                POS := TRUE;
                                                FWD := TRUE;
                                                TEST_STATE := 1;
                                        ELSIF ((VCMD >= 0) AND (IOUT > 0) AND (ICMD < 0)) THEN
                                                POS := TRUE;
                                                FWD := TRUE;
                                                MASK := TRUE; ---
                                                TEST_STATE := 2;
                                        ELSIF ((VCMD >= 0) AND (IOUT <= 0) AND (ICMD < 0)) THEN
                                                POS := TRUE;
                                                FWD := FALSE;
                                                TEST_STATE := 3;
                                        ELSIF ((VCMD >= 0) AND (IOUT < 0) AND (ICMD >= 0)) THEN
                                                POS := TRUE;
                                                FWD := FALSE;
                                                MASK := TRUE;
                                                TEST_STATE := 4;
                                        ELSIF ((VCMD < 0) AND (IOUT >= 0) AND (ICMD >= 0)) THEN
                                                POS := FALSE;
                                                FWD := FALSE;
                                                TEST_STATE := 5;
                                        ELSIF ((VCMD < 0) AND (IOUT > 0) AND (ICMD < 0)) THEN
                                                POS := FALSE;
                                                FWD := FALSE;
                                                MASK := TRUE;
                                                TEST_STATE := 6;
                                        ELSIF ((VCMD < 0) AND (IOUT <= 0) AND (ICMD <= 0)) THEN
                                                POS := FALSE;
                                                FWD := TRUE;
                                                TEST_STATE := 7;
                                        ELSIF ((VCMD < 0) AND (IOUT < 0) AND (ICMD >= 0)) THEN
                                                POS := FALSE;
                                                FWD := TRUE;
                                                MASK := TRUE; --
                                                TEST_STATE := 8;
                                        END IF;

                                        --Test for Mode Change
                                        IF (FWD XOR FWD_PREV) THEN
                        --If a mode change has occurred
                                                IF ((VCMD < 300) AND (VCMD > -300) AND (IOUT <
300) AND (IOUT > -300)) THEN
                                                        D := 0;
                --Reset duty cycle to 1 - D
                                                ELSE
                                                        D:= 333 - D;
                                                END IF;
                                        END IF;
                                        IF MASK THEN
                                                set_mode(FWD, POS, 0, PWM1_PER, PWM_CNTRL,
PWM_CMP);       --Update Action and Compare Registers
                                        ELSE
                                                set_mode(FWD, POS, D, PWM1_PER, PWM_CNTRL,
PWM_CMP);       --Update Action and Compare Registers
                                        END IF;
                                END IF;
```

```
                END IF;
        END PROCESS;
        --Output Signals
        Test1 == REAL(Test_Sig1);
        Test2 == REAL(Test_Sig2);
        Test3 == REAL(Test_Sig3);
        Test4 == REAL(Test_Sig4);
        Q14 == PWM_OUT(0);
        Q23 == PWM_OUT(1);
        M1A == PWM_OUT(2);
        M1B == PWM_OUT(3);
        M2A == PWM_OUT(4);
        M2B == PWM_OUT(5);
        M3A == PWM_OUT(6);
        M3B == PWM_OUT(7);
END ARCHITECTURE arch_DSP;
```