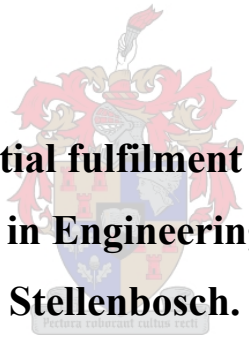
Bidirectional Converter for a Stirling Energy System

H. H. Redecker



Thesis presented in partial fulfilment of the requirements for the degree of Master in Engineering at the University of Stellenbosch.

Supervisor: Dr H. J. Beukes

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DECLARATION

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

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SUMMARY

This thesis discusses a 23 kW three-phase AC bus system that is utilized together with the "Stirling Energy System (SES) Integrated Solar Dish-Stirling Module" to function as a mini-grid for off-grid locations. The system is designed to supply power to 27 rural households. This three-phase AC bus system includes a bidirectional 4-wire PWM converter and a battery bank for energy storage. The simulations and results presented show that the system can function as a rectifier and as an inverter. The system operates as an inverter when the SES starts up and when different AC loads are connected to the AC bus. The unit functions as a rectifier when the battery bank is charged. The design was implemented successfully in a practical system and measurements revealed that the system functioned as a standalone unit.

OPSOMMING

Hierdie tesis bespreek ‘n 23 kW drie-fase vier-draad WS bus stelsel wat saam met die “Stirling Energy System (SES) Integrated Solar Dish-Stirling Module” gebruik word om as ‘n alleenstaande stelsel in ’n plattelandse omgewing te laat funksioneer. Die sisteem is ontwerp om vir 27 plattelandse huise drywing te lewer. Hierdie stelsel behels ‘n drie-fase GS na WS omsetter, saam met loodsuur batterye as energiestoor. Die simulasies en resultate wat gegee word, dui aan dat die omsetter as ‘n wisselrigter en ook as ‘n gelykrigter kan werk. Die stelsel funksioneer as ‘n wisselrigter as die SES aanskakel, en as ekstra laste op die WS bus gekoppel word. Die sisteem funksioneer as ‘n gelykrigter as die batterye gelaai word. Die ontwerp is suksesvol in ‘n praktiese stelsel geimplimenteer wat as ‘n alleenstaande stelsel funksioneer.

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LIST OF ABBREVIATIONS AND SYMBOLS

SES	Stirling Energy System
PV	Photovoltaic
NiCad	Nickel Cadmium
AGM	Absorbed Glass Mat
DOD	Depth of Discharge
SOC	State of Charge
PCU	Power Conversion Unit
IM	Induction Machine
DC-M	DC Motor
IGBT	Insolated Gate Bipolar Transistor
PWM	Pulse Width Modulation
DSP	Digital Signal Processor
UPS	Uninterruptible Power Supply
CH1	Channel 1 of the Oscilloscope
CH2	Channel 2 of the Oscilloscope
CH3	Channel 3 of the Oscilloscope
CH4	Channel 4 of the Oscilloscope
LED	Light-Emitting Diode
EPLD	Erasable Programmable Logic Device
PCB	Printed Circuit Board
MIPS	Million Instructions per Second
ROM	Read Only Memory
I/O	Input Output
WD	Watchdog
ADC	Analog-to-Digital Converter
CAN	Controller Area Network
SCI	Serial Communication Interface

SPI	Serial Peripheral Interface
GPIO	General-Purpose Input/Output
JTAG	Joint Test Action Group
OCP	Over Current Protection
LPF	Low Pass Filter
DBSA	Development Bank of Southern Africa
τ	Time Constant
V_{drop}	Voltage Drop across Inductor (V)
t	Time (s)
R	Resistor (Ω)
C	Capacitor (F)
L	Inductor (H)
$V_{B\ MEASURE\ IN}$	Voltage provided from the SKHI65 referred to the Phase B Current (V)
$V_{B\ MEASURE\ DSP}$	Input Voltage to the DSP referred to the Phase B Current (V)
$I_{AC\ ACTUAL}$	Actual AC Current (A)
I_{TRIP}	Over-Current Trip Level Setting (A)
V_{R11}	Voltage across R11 (V)
$V+$	Input Voltage to Positive Terminal of Operational Amplifier
$V_{DC\ CURRENT\ DSP}$	Input Voltage to the DSP referred to the DC Current (V)
$V_{DC\ IN}$	Input Voltage to the DC Current Measurement Circuit (V)
$I_{DC\ IN}$	Current from the DC Current Sensor (A)
$U_{DC\text{-}Bus}$, V_d	DC Bus Voltage (V)
R_{sa}	Thermal Resistance between Sink and Ambient (°C/W)
V_{LL1}	Line-to-Line Voltage (V)
$\hat{V}_{AN}$	Voltage between Phase A and Neutral (V)
m_a	Modulation Index

CHAPTER 1: INTRODUCTION

1.1 Renewable Energy

Due to the drastic increase of electricity demand throughout the world, represented in Figure 1-1 [1], it is essential to have alternative energy resources to fossil fuels such as coal, natural gas and oil for the generation of electrical power. The amount of power generated by coal, natural gas and oil consumed by the world's population in one day corresponds to 500 000 days for nature to provide these natural resources [24]. This means that energy is consumed 500 000 times faster than nature can produce these sources. About 34% of South African households are still without electricity [2]. Large-scale electrification has been prevented due to the high investment and maintenance costs of expanding interconnected grids to locations where the energy demand is poor. Some of these off-grid locations have been electrified with diesel generators. Because of high fuel costs, a need to find cleaner ways to harvest energy is vital to provide these off-grid locations with power.

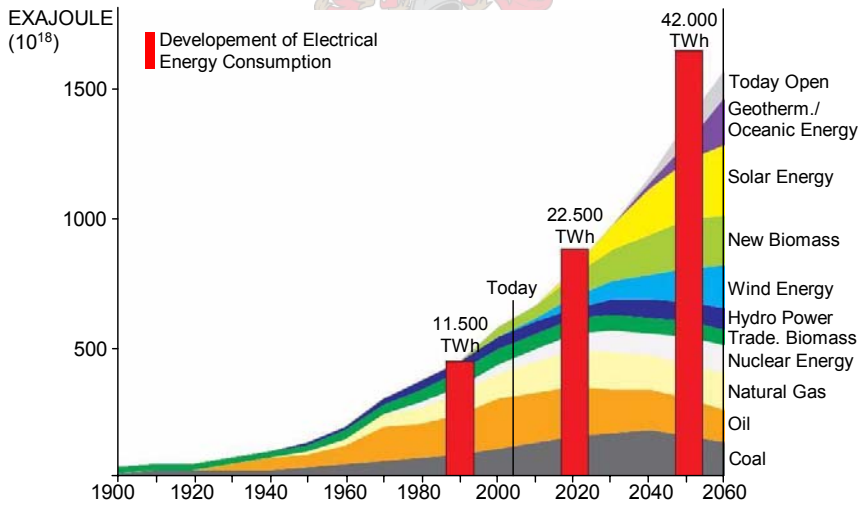


Figure 1-1: Possible Development of Electrical Energy Consumption [1]

The three most extensively available natural resources are hydro, wind and solar. The movement of water is used to generate power by hydro systems. Wind motion is utilized by wind turbines to convert kinetic energy to electrical energy. Solar radiation is the most common kind of energy that is converted to electricity by employing photovoltaic panels

(PV), solar towers, channels, solar dishes, etc. Figure 1-1 shows the possible development of electricity consumption around the world. It is observed that the solar industry has the most promising future. Due to the high level of solar radiation in South Africa, it is most viable to consider solar thermal and photovoltaic systems. Photovoltaic systems are currently the most favourable in terms of their low cost.

This thesis focuses on the design of a 23 kW three-phase AC bus system that is utilized together with the "Stirling Energy System (SES) Integrated Solar Dish-Stirling Module" (Model DSSG-25-MKII) to function as a mini-grid for off-grid locations. This three-phase AC bus system includes a bidirectional PWM converter, with control, and a battery bank for energy storage. A mini-grid is a standalone unit and is often called an island grid.

1.1.1 Island Grids

Supplying electricity to decentralized consumers that cannot be connected to an existing electrical grid is essential throughout the world. At present island grids exist in numerous sectors around the world [2]. An island grid is intended to be standalone and operable in remote areas. Different types of island grids are employed in different regions, depending on the environmental circumstances. It is more likely that wind turbines are employed as energy source in windy areas, where the sun's solar radiation is inadequate. Farms were commonly connected to a low-voltage or intermediate-voltage grid, where diesel generators are the feeding energy source. Due to the increase in the fuel price, farmers started to use hybrid systems. Renewable energy sources were implemented as an alternative to diesel generators.

Energy sources such as photovoltaic (PV) panels, wind turbine generators and solar dishes are examples of renewable energy sources. The most developed system is the PV system. Wind turbine generators are more feasible for higher power ratings than PV. This would make them attractive for pumping. The solar dish concept is more feasible in the

10-50 kW range than photovoltaic panels. Other solar thermal options, such as solar tower or solar troughs, are more feasible at higher ratings (MW) [2]. Lead acid batteries are the leading technologies in energy storage. Other storage devices are examined next.

1.1.2 Storage Devices

Electrical energy can be stored in limited ways. One of the oldest ways to store energy has been by making use of flywheels. These flywheels operate on a simple principle of storing kinetic energy in a rotating mass [3]. Another common storage device is a capacitor, where the energy is stored electrostatically. Large-scale energy storage is done by pumping water to a reservoir or dam at a higher level. The most common storage device is the battery. The versatility of batteries makes it possible to have a large variety of storage space. Sealed lead acid batteries and nickel cadmium (NiCad) batteries are superior for solar applications. A NiCad battery is 2-3 times more expensive [4] than a lead acid battery and is mostly used in very cold environments. The lead acid battery has an excellent power-to-cost ratio and has high charge store efficiency. More detailed aspects are discussed in subsequent chapters.

1.2 Power Electronics

1.2.1 Introduction

The flow of electric energy is processed and controlled by power electronics, which supplies accurate voltages and currents in a form optimally suited for user loads. Figure 1-2 represents a basic power electronic system. The power processor mainly consists of semiconductor devices that are driven from the controller. These semiconductor devices have enormous current and voltage capabilities as well as high switching speeds.

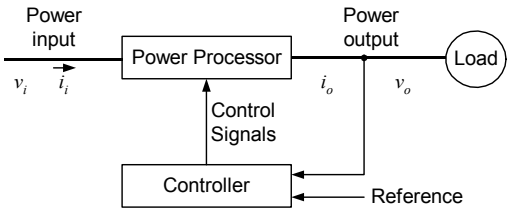


Figure 1-2: Diagram of a Power Electronic System

1.2.2 Converters

A converter is a basic module of a power electronic system, such as in Figure 1-2, which converts power by signal electronics. Converters are divided into four broad categories:

- AC to AC
- DC to DC
- AC to DC
- DC to AC.

A power converter which converts DC to AC is called an inverter. A rectifier converts AC to DC. This thesis presents a design of a converter which is intended to function as an inverter as well as a rectifier. This bidirectional converter consists only of a single semiconductor module and thus rectification and inversion take place successively. Figure 1-3 shows the fundamental blocks of a bidirectional power electronic system.

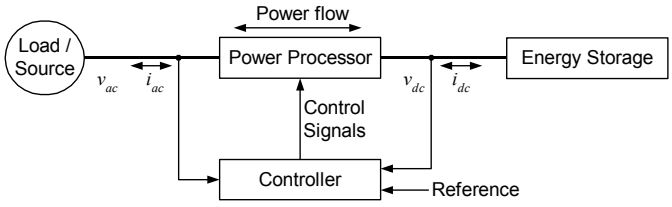


Figure 1-3: Diagram of a Bidirectional Converter

1.2.3 Applications

Power electronics is used in many sectors of the industry, such as in commercial, residential, transportation, aerospace, telecommunications and utility systems [5]. Utility systems include high-voltage DC transmission, supplementary energy sources (photovoltaic, wind, solar) and energy storage systems. The bidirectional converter is employed as a medium to combine a solar energy source together with an energy storage to function as an uninterruptible power supply.

1.3 Thesis Structure

A brief introduction to renewable energy, power electronics and energy storage is provided. Chapter 2 focuses on island grids. Storage devices are discussed in more detail. Diverse systems are represented and compared. Existing units in off-grid locations are discussed and evaluated. Different topologies of island grids are shown and the most suitable topology is chosen after assessment. The system description of the Stirling Energy System (SES) is explained. Simulations of the design are presented to clarify and verify the operation of the AC bus system. Component ratings are revealed through simulations in Chapter 2. Chapter 3 then presents the design and synthesis of an AC bus converter system. System evaluation through experiments, measurements and results is given in Chapter 4. Measurements and experiments were done in the laboratory and on site. Procedures for the final system's implementation on site are also presented. Chapter 5 rounds the thesis off with conclusions and future recommendations for useful research.

CHAPTER 2: ISLAND GRIDS AND STIRLING ENERGY SYSTEM

2.1 Introduction

This chapter examines the research done on a variety of island grids. Different concepts of island grids are presented and evaluated. An island grid entails a topology which interacts with energy sources and an energy storage device to provide a load with clean and reliable power as seen in Figure 2-1. Figure 2-1 represents an example of an island grid where three different energy sources (solar dish, wind turbines and PV panels) feed through power electronic converters into a three-phase AC bus system where the energy is stored in a DC battery bank.

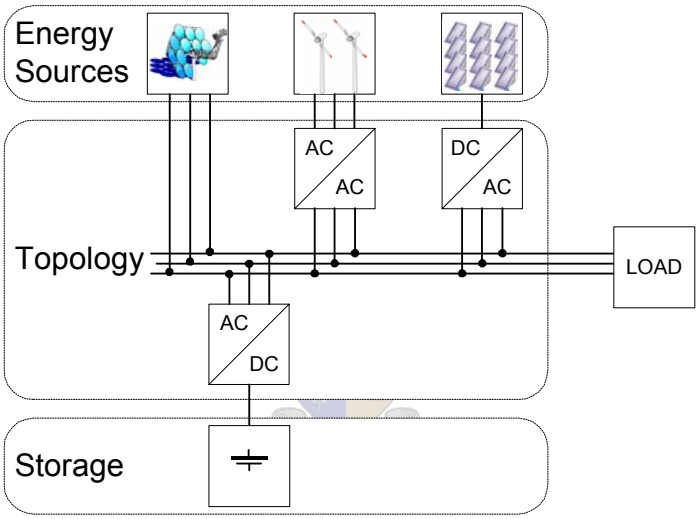


Figure 2-1: Example of an Island Grid

Island grids operate in the power range from several watts to few hundred kilowatts. Photovoltaic panels are used as energy source for smaller systems. The larger systems require bigger energy sources such as wind turbines or solar dishes, which are in the range of 10-50 kW [2].

Before concluding this chapter a final topology is chosen which most suits the implementation of the Stirling Energy System as energy source. An energy storage device for this application is discussed and a conclusion on a final storage device is presented. The final topology is modelled in a simulation program, which reveals the system

operation as well as the component ratings. The system is designed to function in rural areas which are situated at off-grid locations.

2.2 Off-Grid Locations

Off-grid locations are found anywhere around the world where a main grid is not in close proximity to the load. These locations could be farms, settlements between villages, on ships, yachts, islands and rural areas. The electricity consumption at these places is often low compared with the consumption at cities or urban locations. This low demand for electricity is the reason why it is not worthwhile to extend the grid to such decentralized locations. Extension of the main grid to locations which are non-stationary, such as ships or boats, is impossible. A solution to this electrification problem is to implement standalone island grids.

As the economy in rural areas changes, due to bigger energy supply and demand, many local leaders are attracting new large industrial clients into the area [6]. When a large industrial business does locate in a service area, the rural electric cooperative is faced with many issues: the impact of the new load on existing system infrastructures; the potential issue of power quality on its system; and its impact on its customers. This requires that, before a large industrial customer is added, careful studies are made of rates, interconnection guidelines and protection issues. The new customer may require state of the art relay devices and fast-track-type installations to meet start-up demands [6].

Security and maintenance are also of major concern when implementing standalone systems in rural areas. Theft of solar panels is still an issue. Theft of bigger devices such as a wind turbine or a solar dish is less of a concern.

2.3 *Electrical Energy Storage*

Energy storage is vital in an island grid application, where the sun is the only energy source, and where an electricity supply to the consumers is desired 24 hours a day. The amount of energy to be consumed during the night needs to be stored during the day, through some kind of pump or battery charger. Energy is stored in a variety of fashions.

2.3.1 Different Technologies

One of the oldest ways to store energy was by making use of flywheels. The angular momentum of a rotating rotor determines the stored energy. The conversion of electrical energy to mechanical energy and then back again is achieved by an electrical machine. The electrical machine accelerates the flywheel when energy needs to be stored. Energy is acquired from the flywheel when the machine acts as a generator. Flywheels are quite complex [7] and thus the demand is low [8]. Flywheels are not considered as a storage medium for this project due to their complexity.

Large-scale energy storage is done by pumping water from a lower reservoir, or dam, to another water storage which is situated at higher levels. This can still be implemented in the design for future purposes. The excess energy that is not used for battery charging or consumed by the load can be used to pump water to a higher potential. The most common storage devise used in solar applications is the battery.

2.3.2 Batteries

The versatility of batteries allows for a large variety of storage spaces. The most important characteristics [4] of batteries are the ability to be repeatedly charged and discharged without damage, the storage capacity of the battery, the ability to hold charge when not in use, to be charged and discharged with minimum loss of electrical energy,

and to operate for long periods with little or no maintenance. Sealed lead-acid batteries and nickel cadmium (NiCad) batteries are superior for solar applications. A very good deep-cycle battery is the AGM (Absorbed Glass Mat) battery. This battery has the following characteristics [4]:

- The plates in AGMs are tightly and rigidly mounted, and withstand shock and vibration better than any standard battery;
- No spilling, even when they are broken, since all the electrolyte (acid) is contained in the glass mats;
- AGM batteries are "recombinant"- this means that the oxygen and hydrogen recombine inside the battery. The recombining is typically 99% efficient, so almost no water is lost;
- AGMs have a very low self-discharge rate – from 1% to 3% per month is usual.

More than 90% of total energy systems use lead-acid batteries as storage devices because of their main advantages [4]:

- Very good power to cost ratio (less than ⅓ to ½ that of NiCad battery);
- Easy increasing battery storage capacity due to relatively high discharge voltage;
- Long duty charge/discharge cycle (depth of discharge can reach 80%);
- Low level of maintenance;
- Low cost of disposal after being discarded.

The number of times a battery can be charged and discharged does depend on its chemical structure. Thus different batteries last longer (are recharged more often) than others. If only a small amount of power is taken from the battery, before recharging, the cycle life becomes much longer. Depth of discharge (DOD) is the extent to which a battery is allowed to be discharged in normal operation. Beyond the maximum permissible DOD permanent damage is caused to the battery. Batteries with a high DOD are typically called deep-cycle batteries and are most suitable for solar systems. The batteries available for this project are the Deltec High Cycle (12 V, 102 Ah) batteries. Sixty of them are connected in series. These batteries are selected for their low cost; however, they are not perfect for this type of application as seen in Figure 2-2, where

different batteries are compared. The battery utilized is indicated by the black curve. The number of cycles (charge/discharge) corresponding to a DOD of 40% yields about 380 cycles. The AGM batteries would be most suitable, but the price range is quite high, approximately R 2500.00 for a single AGM battery.

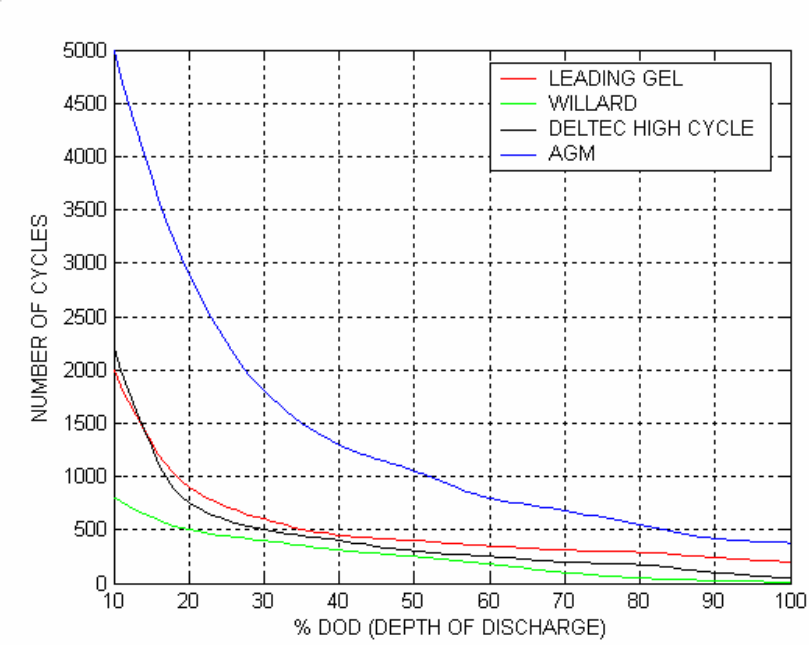


Figure 2-2: % DOD vs. Number of Cycles for Different Batteries

2.3.3 Conclusion

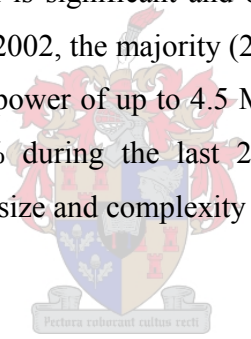
Due to the advantages of a lead-acid battery it is most feasible to make use of them in the design. The relatively low cost makes it the most favourable choice. Since the system was build for research purposes, an average battery was selected. A low level of maintenance is compulsory for off-grid locations. If the system is implemented in an off-grid location and has to last for a few years, it is more suitable to employ an AGM battery with a deeper cycle.

2.4 *Natural Energy Sources*

The sun shining on the earth each day provides vast amounts of solar energy, which can be converted to thermal or photovoltaic energy to power a variety of types of equipment. This is an attractive alternative to the traditional generators because these systems are safe, pollution-free and generate electrical power extensively. The three most extensive available natural resources are hydro, wind and solar power. The focus in this section is on wind and solar sources.

2.4.1 Wind Turbine Generators

Growth in wind-power generation is significant and over 30 GW of capacity had been installed worldwide by the end of 2002, the majority (22 GW) of this being in Europe [9]. The largest wind turbine delivers power of up to 4.5 MW. The cost of producing energy from wind has dropped by 85% during the last 20 years [10]. Wind turbines are unattractive to thieves due to their size and complexity [11].



2.4.2 Photovoltaic Panels

The cost of photovoltaic electricity has decreased dramatically over recent decades. Worldwide PV sales could reach 6 GW by 2010 [9]. PV systems have efficiencies of 10 – 15% which is much lower than that of a solar dish, which is about 29.4%. Research revealed that the efficiency of a PV panel can be increased to about 20% when tracking of the sun is taken into account instead of having a stationary PV panel [9]. PV panels are small in size and low in complexity compared with a solar dish or a wind turbine. This is why theft is a more serious consideration with PV system implementation.

2.4.3 Solar Dish Generators

Solar dish technology is quite new on the market and thus single units are very expensive. Stirling engines are the subject of increased research activity and they might reach their large potential market during the next few years. The big advantage with the Stirling dish is that it works with a closed gas cycle, where no external gas or water needs to be supplied. Hydrogen and helium are commonly used as the working gas, because these gases have high heat-transfer capabilities. The Stirling engine is one of the most efficient devices for converting heat into mechanical energy [12]. The temperature of the thermal receiver typically ranges from 650 ºC to 800 ºC [12]. The system power output per area of solar insolation of 835 W/m^2 is much better than for a PV cell, which is about 200 W/m^2 [12]. The dish/engine systems have demonstrated the highest solar-to-electric conversion efficiency (29.4%) of all solar technologies [13].

2.4.4 Conclusion

The solar dish concept is still in the development stage. It employs high-level technology for system control, but it is not yet well developed enough for the system to operate for long periods at a time. The wind turbine and PV cells are thus more reliable and more attractive to implement. The dish/engine concept has much higher solar-to-electric efficiencies than other solar technologies and is thus vital for future research.

2.5 System Configurations

Two different system configurations are considered in this design. Both are suitable for this type of application. The configurations to be discussed are the DC Bus and AC Bus topologies. Each topology entails an energy source, which is the SES, a battery bank,

power converters and a load. The power produced by the SES needs to be consumed by some kind of load.

2.5.1 DC Bus Topology

The DC bus topology can be observed in Figure 2-3. The solar dish feeds through a three-phase bidirectional converter into the DC bus, where the energy is stored in a DC battery bank. It is compulsory that the three-phase converter is bidirectional to start-up the induction machine of the SES as well as to consume the generated power of the SES. A three-phase inverter then supplies the load with power. The power is converted twice before it is fed to the load. The first conversion stage is done from three-phase AC to DC and the second conversion stage is from DC to three-phase AC. Each conversion stage has a typical efficiency of 95%, which relates to a total typical source-load efficiency of 90.25%.

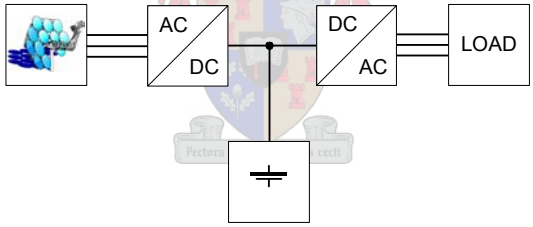


Figure 2-3: DC Bus Topology

The two conversion stages make the DC bus system more complex and thus more expensive. Figure 2-4 shows the three options for where to connect the dump load on the DC bus system. The dump load consumes the excess power generated by the SES. The most efficient position to place this dump load is at position A. Position B and C in Figure 2-4 is situated on the DC bus and on the three-phase AC output respectively, where the power has to be converted at least once before the power is dissipated in the dump load.

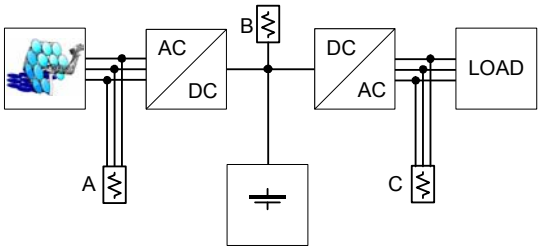


Figure 2-4: DC Bus Topology including Dump Load

The system in Figure 2-3 is simplified by connecting the load directly to the three-phase AC bus, to which the SES is connected, and excluding the DC to three-phase AC inverter. This results in an AC bus topology which is discussed next.

2.5.2 AC Bus Topology

Sunny Island® [22], a company that manufactures converters suitable for island grids, base their designs on an AC grid system. The Sunny Island® systems, however, operate from a 63 V DC battery bank. A number of smaller battery banks are connected in parallel instead of connecting all batteries in series. This is done to ensure continued operation if a single battery fails. A disadvantage with this low DC battery voltage is that a CUK [5] converter (DC/DC), which steps up the voltage to a higher level, needs to be included in the design to get the required AC output voltage. The Sunny Island® topology is shown in Figure 2-5.

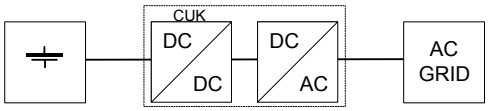


Figure 2-5: Sunny Island® Topology for a Single-Phase Unit

This topology is extended to a three-phase system by adding another two of these single phase units in parallel as seen in Figure 2-6. The system controller is then configured to function for three units.

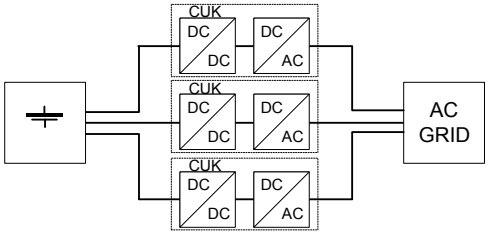


Figure 2-6: Sunny Island® Topology for a Three-Phase Unit

The design of the AC bus system for this project was based on the AC system of Sunny Island®. The main difference is that the design presented in this thesis consists of a three-phase inverter that has one system controller and consists of a single unit instead of three single units as in the Sunny Island® systems. Another big difference is that a high-voltage battery bank is utilized, thus eliminating the use of the CUK converter. Since the power rating of this system is significantly higher (25 kW), parallel high-voltage banks are typically used for energy capacity and redundancy. Figure 2-7 (a) shows the topology implemented in this design. The topology entails a three-phase bidirectional converter connected to a battery bank to modulate an AC grid. This 4-wire AC system provides clean power to single-phase or three-phase loads. The system also absorbs the power generated by an energy source, such as the SES. The single conversion stage has an efficiency of 95% which is better than the total efficiency of the DC bus topology, which was 90.25%.

In Figure 2-7 (a) the dump load is connected to the AC bus. This configuration is more efficient than the DC dump configuration seen in Figure 2-7 (b). The main advantage of the AC load over the DC one is that the former avoids the flow of active power current through the PWM converter. Consequently, the PWM converter rated power is lower [23]. During a normal day of solar insolation the SES provides a power of ± 20 kW. About 10 kW is used to recharge the batteries and the remaining 10 kW are dissipated into the dump load. If the dump load is in position B, as in Figure 2-7 (b), the power ratings of the converter have to be increased by 10 kW, since the power that is dumped needs to be converted to DC. It is thus more reasonable to employ an AC dump load.

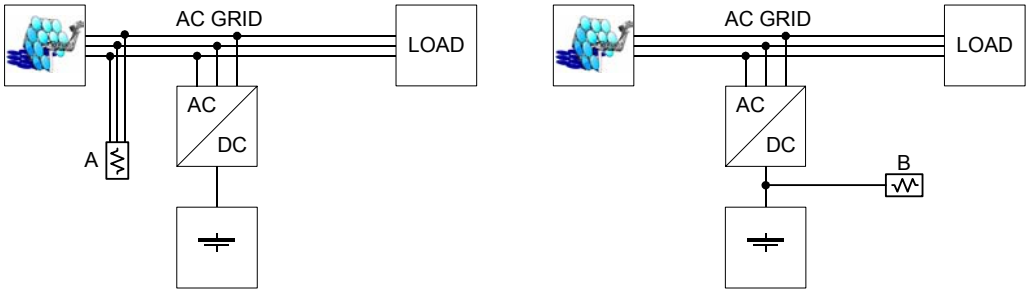


Figure 2-7: Diagram of the AC Bus Topology including (a) AC Dump Load; (b) DC Dump Load

2.5.3 Conclusion

The AC bus topology in Figure 2-7 (a) has a higher efficiency than the DC bus topology in Figure 2-4 and is less complex as well as financially cheaper. The high-voltage battery bank has the benefit that a CUK converter, as in Figure 2-5, is omitted. It can also be concluded that the AC dump load reduces the system power ratings as well as increasing the overall efficiency. The dump load was for research only. The topology in Figure 2-7 (a) was chosen for this design and the simulations in Section 2.7 reveal that this topology is suitable for functioning as a standalone unit for rural applications. The natural energy source of this system is the SES, which is discussed next.

2.6 Stirling Energy System

2.6.1 Introduction

The Stirling Energy System (SES) was initially developed by McDonnell-Douglas in the mid-1980s. The SES is an integrated module that consists of a parabolic dish concentrator and a power conversion unit (PCU). This Dish Stirling Solar Generator set (DSSG-25-MKII) module delivers a gross peak electrical output of 25 kW at V_{LL} = 400 V, 3ϕ, 50

Hz. The DSSG-25- MKII is designed to be grid connected and operable in a solar only mode. When the solar insolation level is below a certain limit, the unit stops delivering power, until a certain solar insolation level is reached. The entire unit is independent of the grid as long as the AC bus voltage is 400 V ± 10% and the capacity is 25 kW with a peak capacity of 280 kW. More than 92% of the solar radiation that hits the dish is reflected to the thermal receiver, leading to an overall solar-to-electric conversion efficiency of 29.4% [25].

2.6.2 System Description and Electrical Interface Requirements

System Elements

The SES is comprised of a parabolic dish, a PCU and a system controller. The parabolic dish consists of 82 mirror facets fixed to a steel frame which is mounted onto a pedestal. The resulting composite parabolic mirror is 11 meters high and 11 meters wide. Each mirror is slightly curved itself so that the whole mirror dish is perfectly parabolic, as seen in Figure 2-8, and has maximum efficiency.

Figure 2-8: Picture of the SES

The PCU is mounted at the dish's focal point. The PCU consists of a Stirling engine which is mechanically connected to a 25 kW induction machine (IM). The system controller controls the unit to track the sun during the day and sets the system to night-stow position, where it remains until the next morning. A small DC motor, which runs from a 12 V DC battery, causes the dish to move in the vertical plane. This motor can de-track the system when a power failure occurs. A small AC machine executes the movement in the horizontal plane.

Stirling Engine

A Stirling engine works in a similar manner to an internal combustion engine in terms of compression and expansion, but it differs from a conventional engine in two fundamental aspects; heat is supplied continuously and externally, and the working gas – which is usually hydrogen or helium - operates in a completely closed system. A Stirling engine "burns" sunlight instead of diesel, gas or coal to produce mechanical torque, which is converted to electrical energy by an induction machine. Figure 2-9 shows the front end of the thermal receiver.

Figure 2-9: Pictures of the Thermal Receiver

Operating Information

The system controller automatically commands the module to turn from a night-stow position to a position where the dish is facing the sun just before it rises over the horizon. The beam is focused on the engine as soon as the system controller records a solar insolation reading of greater than 300 W/m^2 for at least 30 seconds [21]. The thermal receiver of the PCU heats up due to the concentrated heat beam. The module is then commanded to connect itself to the three-phase grid. This connects the IM directly to the grid. The IM cranks and thus consumes a peak current of more than 400 A at start-up. A change in torque to the IM, due to the Stirling engine, results in a faster speed than the IM synchronous speed. The IM starts functioning as a generator and power is delivered to the AC bus. If the solar insolation level, monitored by the system controller, falls below the minimum level of 300 W/m^2, due to cloudy conditions, the module continuous to track the sun, but the beam is taken out of the focal point. The system resumes power generation as soon as the clouds pass and the required solar insolation of 300 W/m^2 is reached again. The solar insolation level must stay above the 300 W/m^2 thresholds for the system to deliver power. During sunset the system controller automatically commands the module to return into the night-stow position.

The tracking of the sun is done by the system controller, which has a mathematical algorithm to determine the position of the sun. Figure 2-10 represents the relationship between the system power output and the solar insolation intensity. Solar insolation levels must be greater than 300 W/m^2 for the module to operate. The module may shutdown when operating at insolation levels above 1000 W/m^2 due to thermal input overload.

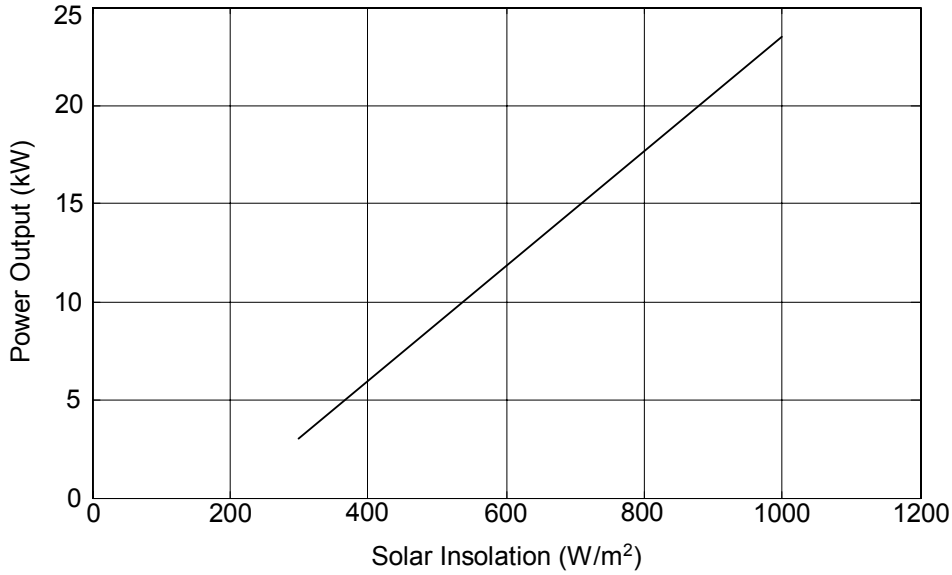


Figure 2-10: Power Output vs. Solar Insolation

Figure 2-11 shows an example of the power produced by the SES as the solar insolation varies [25].

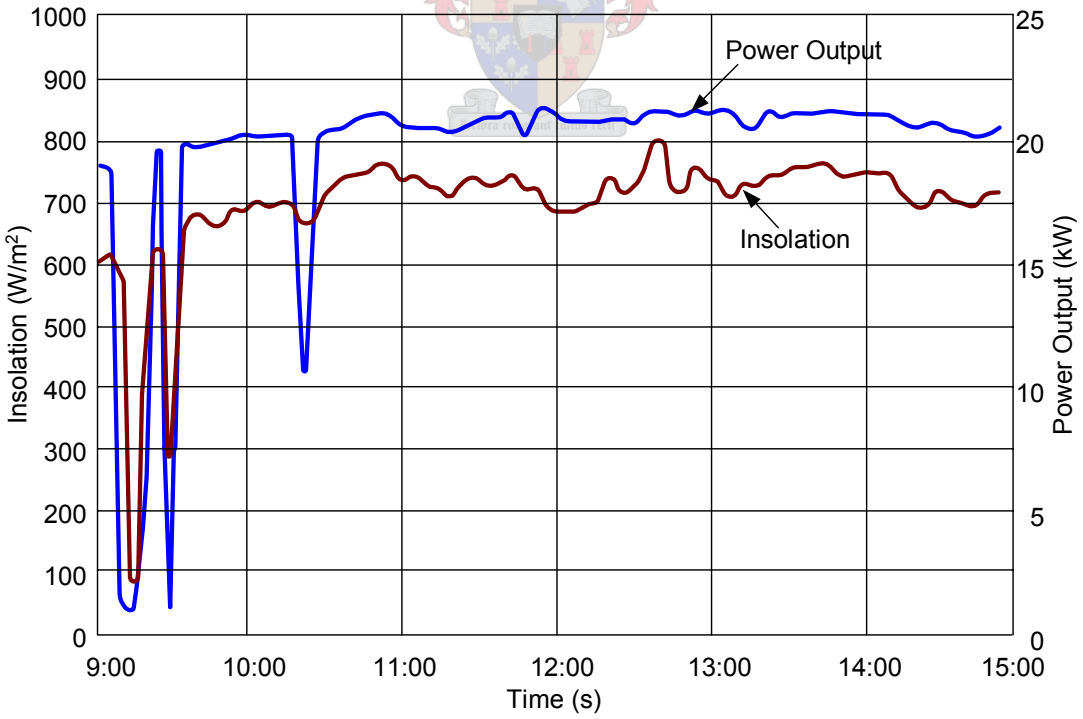


Figure 2-11: Example of SES Power Output as Solar Insolation varies

Electrical Interface Requirements

The PCU of the SES requires a line-line voltage of 400 V ±10%, 50 Hz, three-phase. This power supply must be capable of starting a 25 kW IM, which needs more than 100 kW of energy per start [21]. Measurements taken on site revealed that peak power of 280 kW and peak current of 523 A were consumed to crank the PCU. The three-phase grid also needs to absorb the generated power of the SES. The output requirements of the SES concentrator / PCU is that it be grid connected and delivering an output voltage of 400 V, 50 Hz, three-phase. The SES system controller operates on a single-phase supply voltage of 230 V, 50 Hz.

2.6.3 System Modelling

The AC bus topology discussed in paragraph 2.5.2 resulted in a circuit that could easily be implemented in SIMPLORER™, a power-electronic simulation program. The SES is replaced by an IM where the torque is controlled. The internal parameters of an IM were needed to fulfil the IM modelling requirements.

2.7 Simulation of an AC Bus Converter System

The converter model was created in SIMPLORER™ (Version 6), a power-electronic simulation program, where simulations verified system operation. This section deals with the simulations performed as part of the development. The schematic setup and simulation results are discussed with which the component ratings are determined. These component rating are the minimum requirements for the practical design.

2.7.1 Setup

The main issue with the system implementation in SIMPLORER™ was to model the SES. Other factors such as modelling the battery bank, the load management system, PWM, and filtering the output waveform are also employed in SIMPLORER™. The SES entails a 25 kW induction machine mechanically connected to a Stirling engine. The torque of the Stirling engine on the IM determines the power flow of the SES. Figure 2-12 shows the relationship between the speed of an IM and its corresponding torque. An IM can function in three different modes. These are braking, motoring and generating, as indicated in Figure 2-12. It is observed that the torque is zero when the IM speed equals its synchronous speed. The IM functions as a motor, as soon as the torque and the speed increases above zero, and thus consumes energy. A negative torque corresponds to a generating mode where the speed increases above synchronous speed. From these statements the Stirling engine can be modelled by controlling the applied torque to an induction machine.

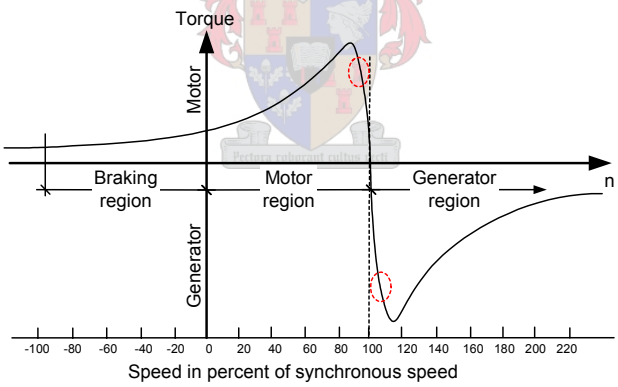


Figure 2-12: Speed Torque Characteristics of an IM

The operating areas for generating and motoring regions are indicated by the red dotted circles in Figure 2-12.

The IM has 2 pole pairs and internal parameters as seen in Figure 2-13. Research revealed that the parameters correspond to a 32 kW IM. Figure 2-13 shows the schematic diagram of the bidirectional converter. The converter consists of 6 IGBTs, an L-C filter,

DC bus capacitors and a big capacitor with a resistor in series to model the battery bank. The total energy of the battery bank is:

$$\begin{aligned} E &= P \cdot t = V \cdot I \cdot t \\ &= (12 \cdot 60) \cdot (100) \cdot (60 \cdot 60) \\ &= 259.2 \text{ MJ} \end{aligned} \tag{2-1}$$

The size of the capacitor that models the battery bank is calculated as follows:

$$\begin{aligned} C &= \frac{2 \cdot E}{V^2} \\ &= \frac{2 \cdot 259,200,000}{(12 \cdot 60)^2} \\ &= 1000 \text{ F} \end{aligned} \tag{2-2}$$

Capacitor C5 and C6 in Figure 2-13 are each 2000 F and model the battery bank. These capacitors have initial voltages of 373 V. The output filter design is discussed in Section 3.5. The inductor values are 400 uH each and the filter capacitor values are 100 uF each. The system also includes the soft start and dump circuits as well as the thyristor dump circuit which is shown in Figure 2-13.

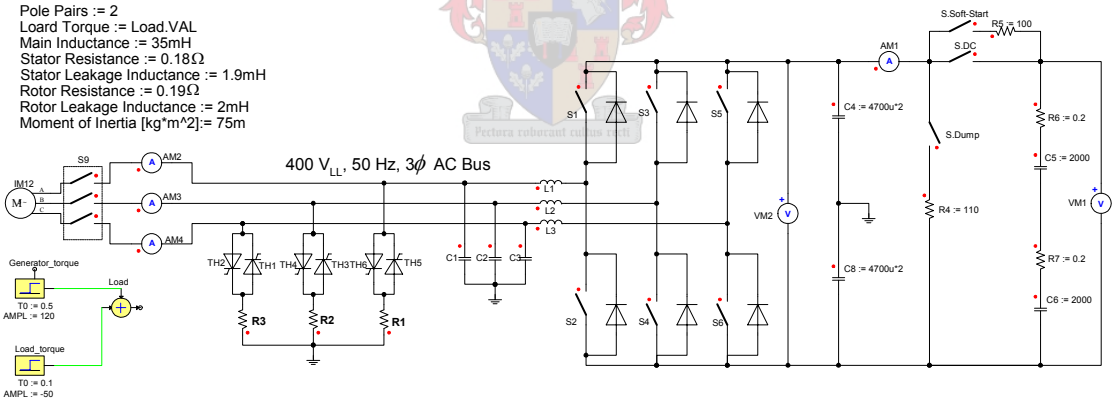


Figure 2-13: Schematic Diagram of the Converter

A switch with a parallel diode represents an IGBT. Each IGBT pair is switched independently from the other. The basic system operation is discussed shortly and the detailed design, such as PWM and component ratings, is discussed in Chapter 3.

2.7.2 System Operation

The basic principle is to modulate an AC grid, as in Figure 2-7 (a), which can supply the required voltage, current and frequency to the SES. The SES has its own control and thus the two systems function independently. The SES is designed to be grid connected and a soft start of such a system is thus not possible. An AC grid is provided as soon as the converter is switched on. Any kind of load can be connected to the AC grid. The power generated by the SES needs to be stored in batteries or consumed by some kind of load. The battery voltage and current are monitored so that the batteries are charged at a permissible rate. The simulations shown in the succeeding paragraphs reveal if the system functionality is successful and reveal the component requirements. These simulation results are compared with practical results in Chapter 4 and are given in APPENDIX C for a clearer comparison.

Simulations of the system were done over a one-second period. Simulations done over a longer period of time are very time consuming and require too much computing power. Data need to be sampled every 5 us to get a reasonable result. All waveforms shown in this subsection correspond to Figure 2-13. The AC bus voltage waveforms of the system are represented in Figure 2-14. The voltages are 120º phase shifted and have magnitudes of 230 V RMS. The voltages are measured across the filter capacitors (C1, C2 and C3). A 5 kHz ripple is observed on the signal. The DC bus voltage corresponds to 746 V.

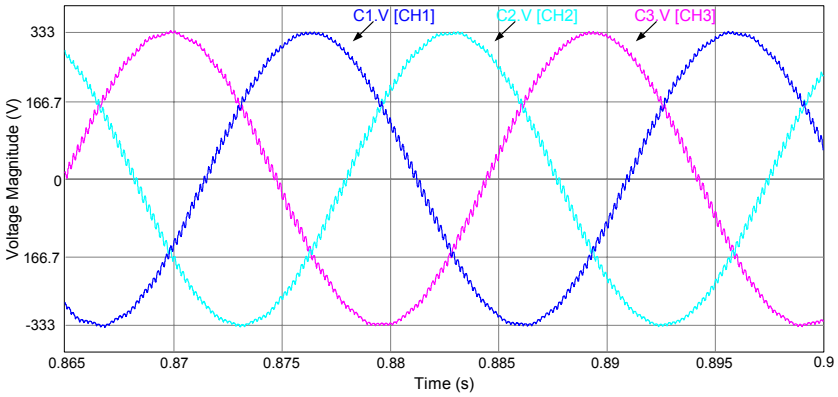


Figure 2-14: Simulation of the AC Bus Voltage Waveform

2.7.3 Inverter and Rectifier Mode

The succeeding simulations show that the bidirectional converter functions in two different modes. An important feature of the system is that the power flow is bidirectional. The graph in Figure 2-15 represents the IM speed vs. time simulation. At 0.1 seconds the three-phase switch (S9), in Figure 2-13, is closed and the IM spins up to about 1490 rpm as seen in Figure 2-15 and Figure 2-16, which is an enlarged graph of Figure 2-15. The IM acts as a motor due to the negative applied torque, which is -50 Nm. Figure 2-17 represents the DC current, which drops negative to start the IM. The battery voltage, as seen in Figure 2-18, decreases due to the energy consumed by the IM. The converter acts as an inverter. The torque is changed to +120 Nm at 0.5 seconds. Figure 2-15 and Figure 2-16 show that that the IM speed rises above the synchronous speed (1500 rpm) and that the DC current in Figure 2-17 reverses direction and thus charges the battery bank at about 10 A. At this time the SES initiates power generation. Now the converter acts as a rectifier and the battery voltage increases as seen in Figure 2-18.

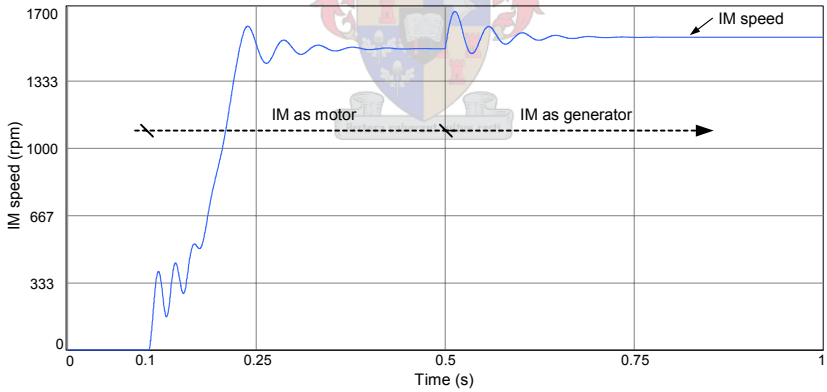


Figure 2-15: Simulation of the IM Speed

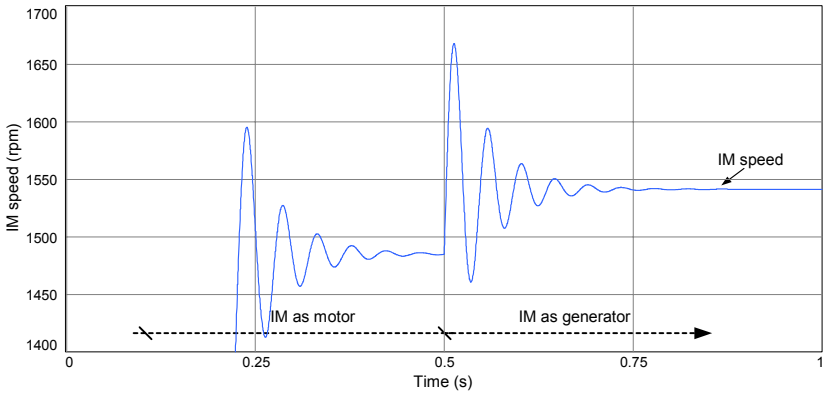


Figure 2-16: Enlarged Simulation of the IM Speed

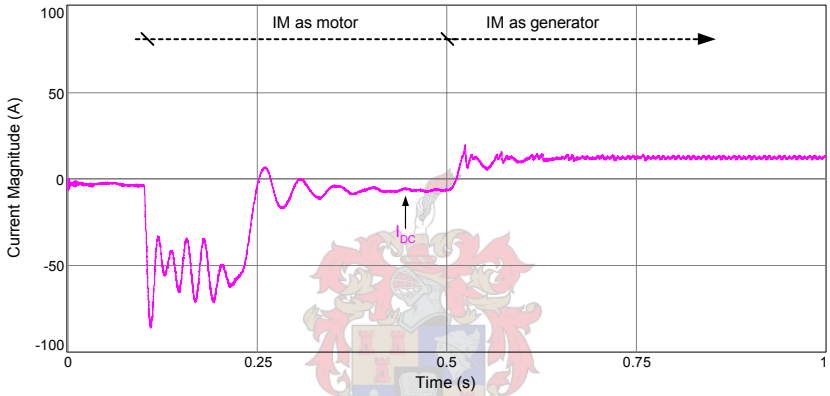


Figure 2-17: Simulation of the DC Current

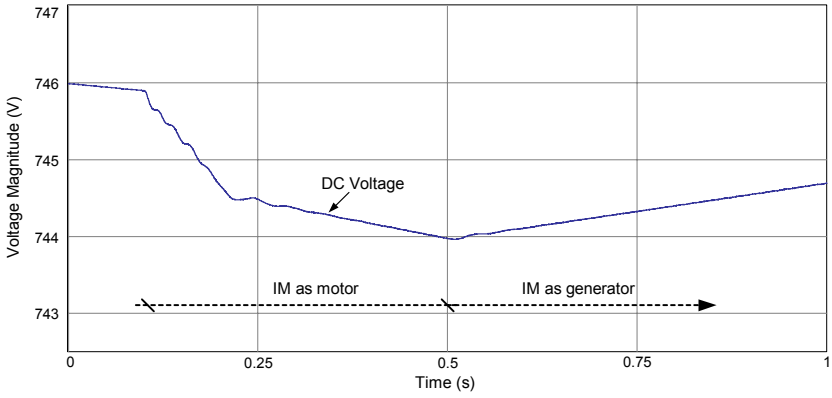


Figure 2-18: Simulation of the DC Battery Voltage

The simulations reveal that the converter is bidirectional and confirm that the SES can be modelled as an IM with a changing torque.

2.7.4 Average-Power Simulation

A resistive load of 4.7 Ω is connected to each phase as a Y-connection with the neutral point connected to ground. The converter functions as an inverter with a total output power of:

$$P_{out3\phi} = \frac{3 \cdot V_{LN}{}^2}{R_{Load}} = \frac{3 \cdot 230^2}{4.7} = 33.77 \text{ kW} \tag{2-3}$$

Figure 2-19 represents the simulated output of the converter when delivering a power of 33.77 kW. The AC voltages are measured across the filter capacitors (C1, C2 and C3). The measured signals correspond to the different channels (CH1, CH2 and CH3) measured on the oscilloscope in Figure 4-4. The phase current I_A [CH4], which corresponds to CH4 in Figure 4-4, is in phase with its phase voltage C1.V as seen in the phasor diagram (Figure 2-20). A power factor (pf) of 1 corresponds to a purely resistive load. I_A [CH4] has a RMS value of about 49 A and the phase voltages have RMS values of 230 V.

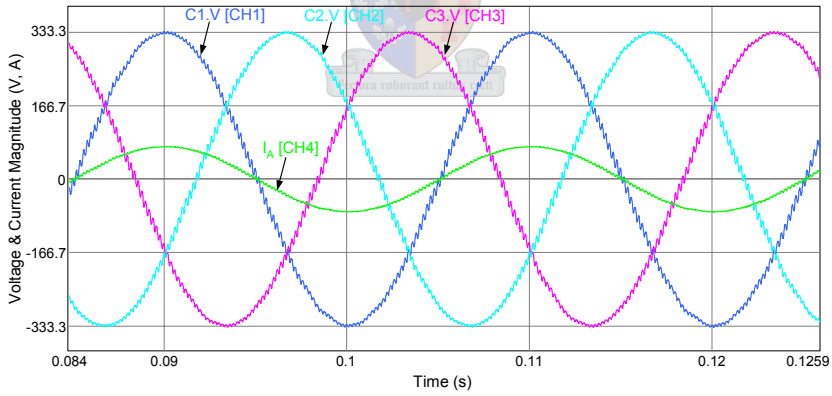


Figure 2-19: Output Waveform of the Average-Power Simulation

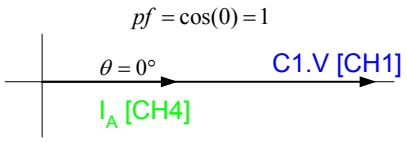


Figure 2-20: Phasor Diagram for a resistive load

The simulated results together with the practical results are shown in APPENDIX C for a better comparison.

2.7.5 High-Power Simulation

This simulation is done in a similar manner to the average-power simulation, except that a load of R_{Load} = 1.1 Ω is connected to each phase. From Figure 2-21 and Figure 2-22 it is seen that a peak current of 300 A is dissipated in the load. The power corresponds to 146 kW. This simulation shows that the inverter can start a 25 kW IM, which utilizes more than 100 kW at start-up. These simulations are verified in Chapter 4 by the high-power test. Figure 2-21 and Figure 2-22 show the three-phase output voltages as well as one single-phase current. The channel colours are the same as in Section 4.2.

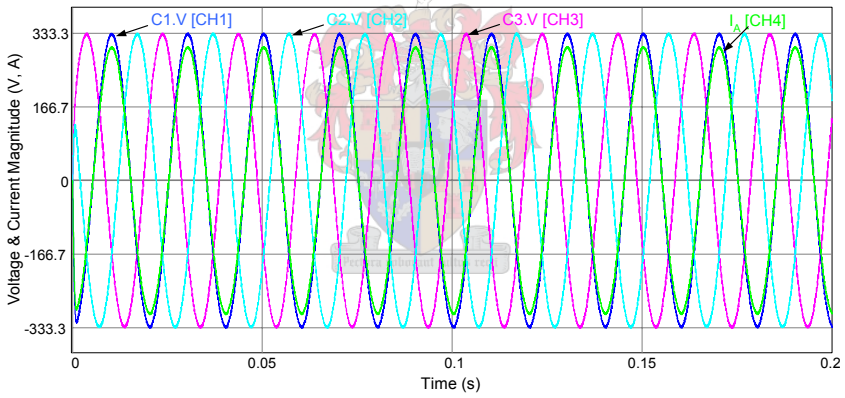


Figure 2-21: Output Waveform of the High-Power Simulation (200 ms)

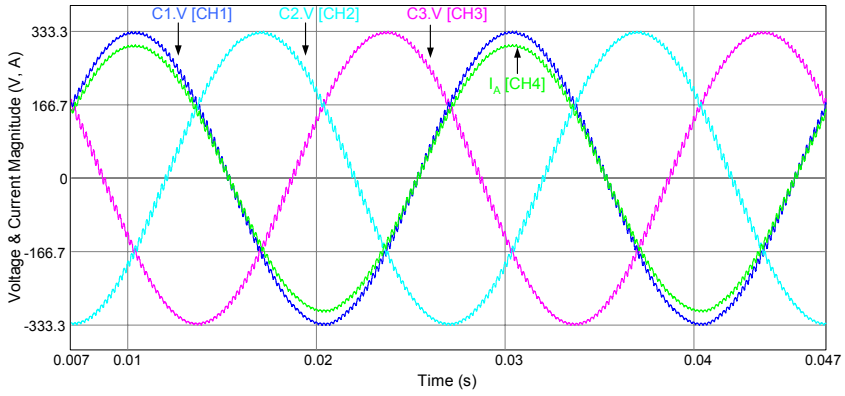


Figure 2-22: Output Waveform of the High-Power Simulation (40 ms)

2.7.6 Peak-Current Simulation

A very big load of R_{Load} = 0.7 Ω is connected to each phase of the inverter. This simulation was done to observe how the inverter responds to high currents. High starting currents are necessary to crank the IM at start-up. It is observed that a peak current of 470 A is drawn from the inverter. Figure 2-23 and Figure 2-24 represent the simulation output waveforms of the peak-current simulation. The phase voltages have RMS values of 230 V. The simulations are verified in paragraph 4.2.5 by Figure 4-9 (a) and Figure 4-9 (b).

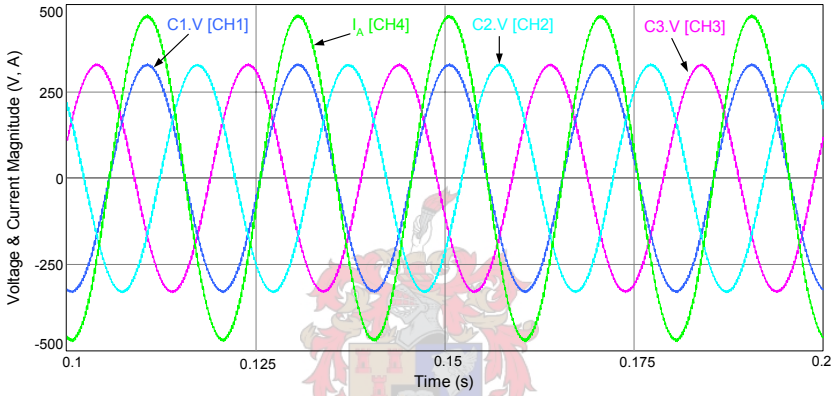


Figure 2-23: Output Waveform of the Peak-Current Simulation (100 ms)

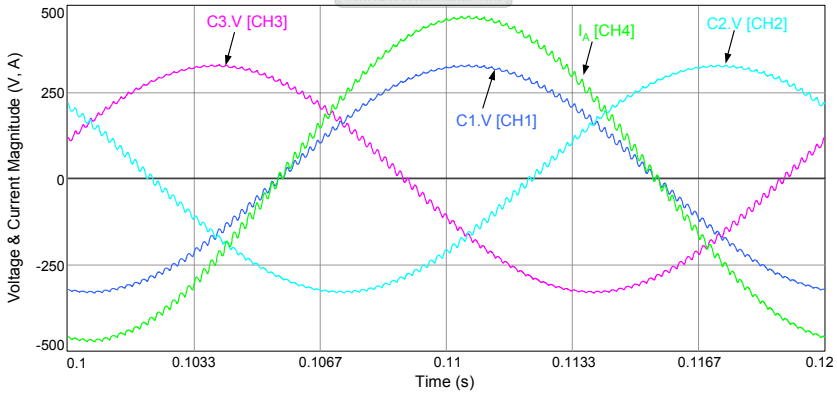


Figure 2-24: Output Waveform of the Peak-Current Simulation (20 ms)

2.7.7 IM Start-up Simulation

The start-up waveform in Figure 2-25 represents two phase voltages and a single-phase current. It is observed that the AC voltage magnitude drop a bit due to the high starting current.

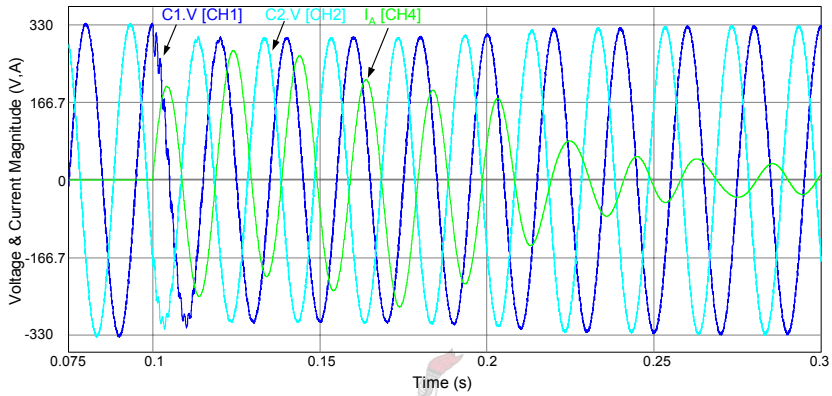


Figure 2-25: Simulation of the Start-up Waveform of IM

The current I_A is 90º out of phase with the voltage in phase A, as observed in Figure 2-25. This is due to the purely inductive load of the IM at start-up. A very bad power factor (pf) of 0 is noted in the phasor diagram of Figure 2-26. Figure 2-27 shows the three-phase current waveforms at start-up. A maximum current of 345 A is consumed by the IM at start-up in the simulation. This high starting current is necessary to crank the IM. Each IM is unique and thus consumes different starting currents. In later chapters it is noted that this peak current differs. Measurements on site revealed that a peak current of about 523 A is consumed at start-up. This was not known prior to design and construction.

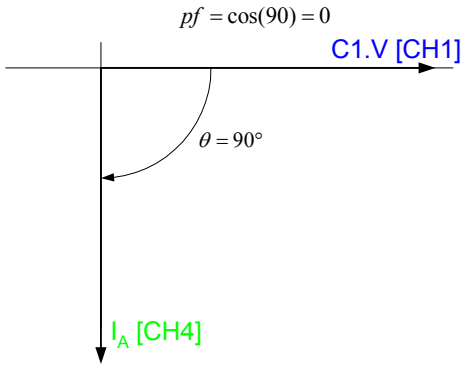


Figure 2-26: Phasor Diagram for a purely inductive load

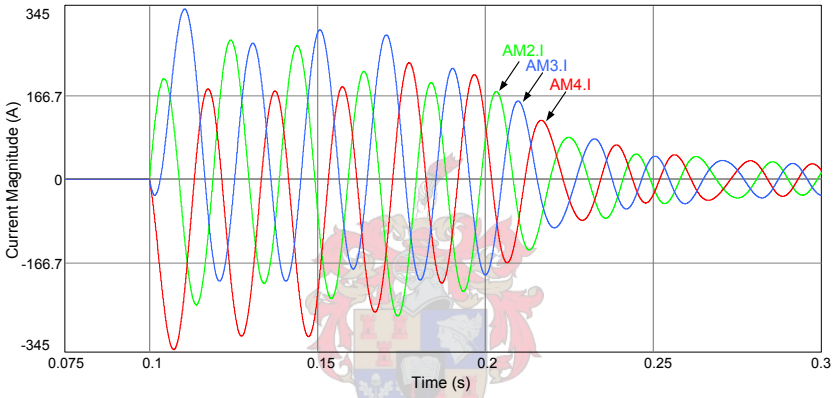


Figure 2-27: Zoom of Simulation of the Start-up Current Waveform of IM

Figure 2-28 shows the current waveforms including the start-up, motoring and generating regions. The IM initiates power generation at t = 0.5 seconds.

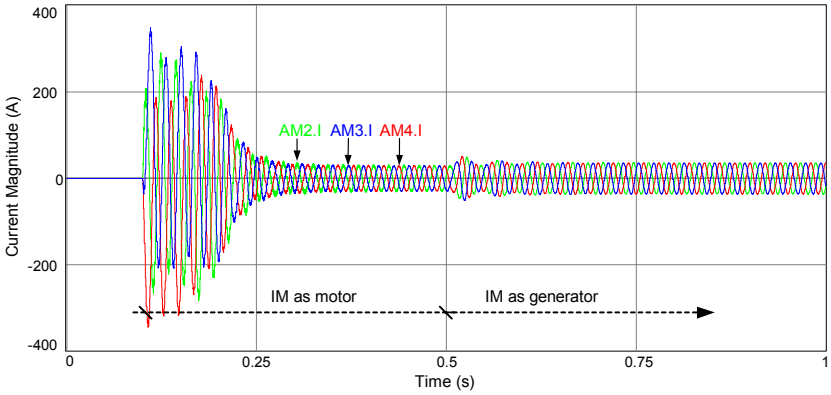


Figure 2-28: Simulation of the Start-up Current Waveform of IM

The power factor in an induction machine (over-excited) is always lagging, while the power factor in a synchronous machine (under-excited) can be varied from lagging to leading [28]. The lagging power factor of the induction machine is shown in the phasor diagram (Figure 2-31), which represent the phase current and voltage, while the IM operates as a motor and as a generator. Figure 2-29 shows the current and voltage waveform, while the IM functions as motor. The current (I_A [CH4]) lags the voltage (C1.V [CH1]) by 60.6˚. The power factor is 0.49, as shown in Figure 2-31. The power factor increases to 1 with an increase in IM speed, where the current lags the voltage by 90˚. With a further increase in speed the IM functions as a generator and the power factor decreases again. Figure 2-30 shows the simulation, where the IM functions as a generator, in which the current lags the voltage by 141˚. The diagram in Figure 2-31 demonstrates that a power factor 0.78 is achieved while the IM is generating power.

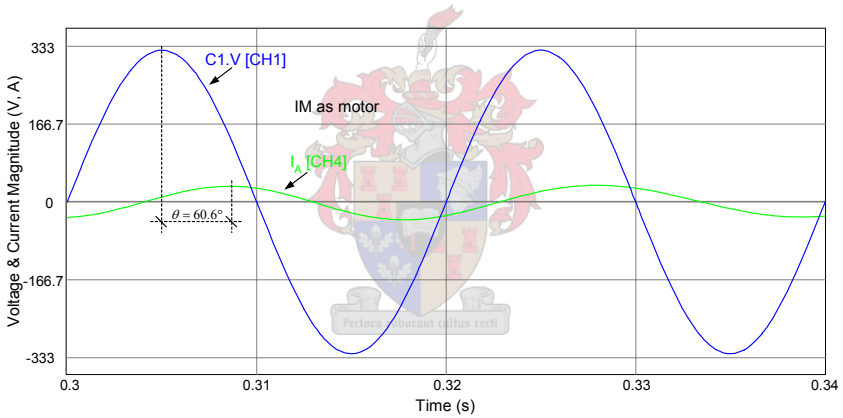


Figure 2-29: Current Lags Voltage for Motor Operation

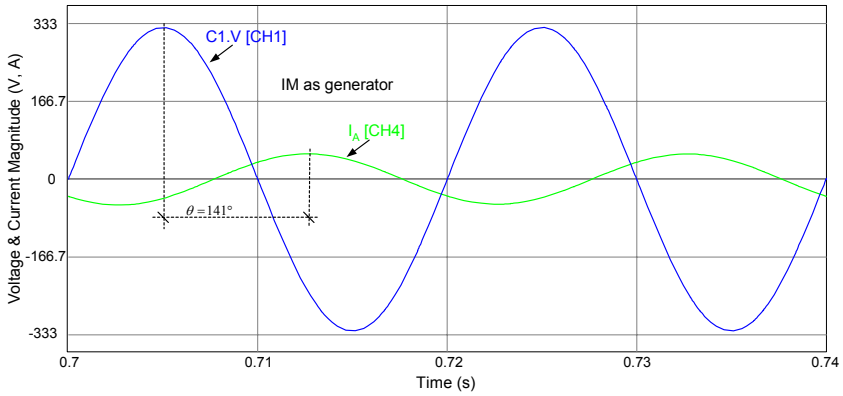


Figure 2-30: Current Lags Voltage for Generator Operation

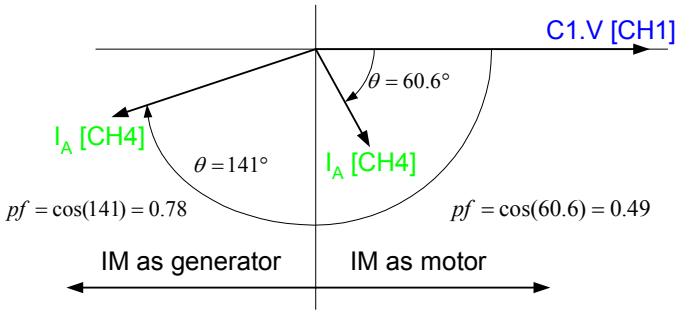


Figure 2-31: Phasor Diagram of the IM for Generating and Motoring Mode

Figure 2-32 gives an enlarged view of Figure 2-28, where the phase shift between motoring and generating mode is indicated. The current lags the voltage by 60.6˚ during motoring mode. The phase angle increases to 141˚ as soon as the IM functions as a generator.

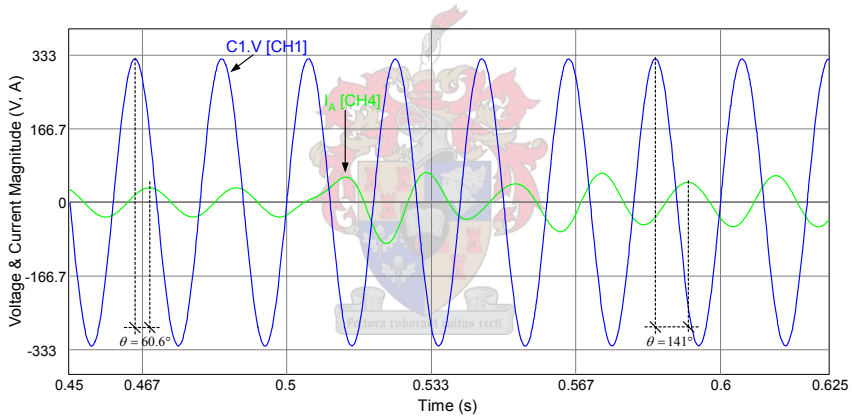


Figure 2-32: Current Lags Voltage for Shift between Motor and Generator Operation

Figure 2-33 shows the enlarged view of the AC currents where the IM functions as a generator.

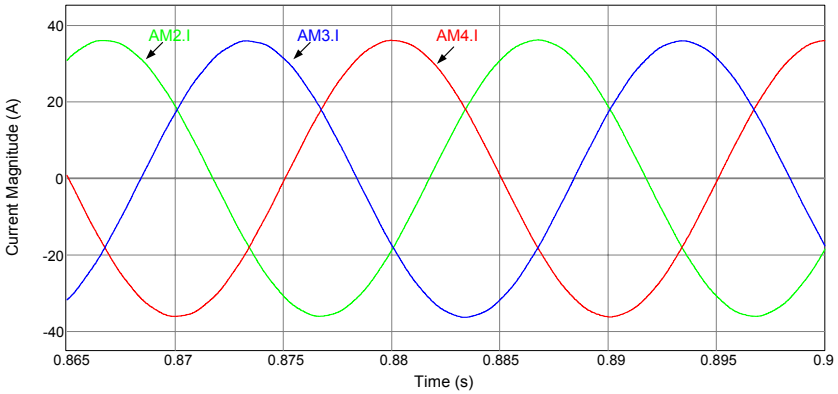


Figure 2-33: Simulation of the Power Generation Current Waveform of IM

Figure 2-34 shows the simulation of the power flow in the converter. A low pass filter is inserted in the simulations to overcome the high ripple harmonics which are present on the AC and as well on the DC side of the converter. The filtering of the signals provides good results for average power values. Peak values, however, are not precise due to filtering. Figure 2-34 and Figure 2-35 show the power of the SES (P_{SES}), the power that is dumped into the dump load (P_{DUMP}), the power of the batteries (P_{DC}) and the combined power value ($P_{DC} + P_{DUMP}$). P_{DUMP} is zero until the IM functions as a generator. $P_{DC} = P_{SES}$ until power is dumped at $t > 0.5$ seconds. At $t = 0.5$ s the IM functions as a generator and delivers power at 20 kW as seen in Figure 2-34 and Figure 2-35.

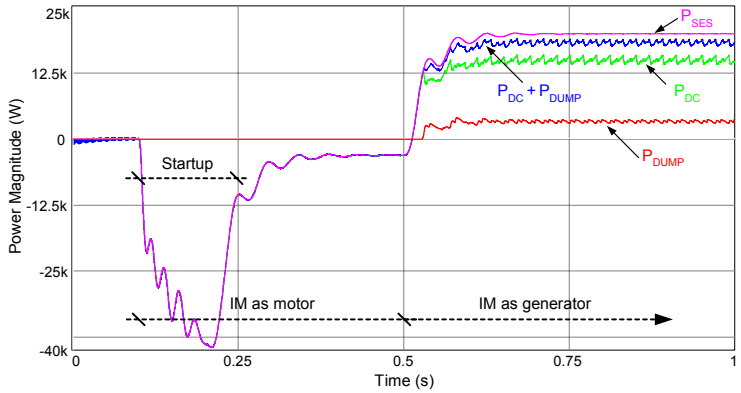


Figure 2-34: Simulation of the Power flow during Start-up, Motoring and Generating Mode

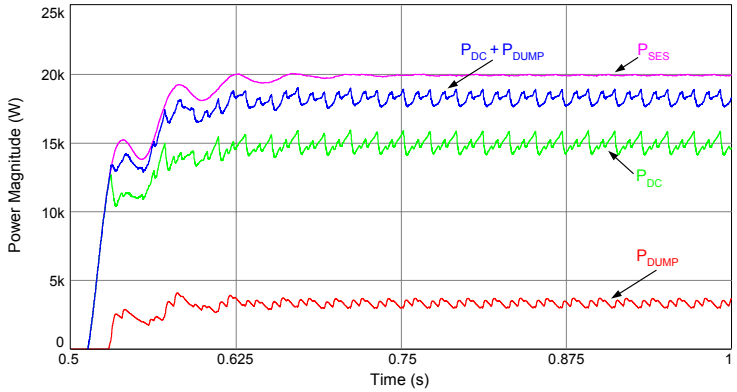


Figure 2-35: Simulation of the Power flow during Generation Mode

2.7.8 Voltage and Current Ripple Simulation

The magnitude of the ripple as well as the magnitude of the fundamental waveform is required to calculate the voltage and current ripple. The peak to neutral fundamental voltage and current magnitudes refer to Figure 2-19. The peak to neutral voltage is V_{PN} = 333 V and the peak to neutral current is I_{PN} = 70.85 A. Figure 2-36 gives an enlarged view of the waveforms in Figure 2-19. The current waveform (I_A) had to be scaled by 4 to get a better view. It is observed in Figure 2-36 that the voltage ripple is 10.5 V and the current ripple corresponds to 7.8/4 = 1.95 A. The percentage voltage ripple is calculated as follows:

$$\begin{aligned}\Delta V_{\%} &= 100 - 100\frac{V_{PN} - V_{Ripple}}{V_{PN}} \\ &= 100 - 100\frac{333 - 10.5}{333} \\ &= 3.15\%\end{aligned} \tag{2-4}$$

And the percentage current ripple corresponds to:

$$\begin{aligned}\Delta I_{\%} &= 100 - 100\frac{I_{PN} - I_{Ripple}}{I_{PN}} \\ &= 100 - 100\frac{70.85 - 1.95}{70.85} \\ &= 2.75\%\end{aligned} \tag{2-5}$$

Practical results in paragraph 4.2.6 confirm the simulations.

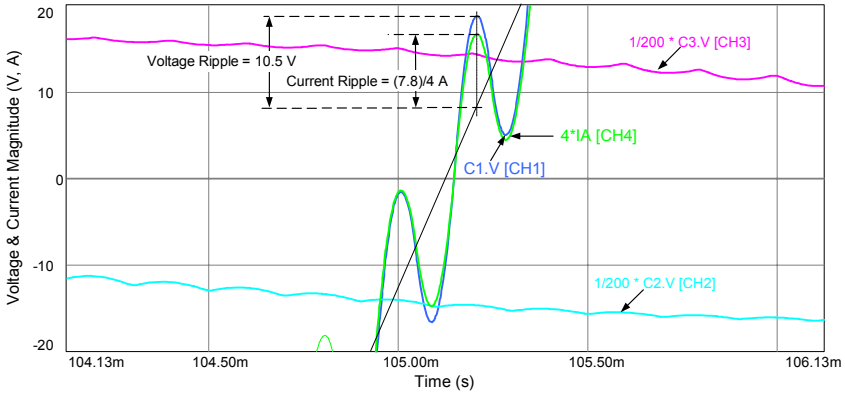


Figure 2-36: Voltage and Current Ripple Simulation

2.7.9 Load Management Simulation

The aim of the load management system is to dump all energy not utilized for battery charging to a dump load. The battery charge rate depends on the state of charge of the batteries. The charging procedure is explained in paragraph 3.6.2. The basic function of the load management system is to charge the batteries at 10 A, when the DC bus voltage is lower than 810 V. If the DC battery voltage is between 810 V and 830 V, the battery charge current is minimized to about zero.

2.7.10 Soft Start and Dump Simulation

The soft start simulation is shown in Figure 2-37, where it is seen that the DC capacitor ($V_{DC\ Bus\ Capacitor}$) voltage increases from 0 V to 746 V. The maximum current that flows through the soft start contactor (S. Soft Start) corresponds to 6.78 A. This current value is calculated with a resistor value of 110 Ω. The design of the soft start and dump circuit is given in Section 3.4. It is noticed, in Figure 2-37, that the soft start contactor is closed the instant the DC capacitor voltage increases, and that it is opened after the DC and AC contactors (S.DC & S.AC) are closed.

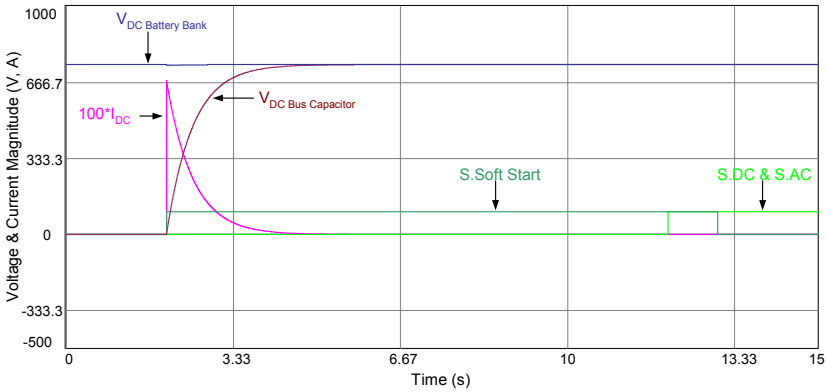


Figure 2-37: Simulation of the Soft Start routine

The converter needs to isolate itself from the high-voltage battery bank, as well as discharge the DC bus capacitors, when a fault arises. This is done by opening the DC and AC contactors and discharging the DC capacitors. Figure 2-38 represents the shutdown simulation of the system. As soon as the shutdown is initiated, the DC and AC contactors are opened. Hereafter the dump contactor is closed and thus discharges the capacitors as seen in Figure 2-38, denoted by the dump current (I_{Dump}).

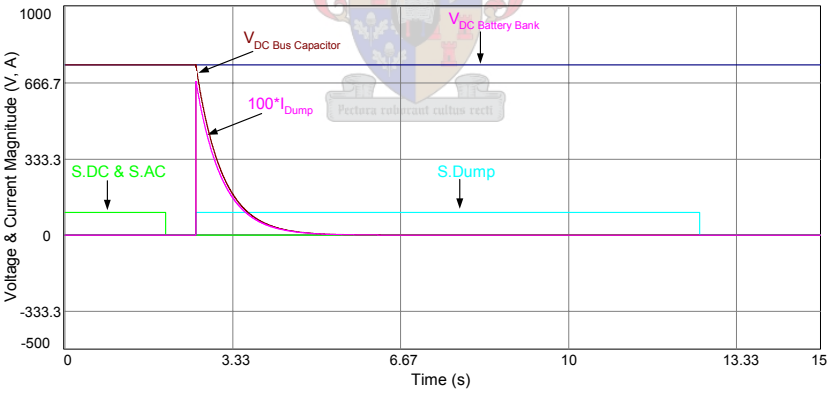


Figure 2-38: Simulation of the Shutdown routine

2.7.11 Component Values from Simulations

Table 1 summarizes the maximum voltage and current magnitudes resulted from the simulations. These values represent the minimum ratings of each component for the practical design.

Components	Peak Voltage (V)	RMS Voltage (V)	Peak Current (A)	RMS Current (A)
IGBT Module	900	800	350	36
Filter Inductors			350	36
Filter Capacitors	335	230		
DC Capacitors	900	800		
DC Contactor	900	800	350	33
Soft Start & Dump Contactor	900	800	7	1
AC Contactor	335	230	350	36

Table 1: Component Ratings Results from the Simulations

2.7.12 Conclusion

The simulations verified the functionality of the system, and revealed the component ratings. The simulation results revealed that the PWM converter system operates as an inverter, when a load is connected to the AC bus and as a rectifier when the battery bank is charged. The simulations revealed that the bidirectional converter could be developed practically and that the practical results should merge with the simulations. The component ratings of Table 1 are used as the minimum requirements in the next chapter, which focuses on the design of the AC bus converter system.

CHAPTER 3: DESIGN AND SYNTHESIS OF AN AC BUS CONVERTER SYSTEM

3.1 Introduction

Island grids and their topologies were discussed in the previous chapter. The final topology chosen was simulated as discussed earlier and results revealed that the design is capable of functioning as a standalone unit together with the "Stirling Energy System (SES) Integrated Solar Dish-Stirling Module" (Model DSSG-25-MKII) as an energy source. This chapter goes through the detailed steps of designing and practically manufacturing a three-phase bidirectional PWM converter. The topology in Figure 2-7 (a) is represented again in Figure 3-1, where it is subdivided into more detailed blocks. Each block characterizes a subsection of this chapter and is discussed separately.

The first subsection describes the system controller, which acts as the brain of the converter. The bidirectional power conversion unit, which converts AC to DC and visa versa, is controlled by the system controller as seen in Figure 3-1. The soft start and dump system together with the energy storage are connected to the DC side of the converter. The AC side entails the filter module, the load management system and the AC bus system. The AC bus system represents different AC loads as well as AC sources, such as the SES.

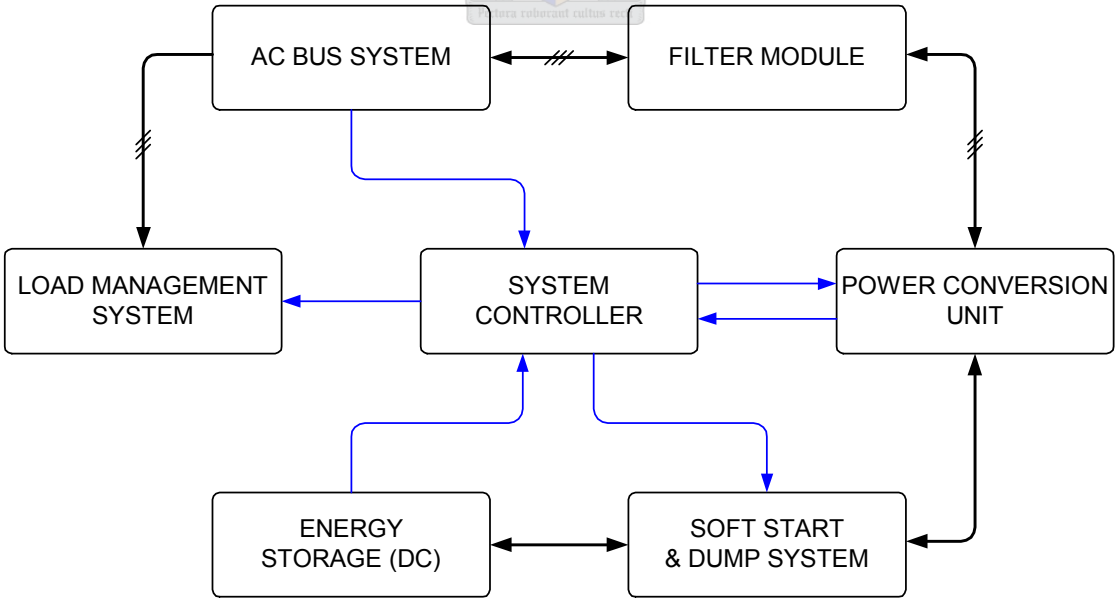


Figure 3-1: Block Diagram of the Bidirectional Converter

3.2 System Controller

The system controller is divided into three main parts. These are the power supply, DSP F2407 controller board and the interface board.

3.2.1 Power Supply

For the system to operate as a standalone unit, in an off-grid location, the system controller requires an initial power supply of 24 V DC before the AC bus is available. The controller receives its power from the AC bus once the unit has started up. Two 12 V DC batteries from the 750 V DC battery bank could be used as a power supply. This is, however, not an appropriate solution, since the two chosen batteries will be discharged more and thus could lead to unbalanced charging of the battery bank.

It is thus necessary to have a separate power source for the system controller to start up the unit. An uninterruptible power supply (UPS) is represented in Figure 3-2. This power supply consists of a 24 V DC switching power supply, a 24 V DC battery charger, two 12 V DC batteries connected in series and a relay.

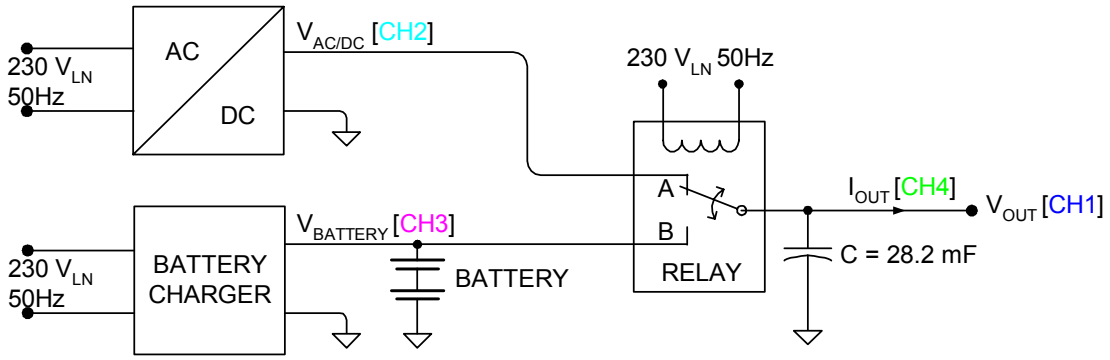


Figure 3-2: Diagram of the 24 V UPS

When no AC grid is available, the relay lever in Figure 3-2 is in position B. The output of the UPS ($V_{AC/DC}$ [CH2]) corresponds to the added battery voltage ($V_{BATTERY}$ [CH3]). During this mode the battery charger is deactivated, because of no AC grid voltage, and an internal diode ensures that no current flows towards the charger from the batteries. The switching power supply is also switched off. As soon as the AC grid is available, the internal AC coil of the relay is magnetized. This pulls the lever from position B to position A, thus connecting the switching power supply ($V_{AC/DC}$ [CH2]) to the UPS output (V_{OUT} [CH1]). This is observed in the graph of Figure 3-3. The batteries are now charged freely with the charger. The current consumption (I_{OUT} [CH4]) is higher than the maximum current consumption of 1.75 A as seen in Table 2, which is given at the end of this paragraph.

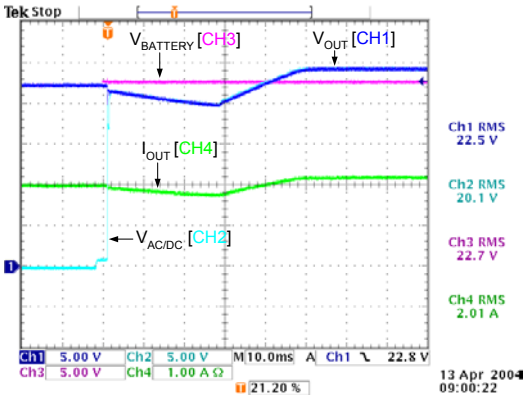


Figure 3-3: UPS output: Switch-over from Battery to Switching Power Supply

Another purpose of the UPS is to power the system controller when the AC grid fails. In this situation the relay lever moves from position A to position B. The output (V_{OUT} [CH1]) remains constant at a voltage of about 24 V DC. Figure 3-4 shows how the output voltage of the UPS behaves. The channels correspond to Figure 3-2. It is observed that the switching power supply voltage ($V_{AC/DC}$ [CH2]) does not drop down to zero the instant the relay switches over from position A to position B. This is because of the internal capacitors of the switching power supply that keep the voltage high for a split second. The relay connects the batteries to the output before the switching power supply voltage falls to zero.

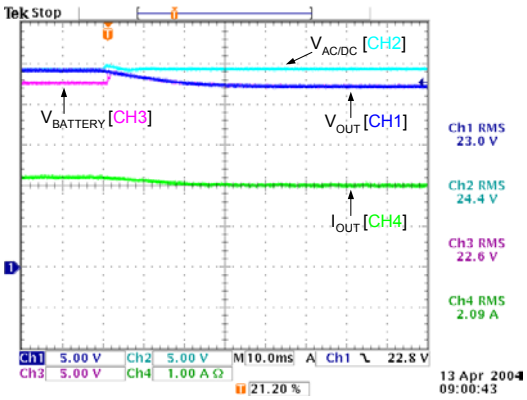


Figure 3-4: UPS output: Switch-over from Switching Power Supply to Battery

A voltage dip is prevented by making use of a smoothing capacitor. This capacitor size was calculated as follows.

Say that the voltage dip must not be bigger than 2.5 V in a time interval of 30 ms. The capacitor value is calculated with the help of the following equations.

$$\tau = R \cdot C \tag{3-1}$$

$$V_{out} - V_{drop} = V_{out} \cdot e^{\frac{-t}{\tau}} \tag{3-2}$$

It is given that:

$$V_{out} = 24 \text{ V}$$
$$V_{drop} = 2.5 \text{ V}$$
$$t = 30 \text{ ms}$$
$$R = 12 \ \Omega$$

This results in a capacitor value of:

$$C = 22.7 \text{ mF}$$

A capacitor value of 28.2 mF is chosen. The switching power supply used is a MEAN WELL S-150. It has an efficiency of 85% and features such as over-voltage and short-circuit protection. A MASCOT 3 step charger TYPE 9640 is utilized as the battery charger. It has three modes of charging. The boost mode charges the batteries at 0.8 A. At a battery voltage of 25 V DC the charger decreases the charging rate exponentially, thus corresponding to the timer mode, until the batteries reach their full capacity. A float

charge is applied to the batteries to ensure that the batteries remain charged. A LED indicates in which mode the charger is operating. The sealed lead-acid batteries have a low self-discharge rate and ratings of 7 Ah and 12 V DC. These rating provide enough energy for the system controller to start the system. Table 2 summarizes the currents consumed by the system controller during different modes of operation.

Situation	Contactor Closed	Operating Voltage (V)	Current consumption (A)
Standby	NONE	24	0.2
Start-up	S. SOFT START	24	0.4
Switch-over between start-up and continuous operation	S. SOFT START S. DC S. AC	24	1.75
Continuous operation	S. DC S. AC	24	1.65
Dump	S. DUMP	24	0.4

Table 2: Current Consumption by the System Controller

3.2.2 DSP F2407 Controller Board

Introduction

The controller board was previously designed [27] and constructed to function as a motor drive controller. Most of the existing features of the previous board were utilized and implemented to be useful in controlling the converter. Extra measurements and output signals had to be implemented which made it suitable as a feedback control system. The controller board comprises a DSP (Digital Signal Processor), an EPLD (Erasable Programmable Logic Device) and various drivers, power supplies and circuitry. All these components are mounted on a four-layer board.

The EPLD is used to combine logic states, such as IGBT errors and a temperature error signal, to provide a power-drive protection signal which protects the system from faults.

The DSP utilized in this design is a TMS320LF2407A [14] from Texas Instruments. This chip is optimized for digital motor control and power conversion applications. Some features of the TMS320LF2407A are listed below [14]:

1) High-performance static CMOS technology:
    - 25 ns instruction cycle time (40 MHz)
    - 40-MIPS performance
    - Low-power 3.3 V design;
2) On-chip memory
    - Up to 32 K words × 16 bits of flash EEPROM (4 Sectors) of ROM
    - Programmable "code security" feature for the on-chip flash/ROM
    - Up to 2.5 K words × 16 bits of data/program RAM
        - 544 words of dual-access RAM
        - Up to 2 K words of single-access RAM;
3) Boot ROM
    - SCI/SPI bootloader;
4) Two event-manager (EV) modules (EVA and EVB), each including:
    - Two 16-bit general-purpose timers
    - Eight 16-bit pulse-width modulation (PWM) channels which enable:
        - Three-phase inverter control
        - Centre- or edge-alignment of PWM channels
        - Emergency PWM channel shutdown with external /PDPINTX pin
    - Programmable Deadband (Deadtime) prevents shoot-through faults
    - Three capture units for time-stamping of external events
    - Synchronized A-to-D conversion;
5) External memory interfaces
    - 192 K word × 16 bits of total memory: 65 K program, 64 K data, 64 K I/O;
6) Watchdog (WD) timer module;
7) 10-bit analog-to-digital converter (ADC)
    - 8 or 16 multiplexed input channels

- 375 ns or 500 ns MIN conversion time
- Selectable twin 8-state sequencers triggered by two event managers;

8) Controller area network (CAN) 2.0 B module;
9) Serial communication interface (SCI);
10) 16-bit serial peripheral interface (SPI);
11) Up to 40 individually programmable, multiplexed general-purpose input/output (GPIO) pins;
12) Up to five external interrupts (power-drive protection, reset, two maskable interrupts).

The Code Composer Development Tool is used as programming platform. Code Composer can evaluate the performance of the processor, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. Programming of the DSP is done serially or with the help of a JTAG. A JTAG port allows the user to have almost full control over the DSP.

The next few sections demonstrate the functioning of the C program. The complete program is given in APPENDIX A. The code is clarified with flow diagrams.

Operating Overview

Figure 3-5 represents a block diagram of the system controller. The interface board is connected between the DSP F2407 controller board and the Semikron driver as observed in Figure 3-5. The basic function of the interface board is to function as a power supply to the Semikron driver as well as to the DSP F2407 board and to convert measurements as well as other signals as explained in paragraph 3.2.3.

The DSP has five input measurements as observed in Figure 3-5 and 6 PWM, 3 relay, 4 error LEDs and one load management output. The DC voltage measurement input is used to vary the modulation index used for pulse width modulation. This change in pulse-

width modulation modifies all 6 PWM outputs. The DC current measurement and DC voltage measurement are employed in the control of the load management system.

Paragraph 3.3.1 discusses the Semikron driver. The load management system is examined in Section 3.6.

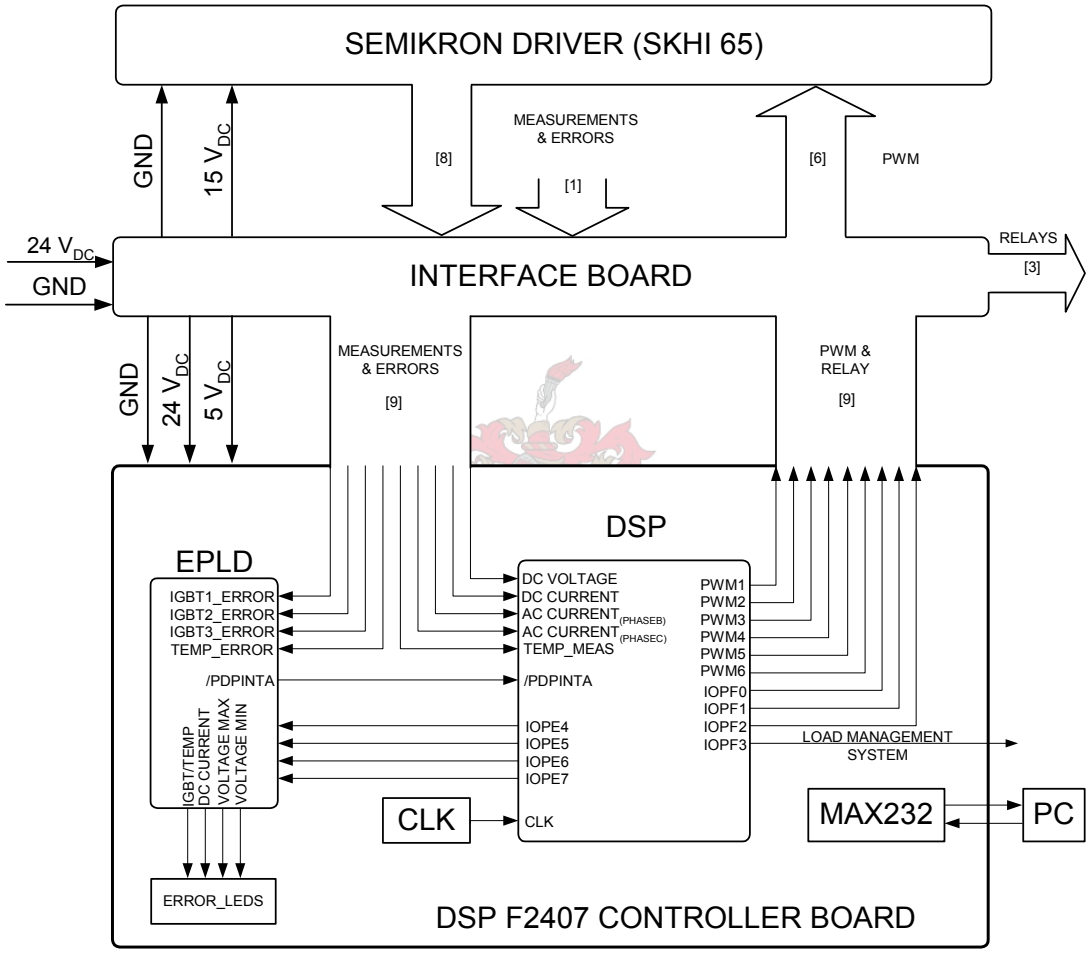


Figure 3-5: Block diagram of the System Controller

Main Program

When the system is manually turned "ON", the DSP starts off with the main program which is executed only once. The main program consists of the following subsequent routines as seen in Figure 3-6.

The first function "F2407_SYSTEM()"disables the Watchdog and enables the Event Managers as well as the A/D clock. Function "F2407_IO_SETUP()" sets up inputs and outputs to the DSP. Function "F2407_ADC()" maps the measured values, such as the DC voltage, to different channels which are then utilized in control algorithms. Three timers are set up in "F2407_TMR_PWM" to generate accurate timing which is used for PWM ("Timer1" 5 kHz), general timing ("Timer2" 305 Hz) and load management ("Timer4" 100 kHz). The initial values for the PWM signals are appointed.

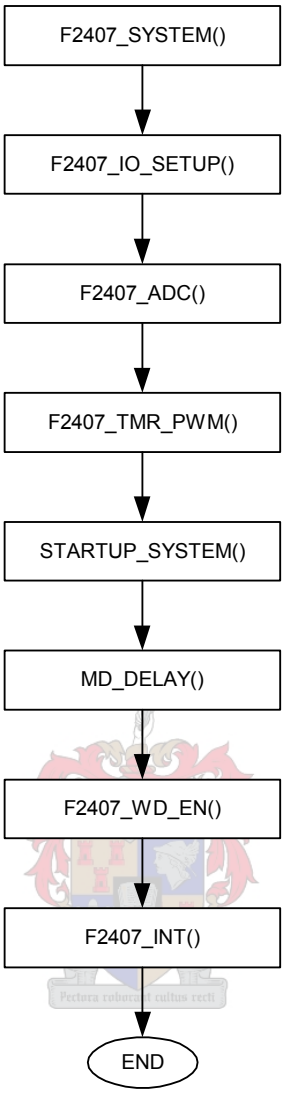


Figure 3-6: Flow Diagram of the Main Program

As soon as the above functions are completed the system starts up by the "STARTUP_SYSTEM()" routine. The main aim of the start-up procedure is to soft start the system to the battery bank as well as to connect the power conversion unit to the grid. This procedure is clarified in Section 3.4. The PWM compare operation is enabled after a small time delay ("MD_DELAY"). The last two procedures ("F2407_WD_EN" and "F2407_INT") enable the Watchdog and the interrupts.

Timer1 Period Interrupt

The Timer1 Period Interrupt is set up to 5 kHz. This means that the Timer1 Period Flag is set every 200 us. The flow diagram in Figure 3-7 represents the interrupt procedure. Each time the interrupt occurs, the functions are called consecutively. The Timer1 Period Flag has to be cleared each time the interrupt occurs.

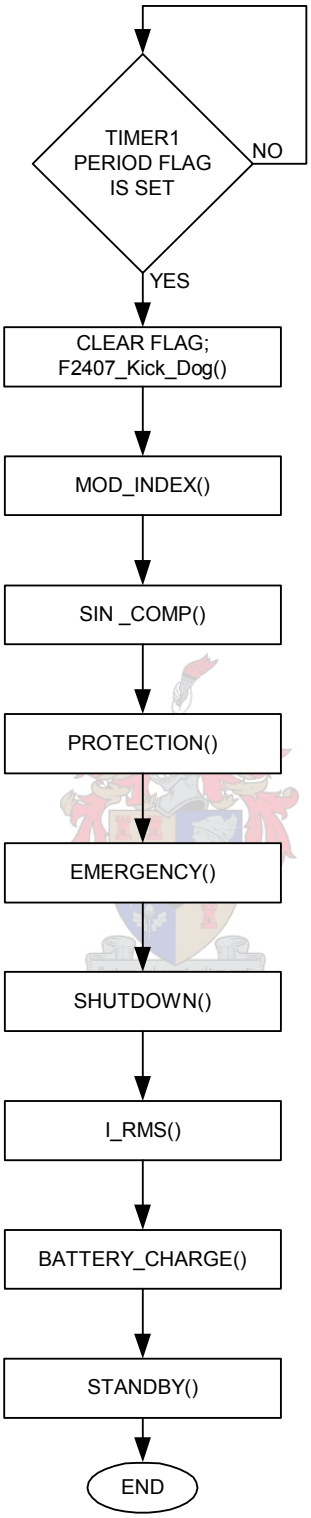


Figure 3-7: Flow Diagram of the INT1 routine

The modulation index value is calculated every 5 kHz during normal operation as observed in Figure 3-8. The system halts from normal operation when either SBF (Standby flag) is set, when the system is in standby mode, or the SDF (Shutdown flag) is set, when the system is in shut down mode. When one of the flags is set, the MOD_INDEX procedure does not calculate a new value for the modulation index. The modulation index (Ampl) is calculated using the following formula [5].

$$\text{Ampl} = \text{k} \cdot \frac{230}{\text{DCVal}} \tag{3-3}$$

The maximum value of "Ampl" corresponds to 1999; k is thus calculated so that an RMS AC output of 230 V is achieved with a minimum DC bus voltage of 650 V. Thus k = 5650. DCVal is the moving average of 30 samples of the DC battery bank voltage. A moving average DC voltage is taken to have a more stable value.

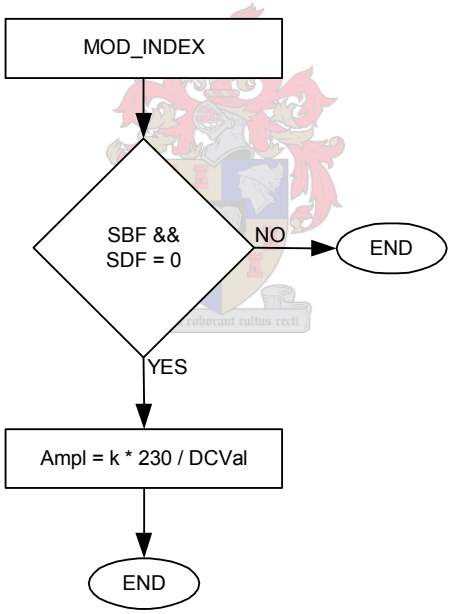


Figure 3-8: Flow Diagram of the MOD_INDEX routine

The objective of this three-phase PWM inverter, as seen in Figure 3-10, is to shape and control the three-phase output voltages in magnitude and frequency of 230 V and 50 Hz respectively with a phase difference of 120° to each other. The input DC voltage (V_d) of the inverter varies. To have balanced three-phase output voltages in a three-phase PWM inverter, the same triangular waveform is compared with three sinusoidal control

waveforms that are 120° out of phase, as shown in Figure 3-9 (a). Figure 3-9 (d) shows the filtered fundamental output voltage.

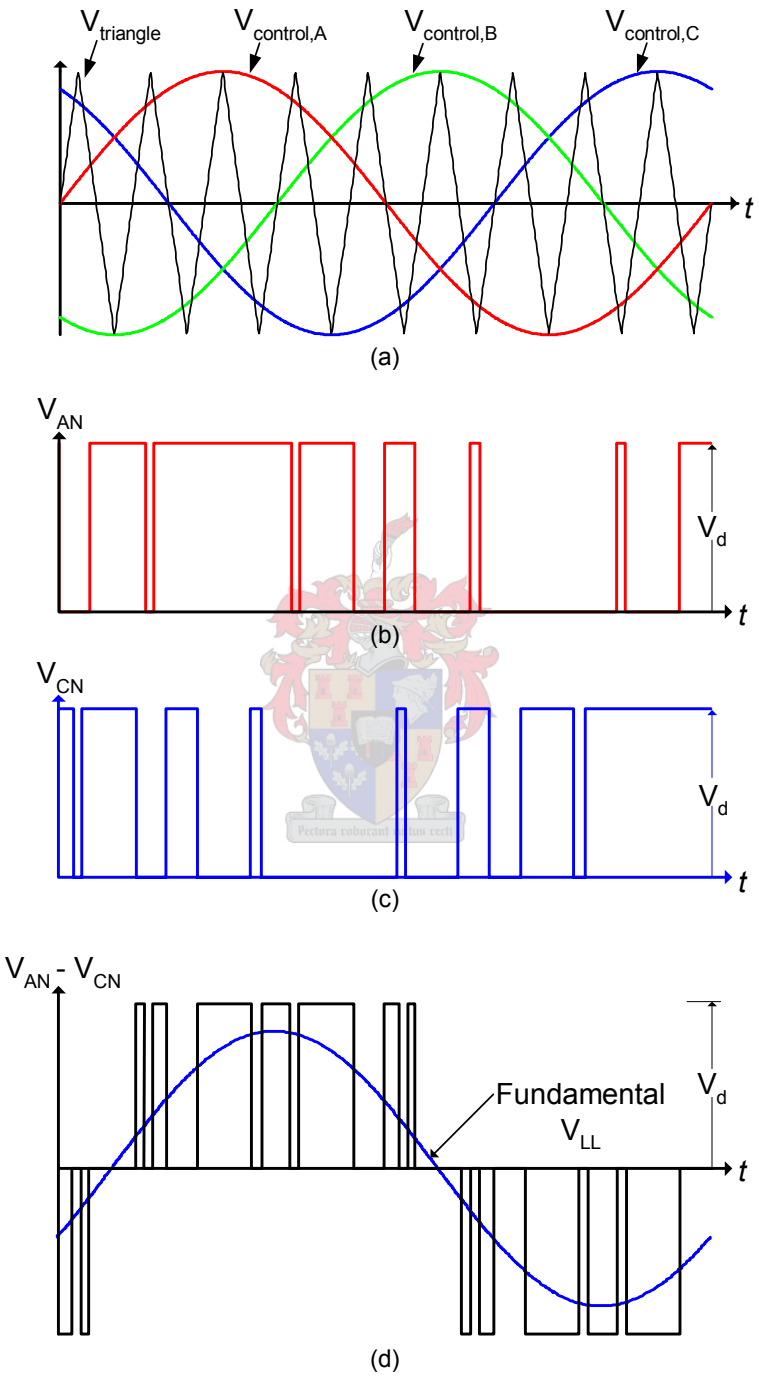


Figure 3-9: Three-Phase PWM Waveforms: (a) Control Voltages and Triangular Waveform; (b) Switching State V_{AN}; (c) Switching State V_{CN}; (d) Fundamental Voltage

The values of a sampled sinusoidal signal are placed in a look-up table which represents the control waveform. Three counters, 120° out of phase, are compared with the control voltage. The compared digital output voltage is fed to the gate of each IGBT via the interface driver. A predefined dead-band value ensures that the IGBTs in an IGBT pair are not switched on simultaneously.

The circuit configuration of the three-phase inverter in Figure 3-10 corresponds to the waveforms in Figure 3-9.

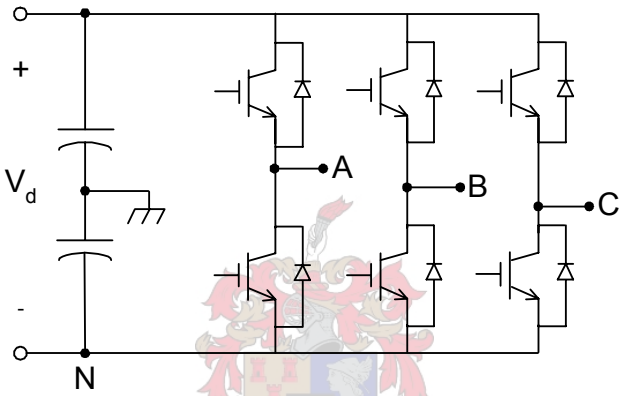


Figure 3-10: Circuit Configuration of a Three-Phase Inverter

The modulation index (Ampl) is used in the next function “SINE_COMP” to determine the switching states for each IGBT. The “Ampl” value is directly proportional to the control waveforms. This signifies that a decrease in the “Ampl” value decreases the control signal as well as the fundamental output voltage as seen in Figure 3-9 (d). The flow diagram of the PWM procedure is shown in Figure 3-11. It is observed that the switching states only change when the system is running under normal operation as explained earlier.

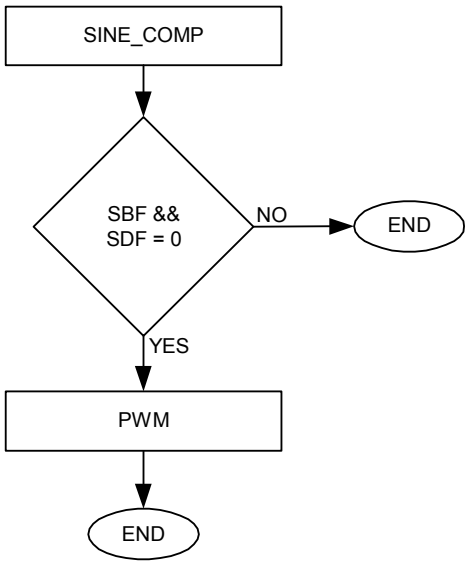


Figure 3-11: Flow Diagram of the SINE_COMP routine

When the converter is functioning under normal operation, providing the required AC output voltages and frequency, various measurements are taken for the sake of system protection. The system is protected against short-circuits, V_{CE} monitoring, AC over-current, over-temperature, DC over-voltage, DC under-voltage and DC over-current. The Semikron driver has internal protection features against short-circuits, AC over-current and over–temperature, and also V_{CE} monitoring. Measuring the DC battery bank voltage as well as the DC current enables the system to protect itself against DC over-voltage, DC under-voltage and DC over-current. Figure 3-12 shows the flow diagram of the code which protects the system from faults.

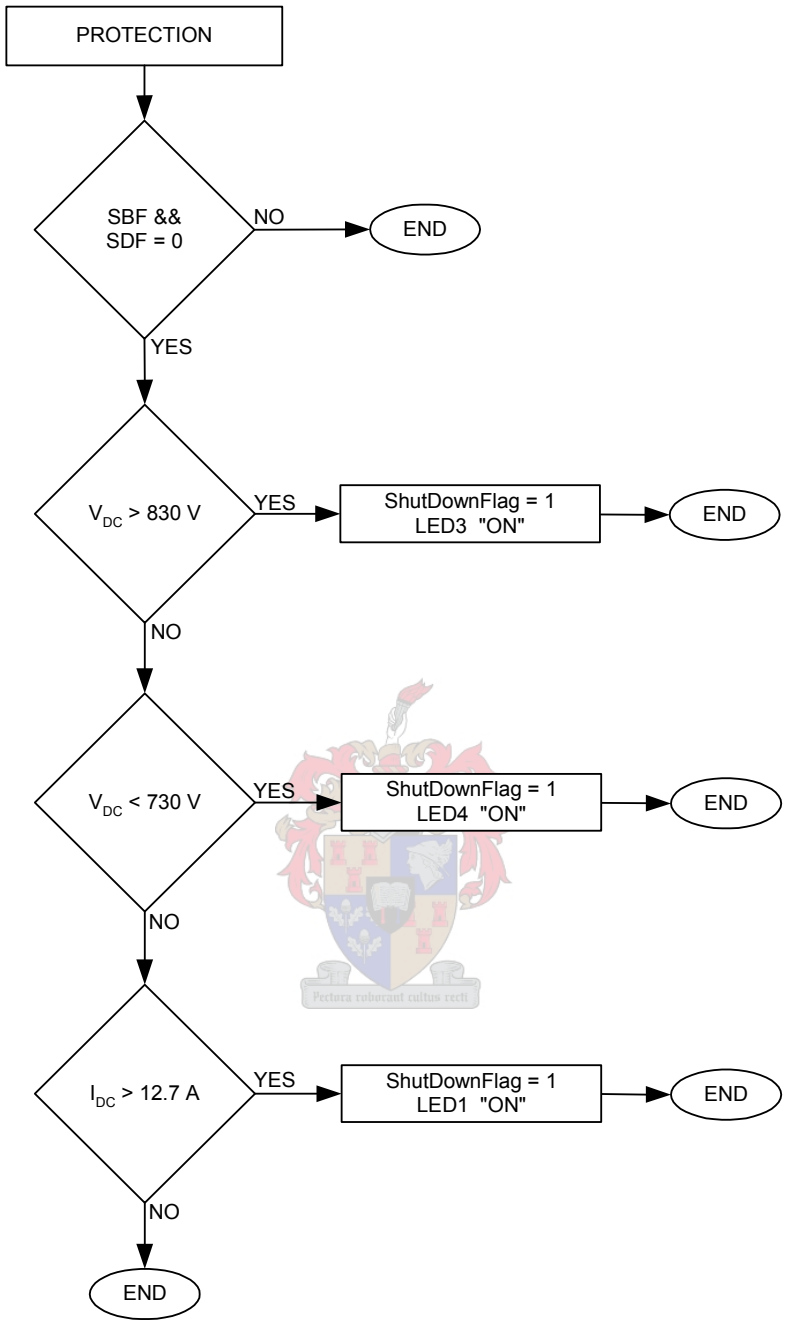


Figure 3-12: Flow Diagram of the System Protection routine

There are two main reasons why the system is shut down at a DC bus voltage of lower than 730 V DC.

1) A DOD greater than 40% reduces the batteries life time as shown in Figure 2-2;

2) The system must provide the required AC output voltage which is V_{LL} = 400 V and is represented with the following formula [5].

$$\begin{aligned} V_{LL1} &= \frac{\sqrt{3}}{\sqrt{2}} \cdot \left(\hat{V}_{AN} \right) \\ &= \frac{\sqrt{3}}{2 \cdot \sqrt{2}} \cdot m_a \cdot V_d \\ &\simeq 0.612 \cdot m_a \cdot V_d \qquad (ma \leq 1.0) \end{aligned} \tag{3-4}$$

The minimum DC battery voltage can now be calculated as follows.

$$\begin{aligned} V_d &= \frac{V_{LL1}}{0.612 \cdot m_a} \\ &= \frac{400}{0.612 \cdot 1} \\ &= 653.59 \text{ V} \end{aligned} \tag{3-5}$$

Each 5 kHz cycle the system checks if the DC battery bank voltage and the DC current are within a certain range. If the DC battery bank voltage is above or below a certain predefined limit, the SDF (Shutdown flag) is set and in turn shuts the system down by the SHUTDOWN() routine. The battery bank is charged at different charging rates, as discussed in paragraph 3.6.2. If, however, the charge current exceeds a certain limit, the system also shuts down. It can be noted, in Figure 3-12, that different LEDs are ignited for different errors. This is implemented so that faults are traced more easily.

The system is switched on or shut down manually by turning a switch, placed on the front of the panel, to its “ON” or “OFF” position respectively. The system inspects the position of the switch every 5 kHz cycle and responds to it. The “Shutdown flag” is set as soon as the switch is in its “OFF” position, which in turn shuts the system down. This is illustrated by the EMERGENCY routine in Figure 3-13.

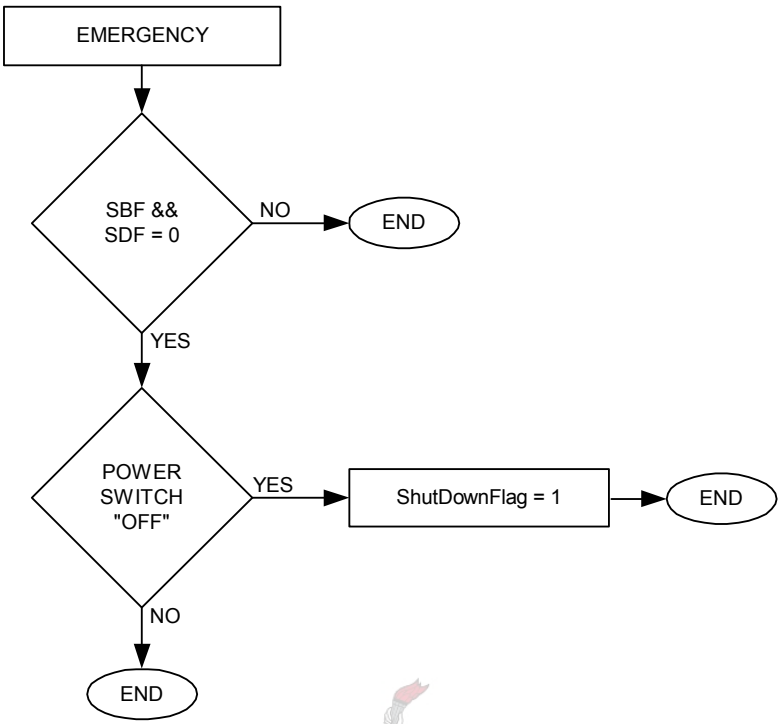


Figure 3-13: Flow Diagram of the EMERGENCY routine

The SHUTDOWN procedure is executed as soon as the SDF (Shutdown flag) is set by one or the other previously discussed routines. The first step is to set all 6 PWM outputs to high impedance, ensuring that all IGBTs of the converter are open. The second step is to isolate the converter from the battery bank as well as from the AC bus. This is done by opening the three-phase AC contactor and the DC contactor. The opening of the AC contactor is necessary, because the reverse diodes of the IGBT module still conduct electricity. The dump resistor burns if the SES generates and the system shuts down without opening the AC breaker. Figure 3-14 represents the sequence of the SHUTDOWN procedure. The DC capacitors are discharged through a dump resistor after the system is isolated from the rest. The dump contactor is closed for 10 seconds and then opened again. This time interval ensures that the DC capacitors are totally discharged and that the system is secure.

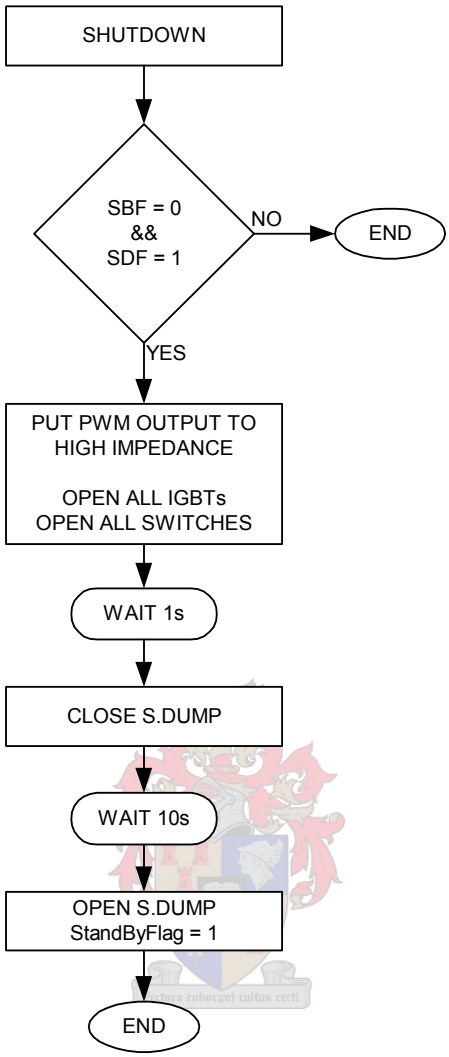


Figure 3-14: Flow Diagram of the SHUTDOWN routine

A SBF (Standby flag) is set, as seen in Figure 3-14, which places the system in a standby mode. In this mode no other operations are performed until the user resets the system manually. This course of action is denoted in Figure 3-15. The Shutdown flag is cleared so that the system does not shut down a second time. If the system shuts down, because of a protection error, the power switch on the front of the box is still in its “ON” position.

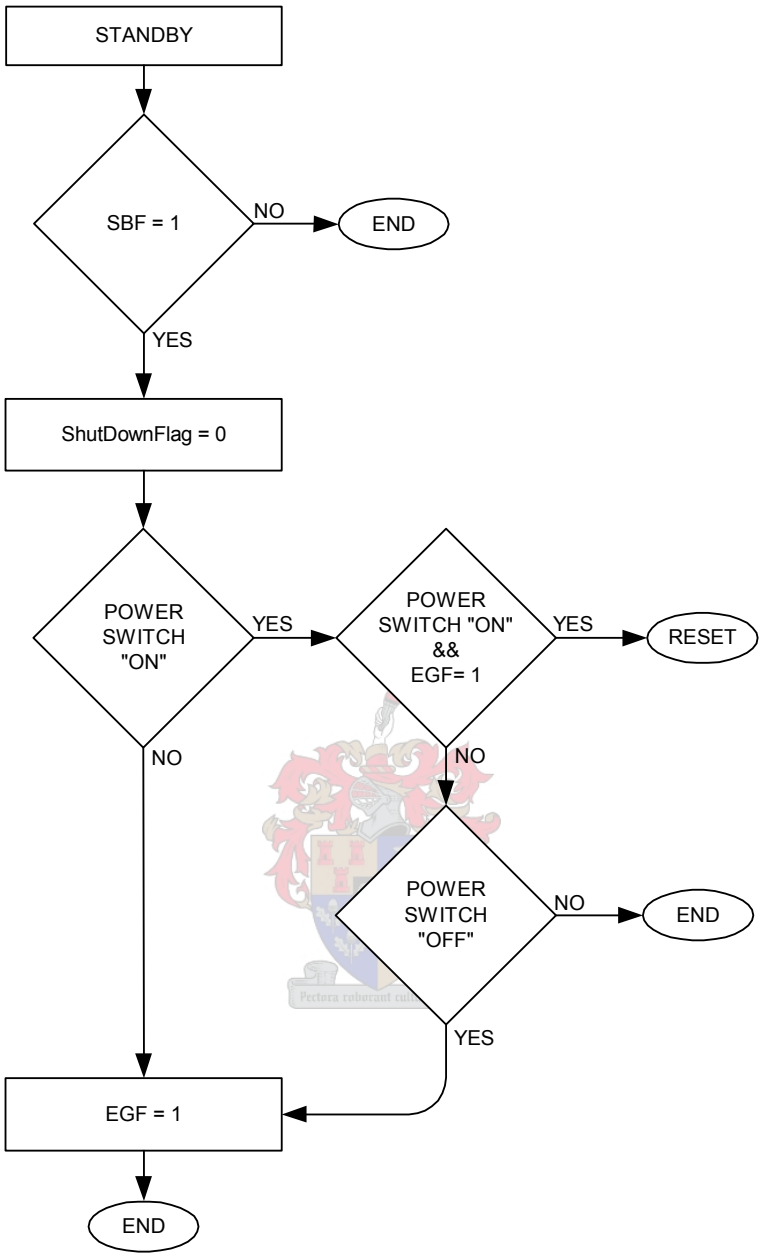


Figure 3-15: Flow Diagram of the STANDBY procedure

To make sure that the system stays shut down, an EGF (Emergency flag) must be set. This flag is set only if the POWER SWITCH is turned to its “OFF” position, as seen in Figure 3-15. To power up the system, the POWER SWITCH is turned to its “ON” position. Now the EGF is set and the POWER SWITCH is in its “ON” position and a “reset” of the system occurs. All flags are reset to their original values by the DSP. The system starts off with the main program, as discussed at the beginning of this section. The

POWER SWITCH is in its "OFF" position if the system is shut down manually. EGF is set automatically. Switching the system on results in a "reset", as seen in Figure 3-15, and program operation restarts at the main function.

3.2.3 Interface Board

An interface board was developed to match the Semikron driver with the DSP controller board. Another purpose of the interface board is to supply power to the DSP board and the Semikron driver board. Figure 3-16 gives an overview of the interface board. The next few paragraphs briefly describe how each building block of the interface board functions.

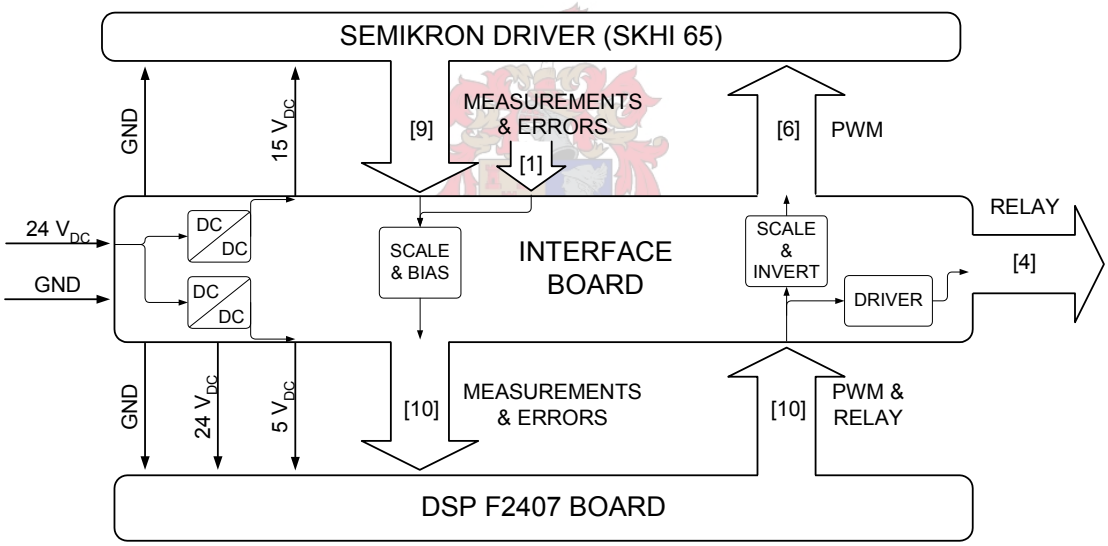


Figure 3-16: Diagram of the Interface Board

DC / DC Converters

The UPS provides the input power to the interface board. This 24 V DC is converted to +5 V DC and +15 V DC to suit the DSP and the Semikron drivers respectively. The part-numbers of the converters used are MEAN WELL SDM30-24S5 and SDM30-24S15,

which are 30 watt DC to DC converters with efficiencies of 79% and 83% respectively. Figure 3-17 shows how these converters are configured. With switches S1 and S2 the DC/DC converters are turned on or off. These switches are represented by the dip switch on the PCB. The variable resistor, connected to the "TRIM" input, is used to fine-tune the output voltage of the DC/DC converter. Capacitors (C13 and C14) are inserted to stabilize the output voltages.

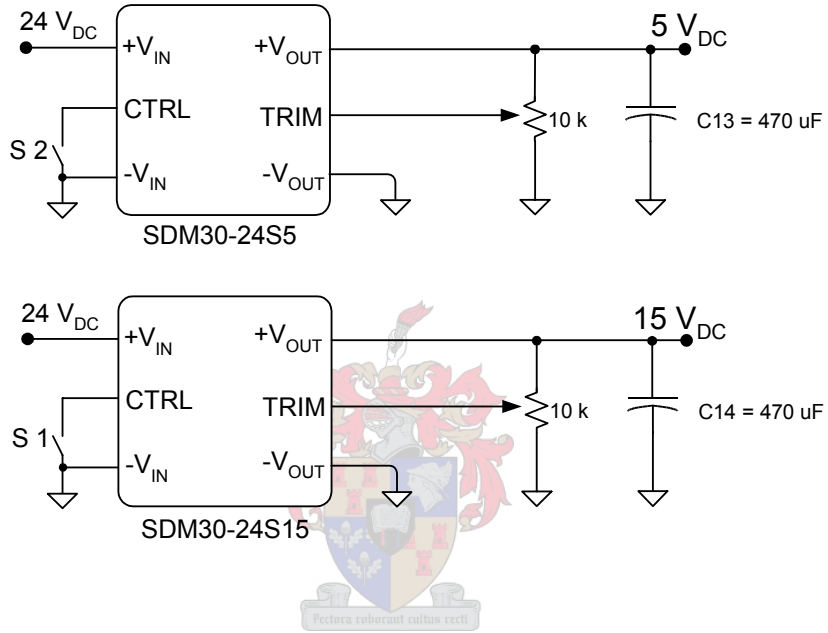


Figure 3-17: Diagram of the DC/DC Converters

Measurements and Errors

The Semikron driver senses voltages, currents and error signals that are employed in the design. These signals are listed below:

- Phase current measurements;
- DC link voltage sensing;
- Temperature-sensing;
- Three IGBT error signals;
- One over-temperature error.

The temperature-sensing feature was not utilized in the design. The phase current measurements are scaled and biased to be useful in the DSP. Figure 3-18 represents the circuit. The Semikron driver provides an output voltage for the measured current (see paragraph 3.3.1). A 10 V reference output voltage refers to the over-current trip level [19], as seen in Table 3. A transfer function for Figure 3-18 is realized with the following few steps. From the specification of the SKHI 65 [16] it is concluded that the voltage given by the current measurement ($V_{B\ MEASURE\ IN}$) is represented by the following equation:

$$V_{B\ MEASURE\ IN} = 10 \cdot \frac{I_{AC\ ACTUAL}}{I_{TRIP}} \tag{3-6}$$

$I_{AC\ ACTUAL}$ is the actual current in the specific phase, and I_{TRIP} corresponds to the trip level setting [16]. The equivalent resistance (R_{IN}), in Figure 3-18, is much larger than the voltage divider network consisting of R12 and R11. This means that nearly no current flows towards R_{IN}.

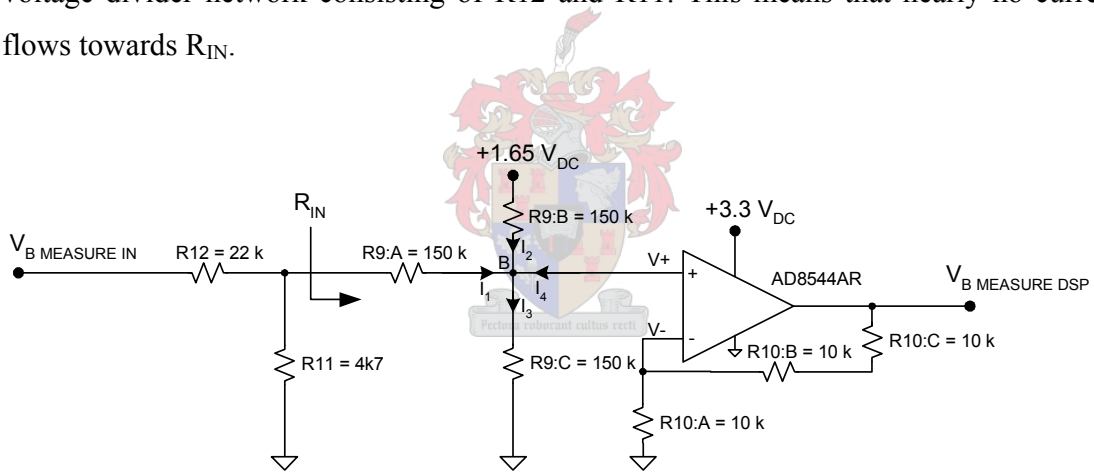


Figure 3-18: Biasing and Scaling of the AC Current

The voltage across R11 is calculated as follows:

$$V_{R11} = \frac{V_{B\ MEASURE\ IN} \cdot R11}{R11 + R12} \tag{3-7}$$

Using Kirchhoff's current law [18] at node B, in Figure 3-18, which states that the total charge flowing into a node must equal the total charge flowing out of the node, at node B in Figure 3-18:

$$I_3 = I_1 + I_2 + I_4 \tag{3-8}$$

The currents are calculated as follows:

$$I_1 = \frac{V_{R11} - V+}{R9:A} \tag{3-9}$$

$$I_2 = \frac{1.65 - V+}{R9:B} \tag{3-10}$$

$$I_3 = \frac{V+}{R9:C} \tag{3-11}$$

$$I_4 = 0 \tag{3-12}$$

Substituting equations (3-9), (3-10), (3-11) and (3-12) into (3-8) results in the transfer function between V_{R11} and V+ (note that R9:A = R9:B = R9:C.):

$$V+ = \frac{1}{3} \cdot \left(V_{R11} + 1.65\right) \tag{3-13}$$

The gain of the operational amplifier circuit is:

$$G = 1 + \frac{R10:B + R10:C}{R10:A} = 3 \tag{3-14}$$

Finally the total transfer function is concluded from equations (3-7), (3-13) and (3-14):

$$V_{B\ MEASURE\ DSP} = V_{B\ MEASURE\ IN} \cdot \left(\frac{R11}{R11 + R12}\right) + 1.65 \tag{3-15}$$

It is seen that, when an input voltage of 10 V is applied, the output voltage is 3.3 V. The circuit in Figure 3-18 was simulated in PSpice and the simulation is shown in Figure 3-19. The output $V_{B\ MEASURE\ DSP}$ is biased at a DC level of 1.65 V as seen at the dotted green line.

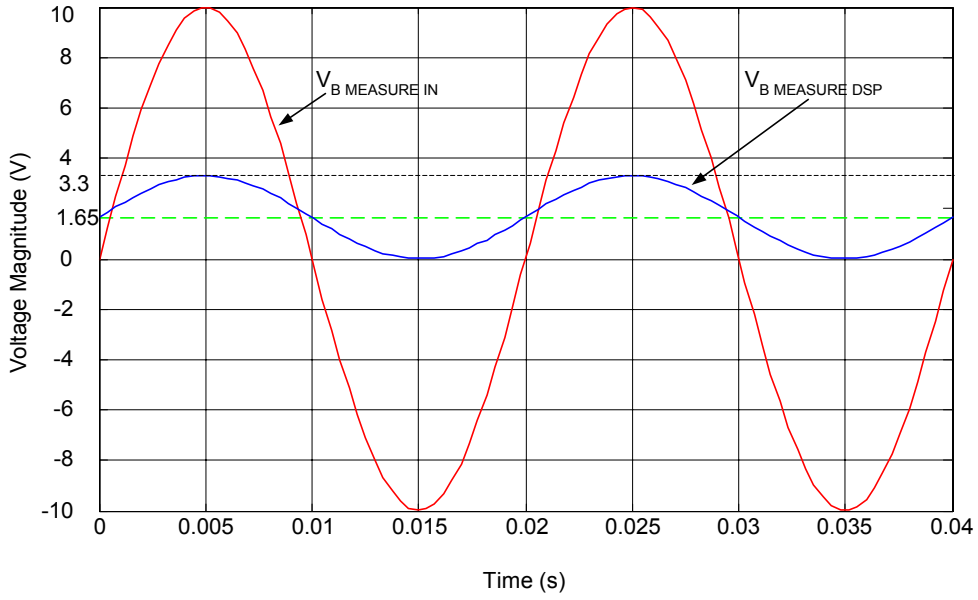


Figure 3-19: Simulation of Biasing and Scaling of the AC Current

Finally, to get a relationship between the $V_{B\ MEASURE\ DSP}$, in decimal figures, and $I_{AC\ ACTUAL}$, in amperes, equations (3-6) and (3-15) are combined to obtain:

$$V_{B\ MEASURE\ DSP}\ (dec) = \left(1.76 \cdot \frac{I_{AC\ ACTUAL}}{I_{TRIP}} + 1.65\right) \cdot \frac{1024}{3.3} \qquad (3\text{-}16)$$

This equation is used to calculate the voltage drop over the filter inductors when a large amount of AC current is drawn from the system. Compensation for the voltage drop over the inductors is important, if the system output voltage needs to be very stable.

DC Current Measurement

Measuring the DC current is necessary to control the battery bank charging current which is used for the load management control system. This current is measured with an external current sensor, which is directly connected to the interface board. The current sensor is a LEM LA205-S, which requires two supply voltages (+15 V and -15 V) and provides a measure signal. The +15 V and -15 V supply voltages are tapped off from the Semikron driver. The DC current must be measured very accurately. The maximum current that should flow into a battery must be smaller than 10% of its rated ampere-hour

rating. This is a precaution that must be considered so as not to harm the batteries. Figure 3-20 shows the circuit which converts the measured DC current from the current sensor to a voltage that is utilized in the DSP.

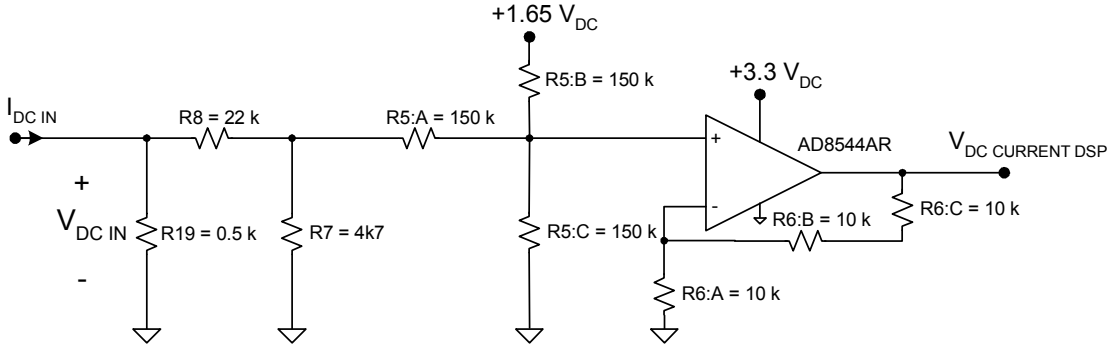


Figure 3-20: Biasing and Scaling of the DC Current

The transfer function for Figure 3-20 is the same as in Figure 3-18, given by:

$$V_{DC\ CURRENT\ DSP} = V_{DC\ IN} \cdot \left(\frac{R7}{R7 + R8} \right) + 1.65 \tag{3-17}$$

where only the resistor names differ and the input voltage $V_{DC\ IN}$ is given as:

$$V_{DC\ IN} = 500 \cdot I_{DC\ IN} \tag{3-18}$$

The 0.5 kΩ resistor is chosen so that a voltage of -10 V to +10 V is generated by the measured DC current. 10% of a 102 Ah rated battery corresponds to a charging current of 10.2 A DC. Both negative and positive currents are measured in the range -12.7 A DC to +12.7 A DC. This is done to get a very fine scale necessary for good control. Equation (3-19) shows the relationship between the actual DC current and the measured DC current:

$$I_{DC\ IN} = I_{DC\ ACTUAL} \cdot \frac{1}{2000} \cdot N \ , \ where\ N = 3. \tag{3-19}$$

N is the number of turns around the current sensor and 1/2000 is the turn ratio of the current sensor itself. $I_{DC\ IN}$ ranges between -19.05 mA DC and +19.05 mA DC. Combing equations (3-17), (3-18) and (3-19) leads to a relationship between $I_{DC\ ACTUAL}$ and $V_{DC\ CURRENT\ DSP}$:

$$V_{DC\ CURRENT\ DSP} = \frac{I_{DC\ ACTUAL} \cdot 3}{2000} \cdot 500 \cdot \left(\frac{R7}{R7 + R8}\right) + 1.65 = \frac{I_{DC\ ACTUAL}}{7.57} + 1.65 \quad (3\text{-}20)$$

This voltage is represented as a decimal value by:

$$V_{DC\ CURRENT\ DSP}\ (dec) = \left(\frac{I_{DC\ ACTUAL}}{7.57} + 1.65\right) \cdot \frac{1024}{3.3} \quad (3\text{-}21)$$

The circuit in Figure 3-20 is simulated in PSpice to verify accuracy. The simulated output is represented in Figure 3-21. $V_{DC\ CURRENT\ DSP}$ voltage is at 1.65 V when the input voltage $V_{DC\ IN}$ equals zero voltage, as seen in Figure 3-21.

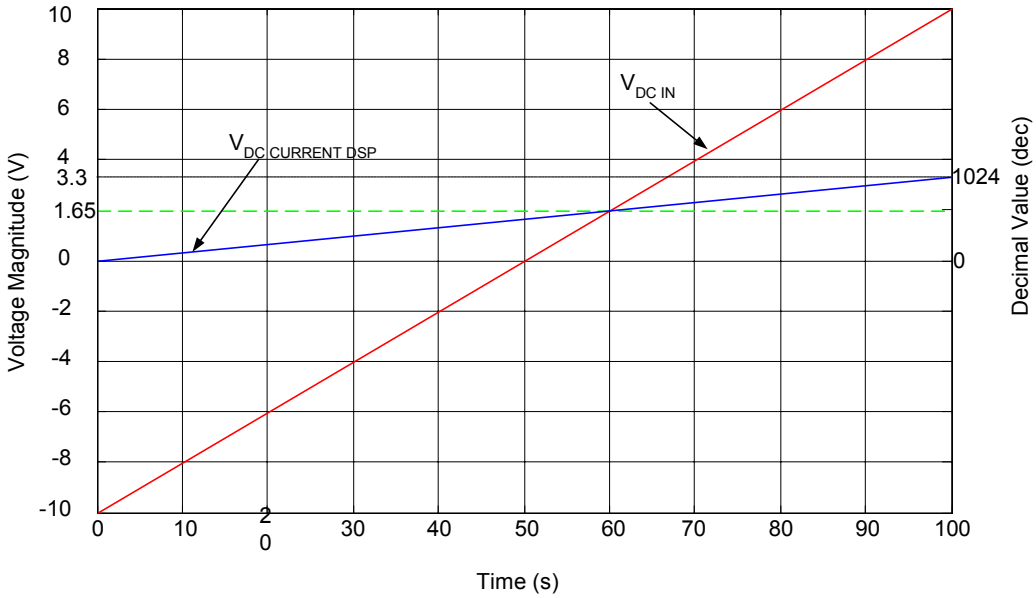


Figure 3-21: Simulation of Biasing and Scaling of the DC Current

DC Link Voltage Sensing

An important measurement is the DC link voltage sensing. This measurement is used to calculate the modulation index, which determines the AC output voltage magnitudes of the three-phase converter. The modulation index is expressed by the following equation [5]:

$$m_a = \frac{Vout}{\frac{U_{DC\text{-}Bus}}{2}} \tag{3-22}$$

The DC link voltage value from the Semikron driver is represented by the following formula:

$$U_{DC\ ANALOG} = \frac{U_{DC\text{-}Bus}}{100} \tag{3-23}$$

1000 V on the DC bus results in a voltage of 10 V on the Semikron driver output. This 10 V DC signal must now be scaled to be utilized in the DSP. The circuit for scaling the signal is shown in Figure 3-22 .

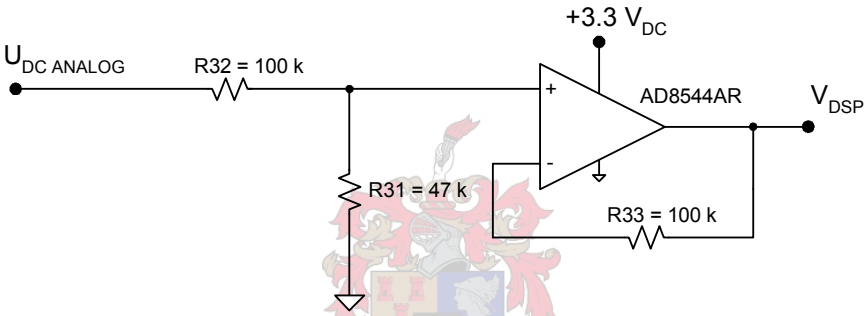


Figure 3-22: Scaling of the measured DC Bus Voltage

The AD8544AR operational amplifier ensures that the input to the DSP is never greater than 3.3 V DC. This operational amplifier has a supply voltage of 3.3 V DC. A resistor divider network scales 10 V to 3.3 V. The transfer function for the circuit in Figure 3-22 is:

$$\frac{V_{DSP}}{U_{DC\ ANALOG}} = \frac{R31}{R31+R32} = \frac{47}{147} = 0.32$$
$$V_{DSP} = 0.32 \cdot U_{DC\ ANALOG} \tag{3-24}$$

A relationship between the actual DC bus voltage and the voltage that is utilized by the DSP is achieved by combining equation (3-23) and equation (3-24). This equation follows:

$$V_{DSP} = \frac{0.32}{100} \cdot U_{DC\text{-}bus} \tag{3-25}$$

IGBT and Over-Temperature Error

The Semikron driver provides an error signal for each IGBT pair (top and bottom). This error signal is set high when an internal V_{CE}, over-current protection (OCP) or temperature fault occurs. These protection signals are used to stop the converter from switching. The three phase error signals and the temperature error signal are open collector outputs of the driver. This means that an external pull-up resistor is necessary for them to function properly. Figure 3-23 shows the diagram. The four error signals are fed into the EPLD, where they are combined with an expression represented by an OR gate. The output of the OR gate is connected to the Power Drive Protect (/PDPINTA) pin of the DSP. This /PDPINTA bit is bit 0 of the EVA interrupt mask register A. This /PDPINTA external interrupt has the highest priority [15]. When this bit is cleared, the PWM output pins are disabled. PWM pins are set to high impedance and the converter stops switching.

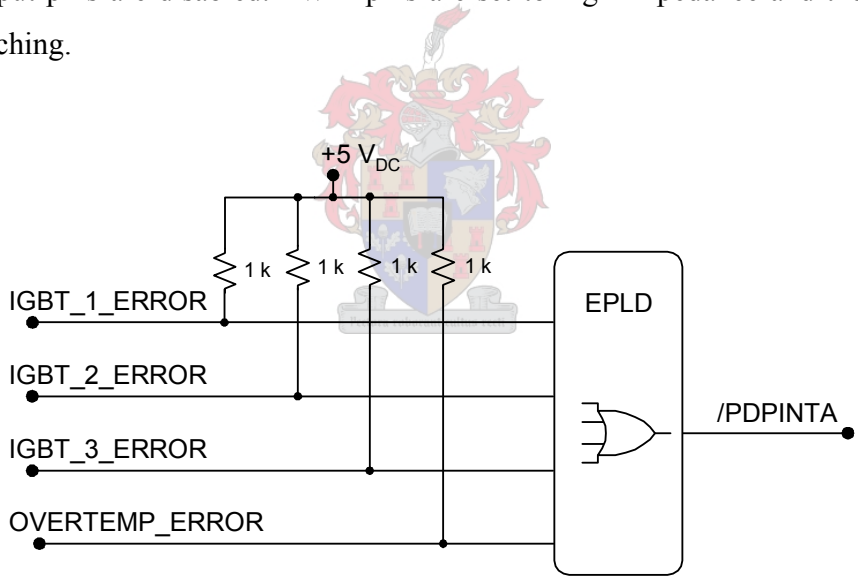


Figure 3-23: Power Drive Protect Circuit

PWM

The on and off levels of the PWM signals from the DSP controller board are 0 V and 3.3 V respectively. The turn-on gate voltage ($V_{G\ (on)}$) of the Semikron driver must be greater than 13.1 V and the turn-off gate voltage ($V_{G\ (off)}$) must be smaller than 3.1 V [19] for the driver to recognize the switching states correctly. This means that the PWM signals have

to be scaled to match the Semikron driver. Figure 3-24 shows how the PWM signals are pulled up to 15 V. When the DSP is powered up, or resets, it sets all of its outputs high (3.3 V) for a split second. A short-circuit occurs when all gate voltages of the IGBTs are high. The top and bottom IGBT of a module may never be switched on at the same time. This implies that the PWM signals have to be inverted to overcome the problem. Figure 3-24 illustrates the scaling and inverting of PWM signals. A driver (SN75451D) for each PWM signal had to be inserted so that the current through the resistor (10 kΩ) has a path to ground.

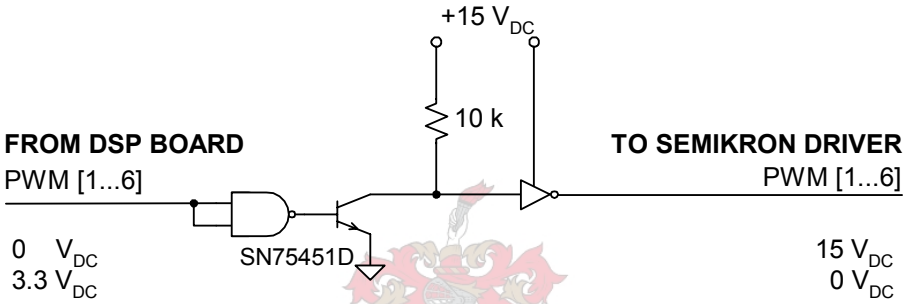


Figure 3-24: Scaling & Inverting of PWM Signals

Relay Driver

AC and DC contactors are necessary for the unit to soft start as well as isolating itself when a fault arises. If a fault occurs and the system must shut down, the contactors disconnect the converter from the battery bank as well as from the AC bus. These relays need to be controlled from the DSP. Figure 3-25 shows the relay driver. Three output pins of the DSP are used as control signals for four relays. The relays consume a current of 0.07 A DC when operating from 24 V DC. Thus an IRF540N MOSFET, with a current and voltage rating of $I_D = 33$ A and $V_{DS} = 100$ V respectively, is a good choice. When pin IOPF0 is at 0 V, the relay is turned on, and vice versa.

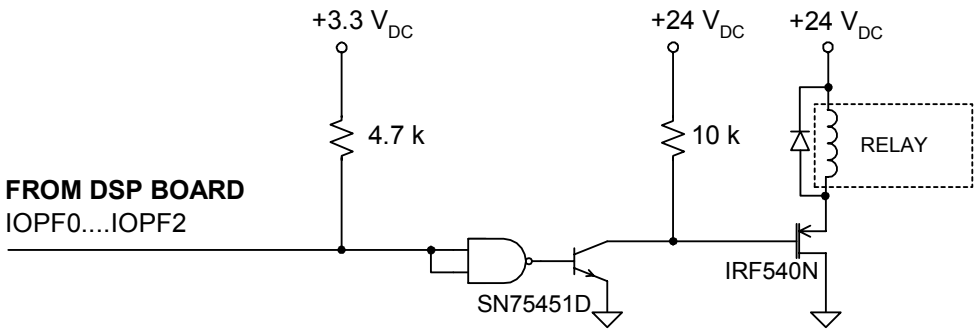


Figure 3-25: Relay Driver

3.3 Power Conversion Unit

The power conversion unit consists of three main parts, namely the Semikron driver SKHI 65, the IGBT module with its heat-sink, and the DC bus and snubber capacitors. These are discussed in the next few sections.

3.3.1 IGBT Module Driver

The SKHI 65 is a six-pack gate driver suitable for SKIM®5 IGBT modules manufactured by Semikron. It has features such as [16]:

- CMOS compatible inputs;
- Wide range power supply;
- V_{CE} monitoring;
- Short-circuit protection;
- Over-current protection;
- DC-link voltage detection;
- Temperature sensing;
- Under-voltage monitoring;
- DC bus voltage of up to 1200 V DC;
- Separate interfaces to connect external phase current sensors.

This driver is mounted onto the SKIM module. For the over-current protection to be enabled, it is necessary to connect external phase current sensors with a turns ratio of 1:2000. The LA 205-S current transducers [17] are utilized. Figure 3-26 shows how the current sensors are connected to the driver. Each sensor has a +15 V DC and -15 V DC supply. The measured value is available at the third pin.

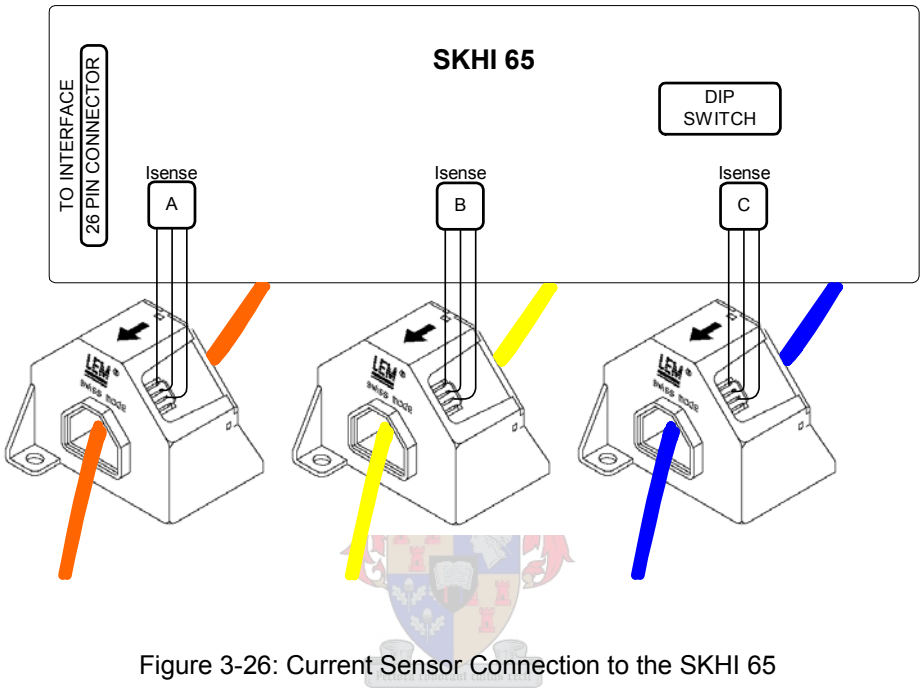


Figure 3-26: Current Sensor Connection to the SKHI 65

The over-current trip level is selected via the settings of the dipswitch, as seen in Table 3. The maximum over-current trip level of 723.8 A refers to 10 V, for measuring purposes, as seen in Table 3 indicated by the red region. The blue region, in Table 3, signifies the over-current factor for the module (SKIM500GD128DM) employed.

If the AC output current is higher than a maximum permissible value, according to the trip level setting in Table 3, the IGBTs are immediately switched off and switching pulses from the controller are ignored.

DIP Setting Please note: 0 = on; 1 = off					turns ratio 1:2000	overcurrent trip level	SKiM400GD063D	SKiM400GD128D	SKiM500GD128DM	SKiM250GD174D
					lanalogOUT		Ic = rated current [A] @ Theatsink = 25°C	Ic = rated current [A] @ Theatsink = 25°C	Ic = rated current [A] @ Theatsink = 25°C	Ic = rated current [A] @ Theatsink = 25°C
DIP 4	DIP 5	DIP 6	DIP 7	DIP 8	[mV / A]	[A]	overcurrent factor	overcurrent factor	overcurrent factor	overcurrent factor
0	0	0	0	0	13,82	723,8	1,65	2,07	1,61	2,90
1	0	0	0	0	14,42	693,5	1,58	1,98	1,54	2,77
0	1	0	0	0	15,15	659,9	1,50	1,89	1,47	2,64
1	1	0	0	0	15,76	634,6	1,44	1,81	1,41	2,54
0	0	1	0	0	16,64	600,9	1,37	1,72	1,34	2,40
1	0	1	0	0	17,25	579,8	1,32	1,66	1,29	2,32
0	1	1	0	0	17,98	556,1	1,26	1,59	1,24	2,22
1	1	1	0	0	18,59	538,0	1,22	1,54	1,20	2,15
0	0	0	1	0	19,65	508,8	1,16	1,45	1,13	2,04
1	0	0	1	0	20,26	493,6	1,12	1,41	1,10	1,97
0	1	0	1	0	20,99	476,4	1,08	1,36	1,06	1,91
1	1	0	1	0	21,60	463,0	1,05	1,32	1,03	1,85
0	0	1	1	0	22,48	444,8	1,01	1,27	0,99	1,78
1	0	1	1	0	23,09	433,2	0,98	1,24	0,96	1,73
0	1	1	1	0	23,82	419,8	0,95	1,20	0,93	1,68
1	1	1	1	0	24,42	409,4	0,93	1,17	0,91	1,64
0	0	0	0	1	25,65	389,8	0,89	1,11	0,87	1,56
1	0	0	0	1	26,26	380,9	0,87	1,09	0,85	1,52
0	1	0	0	1	26,99	370,5	0,84	1,06	0,82	1,48
1	1	0	0	1	27,59	362,4	0,82	1,04	0,81	1,45
0	0	1	0	1	28,48	351,1	0,80	1,00	0,78	1,40
1	0	1	0	1	29,08	343,8	0,78	0,98	0,76	1,38
0	1	1	0	1	29,82	335,4	0,76	0,96	0,75	1,34
1	1	1	0	1	30,42	328,7	0,75	0,94	0,73	1,31
0	0	0	1	1	31,49	317,6	0,72	0,91	0,71	1,27
1	0	0	1	1	32,09	311,6	0,71	0,89	0,69	1,25
0	1	0	1	1	32,83	304,6	0,69	0,87	0,68	1,22
1	1	0	1	1	33,43	299,1	0,68	0,85	0,66	1,20
0	0	1	1	1	34,32	291,4	0,66	0,83	0,65	1,17
1	0	1	1	1	34,92	286,4	0,65	0,82	0,64	1,15
0	1	1	1	1	35,66	280,5	0,64	0,80	0,62	1,12
1	1	1	1	1	36,26	275,8	0,63	0,79	0,61	1,10

Table 3: Over-Current Trip Level Setting

3.3.2 IGBT Module and Heat-Sink Design

The IGBT module implemented is a SKIM500GD128DM, part of the SKIM®5 range manufactured by Semikron. This module has 6 IGBTs connected, as seen in Figure 3-27. A big advantage of an IGBT is that it requires only a small amount of energy to switch the device. This is due to its high impedance gate.

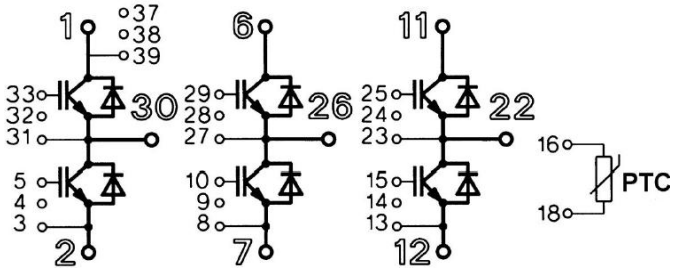


Figure 3-27: Configuration of IGBT Module [19]

Pins 1, 6 and 11 are connected to the positive side of the DC battery bank. Pins 2, 7 and 12 represent the negative terminal of the battery bank. Pins 30, 26 and 22 represent phase A, B and C respectively. Each IGBT pair is switched independently of the other. The PWM driver signal for each IGBT is connected to its base, which has pin numbers of 33, 5, 29, 10, 25 and 15. Each IGBT pair, top and bottom, may never be switched on simultaneously. This will result in a short-circuit between the positive and the negative battery terminal.

This module has been chosen since it is capable of handling very high peak currents of 723 A [16]. The module suits the voltage and current requirements. It can handle a DC link voltage of 1200 V. Another big advantage is that is uses the existing SKHI 65 driver, which has important features, as discussed in the previous section. The ratings of this module are greater than those required in Table 1.

Each IGBT pair is fitted on a copper base plate which has a very good heat transfer coefficient. The whole module is fitted onto a heat-sink with forced air cooling. The size of a heat-sink is calculated by using the following formula:

$$R_{sa} = \frac{T_{s(\max)} - T_a}{P_D} \tag{3-26}$$

R_{sa} is the thermal resistance between the sink (heat-sink) and the ambient. The objective is to find the required R_{sa} for a given power loss (P_D) and then estimate the area of the heat-sink, with the help of a table. Figure 3-28 shows an electrical equivalent circuit for the heat flow from the device to the ambient. $T_{s\,(max)}$, from Figure 3-28, is the maximum temperature of the sink and T_a is the ambient temperature. P_D is the total power dissipated in the module by all IGBTs and diodes.

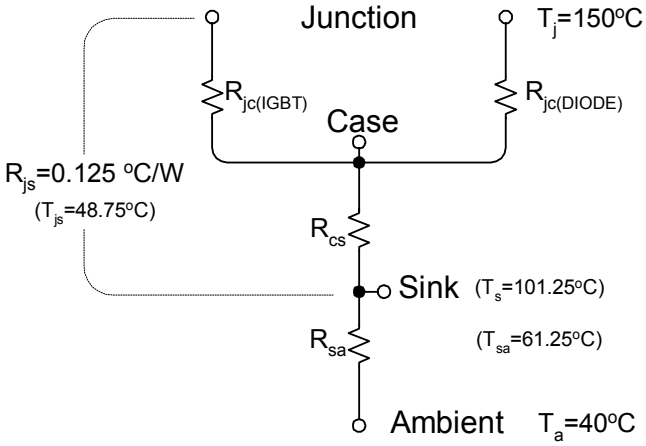


Figure 3-28: Electrical Equivalent Circuit for Heat Flow from Device to the Ambient

A few calculations are necessary to find the power (P_D) dissipated in the module. Say that the output current of the phase A is given by:

$$i_L = I_O \sin(\omega_1 \cdot t) \tag{3-27}$$

where I_O = 53 A is the peak of the current waveform which corresponds to a system power output of 25 kW. Figure 3-29 gives a detailed drawing of the output current and the duty cycle.

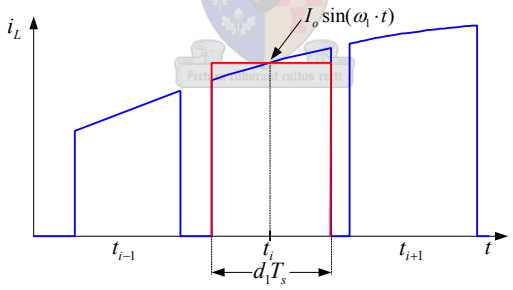


Figure 3-29: Output Current

The duty cycle is given by:

$$d_1 = \frac{1}{2}\left(1 + m_a \sin(\omega_1 \cdot t)\right) \tag{3-28}$$

The energy dissipated in the switch during the i^{th} switching period is approximated by:

$$E_{i(cond)} \approx \mathrm{V_{ON}} \cdot d_1 T_s \cdot I_O \cdot \sin(\omega_1 \cdot t_i)$$
$$= \mathrm{V_{ON}} \cdot \frac{1}{2}\left(1 + m_a \sin(\omega_1 \cdot t_i)\right) \cdot I_O \sin(\omega_1 \cdot t_i) \cdot T_s$$

The average power dissipated, of the control signal in the switch, over a period T_s is given by:

$$P_{cond} = \frac{1}{T_1}\sum_{i=1}^{N} \mathrm{E_{i(cond)}}$$
$$= \frac{1}{T_1}\sum_{i=1}^{N} \frac{1}{2} \cdot \mathrm{V_{ON}}\left(1 + m_a \sin(\omega_1 \cdot t_i)\right) \cdot I_O \sin(\omega_1 \cdot t_i) \cdot T_s$$
$$\approx \frac{1}{T_1}\int_0^{T_1/2} \frac{1}{2} \cdot \mathrm{V_{ON}}\left(1 + m_a \sin(\omega_1 \cdot t_i)\right) \cdot I_O \sin(\omega_1 \cdot t_i) dt$$
$$= \frac{\mathrm{V_{ON}}}{2T_1}\int_0^{T_1/2} \left(I_O \sin(\omega_1 \cdot t_i) + m_a I_O \sin^2(\omega_1 \cdot t_i)\right) dt$$
$$= \frac{\mathrm{V_{ON}}}{2T_1}\left[\frac{-I_O}{\omega_1}\cos(\omega_1 \cdot t_i) + m_a I_O\left(\frac{t}{2} - \frac{\sin 2\omega_1 \cdot t}{4\omega_1}\right)\right]_0^{T_1/2}$$
$$= \frac{\mathrm{V_{ON}}}{2T_1}\left[2\frac{I_O}{\omega_1} + m_a I_O \frac{T_1}{4}\right]$$
$$= \mathrm{V_{ON}}\left[\frac{I_O}{2\pi} + \frac{m_a I_O}{8}\right]$$
$$= 2\left[\frac{53}{2\pi} + \frac{53}{8}\right]$$
$$= 30.12 \text{ W} \quad \text{per IGBT}$$

The following steps need to be fulfilled to calculate the switching losses. The energy that is dissipated in a switching cycle, by a single switch, is approximated by:

$$E_{i(swicth)} \approx \frac{1}{2}\mathrm{V_d} \cdot I_O \cdot \sin(\omega_1 \cdot t_i)(t_{on} + t_{off})$$

The average power over one period of the control signal is calculated as follows:

$$
\begin{aligned}
P_{swicth} &\approx \frac{1}{T_1}\sum_{i=1}^{N}\frac{1}{2}\mathrm{V_d}\cdot I_O\cdot\sin(\omega_1\cdot t_i)(t_{on}+t_{off}) \\
&= \frac{1}{T_1 T_s}\frac{1}{2}\mathrm{V_d}\cdot I_O\cdot(t_{on}+t_{off})\sum_{i=1}^{N}\sin(\omega_1\cdot t_i)T_s \\
&\approx \frac{1}{T_1 T_s}\cdot\frac{1}{2}\mathrm{V_d}\cdot I_O\cdot(t_{on}+t_{off})\int_0^{T_1/2}\sin(\omega_1\cdot t)dt \\
&= \frac{f_s}{2\pi}\cdot\mathrm{V_d}\cdot I_O\cdot(t_{on}+t_{off}) \\
&= \frac{5\times10^3}{2\pi}\cdot 800\cdot 53\cdot(190\times10^{-9}+650\times10^{-9}) \\
&= 28.34\ \mathrm{W} \quad \text{per IGBT}
\end{aligned}
$$

The average current through the diode in the opposing switch is given by:

$$
\begin{aligned}
I_{D2} &= I_L - I_{S1} \\
&= \frac{1}{T_1}\int_0^{T_1/2} I_O\sin(\omega_1 t)dt - I_{S1} \\
&= \frac{I_O}{\pi} - I_{S1} \\
&= \frac{I_O}{\pi} - \left(\frac{I_O}{2\pi}+\frac{m_a I_o}{8}\right) \\
&= \frac{I_O}{2\pi} - \frac{m_a I_o}{8} \\
&= 1.81\ \mathrm{A}
\end{aligned}
$$

And the power dissipated in the diode is:

$$
\begin{aligned}
P_{cond} &= V_{ON} I_{D2} \\
&= 2.3\cdot 1.81 \\
&= 4.16\ \mathrm{W}
\end{aligned}
$$

The total power dissipated in the IGBT module is calculated as follows:

$$
\begin{aligned}
P_D &= 6\cdot(30.12+28.34+4.16) \\
&= 375.72\ \mathrm{W}
\end{aligned}
$$

The temperature difference between the junction and the sink (T_{js}), as seen in Figure 3-28, is calculated with the help of its thermal resistance (R_{js}), which is given in the data sheets [19].

$$T_{js} = P_D \cdot R_{js}$$
$$= 375.72 \cdot 0.125$$
$$= 46.97\ ^{o}\text{C}$$

The maximum temperature at the sink is now:

$$T_{s(\max)} = 150\text{-}46.97 = 103.03\ ^{o}\text{C}$$

Equation (3-26) results in a value for R_{sa}, which is required to ascertain the size of the heat-sink.

$$R_{sa} = \frac{T_{s(max)}\text{-}T_a}{P_D}$$
$$= \frac{103.03\text{-}40}{375.72}$$
$$= 0.168\ ^{o}\text{C}/\text{W}$$

From a Semikron Table [20] it is concluded that a P16/300 type heat-sink is sufficient. This heat-sink functions with thermal resistances of up to $0.03\ ^{o}\text{C}/\text{W}$ with forced air cooling. The dimensions of the employed heat-sink are 300 mm × 200 mm × 77 mm.

3.3.3 DC Bus Capacitor and Snubber Network

In a 4-wire three-phase converter the neutral is connected to the centre of the DC bus. This centre-tapped configuration make unbalanced loading on the converter possible. This means that different loads can be connected to different phases. The system control station of the SES requires a power source with access to 230 V RMS. The system control station includes a system controller, meteorological equipment and miscellaneous office equipment such as a computer [21]. Not only does the SES require a single-phase supply, but so does the cooling equipment. The different single-phase loads are split up and connected between different phases and neutral. This is done to minimize unbalanced loading. The DC capacitors provide reactive power to the load. Figure 3-30 shows the capacitor set up. The ripple frequency of the DC capacitor is twice the switching frequency, i.e. 10 kHz. The capacitance value for a maximum DC ripple of ±10% is calculated with the help of the following formula [29]:

$$C = \frac{2 \cdot P_{out}}{(2 f_s)\left(V_1^2 - V_2^2\right)} \tag{3-29}$$

where:

V_1 = maximum ripple voltage

V_2 = minimum ripple voltage

Rewriting equation (3-29) and solving yields:

$$\begin{aligned} C &= \frac{2 \cdot P_{out}}{\left(2 \cdot 5 \cdot 10^3\right)\left(820.6^2 - 671.4^2\right)} \\ &= \frac{2 \cdot 25 \cdot 10^3}{2.22 \cdot 10^9} \\ &= 22.46 \text{ uF} \end{aligned} \tag{3-30}$$

Each chosen capacitor has a value of C = 4700 uF and is rated for a DC voltage of 450 V DC. The total capacitance between the positive node and negative node is 4700 uF. A 10 W, 33 kΩJ resistor is mounted across each capacitor to ensure that the voltage is divided equally across each capacitor. The DC bus voltage may never rise higher than the rated voltage of the capacitors. A DC over-voltage damages the capacitors as well as the batteries. The unit is protected against DC over-voltage. The battery bank, holding the DC link very stable, reduces the voltage ripple. This implies that only small DC bus capacitors are necessary.

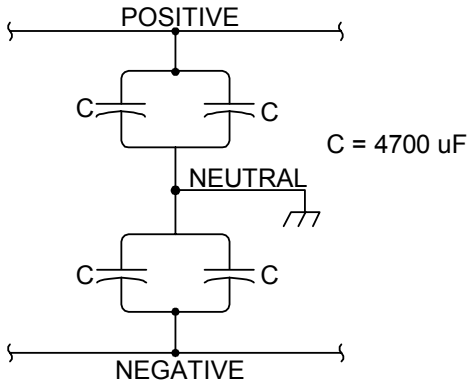


Figure 3-30: Configuration of the DC Bus Capacitor

Snubbers are circuits which are placed across semiconductor devices for protection, to improve performance and to achieve one or more of the following [5]:

- Reduce or eliminate voltage or current spikes;
- Limit dI/dt or dV/dt;
- Shape the load line to keep it within the safe operating area;
- Transfer power dissipation from the switch to a resistor or a useful load;
- Reduce total losses due to switching;
- Reduce EMI by damping voltage and current ringing.

Snubbers from WIMA of ratings 0.47 uF, 2000 V_{DC} and 700 V_{AC} are utilized.

3.4 *Soft Start and Dump System*

The converter needs to isolate itself from the high-voltage battery bank, as well as discharge the DC bus capacitors, when a fault arises. This needs to be performed for the sake of the safety of the person working on it. The soft start and dump circuit configuration is shown in Figure 3-31.

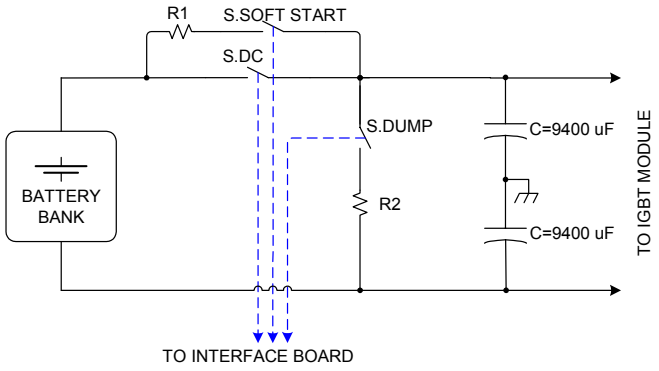


Figure 3-31: Diagram of the Soft Start and Dump Circuit

The main purpose of the soft starter is to limit the inrush current to the DC capacitors. The time constant (τ) determines the time a capacitor charges through a resistor. A capacitor is charged up 99.3% after a time interval of $t = 5 \cdot \tau$ [18]. The charging of the capacitors should be around 3 seconds. Thus the resistor value R1 is calculated as follows.

$$\begin{aligned} 5 \cdot \tau &= 5 \cdot R \cdot C = 3 \text{ s} \\ R &= 127 \ \Omega \end{aligned} \tag{3-31}$$

110 Ω is chosen for R1 and R2 in Figure 3-31. Two 220 Ω 50 W resistors are connected in parallel to get a higher power rating. The high-power switching relays used are KILOVAC EV-200 and are ideally suited for battery switching. The capacitors are initially discharged. At start-up the DSP commands to close switch S.SOFT START for 10 seconds. This charges the DC bus capacitor through R1, in Figure 3-31, from the battery bank. Relay S.DC is closed shortly before S.SOFT START opens again. Now the battery bank is directly connected to the capacitors as well as to the IGBT module. S.SOFT START is opened again. The start-up procedure is clarified with the flow-diagram in Figure 3-32. If, however, during start-up the POWER SWITCH is turned off, the system shuts down as observed in Figure 3-32, when the Shutdown Flag is set.

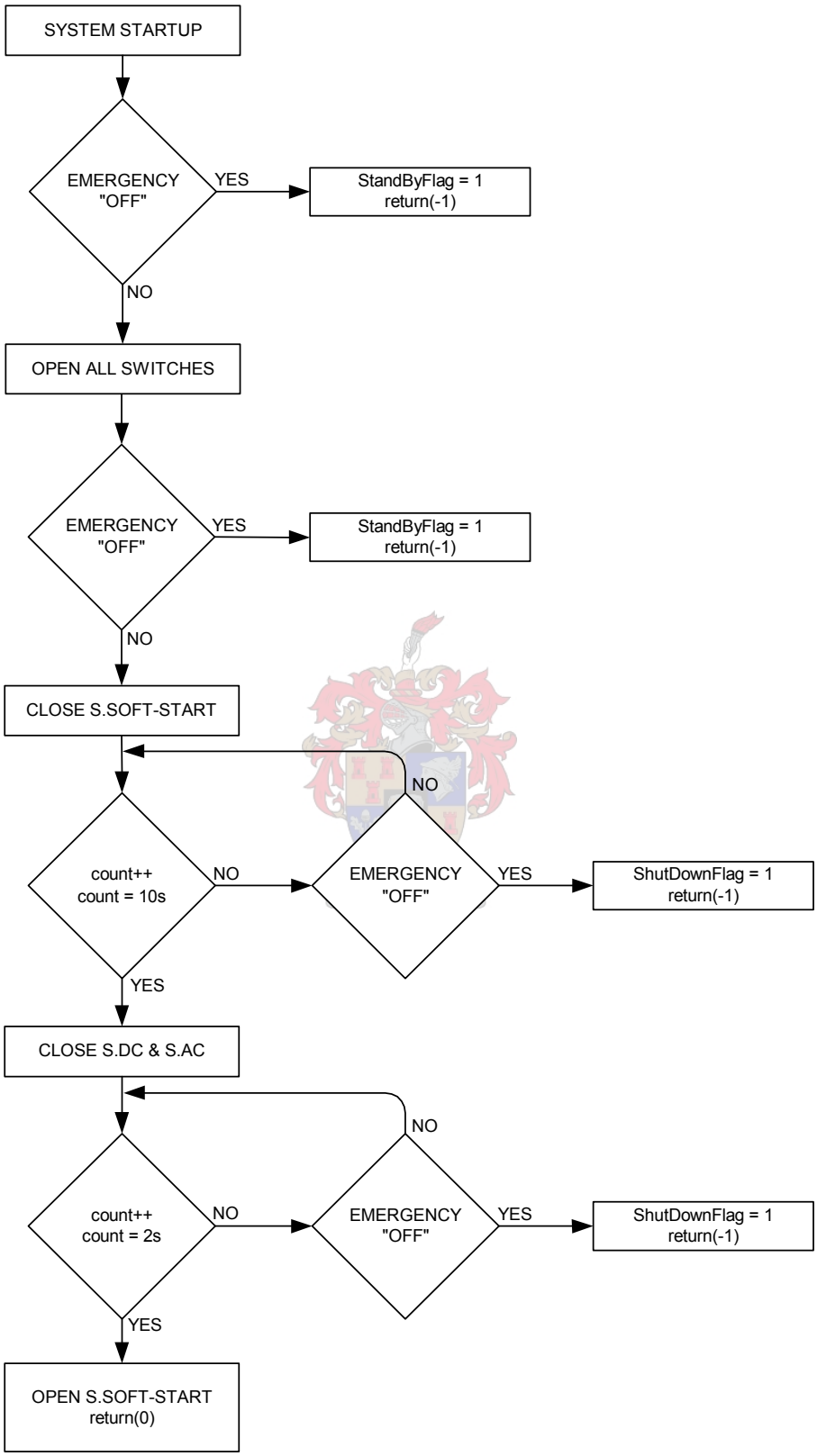


Figure 3-32: Flow diagram of the Start-up Procedure

The purpose of the dump circuit is to discharge the DC bus capacitors through R2. This is done as soon as a fault occurs. The DSP controls the dumping relay S.DUMP. The energy required for charging a capacitor corresponds to the energy given off by the capacitor when the capacitor is discharged. This is why the resistors have the same ratings. Both R1 and R2 are aluminium-housed wire-wound resistors, which are directly mounted onto the heat-sink. The shutdown procedure was shown in Figure 3-14.

3.5 Filter Module

The output filter is designed to provide a sinusoidal output voltage with a low-current ripple and therefore providing clean power to the load. The voltage output of the three-phase converter contains sideband harmonics, due to PWM, centred around multiples of the switching frequency (f_s) given by:

$$f_h = n \cdot f_s \pm m \cdot f_1 \tag{3-32}$$

where f_h are the harmonic frequency components, in Hz, and f_1 is the fundamental frequency. The transfer function for the low pass filter (LPF) in Figure 3-33 is given by:

$$H(s) = \frac{1}{s^2 LC + 1} \tag{3-33}$$

The resonance frequency is given by:

$$f_0 = \pm \frac{1}{2\pi\sqrt{LC}} \tag{3-34}$$

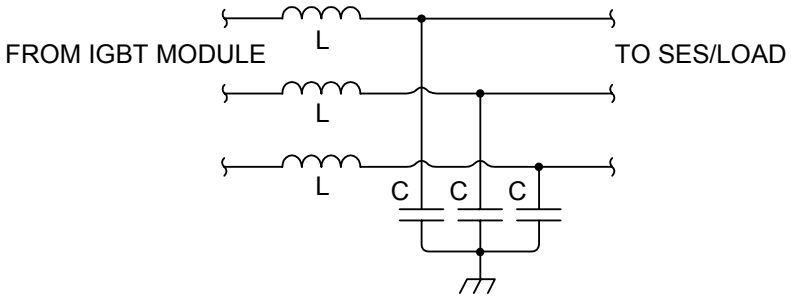


Figure 3-33: Circuit Configuration of the L-C Filter

The most dominant harmonics occur at the carrier frequency f_s and the first sideband harmonics $f_h = f_s \pm 2f_1$. This is observed in Figure 3-34, where the harmonic spectrum is shown. For this reason the cut-off frequency (f_0) must fulfil the following condition.

$$f_1 < f_0 < f_h = f_s - 2f_1 \tag{3-35}$$

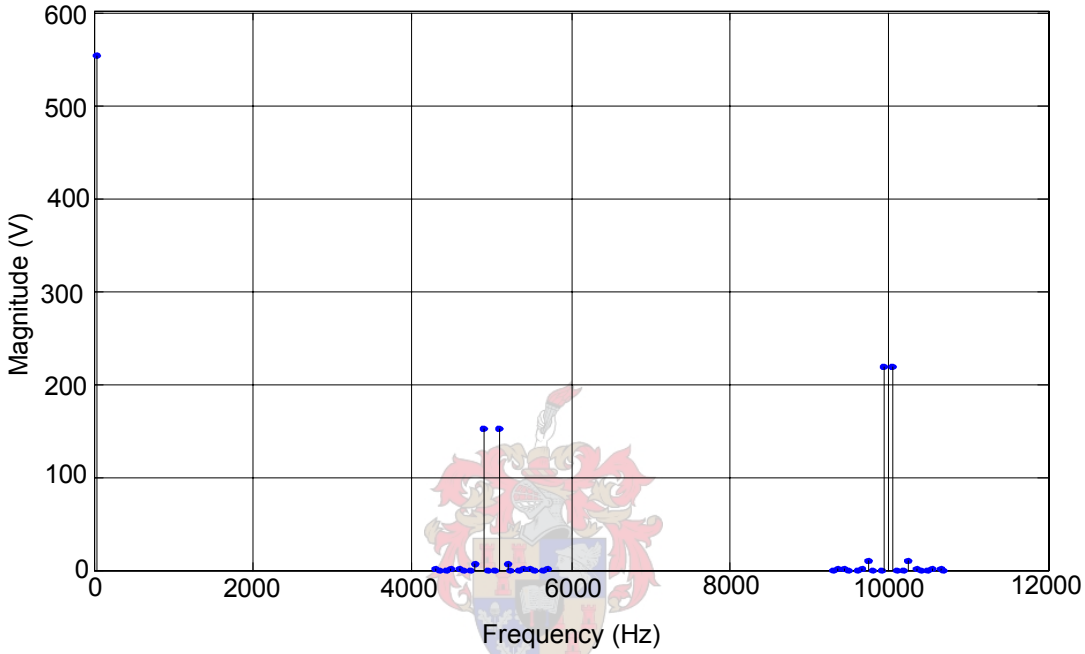


Figure 3-34: Harmonic Spectrum of the Converter

A voltage and current ripple of 5% is good. The current ripple at 25 kW is calculated as follows:

$$\Delta I_L = \frac{P_{1\phi}}{V_{LN}} \cdot 0.05 = \frac{25 \cdot 10^3}{3} \cdot \frac{1}{230} \cdot 0.05$$
$$= 1.81 \text{ A}$$

The capacitance value can now be calculated with the following formula [5]:

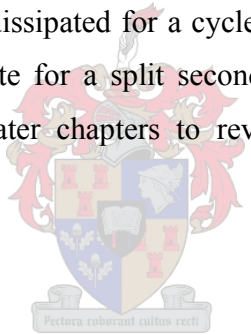
$$\Delta V_o = \frac{\Delta Q}{C} = \frac{1}{C} \frac{1}{2} \frac{\Delta I_L}{2} \frac{T_S}{2}$$

$$C = \frac{1}{\Delta V_o}\frac{1}{C}\frac{1}{2}\frac{\Delta I_L}{2}\frac{T_S}{2}$$
$$= \frac{1}{(325 \cdot 0.05)}\frac{1}{2}\frac{1.81}{2}\frac{1}{2 \cdot 5000}$$
$$= 2.78 \text{ uF}$$

Two 50 uF capacitors are connected in parallel. A cut-off frequency of 800 Hz is selected. A capacitor value of 100 uF results in an inductor value of:

$$L = \frac{1}{C \times (2\pi f_0)^2} = 395 \text{ uH} \tag{3-36}$$

Connecting two 50 uF capacitors in parallel, per phase, results in a capacitance of 100 uF per phase. The inductors are specially designed and made up for this type of application. They are designed for a switching frequency of 5 kHz, an RMS current of 55 A, an inductance of 400 uH and a peak current of 450 A. Tests on the SES revealed that peak currents of more than 450 A are dissipated for a cycle. This was not known prior to the design. Thus the inductors saturate for a split second. The output waveforms, for the practical results, are shown in later chapters to reveal if the L-C filter design was successful.



3.6 Load Management System

3.6.1 Thyristor Driver and Dump Load

The power generated by the SES must be utilized by some consumer, load or energy storage device. The aim of the thyristor circuit is to dump all the extra energy, which is not used for battery charging, to a dump load. Other AC appliances can be connected to the AC bus. Figure 3-35 illustrates how the thyristor module is implemented into the design. The dump load is Y-connected as shown in Figure 3-35. The analog three-phase thyristor trigger module utilized here is manufactured by Semikron and has a part number RT380T. This encapsulated thyristor module is designed to trigger 6 thyristors with phase

regulation to control the power dissipated in the load. External R-C snubbers are used to protect the thyristors and to facilitate their triggering. This R-C snubber circuit design is made by Semikron. The thyristors are mounted on a heat-sink with forced air cooling. The control voltage is selectable between 0-5 V DC and 0-10 V DC. The 0-5 V DC scale is chosen for this design. All thyristors stop conducting when the control voltage is 0 V. The control voltage is proportional to the conducting state. The thyristors act as a short-circuit, when a voltage of 5 V DC is applied, and all the power is dissipated into the dump load.

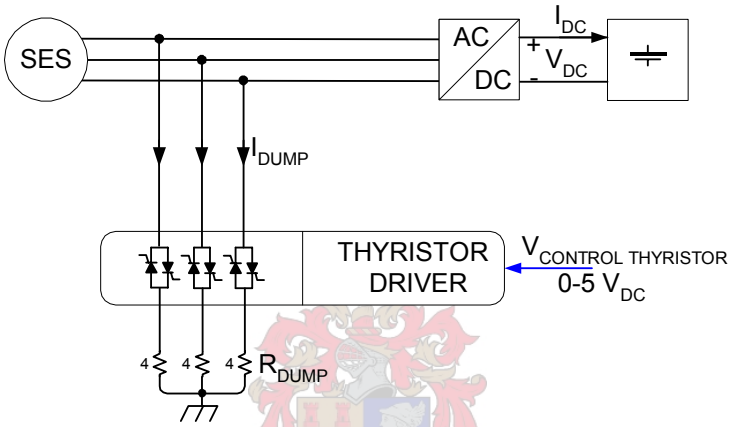


Figure 3-35: Thyristor and Dump Load Setup

The DSP provides a control signal for the thyristor driver. Only digital outputs are available from the DSP. This means that one digital output signal from the DSP is converted, by a low pass filter, to an analog signal. Output IOPF3/T4PWM/T4CMP from the DSP is used for the thyristor control. An internal DSP timer 4 is set up to count at a frequency of 100 kHz. Each time the timer value is above the T4CMPR value, which ranges from 0 to 100 and represents the duty cycle, the output (IOPF3) is set high. This compare operation is clarified in Figure 3-36.

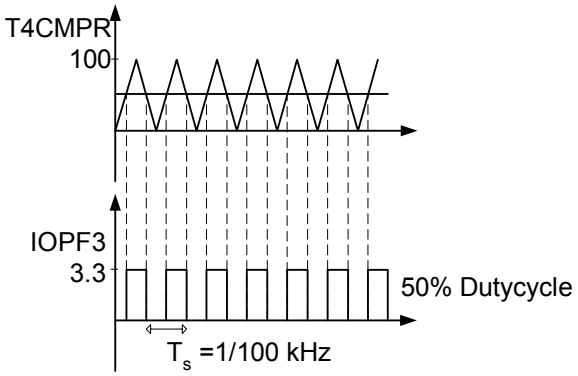


Figure 3-36: Timer 4 Compare Operation

The low pass filter in Figure 3-37 illustrates how this digital pulse-width controlled signal is converted to an analog signal. The operational amplifier used is a LM324. The gain of the amplifier is 200/190.

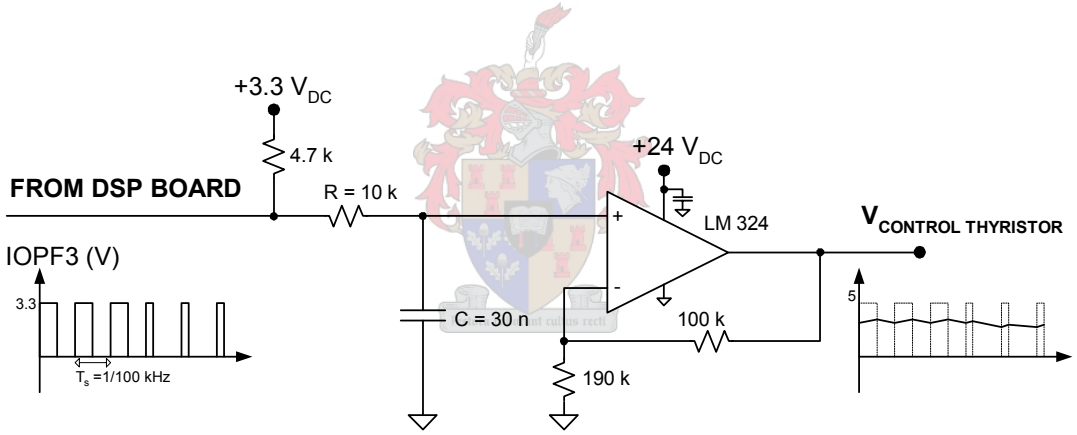


Figure 3-37: Low Pass Filter for Control Signal of Thyristor Driver

The transfer function of the filter in Figure 3-37 is given by:

$$\frac{V_{CONTROL\ THYRISTOR}}{IOPF3} = \frac{200}{190} \cdot \frac{1}{s \cdot R \cdot C + 1} \tag{3-37}$$

The bode-plot in Figure 3-39 shows the frequency response of the R-C filter. The 3 dB cut-off frequency lies at:

$$f_{3dB} = \frac{1}{2\pi} \cdot \frac{1}{R \cdot C} = 530\ Hz \tag{3-38}$$

Figure 3-38 demonstrates that the digital signal (CH2) is filtered to an analog signal (CH1) with only a small ripple. The left-hand figure shows a digital signal with a duty cycle of 28% and the right-hand figure a duty cycle of 78%.

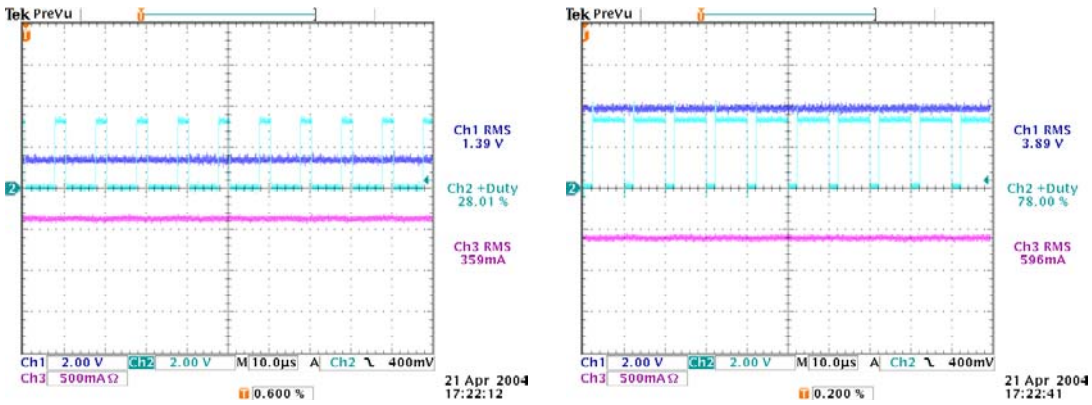


Figure 3-38: Results of Filtering the Control Signal for the Thyristor Driver

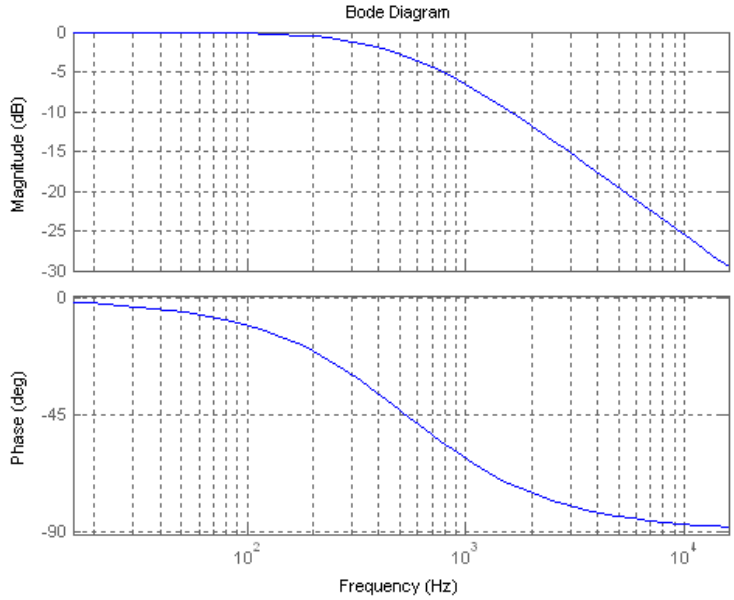


Figure 3-39: Bode Plot of the Low Pass Filter for the Control Signal of the Thyristor Driver

Let's shift the focus back to the main purpose of the thyristor circuit. The purpose is to dump all energy to the load, except the energy that is used to charge the battery bank. This is done by controlling the energy that is used for battery charging. The DC current

measurement, as explained in paragraph 3.2.3, as well as the DC voltage measurement is used to determine what the control voltage ($V_{CONTROL\ THYRISTOR}$) of the thyristor driver is.

3.6.2 Battery Charging

Charging of the batteries takes place during the day, when the SES is the source of energy. The thyristor driver starts regulating the power dissipated into the dump load if the DC current, flowing into the battery bank, is greater than a predefined reference value. This power consumption by the dump load decreases the current that flows towards the batteries. A proportional feedback control system is utilized to regulate the charging current. This control diagram is presented in Figure 3-40.

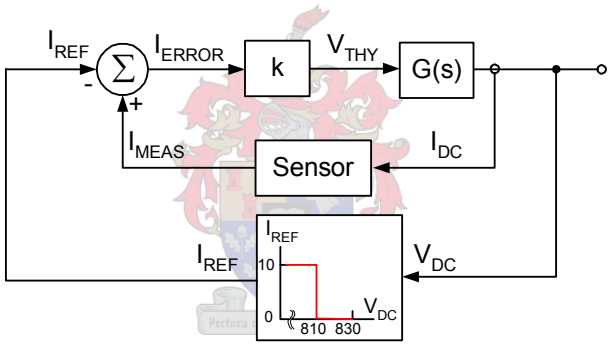


Figure 3-40: Diagram of a Proportional Feedback Control System

The charging current depends on the battery state as seen in Figure 3-41. In normal operation the battery is in normal state “N1” or “N2”. When the battery bank is in its “overload (O)” or “low (L)” state, the converter is shut down. In these O or L states the battery bank is in a position to be permanently damaged. The batteries are charged at a charge rate of C/10, which equals 10 A, for a 100 Ah battery. The battery voltage vs. state of charge (SOC) graph [26], for lead-acid batteries, is shown in Figure 3-42 and Figure 3-43. Figure 3-42 corresponds to a battery voltage while a battery is under charge and Figure 3-43 corresponds to the voltage while a battery is discharged. The voltage per battery is 13.5 V at a SOC of 75% as shown in Figure 3-42. If the SOC of the battery bank is between 75% and 85% the charge current is minimized. A maximum charge

voltage of 13.8 V is allowed on the batteries, as seen in Figure 3-41. During state "N2" the battery bank voltage is between 730 V and 810 V. As soon as the voltage reaches a level of 810 V the charging current is decreased to zero. This ensures that the battery is in a high SOC. Most of the energy supplied by the SES is dumped into the dump load while the batteries are in a high SOC. If, however, the battery bank voltage exceeds a voltage of 830 V, the system shuts down to prevent overcharging of the battery bank. A DOD of 40% corresponds to a SOC of 60%. From Figure 3-43 it is concluded that a SOC of 60% corresponds to a battery voltage of 12.15 V. At this voltage level the system shuts down to prevent a deep discharge, as seen in Figure 3-41.

The DC current (I_{DC}) and the DC voltage (V_{DC}), in Figure 3-40, are utilized in the feedback control. The current reference (I_{REF}) value depends on the DC voltage as explained. The control signal for the thyristors depends on the feedback error ($I_{ERROR} = I_{MEAS} - I_{REF}$), multiplied by a gain k, and is given by the following formula:

$$V_{CONTROL\ THYRISTOR} = k \cdot (I_{MEAS} - I_{REF}) \tag{3-39}$$

This control technique was not tested perfectly, since a source such as a SES was not available. Paragraph 4.2.7 reveals how the load management system is tested.

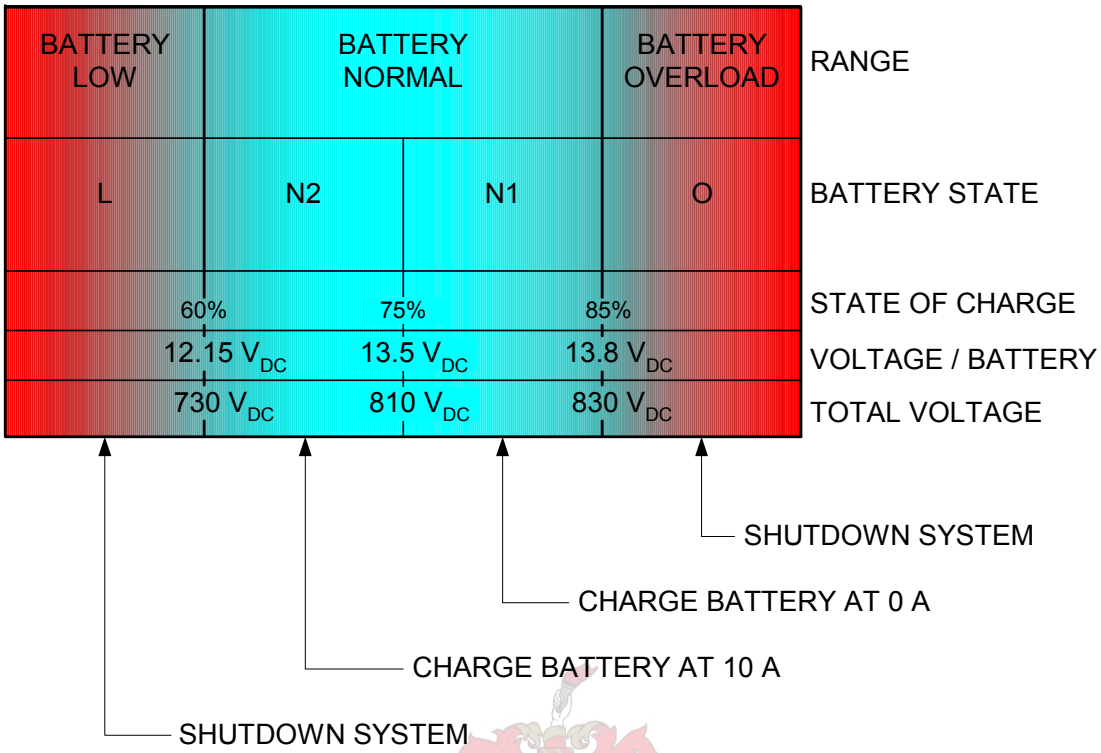


Figure 3-41: Dependency of the Battery State and the Charge Degree

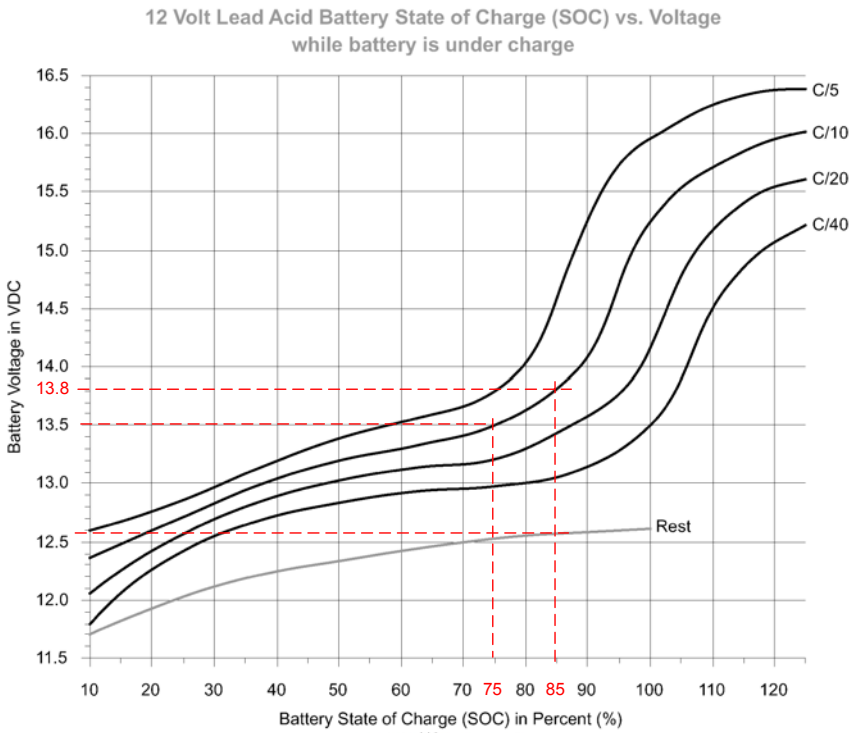


Figure 3-42: State of Charge vs. Voltage while Battery is under Charge [26]

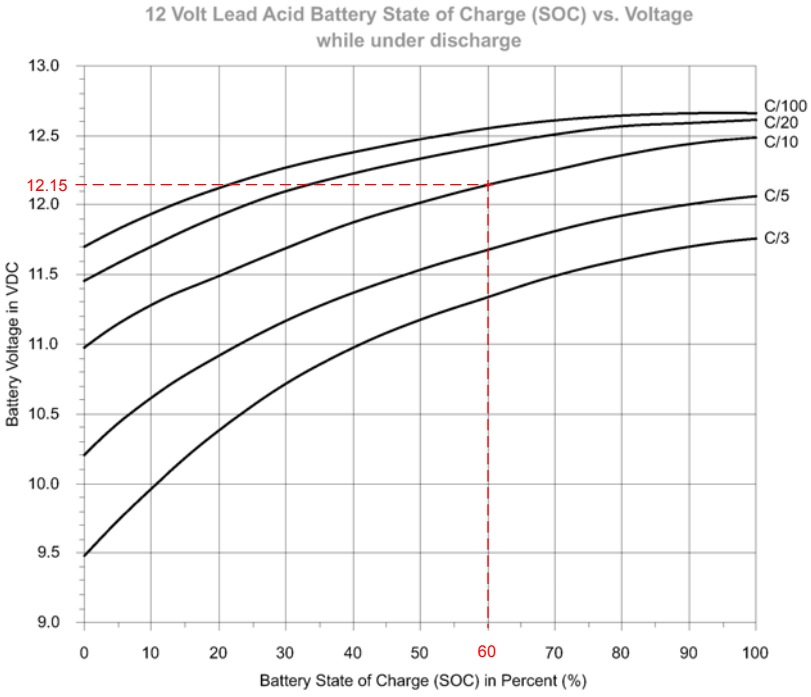


Figure 3-43: State of Charge vs. Voltage while Battery is under Discharge [26]

Figure 3-44 elaborates on the control technique by means of a flow diagram. The batteries are only charged when the converter acts as a rectifier. The measured DC current, corresponding to the charge current, is scaled to a finer scale. This scaled value "IDCScale" is then used to determine what the duty cycle, in other words $V_{CONTROL\ THYRISTOR}$, is. Equation (3-39) is represented again in equation (3-40), where the reference value and the gain are substituted. $V_{CONTROL\ THYRISTOR}$ is given by the following equation, which corresponds to a charge rate of 10 A:

$$\begin{aligned} V_{CONTROL\ THYRISTOR\ 10A} &= \frac{27}{9}\left(\left(\frac{I_{DC\ ACTUAL}}{7.57}+1.65\right)\cdot\frac{1024}{3.3}-893\right) \\ &= 123\cdot I_{DC\ ACTUAL}-1143 \end{aligned} \tag{3-40}$$

At a charge rate of nearly 0 A the value is given by the following formula:

$$\begin{aligned} V_{CONTROL\ THYRISTOR\ 0A} &= \frac{28}{5}\left(\left(\frac{I_{DC\ ACTUAL}}{7.57}+1.65\right)\cdot\frac{1024}{3.3}-517\right) \\ &= 229\cdot I_{DC\ ACTUAL}-28 \end{aligned} \tag{3-41}$$

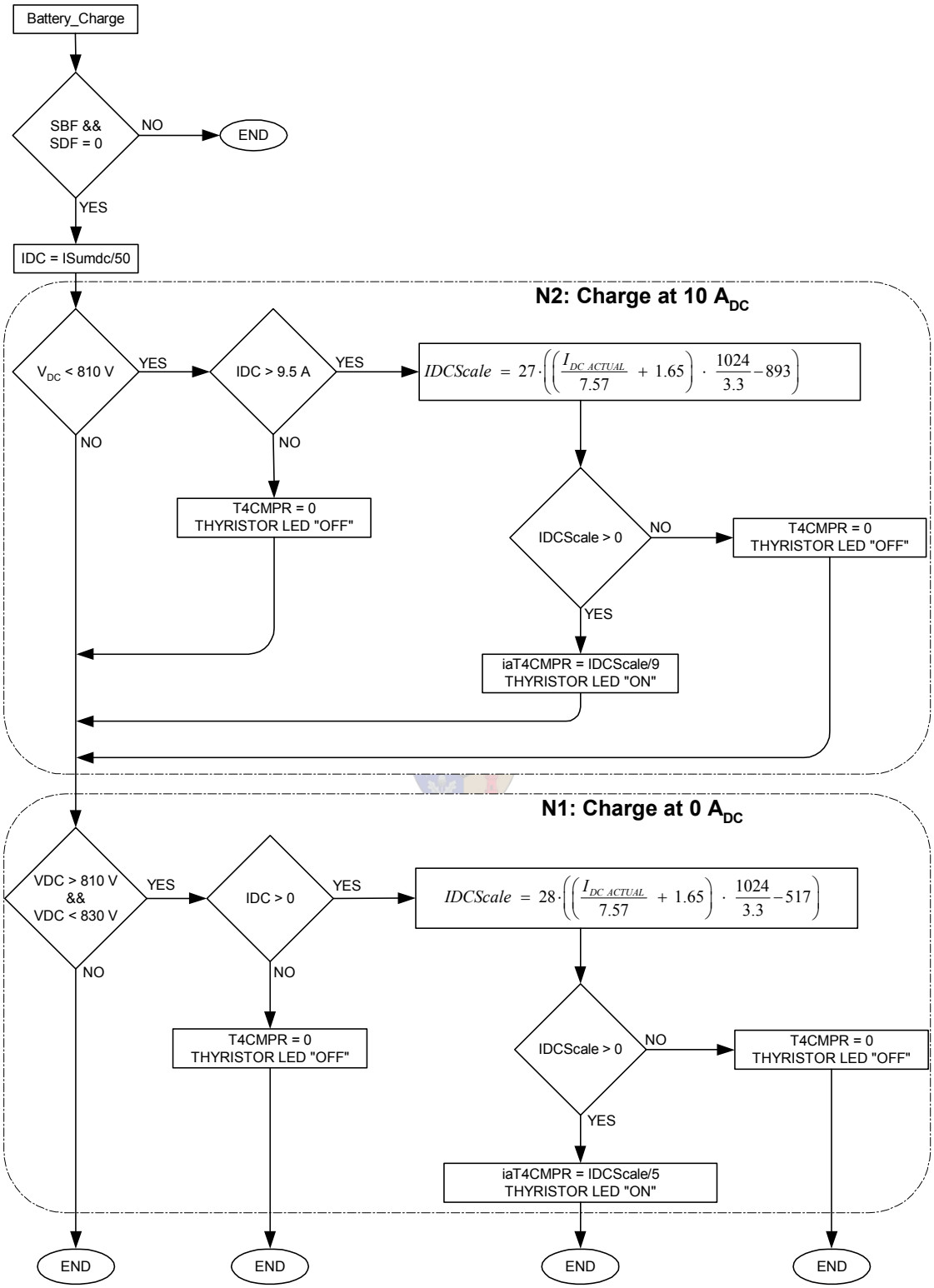


Figure 3-44: Flow diagram of the Battery Charging Algorithm

3.7 *Energy Storage Size*

This section deals with the total amount of energy available from the system that is used to provide rural households with constant electricity during the day and night. The energy storage capacity depends on the size of the load. The sizing of the application is examined first and from that the energy capacity is calculated.

3.7.1 Sizing the Load

The loads in this case are rural households. The total basic energy needs of a single rural household for a 24-hour day are estimated as follows [2]:

Lighting:	0.3 kWh	(4 lamps, each being a 15 W bulb, used for 5 hours)
Audio-visual:	0.2 kWh	(Average television about 40 W for 5 hours per day)
Refrigeration:	3.6 kWh	(A typical refrigerator consumes 110 kWh per month)
Pumping:	0.1 kWh	(11 kW pump for 10 hours a day for 1000 households)
Total:	4.2 kWh	

The households utilize some energy during the day and some energy during the night. Table 4 provides the different energies consumed by a household during the day, which consists of 10 hours, and during the night, which consists of 14 hours.

Energy need	10 hour Day (kWh)	14 hour Night (kWh)	24 hour Day (kWh)
Lighting		0.3	0.3
Audio-visual	$0.2\times10/24=0.0833$	$0.2\times14/24=0.1167$	0.2
Refrigeration	$3.6\times10/24=1.5$	$3.6\times14/24=2.1$	3.6
Pumping	0.1		0.1
Total	1.6833	2.5167	4.2

Table 4: Energy Consumption by a Rural Household during Day and Night

It is seen that more energy is consumed during the night than during the day. To provide energy to an equal number of households, during the day and night, the energy sources have to be balanced. This means there are 27 households supplied continuously with energy, as calculated in the next paragraph.

3.7.2 Sizing the Energy Storage Capacity

A battery bank, consisting of 60 lead acid batteries ("Deltec High Cycle"), is utilized in this design for demonstration purposes. The total energy (E) available from a single battery bank when discharged from full capacity to 40% DOD is:

$$\begin{aligned} E &= DOD \cdot Ah \cdot V \cdot N \\ E &= 0.4 \cdot 102 \cdot 12.5 \cdot 60 \\ E &= 30.6 \text{ kWh} \end{aligned} \tag{3-42}$$

Ah and V are the ampere hour and voltage ratings of a single battery respectively. N is the number of batteries. The amount of energy in equation (3-42) is not enough to provide power to 27 households during the night, as seen by the following calculation:

$$N_{per\ night\ (one\ battery\ bank)} = \frac{E_{total\ (one\ battery\ bank)}}{E_{per\ household\ (night)}} = \frac{30.6 \cdot 10^3}{2.5167 \cdot 10^3} \approx 12 \text{ Households}$$

It is thus necessary to calculate the capacity of a battery bank that can supply 27 rural households with power. If the SES supplies average power of 20 kW for 10 hours, during the day, it provides energy of 200 kWh. An average lead-acid battery has an efficiency of 45%. During the day the batteries are recharged, which requires more than twice the amount of energy dissipated during the previous night, which corresponds to $E_{total\ (night)}/0.45$. Other power consumption, excluding the households, such as the SES controller, miscellaneous office equipment and meteorological equipment that are required for the SES control, require a maximum energy of about 1 kWh. The total energy that is left for household purposes during the day is calculated as follows:

$$\begin{aligned} E_{total\ (day)} &= E_{SES} - E_{SES\ control\ +\ other} - E_{total\ (night)} / 0.45 \\ &= 200 \cdot 10^3 - 1 \cdot 10^3 - E_{total\ (night)} / 0.45 \end{aligned} \tag{3-43}$$

The number of households that is supplied with the remaining power during the day is thus:

$$N_{per\ day} = \frac{E_{total\ (day)}}{E_{per\ household\ (day)}} = \frac{200 \cdot 10^3 - 1 \cdot 10^3 - E_{total\ (night)} / 0.45}{E_{per\ household\ (day)}} \tag{3-44}$$

And the number of households that is supplied with the battery power during the night is thus:

$$N_{per\ night} = \frac{E_{total\ (night)}}{E_{per\ household\ (night)}} \tag{3-45}$$

$N_{per\ day}$ must equal $N_{per\ night}$ to supply an equal number of households with electricity. Thus:

$$\frac{200 \cdot 10^3 - 1 \cdot 10^3 - E_{total\ (night)} / 0.45}{E_{per\ household\ (day)}} = \frac{E_{total\ (night)}}{E_{per\ household\ (night)}} \tag{3-46}$$

Solving equation (3-46) and substituting the values from Table 4 results in the energy that is required in the night by 27 households. The calculation is presented:

$$\begin{aligned} E_{total\ (night)} &= \frac{199 \cdot 10^3 \times 0.45 \times E_{per\ household\ (night)}}{0.45 \times E_{per\ household\ (day)} + E_{per\ household\ (night)}} \\ &= 68.83 \text{ kWh} \end{aligned} \tag{3-47}$$

$E_{total\ (night)}$ corresponds to the total required battery capacity. A possible way to obtain the required energy is to connect two battery banks in parallel, which results in a total capacity, when discharged from full capacity to 40% DOD, of:

$$\begin{aligned} E &= DOD \cdot Ah \cdot V \cdot N \\ E &= 0.4 \cdot 204 \cdot 12.5 \cdot 60 \\ E &= 61.2 \text{ kWh} \end{aligned} \tag{3-48}$$

This energy capacity must be increased by a few kWh to obtain the required value of 68.83 kWh. Two possible solutions to this problem are either to add a third battery bank of 60 batteries in series or to increase the DOD. Adding a third battery bank for an extra 7.6 kWh seems to be too much. Thus it is necessary to increase the DOD to a level of:

$$DOD = \frac{E}{Ah \cdot V \cdot N}$$
$$DOD = \frac{68.83 \cdot 10^3}{204 \cdot 12.5 \cdot 60} \quad (3\text{-}49)$$
$$DOD = 0.45$$

The number of discharge and charge cycles with a DOD of 45% in Figure 2-2 decreases by about 50 times. This is reasonable. The following equations show that 27 households are supplied with power during the day and night with a battery bank consisting of two parallel banks, each utilizing 60 batteries in series. The number of rural households per day is calculated from equation (3-44) which results in:

$$N_{per\ day} = \frac{E_{total\ (day)}}{E_{per\ household\ (day)}} = \frac{200 \cdot 10^3 - 1 \cdot 10^3 - E_{total\ (night)} / 0.45}{E_{per\ household\ (day)}}$$
$$= \frac{200 \cdot 10^3 - 1 \cdot 10^3 - 68.83 \cdot 10^3 / 0.45}{1.6833 \cdot 10^3} = \frac{46.04 \cdot 10^3}{1.6833 \cdot 10^3}$$
$$\approx 27 \text{ Households}$$

The household number during night follows from equation (3-45):

$$N_{per\ night} = \frac{E_{total\ (night)}}{E_{per\ household\ (night)}}$$
$$= \frac{68.83 \cdot 10^3}{2.5167 \cdot 10^3}$$
$$\approx 27 \text{ Households}$$

If, however, the SES is shut down during the day, because of cloudy conditions, and thus provides no power, the number of households that are supplied only from the battery bank is calculated as follows:

$$N_{per\ 24h\ from\ battery\ bank} = \frac{E_{total}}{E_{per\ household}} = \frac{68.83 \cdot 10^3}{4.2 \cdot 10^3} \approx 16 \text{ Households}$$

From the above calculations it can be said that 16 households are supplied with power only from the battery bank per day, consisting of 24 hours. This, however, only happens when the SES is shut down during the day.

Table 5 summarizes the energy provided by the bidirectional converter system under different circumstances.

Energy Source	Duration (h)	Available Energy (kWh)	Power (kW)	Number of Households (N)
Battery Bank	14 (night)	68.83	4.91	27
SES	10 (day)	46.04	4.6	27
Battery Bank *	24 (day & night)	68.83	2.87	16

* Battery bank is the only energy source, because of cloudy conditions or SES failure.

Table 5: Power Output of the System during Solar/Non-Solar Mode.

These batteries are discharged during the night and charged during the day. It is compulsory that good care must be taken over the batteries. Batteries are damaged when the charge/discharge rate is too high. The charging procedure is discussed in paragraph 3.6.2. The battery bank voltage is monitored permanently to make sure that the voltage is in a safe region. The charge rate depends on the Ah rating of the battery storage. Thus, if two battery banks are connected in parallel, the charge rate is doubled. This was not implemented in the design since it was intended for demonstration purposes only.

3.8 Construction

The entire layout design was done before the converter was manufactured. Construction included cutting metal plates to attach circuit components, drilling holes, tabbing the holes and mounting everything together to build a system as indicated in Figure 3-45. Cables were crimped to ensure neatness and stability; wires were colour-coded and fixed to the metal frame. A part of the converter is shown in Figure 3-45. The controller board is mounted beneath the interface board, which is seen in the left bottom corner of Figure 3-45. The lengths of the wiring for the system controller were minimized to overcome electromagnetic interference (EMI). The cable used for control signals is an IDC ribbon cable. The high-current cables which are utilized are 16 mm^2 flexible cables. Single components can be replaced at any time without dismantling the whole unit.

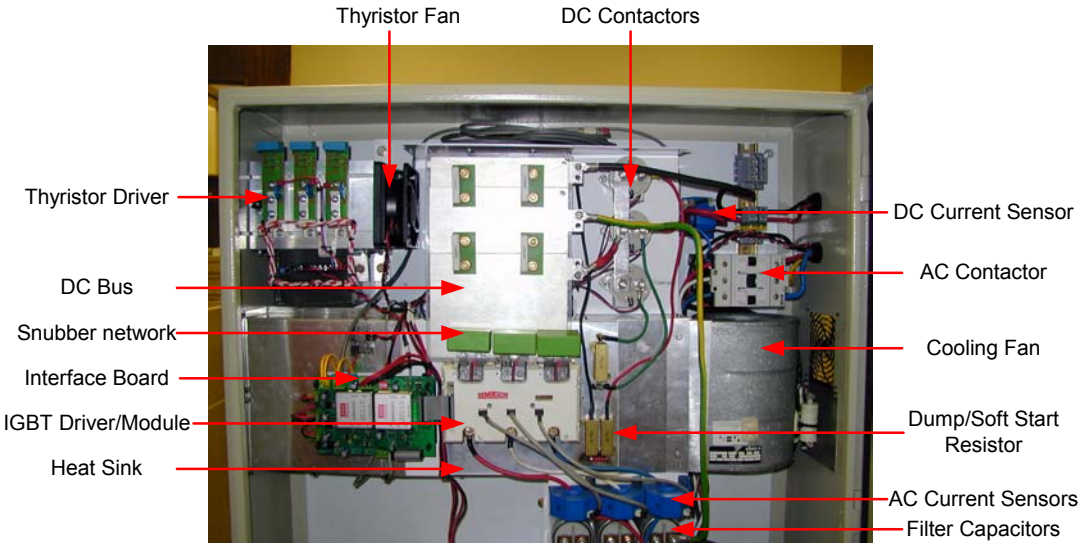


Figure 3-45: Picture of the Converter

The converter is placed in an electrical watertight box, as seen in Figure 3-45. Figure 3-46 represents the front panel, which indicates in which mode the converter is functioning and which switches are open or closed. It can also be consulted to ascertain whether the SES is generating more power than utilized by charging of the battery bank. A different LED lights up to show that the system is dumping the excess power.

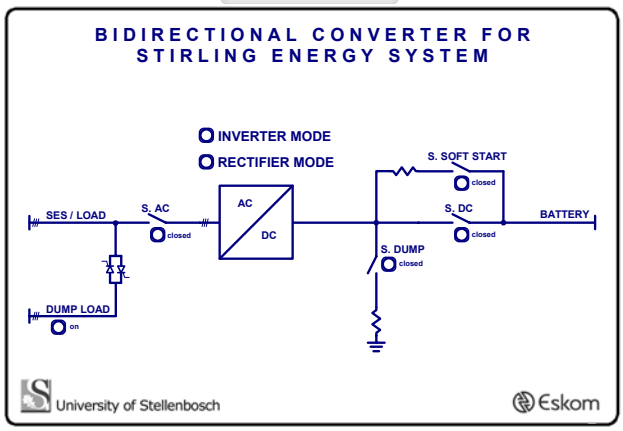


Figure 3-46: Diagram of Front Panel

3.9 Conclusion

The bidirectional converter was designed to be user-friendly and easy to operate. This was achieved through protection features which control the system to operate as safely as possible. Only a single switch was used to operate the unit.

The 12 V batteries are recharged automatically during operation. The DSP controller board was tested several times and no problems occurred. The interface board functioned well by supplying power to the controller and scaling signals such as measurements. All measurements were precise. This showed that the PCB layout was successful and that the current sensors utilized were accurate. The DSP could be easily reprogrammed at any later stage. The IGBT module included a driver which had important features to protect it. The heat-sink design was successful, which is shown in paragraph 4.2.9, where temperature measurements are done to show that the generated heat is transferred to the outside of the box with the help of cooling fans. High-voltage and low-voltage components were placed separately. The converter layout was designed so that each component could easily be replaced. The next chapter discusses the practical results achieved. The system was tested in the laboratory and on site.

CHAPTER 4: PRACTICAL EXPERIMENTS AND RESULTS

4.1 Introduction

The final implementation was done at the Development Bank of Southern Africa (DBSA), which is situated in Midrand, Johannesburg. The system operated as a standalone unit. The bidirectional converter was tested in the laboratory, where the system could easily be altered if changes needed to be made. All possible experiments were done in the laboratory to make sure that the system would function on site. The system, however, could not be tested perfectly before the implementation on site. The SES could not be modelled in the laboratory. All experiments done in the laboratory showed good results. After several unsuccessful start-ups on site, the SES finally started up and initiated power generation. The generated power was used to recharge the battery bank and the excess power was dissipated into the dump load.

4.2 Experiments and Results in the Laboratory

4.2.1 Introduction

Before the bidirectional converter was implemented on site, some tests needed to be performed to ensure an effective product on site. The bidirectional converter was tested in the laboratory, where sufficient power sources and loads were available, for numerous real-time operating conditions. The following power sources were available: a battery bank consisting of 60 batteries in series, which is identical to the one used for final implementation; a high-voltage DC power supply, where one could vary the voltage from 0 V DC to 848 V DC. This power supply was made up of a three-phase variac, a three-phase transformer and a rectifier. The power supply configuration is shown in Figure 4-1. The AC line voltage was varied with the help of a three-phase variac. To get a high DC voltage, the three-phase voltages are transformed to a higher voltage. This is done with

the help of the transformer, which has a turns ratio of $N1/N2 = 2/3$. The full bridge rectifier converts the AC voltages to a DC voltage, as seen in Figure 4-1.

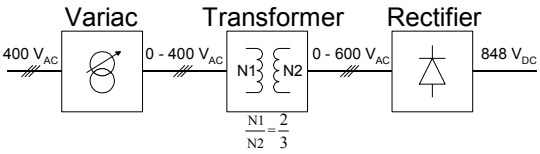


Figure 4-1: Configuration of the 848 V DC Power Supply

The available load was purely resistive and its size was altered to suit the experiment. The next few sections describe the experiments.

4.2.2 Inverter and Rectifier mode

The practical setup for this experiment includes a DC motor (DC-M), an IM, the converter and a battery bank. The IM was connected to DC-M with a shaft, as shown in Figure 4-2. The DC motor was connected as an external motor, which was used to alter the IM speed. The DC motor field windings were connected to a 220 V DC supply. The IM was connected to the bidirectional converter and the battery bank was linked to the DC side of the converter, as presented in Figure 4-2.

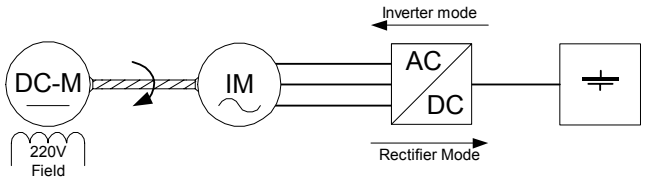


Figure 4-2: Practical Setup of the Inverter and Rectifier Mode Test

The experiment was commenced by turning the power switch of the converter to its "ON" position. The DC capacitors were charged by the soft start procedure and after a few seconds the converter started to switch. The IM spun up to synchronous speed (1500 rpm). The speed was measured with a digital speed meter. Measurements done by an

oscilloscope confirmed that the DC current was flowing from the battery bank in the direction of the converter. The converter functioned as an inverter. The speed of the IM increased as soon as the DC variac voltage was increased above the rated voltage of the IM. This was observed on the digital speed meter. It was observed that the IM functioned as a generator and that the DC current flowed into the batteries, thus charging them. This demonstrated the rectifier mode.

4.2.3 Average-Power Test

The high-voltage DC power supply was employed in this test instead of the battery bank. This was done to spare the batteries from discharging too much. A resistive load of R_{load} = 4.7 Ω, connected as a Y-configuration, was connected to each phase as shown in Figure 4-3.

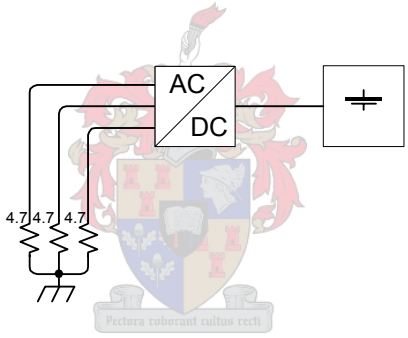


Figure 4-3: Practical Setup of the Average-Power Test

The system was switched on for 4 hours and measurements revealed: V_{DC} = 746 V; V_{AC} = 230 V per phase; I_{AC} = 49 A per phase; P_{avg} = 33.77 kW.

The output waveforms are presented in Figure 4-4, which are identical to those simulated in Figure 2-19. CH1, CH2 and CH3 represent the phase voltages of phase A, phase B and phase C respectively. CH4 is the load current of phase A. APPENDIC C reveals the similarities between the simulations and the practical results.

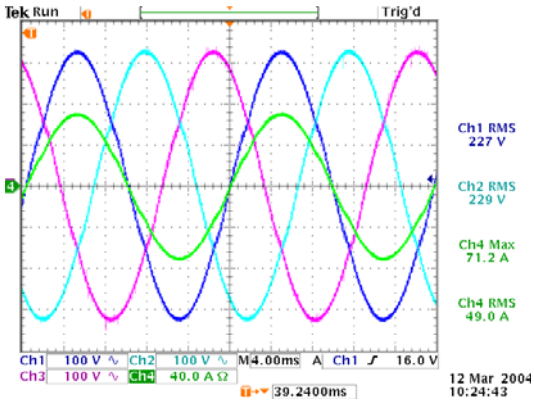


Figure 4-4: Output Waveform of the Average-Power Test

4.2.4 High-Power Test

This experiment was done to demonstrate that the converter can easily start up a 25 kW induction machine. The starter requirements of 100 kW [21] of energy per start are also met by this test. The bidirectional converter was connected between the battery bank and a load, as seen in Figure 4-5. A resistive load of R_{load} = 1.1 Ω was connected to each phase. The battery voltage was V_{DC} = 746 V.

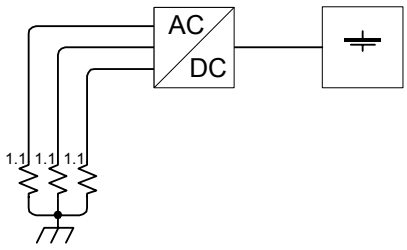
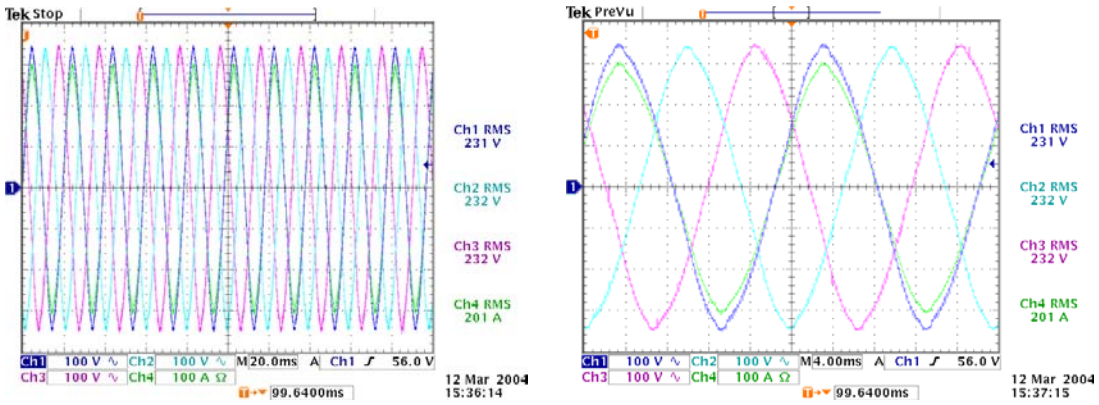


Figure 4-5: Practical Setup of the High-Power Test

The system was switched on for 10 seconds. A good-quality three-phase AC bus voltage as well as the output current of phase A is shown in Figure 4-6 (a) and Figure 4-6 (b). The latter is an enlarged view of Figure 4-6 (a). These results are again very similar to those simulated in Figure 2-21 and Figure 2-22 of Chapter 2, which are shown once again in APPENDIX C.



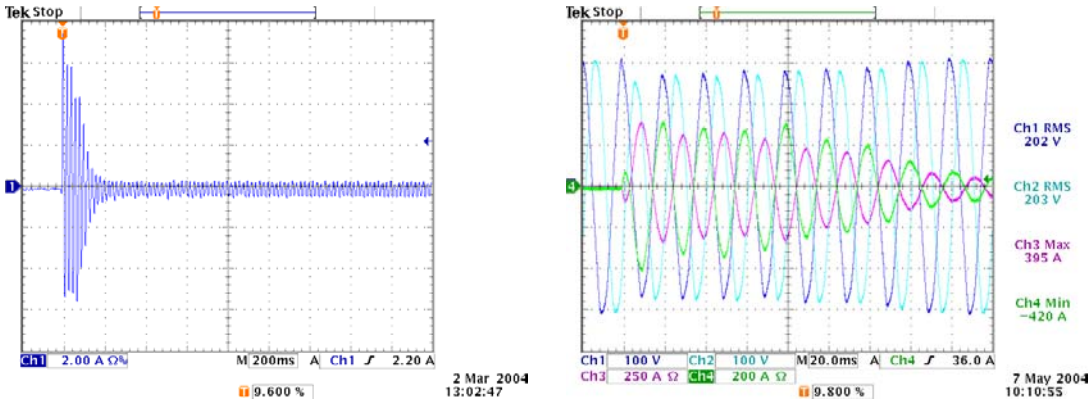
(a) (b)

Figure 4-6: Output Waveform of the High-Power Test for a Time Interval of: (a) 200 ms (b) 40 ms

These voltage and current values result in a power of 144 kW. The current in phase A is in phase with the voltage in phase A, due to the purely resistive load. The impedance of the induction machine is, however, more inductive than resistive.

4.2.5 Peak-Current Test

Very high currents are consumed when the SES starts up, as seen in Figure 4-7 (a) and in Figure 4-7 (b). This high starting current is utilized to crank the IM. Figure 4-7 (a) shows only the starting current, which was measured before the system was installed. The waveform in Figure 4-7 (b) was taken on the SES on site after the system was installed in Johannesburg. At this time the SES operated from the ESKOM grid. In Figure 4-7 (a) and (b) it is shown that the SES consumes a peak current of 420 A for one cycle (20 ms), and 300 A for another two cycles. Both figures show only a single-phase current. It is concluded from Figure 2-27 that the start-up currents in the other two phases could have greater magnitudes.



(a) (b)

Figure 4-7: Start-up Waveform of the SES: (a) Phase Current; (b) AC Voltages and AC Current

The bidirectional converter was connected between the battery bank and a big load. A resistive load of R_{load} = 0.7 Ω is connected to each phase as seen in Figure 4-8. The battery voltage was V_{DC} = 746 V.

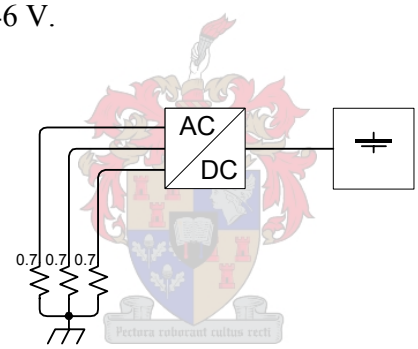
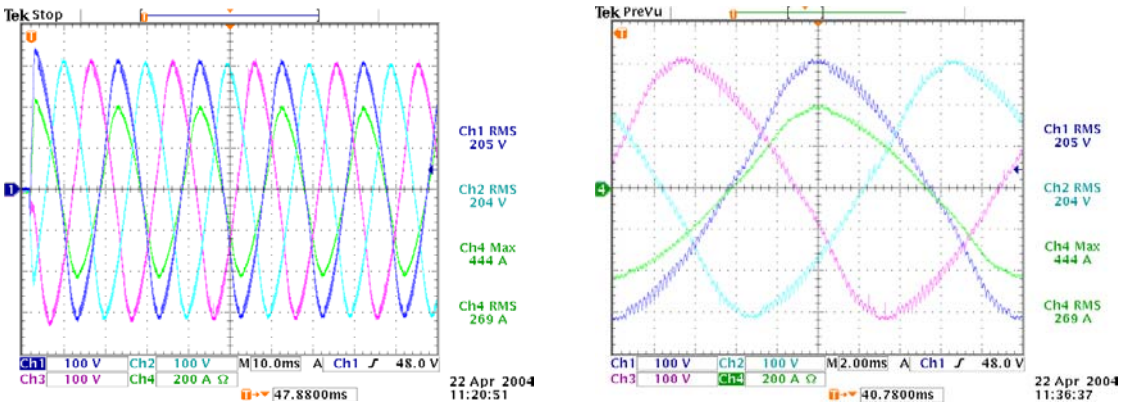


Figure 4-8: Practical Setup of the Peak-Current Test

The DSP was programmed so that the converter switches for 5 cycles (100 ms) before shutting down. This time gap is much greater than the required value of 20 ms. The switch of the converter was turned to its "ON" position. The converter started up and initiated switching. After 100 ms the inverter stopped switching and shut down. Using an oscilloscope, the output voltages as well as the output current were measured, as seen in Figure 4-9. Figure 4-9 (b) shows an enlarged view of Figure 4-9 (a). The RMS output voltage of each phase is about 205 V_{RMS}, which is nearly within the 10% margin of 230 V. The RMS current is 269 A and the peak current is 444 A. These results show that the converter can handle very high peak currents and at the same time provide the necessary AC output voltages. This experiment showed that the inverter can handle a high-peak

current of 444 A. The results are as expected and match the simulations in Figure 2-23 and Figure 2-24.



(a) (b)

Figure 4-9: Waveform of the Peak-Current Test for a Time Interval of: (a) 100 ms; (b) 20 ms

4.2.6 Voltage and Current Ripple Measurement

The voltage and current ripple are calculated from the results achieved from the average-power test in Figure 4-4. The peak to neutral voltage is V_{PN} = 330 V and the peak to neutral current is I_{PN} = 70 A. Figure 4-10 gives an enlarged view of the waveforms in Figure 4-4. It is shown in Figure 4-10 that the voltage ripple is 8 V and the current ripple corresponds to a value of 1.62 A. The percentage voltage ripple is calculated as follows:

$$\begin{aligned} \Delta V_{\%} &= 100 - 100\frac{V_{PN} - V_{Ripple}}{V_{PN}} \\ &= 100 - 100\frac{330 - 8}{330} \\ &= 2.42\% \end{aligned} \tag{4-1}$$

And the percentage current ripple is:

$$\begin{aligned}\Delta I_{\%} &= 100 - 100\frac{I_{PN} - I_{Ripple}}{I_{PN}} \\ &= 100 - 100\frac{70 - 1.62}{70} \\ &= 2.31\%\end{aligned} \tag{4-2}$$

It is concluded that the filter design was successful. The practically measured ripple values are better than the ripple values achieved in the simulations done in paragraph 2.7.8.

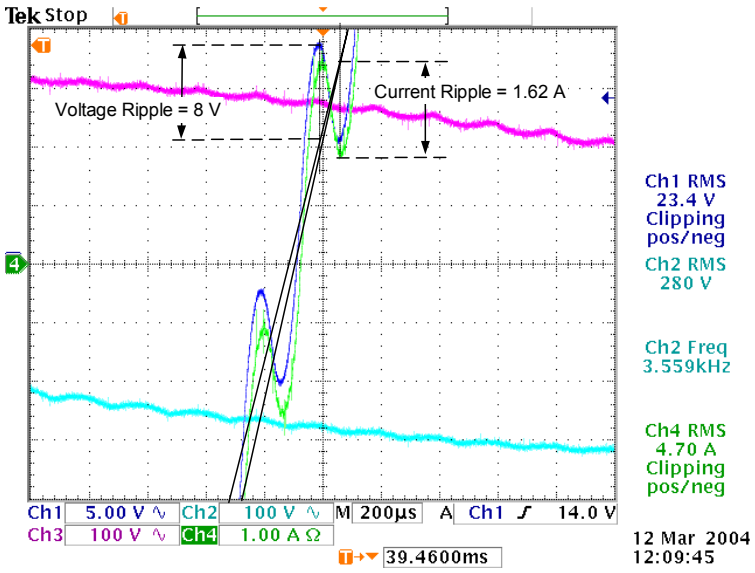


Figure 4-10: Voltage and Current Ripple Measurement

4.2.7 Load Management Control

The SES could not be modelled in the laboratory and thus the load management control could not be tested perfectly. To model a SES, a power source is required that delivers a constant power no matter if the load is big or small. Without load the SES overheats. The best way to test the load management control is to disconnect the converter from the AC bus, as seen in Figure 4-11, and having a constant three-phase 400 V_{LL} voltage source connected to the AC bus. A separate DC bench power supply together with a varying resister was used to model the DC current, which represents the DC current that flows

into the battery bank. The current sensor, which normally measures the current through the positive terminal of the battery bank, measured the DC current provided by the bench power supply. This DC current was varied with the resistor R_{DC}, as seen in Figure 4-11. The circuit configurations of the thyristor driver and its load R_{DUMP} are shown in Figure 4-11.

The different channels (CH1, CH2, CH3 and CH4) in Figure 4-12 and Figure 4-13 refer to the measured values in Figure 4-11. If the battery bank voltage is between 730 V and 810 V, as in Figure 4-12, the charging current corresponds to 10 A. Section 3.6 discussed the operation of the load management. The thyristor driver started conducting at a DC current (CH3) of 9.62 A, as seen in Figure 4-12 (b). In Figure 4-12 (c), (d), (e) and (f) it is shown how the load currents (I_{DUMP} "CH4") vary with an increase of the DC current, which is proportional to the thyristor control voltage (CH1). The load current (I_{DUMP} "CH4"), in Figure 4-12 (f), is a perfect sine wave. This means that the thyristors are acting as a short-circuit and a power of

$$P_{3\phi} = 3 \cdot \frac{V_{LN}{}^2}{R} = 3 \cdot \frac{230^2}{4} = 39.6 \text{ kW} \tag{4-3}$$

is dissipated in the load. This amount of power is far greater than the SES maximum output. It is observed that the thyristors are never conducting permanently. The control strategy is closed and thus the charging of the batteries is always around 10 A. In paragraph 4.3.4, where the system is tested together with the SES, it is observed that the charging procedure does not function perfectly.

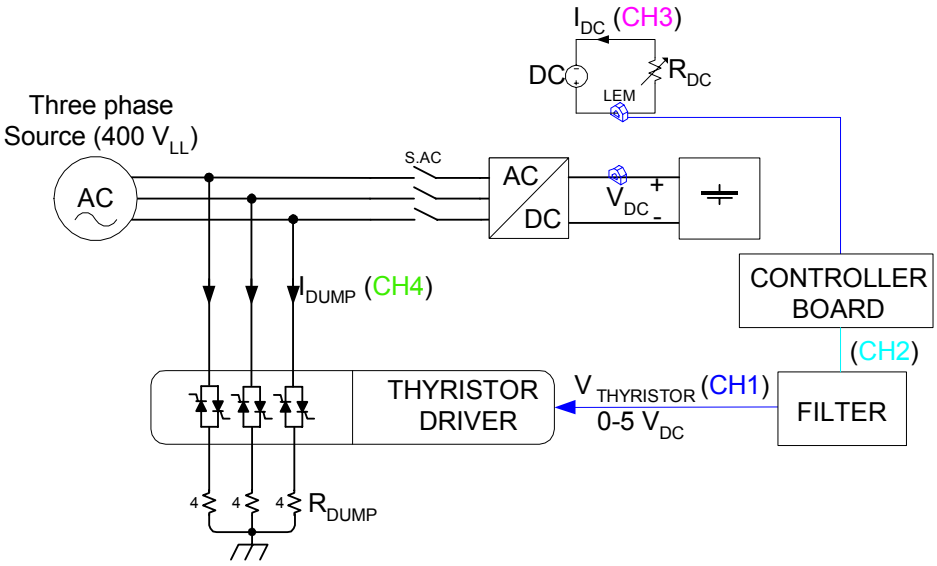


Figure 4-11: Circuit of Load Management Control

If the battery bank voltage is between 810 V and 830 V the charging current is close to zero amperes. The output graphs for the load management result at a high battery voltage are given in Figure 4-13. The thyristors start conducting at a charge current of 152 mA, as shown in Figure 4-13 (a). Figure 4-13 (a), (b), (c), (d) and (e) show how the conducting state of the thyristors increases with an increase in the DC current. This control scheme is designed to decrease the charging current of the battery bank to a minimum. To decrease the current to exactly zero is difficult. Control of the thyristors is lost when the DC contactor is opened. The charging current is zero, if the DC contactor is opened, but the amount of power dissipated in the dump load cannot be controlled. Another problem arises when the SES suddenly acts as a load instead of a source and power needs to be drawn from the battery bank.

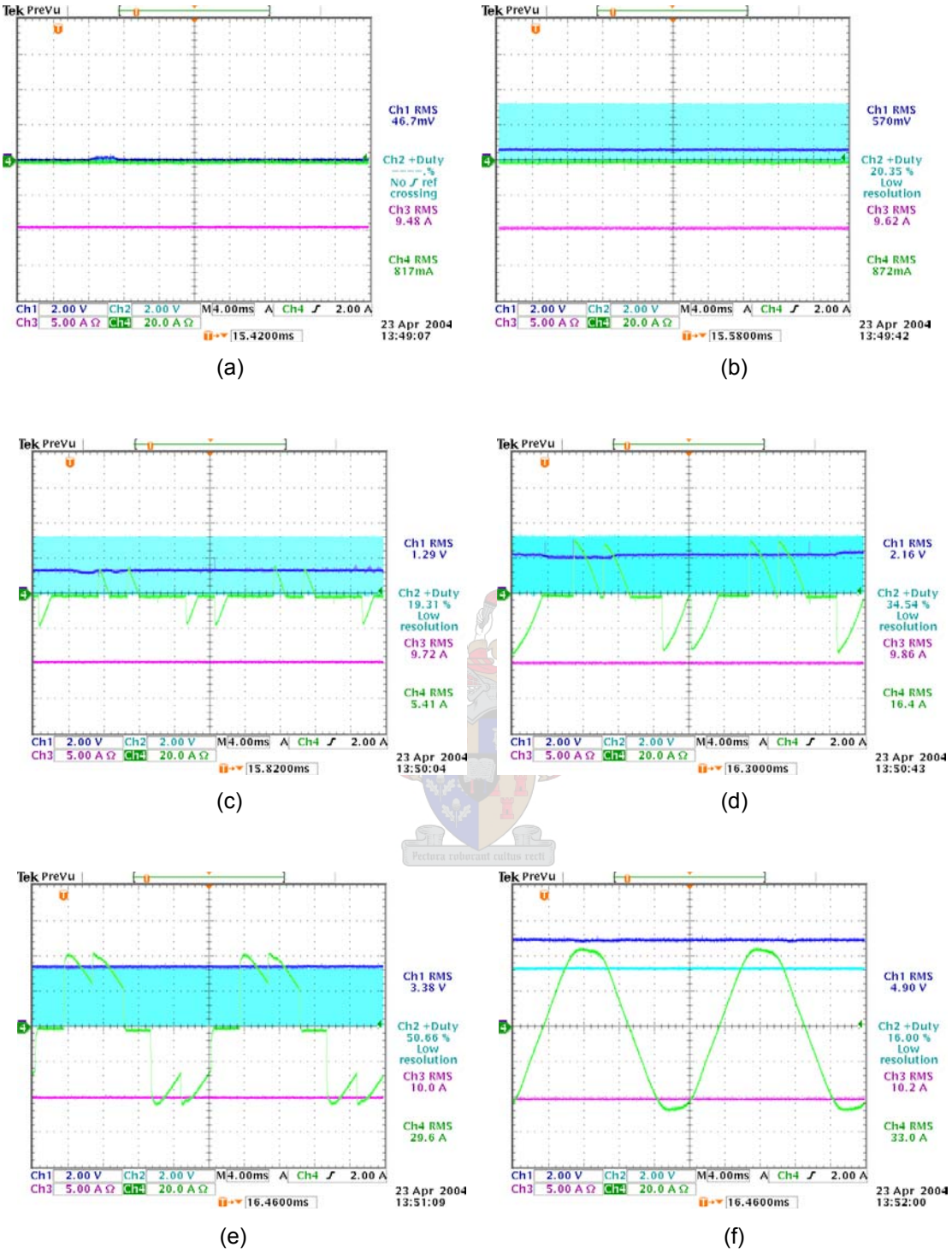


Figure 4-12: Load Management Results for 730 V < V DC < 810 V and a DC Current of (a) 9.48 A; (b) 9.62 A; (c) 9.72 A; (d) 9.86 A; (e) 10 A and (f) 10.2 A

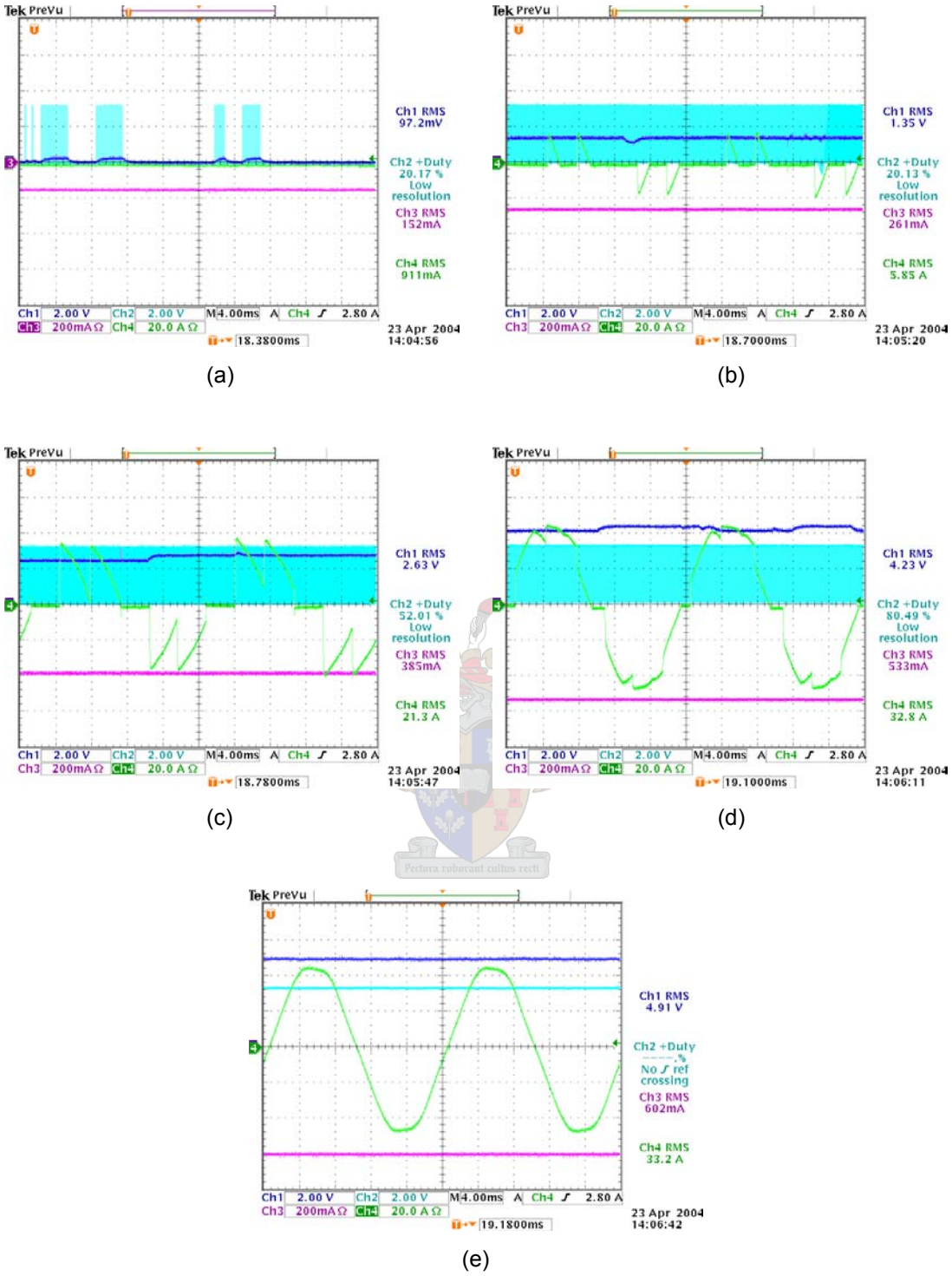


Figure 4-13: Load Management Results for 810 V < V DC < 830 V and a DC Current of (a) 152 mA (b) 261 mA; (c) 385 mA; (d) 533 mA and (e) 602 mA

4.2.8 Protection Tests

The unit is protected from DC over-voltage, DC under-voltage and DC over-current. The protection routine was tested and showed good results.

The first test done was the over-voltage protection test. The converter shut down at a voltage of $V_{DC} > 830$ V, which corresponds to the DC bus voltage when the batteries are fully charged. The bidirectional converter was connected between the high DC varying power supply and the load. The system was switched on and initiated switching. The DC bus voltage was slowly increased up to a level of about 830 V, where the system shut down. It opened the three-phase AC contactor as well as the DC contactor. This isolated the converter from the battery bank as well as from the AC load/source. The DC capacitors are discharged via the dump resistor. A LED (LED3) inside the electrical box ignited to show what error had occurred. This function protects the batteries from overcharging.

The second test done protects the batteries from undercharging. The converter shut down at a voltage of $V_{DC} < 730$ V. This test was done in the same way as that in the experiment above. The only difference is that the system shut down when the DC battery voltage reached a voltage of 730 V or below. A different LED (LED4) ignites to show that an under-voltage error has occurred.

The third test examined the battery charge current. If the DC current, flowing into the batteries, is above 12.7 A the system shuts down. This function is another form of protection for the batteries. This function was tested with a bench power supply which could deliver a current of 13 A. The system shut down at a current value of 12.7 A. If the over-current fault occurs, a different LED (LED2) ignites and the system shuts down safely.

The system can easily be shut down. The switch on the front of the box must be switched to its "OFF" position. This isolates the converter from the battery bank and the load or the SES. This feature was tested numerous times.

4.2.9 Temperature Measurements during Operation

Thermal management is an important aspect in electronic design. Every electronic component is rated for a specific temperature range. A component may not function correctly if its operating temperature is outside its temperature range. Table 6 provides a few examples of components used and their temperature range.

Component	T_{MIN} (˚C)	T_{MAX} (˚C)
SKIM500GD128DM	-40	+150
SKHI65	-40	+85
12V Lead-Acid Battery	5	+50
EV200 (Contactor)	-40	+85
IRF540N	-55	+175
SN75451	0	+70
Inductor	0	+150

Table 6: Temperature Range for some Components utilized

Temperature measurements were done to ensure that the system functions in the specified temperature range which suits each component. Some power is converted to heat through power conversions. The two main devices, in this system, that generate most heat are the filter inductors and the IGBT module. Due to a physically closed system, the heat spreads in the air throughout the enclosure.

From Table 6 it is concluded that the heat-sink temperature of the IGBT module may never rise above 150˚C. The air temperature inside the converter box may never rise above a temperature of 50˚C, which corresponds to the lowest maximum temperature of all components. The last temperature consideration is the temperature of the inductors. The inductors build up great heat due to the energy they must store during switching. The temperature of the inductors must not exceed 150˚C. Forced air cooling decreases the

temperature on the heat-sink as well as the temperature inside the converter box. Figure 4-14 shows the temperature flow model of the system.

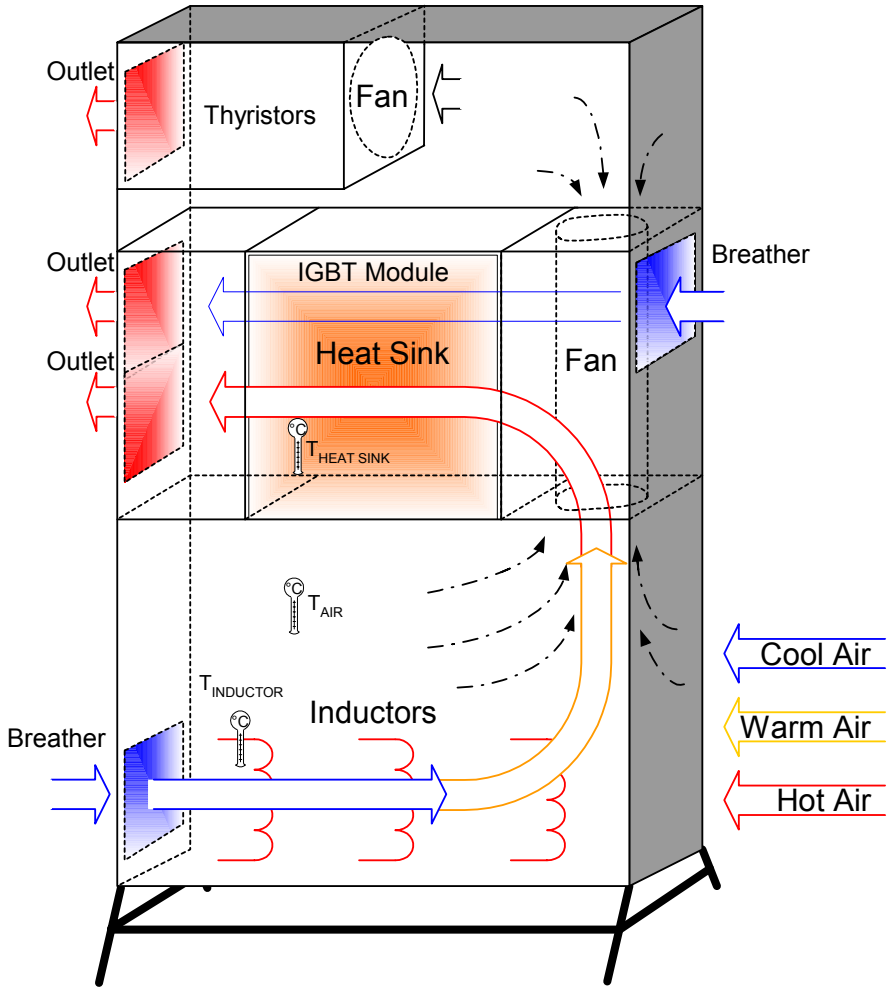


Figure 4-14: Temperature Flow inside the System

The system has two breather intakes and three outlets as seen in Figure 4-14. A small fan, placed in the top left corner of the box, cools down the thyristors. A bigger fan, placed onto the heat-sink where the module is mounted, sucks fresh air from the right intake as well as from the bottom left intake. The cool air from the bottom left corner decreases the inductor temperatures. The air is warmed up before it reaches the fan. This warm air is used to cool down the heat-sink. To compensate for the warm air, a breather hole is inserted onto the right side of the box, which decreases the heat-sink temperature.

Temperature sensors were placed on three different devices. The heat-sink temperature, one inductor temperature and the air temperature in the box were considered as seen in Figure 4-14. These measurements give a good overall impression of the temperature flow in the box. The system was connected as in Figure 4-15.

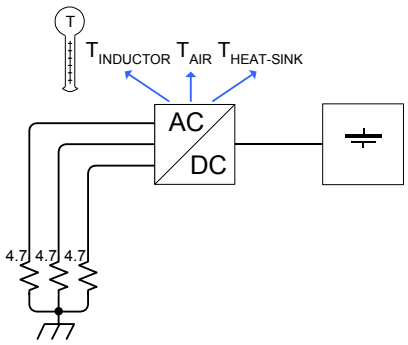


Figure 4-15: Practical Setup for Temperature Measurements

The converter box was closed, so that no air could flow into the box except through the breather holes mounted on the sides, and was switched on for about four hours. Measurements revealed: V_{DC} = 746 V; V_{AC} = 230 V per phase; I_{AC} = 49 A per phase; P_{avg} = 33.77 kW. The output waveforms are identical to those in Figure 4-4. Each five minutes a temperature reading for all three devices was taken. Theses reading were then plotted with MATLAB®. The inductor temperature was plotted against time, shown in Figure 4-16.

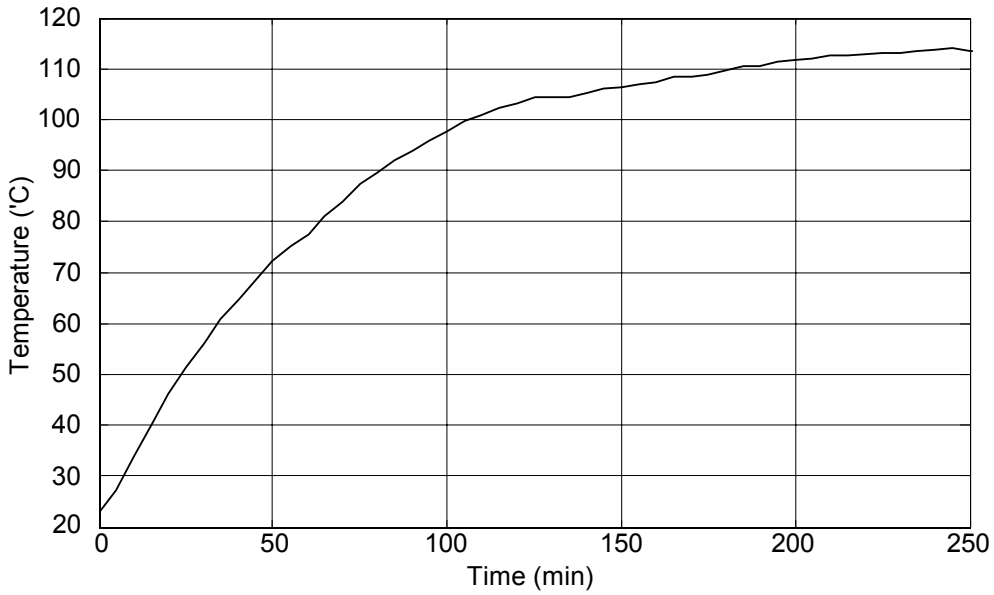


Figure 4-16: Inductor Temperature vs. Time

The inductor temperature stabilizes at about 115 ˚C, as shown in Figure 4-16. The system was delivering power at 33.77 kW, for this experiment, which is much greater than under normal operation. This implies that the heat generated during normal operation is less than that shown in Figure 4-16. The measured inductor temperature values are quite high, but they are in the temperature range and thus functioning sufficiently.

Figure 4-17 shows the temperature against time graph of the heat-sink. It is observed that the temperature stabilizes after about four hours (240 min) to 48˚C. This temperature value is far below that of the maximum permissible value of 150˚C. It is thus acceptable to use the warm air of the inductors to cool off the heat-sink. The air intake is the same for both breather holes. It is concluded that the heat-sink design was successful.

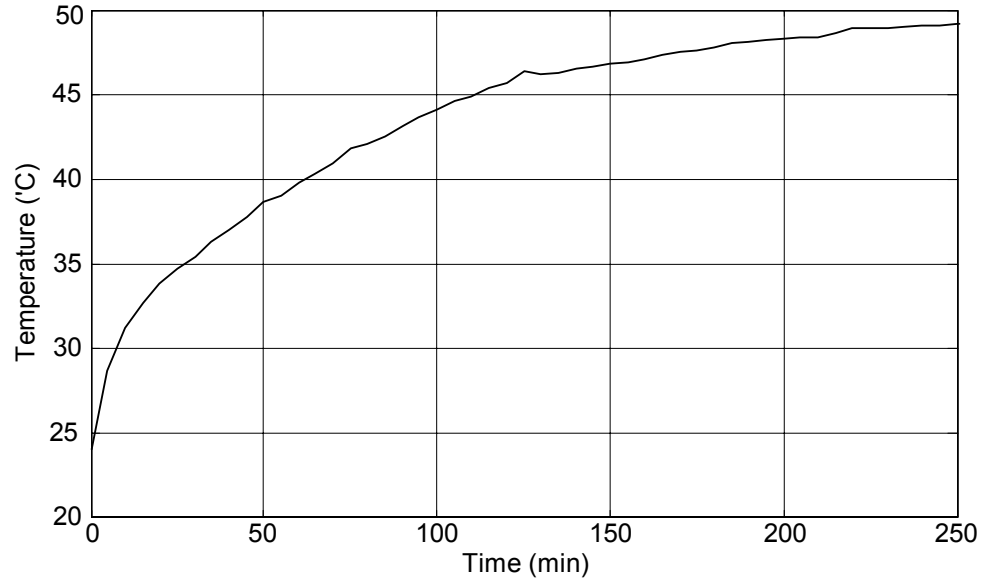


Figure 4-17: Heat-Sink Temperature vs. Time

Figure 4-18 shows the air temperature against time graph. The curve flattens at about 35.5˚C. This value is below the maximum operating temperature of the 12 V batteries. It is concluded that all three measured temperatures are within the permissible range.

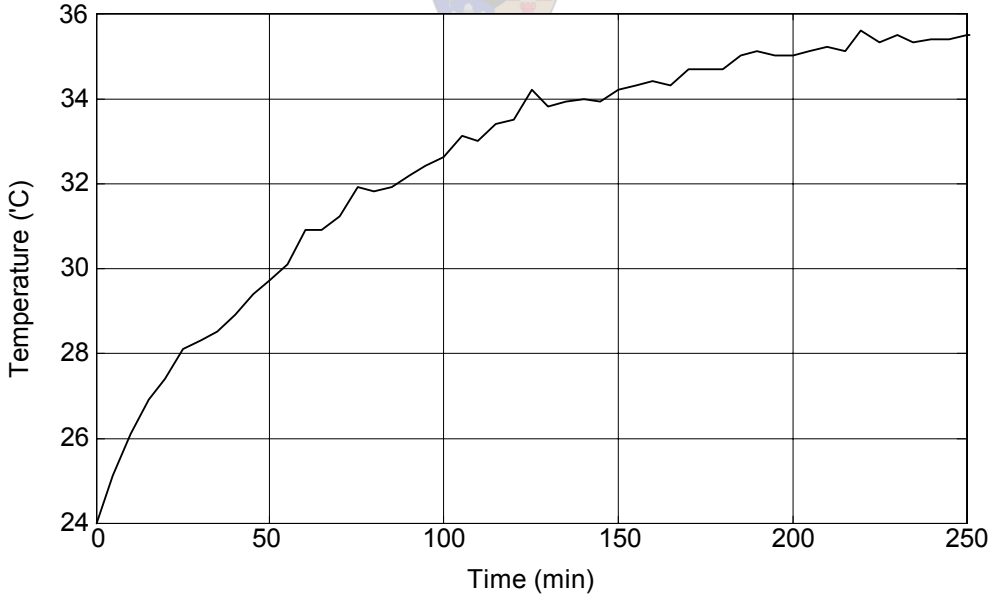


Figure 4-18: Air Temperature vs. Time

4.3 Implementation and Results on Site

4.3.1 Introduction

The converter together with the batteries was transported to Midrand, Johannesburg. The system was implemented at the Development Bank of Southern Africa (DBSA). After the delivery was made on site, the system was installed in the inside of a normal container. The container is situated 10 metres away from the SES. Figure 4-19 shows a picture which was taken of the converter unit inside the container.

Figure 4-19: Picture of the Converter Implemented at Site

The battery rack was placed in the one corner of the container. Fifteen batteries are connected in series in each shelf. Each of the four shelves has a positive and a negative terminal. A DC voltage of 746 V was obtained when all four shelves were connected in series. High-power fuses were connected to the battery bank terminals for safety. The battery rack is shown in Figure 4-20.

Figure 4-20: Picture of the Battery Rack Implemented at Site

Figure 4-21 shows a picture taken at the DBSA with the SES in the foreground. The SES just "woke up" and started to turn the dish towards the sun.

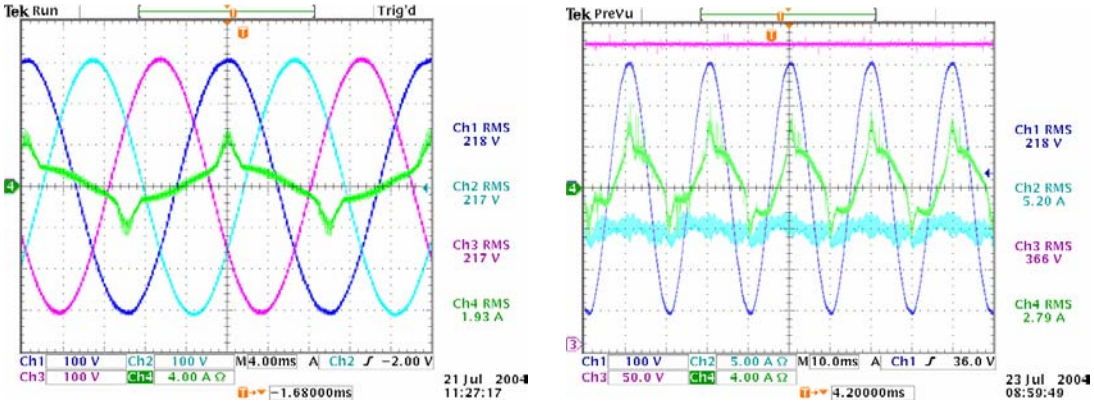
Figure 4-21: Picture of the SES with the DBSA in the Background

Field experiments were not as uncomplicated as lab tests. Each time the SES started up, it needed to focus the concentrated sun beam on the thermal receiver. The time required for a single experiment ranged between 30 minutes and two hours, depending where the sun is situated at that time during the day. The SES must be in the night-stow position before

an experiment is done. From this position it "wakes up" and starts moving towards the sun. If a start-up was not successful, the dish moved to an offset-track position where it is safe from getting burned by the heat beam. The dish must first go to the night-stow position before the next start-up is made.

4.3.2 Inverter Operation before Start-up

System operation was started by switching the system on. The SES was connected to the three-phase AC bus. Figure 4-22 (a) shows the three-phase output voltages as well as the phase current of phase A. CH1, CH2 and CH3 represent the phase voltages of phase A, B and C respectively. These output waveforms, in Figure 4-22 (a), were measured while the SES was in night-stow position. This means that no current is consumed by the SES. The current drawn from the system is utilized in the inverter fans. An RMS value of 1.93 A is consumed by the fans. The phase voltages are 120˚ phase shifted and correspond to the same phase sequence as the phase sequence of ESKOM. It is compulsory that the phase sequences match up with ESKOM. If the sequence differs, the solar dish pivots in the wrong direction and thus never finds the sun. As soon as the solar dish is in motion, it consumes a small amount of current. This is shown in Figure 4-22 (b), where an amount of 2.79 A per phase is drawn from the inverter.



(a) (b)

Figure 4-22: Inverter Output before Start-up: (a) SES is stationary (b) SES is in tracking mode.

CH2 in Figure 4-22 (b) represents the DC current flowing out of the batteries which correspond to 5.2 A. CH3 is measured between neutral and the positive terminal of the battery bank.

4.3.3 Start-up

The control system of the SES operates from the three-phase supply. It is thus compulsory that the three-phase output voltages remain within a certain range during operation and especially during start-up. A soft start of the induction motor is thus impossible. If the AC voltages fall outside of a certain threshold of 360 V < V_{LL} < 440 V, the system controller recognizes the error and operation discontinues. The main problem to overcome was to meet the enormous starting current of the IM. A peak current of 528 A was measured during start-up. The over-current protection feature tripped the IGBT module several times when the SES initiated start-up, as seen in Figure 4-23, which is an example of an unsuccessful start-up. The IGBT module is rated for a peak current of 723 A [16]. After several unsuccessful start-ups, it was concluded that the SKHI 65 driver's trip feature is not accurate and that it tripped at lower current levels than rated for. Later it was realized that the filter inductors saturated and that the measured current corresponded to the filtered current. The saturation of the inductors is examined at the end of this section.

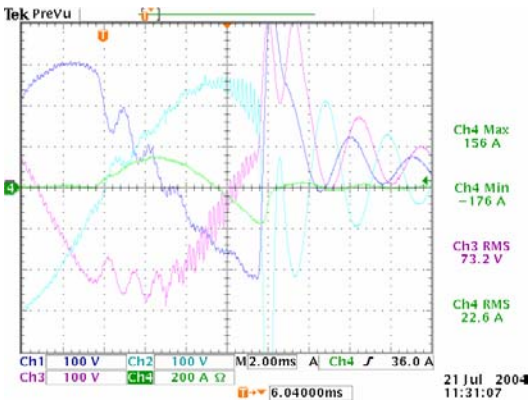


Figure 4-23: Unsuccessful Start-up of the SES with a Total Current Protection

It is noticed that the peak current measured at the instant that the module tripped (in Figure 4-23) corresponded to 176 A. The current is represented by CH4. All three output phases had current sensors connected to the driver and thus a total over-current protection was available. The phase current (CH4), in Figure 4-23, was measured only on phase A. Due to a lack of current probes the other two phases could not be measured simultaneously. It is concluded from Figure 2-27 that the current in the other two phases could have tripped the module, since their magnitudes could have been higher.

A possible solution to this problem was to decrease the amplitude of the starting current. This was done by reprogramming the DSP so that the AC bus voltage is smaller. Current is proportional to voltage. The implementation was successful in that the SES started up, as observed in Figure 4-24. Figure 4-24 shows three different successful start-ups with their enlarged views next to them. The system controller of the SES, however, gave an error signal due to an under-voltage on the AC bus, which corresponded to about 190 V RMS, as seen in Figure 4-24. This resulted in a command that set the SES to an offset-track, where it had to be reset. Decreasing the AC bus voltage was thus no solution.

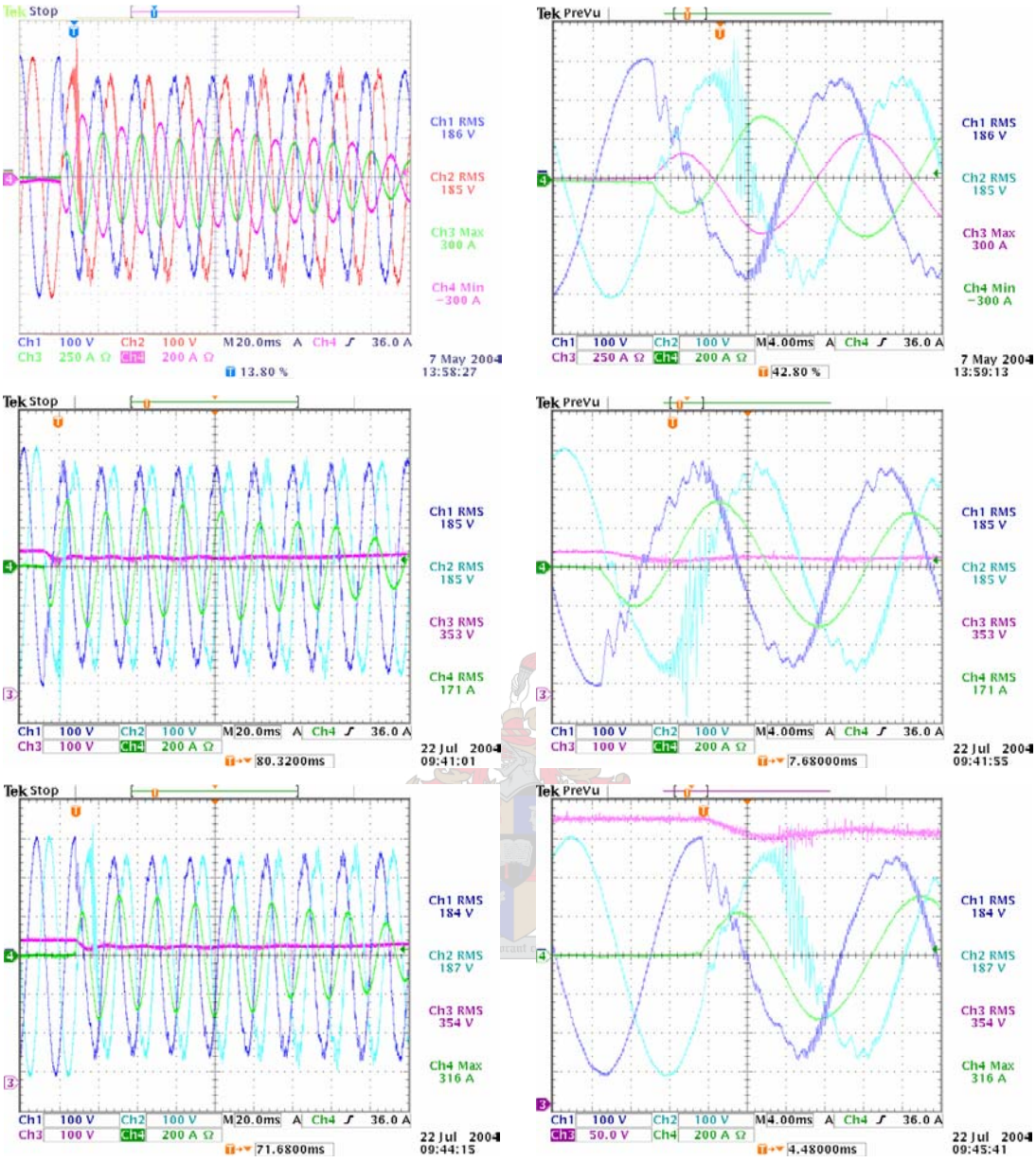


Figure 4-24: Successful Start-ups of the SES from the Inverter but unacceptable Bus Voltages

Another option considered was to disconnect two current sensors, those of phase B and C, and measure the current of the third phase (A). This was done to ascertain that the module tripped because an over-current fault. The module was thus only protected on phase A. Figure 4-25 reveals some unsuccessful start-ups with only one current protection. It is observed that the module tripped at currents with peak magnitudes of 470 A, 440 A and 368 A. The current was measured behind the filter inductors. At the end of

this section it is shown that the current ripple before the L-C filter caused the module to trip. The magnitude of the peak current including the current ripple, before the L-C filter, is not known.

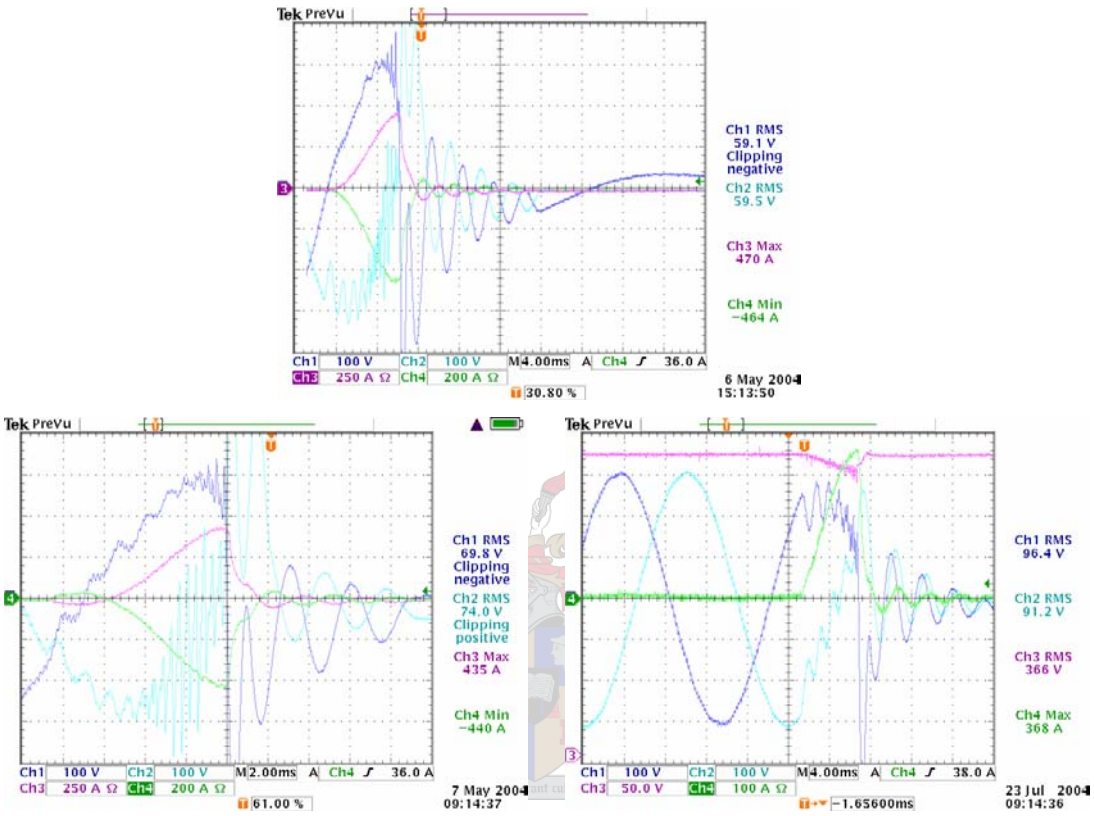
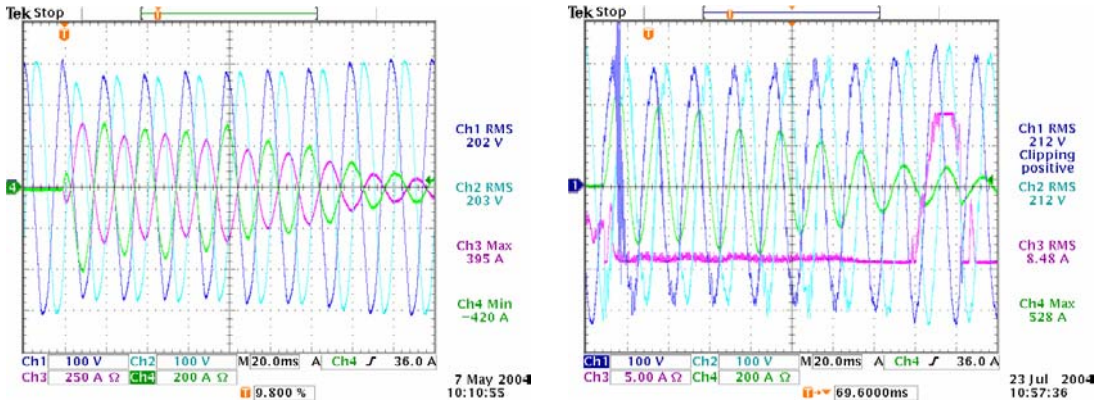


Figure 4-25: Unsuccessful Start-ups of the SES with only One-Phase Current Protection

Now all the current sensors were disconnected to disable the over-current protection feature, with the aim of having a current lower than the maximum value of 723 A. This was done since no other option seemed available. The ESKOM start-up is shown once again in Figure 4-26 (a). Figure 4-26 (b) shows the successful start-up from the inverter. The magnitude of the start-up voltages were within the range of the required SES controller voltages. CH3 in Figure 4-26 (b) represents the DC current. This current was measured with a probe which can measure 8 A RMS maximum. That is the reason why the current magnitude clips at ±8 A.



(a) (b)

Figure 4-26: Successful Start-up of the SES: (a) from the Inverter (b) from ESKOM

Figure 4-27 shows another successful start-up. The DC bus voltage (measured between positive terminal and ground) represented by CH3 in Figure 4-27 drops about 25 V.

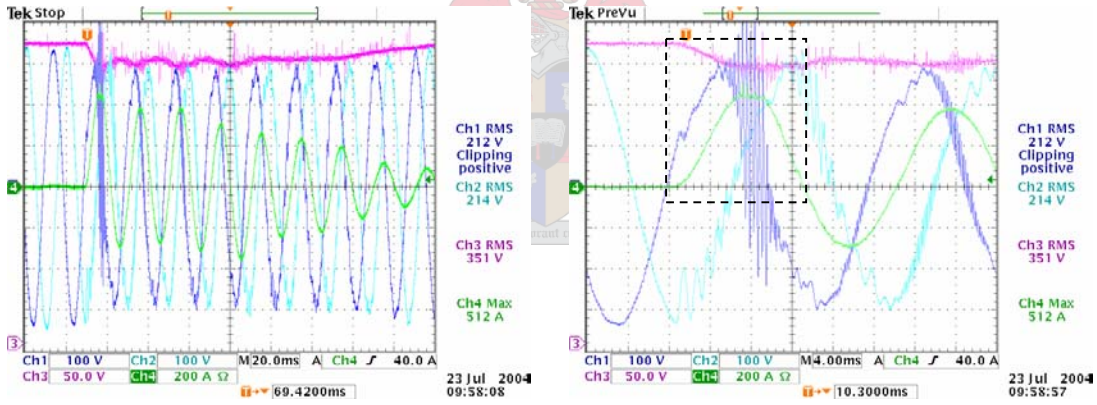


Figure 4-27: Successful Start-up of the SES from the Inverter with its enlarged view

The simulated result in Figure 2-25 matches the start-up waveforms in Figure 4-26 and Figure 4-27.

It is noticed in Figure 4-24 that the AC voltage drop at start-up is larger compared to those in Figure 4-26 and Figure 4-27. Another observation is that the peak currents in Figure 4-24 are less than those in Figure 4-26 and Figure 4-27.

The saturation of the filter inductors led to high-current ripples, which in turn caused the IGBT module to trip. The inductance (L) of an inductor decreases rapidly as it saturates and thus causes the inductor to act as a short-circuit. It is shown in Figure 4-28, which is an enlarged view of Figure 4-27 indicated by a square, that the inductors saturate at about 440 A. They are designed to withstand a peak current of 440 A. Figure 4-29 shows the current which is flowing through the inductor.

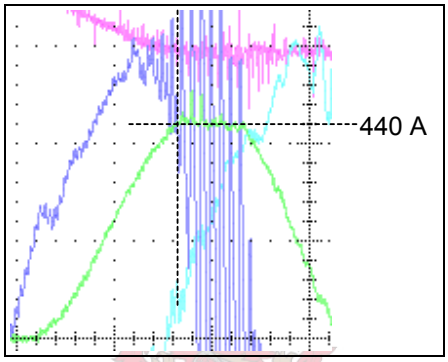


Figure 4-28: Enlarged view of Figure 4-27 where the Saturation Current is observed

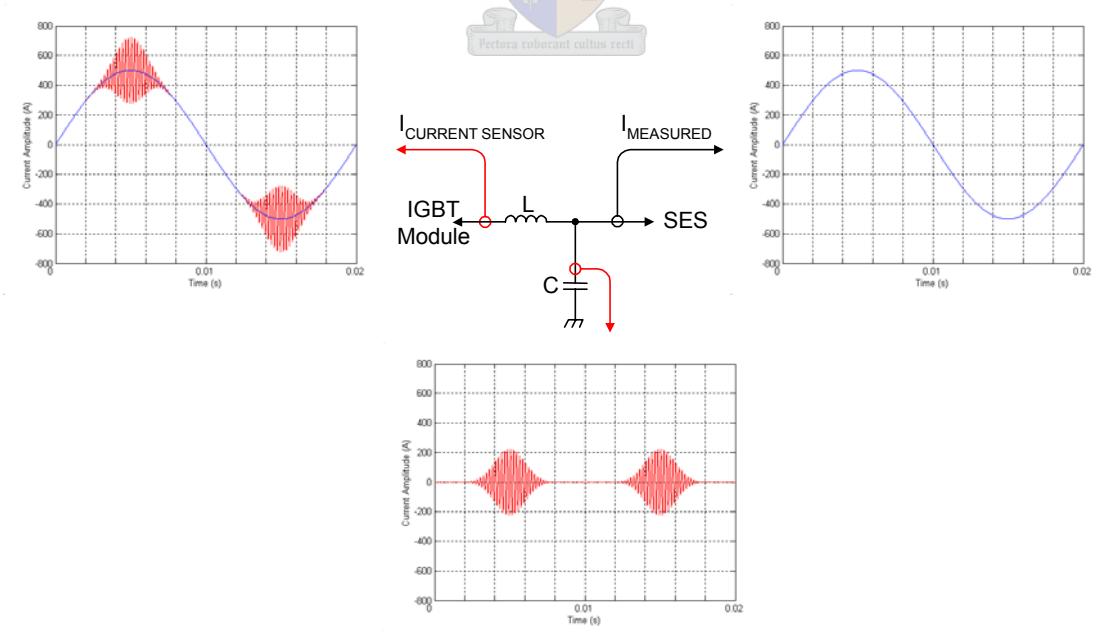


Figure 4-29: Diagram of the Filter including the Effect of Saturation

The current measured during measurements on site corresponds to $I_{MEASURED}$. This current did not include the ripple current that flowed into the filter capacitor (C), as seen in Figure 4-29. The measured current that caused the module to trip corresponds to $I_{CURRENT\ SENSOR}$. The peak value of $I_{CURRENT\ SENSOR}$ is far greater than the peak current measured ($I_{MEASURED}$).

4.3.4 Load Management Control

The basic operation of the load management control functioned acceptably. The SES initiated power generation after a successful start-up, which was shown in Figure 4-26 (b). The DC over-current protection feature had to be disabled after it had shut down the system. A DC over-current error occurred, since the time utilized for the load management system to react to an over-DC-current was too long. The DC current, represented by CH4 in Figure 4-30 (d), increased to a level above 12.7 A before the system could compensate and the power generated by the SES could be dumped. After the protection feature was disabled, the system was restarted and measurements were taken as seen in Figure 4-30. It is observed that the system oscillated. The cause of this is that the gain (k) of the feedback control system in Figure 3-40 was too large. This could easily be solved by reducing the gain. Simulations at the end of this paragraph show how this is achieved as well as what the output waveforms should look like. Practical implementation of this was not possible.

CH3 in Figure 4-30 (a) represents the DC current which was measured with an 8 A RMS current probe. This is the reason why the waveform clips at ±8 A. Only one current probe was available. It is noticed that the DC current alternates between charging and discharging of the batteries. The thyristor dump signal (CH1) is either high or low as a result of the large feedback gain. CH4 in Figure 4-30 (a) represents the phase current (phase A) generated by the SES. This current corresponds to a generated power from the SES of:

$$\begin{aligned} P_{out3\phi} &= 3 \cdot V_{LN} \cdot I_L \\ &= 3 \cdot 220 \cdot \frac{44.6}{\sqrt{2}} \\ &= 20.81 \text{ kW} \end{aligned} \tag{4-4}$$

This generated power was consumed by the battery bank as well as by the dump load. The battery bank could not be charged at a constant rate due to the feedback oscillations.

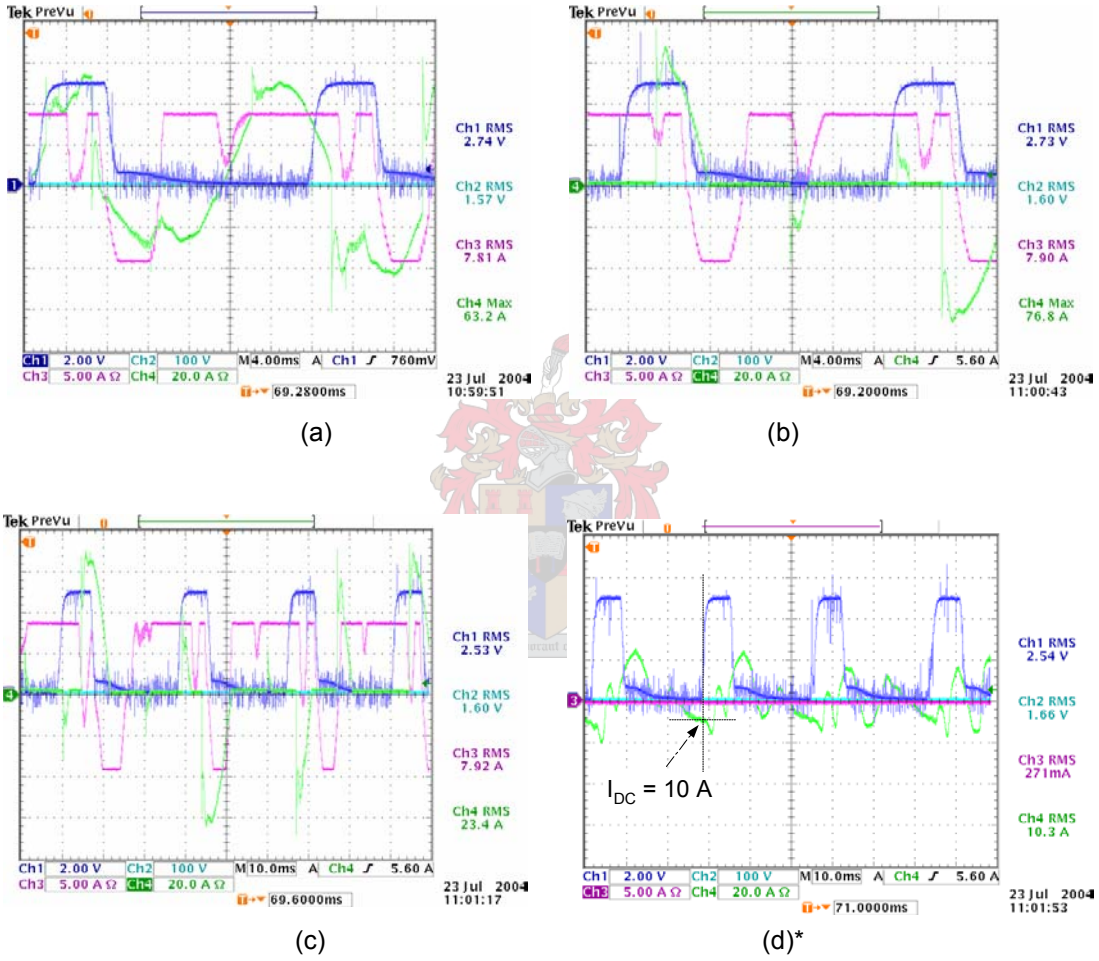


Figure 4-30: Load Managements Results showing Thyristor Dump Signal "CH1" and: (a) AC Current Input; (b) DC and Dump Current; (c) DC and Dump Current; (d) DC Current

(*Figure 4-30 (d) Note: Positive current (CH4) corresponds to discharging of the battery bank)

The oscilloscope result presented in Figure 4-30 (c) is shown again in Figure 4-31 where three different states (A, B and C) have been declared on the time scale. Each state

represents a different system operation, as shown in more detail in Figure 4-32, indicated by three different blocks. Each state corresponding to their system operation is described in detail.

During state A the converter functions as a rectifier, as seen in Figure 4-32, where the indicated DC current (CH3) flows towards the battery bank. The thyristor control signal (CH1) is low during this 12 ms time interval (t_A). No power is dissipated by the dump load ($P_{DUMP} = 0$). The total power generated by the SES is stored in the battery bank ($P_{SES} = P_{BATTERY}$).

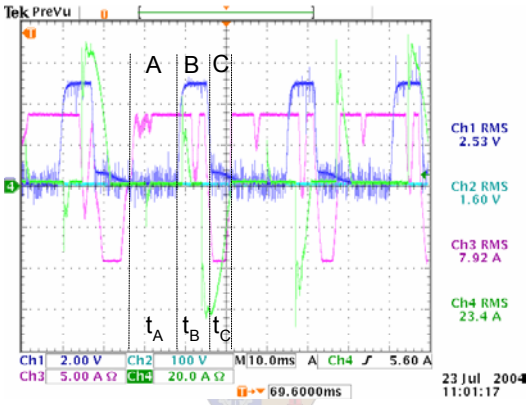


Figure 4-31: Load Managements Result with indicated States

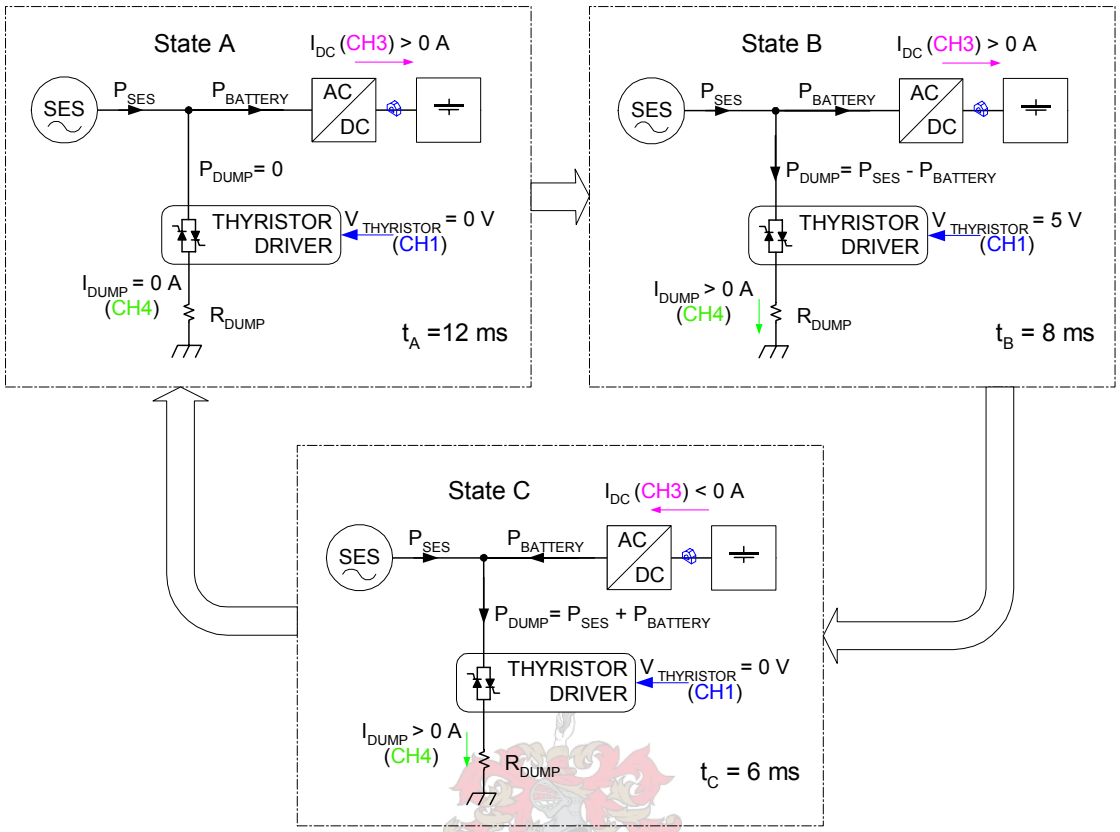


Figure 4-32: Load Management Operation for different States corresponding to Figure 4-31

The first dissipation of power into the dump load occurs in state B. This is seen in Figure 4-31 by the non-zero dump current (CH4) of phase A. The difference in generated power and the power stored is dumped ($P_{DUMP} = P_{SES} - P_{BATTERY}$). From Figure 4-30 (d) it is observed that the thyristor control signal (CH1) changes its value from 0 V to 5 V as soon as the DC current reaches a value of 10 A. (Note that a positive DC current in Figure 4-30 (d) discharges the batteries.)

The converter acts as an inverter during state C, which is observed by the negative DC current (CH3) in Figure 3-31. The cause of this is that the thyristor module is acting as a short-circuit and a power of 39.6 kW, from equation (4-3), is dissipated in the dump load. The SES only generated 20.81 kW. The rest of the power is taken from the battery bank ($P_{DUMP} = P_{SES} + P_{BATTERY}$). The maximum current the batteries are discharged, as seen in Figure 4-30 (d), corresponds to 24 A. This signifies that a maximum power of 17.9 kW is

drawn from the battery bank, which has a voltage of 746 V. This shows that a total power of 38.71 kW is dumped into the dump load, which matches equation (4-3). The batteries are discharged for t_C = 6 ms. This process is repeated periodically starting at state A again.

The above system operation was simulated with SIMPLORER™ to verify that the oscillation occurred because of a too large gain k in the feedback control system. Figure 4-33 shows the simulated waveform corresponding to Figure 4-31. The three different states (A, B and C) are again indicated to verify system operation.

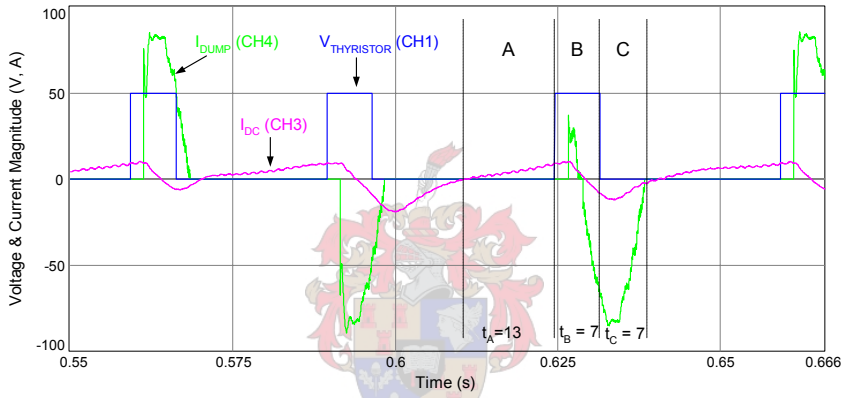


Figure 4-33: Simulation of the Load Management Results corresponding to Figure 4-31

During state A, in Figure 4-33, it is observed that the DC current (I_{DC} (CH3)) flows towards the batteries and that no power is dumped into the dump load. The thyristor control signal ($V_{THYRISTOR}$ (CH1)) is zero, as seen in Figure 4-33. Power is dumped during state B and state C. The thyristor control signal is high during state B. The simulations match the practical results.

The practical result of Figure 4-30 (d) is verified through the simulation in Figure 4-34. The thyristor control signal ($V_{THYRISTOR}$ (CH1)), in Figure 4-34, is set high at a DC current (I_{DC} (CH3)) of 10 A as shown. The channels (CH1 and CH2) refer to Figure 4-30 (d).

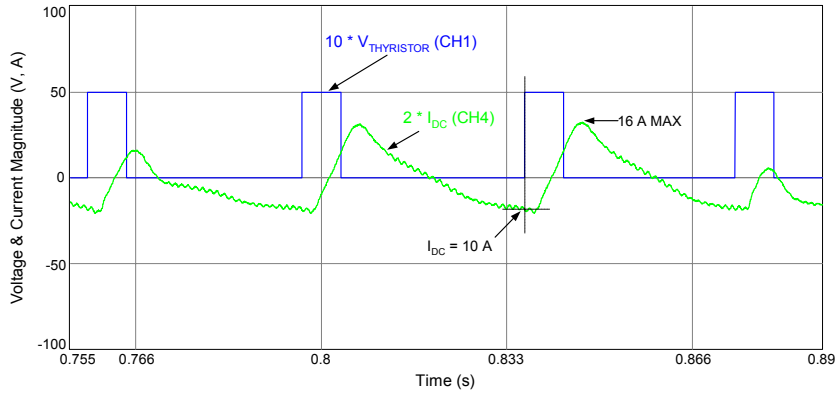


Figure 4-34: Simulation of the Load Management Results corresponding to Figure 4-30 (d)

The gain (k) for the previous simulations corresponded to that in equation (3-40), which was k = 123. This gain was reduced and the system was simulated once more. Figure 4-35 represents the simulated output waveforms of the DC current (I_{DC}), the currents that are dumped into the dump load (R1.I, R2.I and R3.I) and the thyristor control signal ($V_{THYRISTOR\ CONTROL}$). The thyristor control signal is directly proportional to the DC current (I_{DC}). This is the reason why the signal goes negative, as in Figure 4-35. In the practical model, however, the thyristor driver signal is limited between 0 V and 5 V. The thyristor driver in the simulations only reacts to positive values. The motoring and generating regions are shown once again in Figure 4-35.

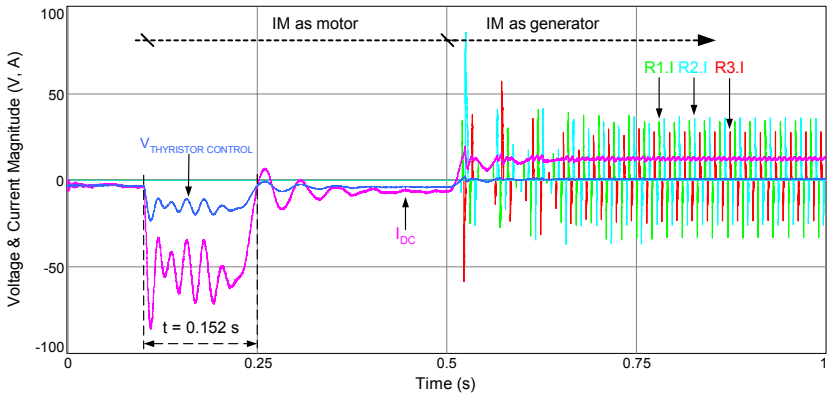


Figure 4-35: Simulation of the Load Management Result showing a Charge Rate of 10 A

Figure 4-36 shows an enlarged view of Figure 4-35. In Figure 4-36 it is observed that the charge current is about 10 A and that the dump currents are triggered by thyristors, which

are phase-angle regulated. The thyristor control signal ($V_{THYRISTOR\ CONTROL}$) had to be scaled by 10 to obtain a better view.

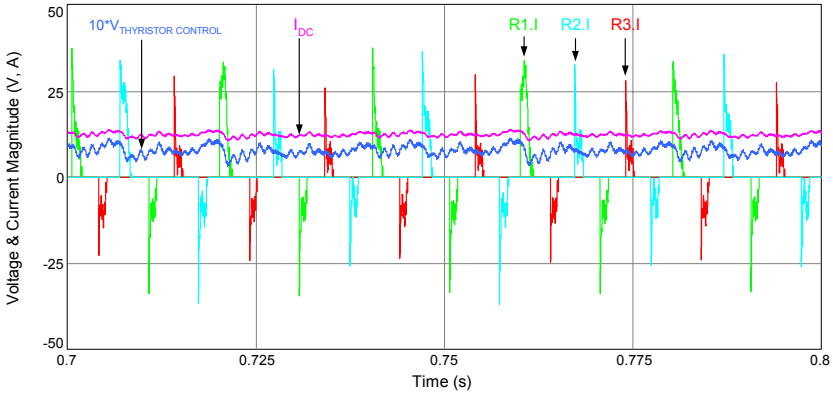


Figure 4-36: Simulation revealing an Enlarged View of Figure 4-35

An interesting event is noticed in Figure 4-35, namely that the DC current becomes positive at 0.25 seconds, which takes place just after the IM reaches synchronous speed. The time elapsed for this overshoot occurred 0.152 seconds after the instant the IM was connected to the grid. This is also observed in Figure 4-37, where the time lapse (t = 0.152 s) is the exactly the same as that in the simulation. This signifies the accuracy of the simulations.

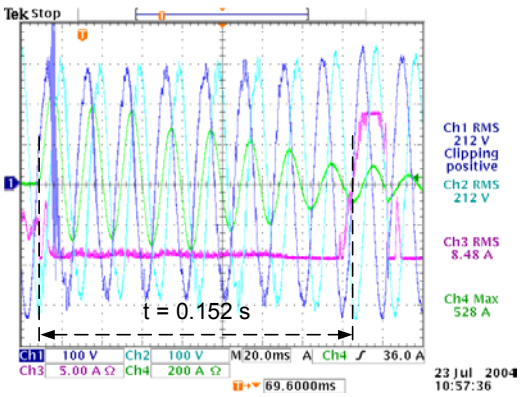


Figure 4-37: Successful Start-up of SES representing the DC Current Overshoot

4.3.5 Protection Test and Efficiency

The module's protection features were all tested as explained in paragraph 4.2.8. The DC over-voltage and DC under-voltage protection features were not tested on site. The DC over-current protection feature was tested, as explained in paragraph 4.3.4, where the system shutdown since a DC over-current occurred. The LED (LED2) ignited and revealed which fault had occurred. The over-current trip feature, available from the SKIM driver, shut the system down a few times. The cause of this shutdown could be traced by LED1, which ignited after an over-current trip fault had occurred. The system could also be shut down manually, which was also tested by switching the converter off with the POWER switch.

The efficiency of the system depends on the solar insolation level and on the reflected sun beams from the mirrors. The mirrors of the parabolic dish were cleaned a day before the experiments were done. Normal operating conditions are defined as:

- Solar insolation 300-1000 W/m^2
- Mirrors Clean
- Operation Steady state (not transient start-up or shutdown)
- Temperature 10^o to 43^o C (50-110^o F)
- Wind velocity Less than 6 m/s (13.5 mph)
- Elevation Less than 1500 m

The solar insolation level for normal operating conditions was given in Figure 2-10, where it is read off that a solar insolation of 875 W/m^2 corresponds to 20.81 kW output power. The total area of the mirrors is 100 m^2. This results in a good solar-to-electric efficiency of:

$$\begin{aligned}\eta_{solar-to-electric} &= \frac{P_{out}}{P_{in}} \cdot 100 \\ &= \frac{20810}{100 \cdot 875} \cdot 100 \\ &= 23.78\%\end{aligned} \tag{4-5}$$

4.4 *Summary*

The practical experiments done in the laboratory were very successful in that the results attained matched the simulated results in Section 2.7. The output voltage and current waveforms were identical to those simulated. This revealed that the filter design was successful. The components chosen were all suitable for the power rating of the converter. None of the components failed or had to be replaced during the laboratory experiments. The converter was tested for a power output of 213 kW for 0.1 seconds. This amount of power is quite large for a small inverter. The output voltage of the inverter could be controlled and was stabilized between 360 V and 440 V. These were the required voltage magnitudes for the SES to operate in a safe region. The voltage drop over the filter inductors could be measured accurately so that the system could compensate for a large starting current. It was proven that the current and voltage ripple of the practical measurement were smaller than those in the simulations. This was thus satisfactory. The temperature measurements revealed that the heat-sink design was successful and that the cooling fans replaced warm air with cool air, thus decreasing the overall temperature of the system.

The physical implementation of the unit on site was successful. The experiments done on site revealed that there were start-up problems. The current drawn from the SES during start-up was higher than expected. It was realized that the inductors saturated. Decreasing the AC bus voltage and disconnecting two current sensors increased the possibility of a successful start-up. It was noted that the system controller of the SES is very sensitive to its supply voltage and thus made it not possible to decrease the starting current. After

disabling the total current protection feature, the SES was started up successfully. The power generated from the SES was dumped into the dump load and at the same time utilized for recharging the battery bank. This proved that the system could function as a standalone unit. Small weaknesses in the feedback control system prevented the system from operating perfectly. The problem was solved and simulation showed how the system should function. The efficiency of the SES was very good when measurements were done.

CHAPTER 5: CONCLUSIONS AND RECOMMENDATIONS

5.1 Background Conclusion

It is concluded that the system design was successful in that it proved to be standalone. Lead-acid batteries were chosen as energy storage device due to their advantages. It was said that the solar dish concept is still in the developmental stage and that this field needed some research. The wind turbine and the PV panel concept are more advanced compared to the solar dish. The dish/engine concept has much higher solar-to-electric efficiencies than other solar technologies and is thus vital for future research. The AC bus topology was chosen, since it has a higher efficiency than the DC bus topology. The high-voltage battery bank has the benefit that a CUK converter is omitted. It can also be concluded that the AC dump load reduces the system power ratings as well as increasing the overall efficiency. 27 Rural households can be supplied by power from the system during the day and the night.

5.2 Consistency of Simulations Compared to Practical Results

The simulation results were consistent and were very satisfactory. The bidirectional converter was manufactured practically and experiment results merged with the simulations. SIMPLORER™ is thus a reliable product and is trustworthy. The experiments done on site revealed that there were start-up problems. The current drawn from the SES during start-up was higher than expected. This led to saturation of the filter inductors, which act as a short-circuit and the result was that the peak current ripples where higher than the IGBT module's over-current trip level. The power generated from the SES was dumped into the dump load and at the same time utilized for recharging the battery bank. This proved that the system could function as a standalone unit. Small weaknesses in the feedback control system prevented the system from operating perfectly. The problem was solved and simulation showed how the system should function. The efficiency of the SES was very good when measurements were done.

5.3 Future Work and Recommendations

If the system is to be implemented in an off-grid location, and has to last for a few years, it needs to be improved in three different aspects.

The filter inductors have to be redesigned for a maximum current of 600 A peak. This will ensure that the inductors will not saturate. The chosen IGBT module would function perfectly with a non-saturated current.

To get a constant power output from the system, during the day and night, a greater energy storage device would be required. It would be more appropriate to implement an AGM battery with a deeper cycle as energy storage. Large-scale energy storage can be done by pumping water from a lower reservoir, or dam, to another water storage facility which is situated at higher levels. The dump load was intended for research only and thus different loads or energy storage devices could be connected.

The load management control could not be tested perfectly and is thus in need of some development. The 10 V scale of the thyristor module could be a better solution to achieve better control.

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APPENDIX A: C-CODE

File: SES.c

```
    project:    Bidirectional converter for a Stirling Energy System
    developer:  H.Redecker
    company:    University of Stellenbosch

--------------------------------------------------------------------------
2004/03/25
/* ------------------------------------------------------------------------ */
#include "F2407Regs.h"       /* include F2407Regs.h in Source file */
#include "FPGA_ADD.h"        /* include FPGA_ADD.h in Source file */
#include <math.h>

#define _SES

void F2407_SYSTEM(void);
void F2407_IO_SETUP(void);
void F2407_ADC(void);
void F2407_TMR_PWM(void);
int STARTUP_SYSTEM(void);
void EMERGENCY(void);
void STANDBY(void);
void SHUTDOWN(void);
int MD_Delay(void);
void F2407_WD_EN(void);
void F2407_Int(void);
void Sin_Comp(void);
void I_RMS(void);
void BATTERY_CHARGE(void);
void PROTECTION (void);
void Mod_Index(void);
void F2407_Kick_Dog(void);


int Sin32767(int);
unsigned int DCValSe;
unsigned int dcBus;
unsigned int IaMEASURE;
unsigned int IbMEASURE;
unsigned int IcMEASURE;
unsigned int I_Trip;
unsigned int Ia;
unsigned int Ib;
unsigned int Ic;
unsigned int Temp_Meas;
unsigned int Ampl = 1998;
unsigned int Ampl1;
unsigned int trip;
unsigned int StandbyFlag = 0;
unsigned int ShutdownFlag = 0;
unsigned int HaltFlag = 0;
unsigned int EmergencyFlag = 0;
unsigned int RMSI;
signed int IaAC1;
signed int IaAC2;
unsigned int IaABS;
unsigned int Vavg;
unsigned int Iavg;
unsigned int DCValAverage = 0;
unsigned int Sum1 = 0;
unsigned int Sum2 = 0;
unsigned int Vdrop;
unsigned int IDC;
unsigned int VDC =0;
```

```
/*--.....................................................................--
                            Main Program
--.....................................................................--*/
void main(void)
{
    F2407_SYSTEM();
    F2407_IO_SETUP();
    F2407_ADC();
    F2407_TMR_PWM();
    STARTUP_SYSTEM();
    MD_Delay();
    F2407_WD_EN();
    F2407_Int();
}


/*--.....................................................................--
                            SYSTEM SETUP
--.....................................................................--*/
void F2407_SYSTEM(void)
{

#define wd_DISABLE (1<<6)
#define wd_CHK     0x28

    iaWDCR    = wd_DISABLE|wd_CHK; /* Disable Watchdog */
    iaSCSR1   = 0x008C;            /* Enable EVA,EVB,A/D Clock (p:2-4)*/

}


/* --.....................................................................--
                          IO Setup (Chapter 5)
--.....................................................................*/
void F2407_IO_SETUP(void)
{

    iaMCRA     = 0x0FC7;              /* PWM1-PWM6,SCITXD,SCIRXD,XINT1 */
    iaMCRC     = 0x0801;              /* Clockout & T4PWM/T4CMP selected */
    iaPEDATDIR = 0xFFFF;              /* IOPE0 - IOBPE7 (LED1-3 & EPLD_LED1-4) OFF */
    iaPBDATDIR = 0xB0A0;              /* IOPB7 LED1=OFF,T1PWM/T2PWM output */
                                      /* Reset FPGA */
    iaPFDATDIR = 0xFFFF;              /* Set IOPF0,1,2,3 to low and output. p5-13*/
}

/*--LED's:    IOPE1: LED1 Inverter             iaPEDATDIR &= ~(1<&lt1);
              IOPE2: LED2 Rectifier            iaPEDATDIR &= ~(1<&lt2);
              IOPE3: LED3 Thrysistor Dump      iaPEDATDIR &= ~(1<&lt3);
              IOPE4: EPLD_LED1 Temp|IGBT_ERROR iaPEDATDIR &= ~(1<&lt4);
              IOPE5: EPLD_LED2 Over currentDC  iaPEDATDIR &= ~(1<&lt5);
              IOPE6: EPLD_LED3 Over voltageDC  iaPEDATDIR &= ~(1<&lt6);
              IOPE7: EPLD_LED4 Under voltageDC iaPEDATDIR &= ~(1<&lt7);------*/


/* --.....................................................................--
                A/D Setup
--.....................................................................*/
void F2407_ADC(void)
{
    iaADCTRL1 = 0x4000;               /* Reset A/D Module */
    asm (" NOP");                     /* Delay */
    iaADCTRL1 = 0x0100;               /* Tlk = 100ns */
    iaMAXCONV = 0x0005;               /* 6 Conversion MAX_CONn+1 */
    iaCHSELSEQ1 = 0x7E63;             /* "CH3(DC-Bus)RESULT0","CH6(IDC)RESULT1",
                                      /* "CH14(Ib)RESULT2","CH7(Ia)RESULT3" Selected */
    iaCHSELSEQ2 = 0x0540;             /* "CH0(Vdc)RESULT4" , " CH4(Temp_Meas)RESULT5 */
                                      /* "CH5(EMERGENCY) RESULT6" */
}
```

```
/* ------------------------------------------------------------------
                  Timer & Compare Setup (p 6-38 compare units)
------------------------------------------------------------------*/
void F2407_TMR_PWM(void)
{

    /*  Assume CPUCLK=40MHz

        Timer1: To generate PWM
        Set to 5 kHz (taking into account up/down couting mode, Period = TPRD*2).
        Set to continuous up/down mode (for PWM generation).
        Set prescale to 1 (clock divide by two).

        Timer2: To generate accurate timing for 305 Hz

        Timer4: To generate accurate timing for up/down 100 kHz */


    iaCOMCONA = 0x0000;      /* Put PWM Output in High Impedance State */
    iaT1PR    = 2000;        /* 40 MHz/5 kHz/2/2=2000 ; */
    iaT2PR    = 0xFFFF;      /* 40 MHz/305 Hz/2 = 65536; Only Up Count */
    iaT4PR    = 100;         /* 40 MHz/100 kHz/2/2 = 100; Up-Down Count(timer4 period
                                regis.) */

    iaACTRA   = 0x0999;      /* PWM2,4,6 Active High. PWM1,3,5 Active Low (action control
                                regis.)*/

    iaCMPR1   = (2000/2);    /* No Use, Get's Updated Later (compare register)*/
    iaCMPR2   = (2000/3);    /* No Use */
    iaCMPR3   = (2*(2000/2));/* No Use */

    iaT1CNT   = 0xFFFE;      /* Counter1 Starting Value */
    iaT2CNT   = 0xFFFE;      /* Counter2 Starting Value */

    iaDBTCONA= 0x06EC;       /*Deadband Prescale x/8,Enable All Deadband Units,DB=1.2us */


    iaT2CON    = 0x1180;     /* Timer2 To Generate Accurate Delay Timing */
    iaT1CON    = 0x0942;     /* Start Timer1 and Timer2 */
    iaT4CON    = 0x0942;     /* Start Timer4 */
    iaGTPCONB = 0x0044;      /* Enable GP timer outputs; GP timer4 compare */


}


/*--------------------------------------------------------------------
                              STARTUP_SYSTEM
--------------------------------------------------------------------*/
int STARTUP_SYSTEM(void)
{

  static int DL_Clk = 0;

/*  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - */
  while(DL_Clk < 1000)       /* Loop for (1000 * 1/305)sec = 3.278sec  */
  {
    while(~(iaEVAIFRB)&(1)); /* Wait  for 305Hz Timer2 Period Flag */
    {
    iaEVAIFRB |= 1;          /* Clear Flag */
    iaADCTRL2 = 0x2000;      /* START A/D */
    DL_Clk++;
    trip    = (iaRESULT6 >> 6);
    DCValSe = (iaRESULT0 >> 6); /* Measure DCValSe */
    }
  }
/*  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - */
```

```
    if ((trip >= 832))        /* "if on" 0x0340 = > 832 which corresponds to 2.68V*/
    {

          if (DCValSe >= 0)           /*((DCValSe < 850) && (DCValSe > 730))
          {                           /* check if battery is ok */
                                      /* if yes thes open switches */
          iaPFDATDIR |= (1);          /* S.dump        1 relay off */
          iaPFDATDIR |= (2);          /* S.dc     10 relay off */
          iaPFDATDIR |= (4);          /* S.soft-start 100  relay off */
          }

         else
         {
         DL_Clk = 0;
         ShutdownFlag = 1;            /* Set flag to trigger Shutdown procedure */
         return(-1);                  /* if battery is not ok then shutdown */
         }
     }
     else
     {
     StandbyFlag = 1;
     return(-1);
     }

/*  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - */
        DL_Clk = 0;
        while(DL_Clk < 610)           /* Loop for (610 * 1/305)sec = 2sec  */
        {
         while(~(iaEVAIFRB)&(1));     /* Wait  for 305Hz Timer2 Period Flag */
         iaEVAIFRB |= 1;              /* Clear Flag */
         iaADCTRL2 = 0x2000;          /* START A/D */
         DL_Clk++;

         trip = (iaRESULT6 >> 6);
         if (trip <= 0x00E8)          /* "if off" 0x00E8 corresponds to 0.75V */
         {
         StandbyFlag = 1;
         return(-1);
         }
        }
/*  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - */

        iaPFDATDIR &= ~(4);           /* S.soft-start relay on.Charging the DC-Cap */

/*  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - */
        DL_Clk = 0;
          while(DL_Clk < 3050)        /* Loop for (3050 * 1/305)sec = 10sec */
        {
          while(~(iaEVAIFRB)&(1));    /* Wait  for 305Hz Timer2 Period Flag */
          iaEVAIFRB |= 1;             /* Clear Flag */
          iaADCTRL2 = 0x2000;         /* START A/D */
          DL_Clk++;
         trip = (iaRESULT6 >> 6);
        if (trip <= 0x00E8)           /* 0x00E8 corresponds to 0.75V */
        {
          ShutdownFlag = 1;           /* Set flag to trigger Shutdown procedure */
        return(-1);
        }
        }
/*  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - */

          iaPFDATDIR &= ~(2);         /* S.dc relay on */

/*  - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - */
```

```
          DL_Clk = 0;
          while(DL_Clk < 610)          /* Loop for (610 * 1/305)sec = 2sec */
        {
          while(~(iaEVAIFRB)&(1));     /* Wait  for 305Hz Timer2 Period Flag */
          iaEVAIFRB |= 1;              /* Clear Flag */
          iaADCTRL2 = 0x2000;          /* START A/D */
          DL_Clk++;
          trip = (iaRESULT6 >> 6);

        if (trip <= 0x00E8)            /* 0x00E8 corresponds to 0.75V */
        {
          ShutdownFlag = 1;            /* Set flag to trigger Shutdown procedure */
        return(-1);
        }
        }
        DL_Clk = 0;


     iaPFDATDIR |= (4);                /* S.soft-start relay off */
     return(0);
}


/*--.....................................................................--
                              Delay
--.....................................................................*/
int MD_Delay(void)
{

  static int DL_Clk1 = 0;
  iaPBDATDIR = 0xB080;                 /* RESET FPGA */

  while(DL_Clk1 < 1000)                /* Loop for (1000 * 1/305)sec = 3.278sec  */
    {
    while(~(iaEVAIFRB)&(1));           /*  Wait  for 305Hz Timer2 Period Flag */
    iaEVAIFRB |= 1;                    /*  Clear Flag */
    iaADCTRL2 = 0x2000;                /* START A/D */
    DL_Clk1++;

      trip = (iaRESULT6 >> 6);

      if (trip <= 0x00E8)              /* 0x00E8 corresponds to 0.75V */
      {
        ShutdownFlag = 1;              /* Set flag to trigger Shutdown procedure */
      return(-1);
      }

    }

  iaCOMCONA = 0x8200;                  /* Enable Compare Operation */
                                       /* and set pwm outputs not to high impedence state
                                      =>enable */
  iaCOMCONB = 0x8200;
  return(0);
}


/*--.....................................................................--
                          Watch Dog Timer Setup
--.....................................................................--*/
void F2407_WD_EN(void)
{

  iaWDCR = 0x28;          /* Enable Watchdog AND set WDCLK divider to 64 (p-11-11)*/

}
```

```
/* ------------------------------------------------------------------
                          Interrupt Setup
------------------------------------------------------------------*/
void F2407_Int(void)
{

    /*
        INT1: Power Drive Protection
        INT2: Timer 1 Period Interrupt
        INT3: Timer 2 Period Interrupt
        INT4: None
        INT5: None
        INT6: None
    */

    asm ("  CLRC INTM");     /* Enable Interupts Globally (asembler Code) */

    iaIFR     = 0xFFFF;      /* Clear all Flags */
    iaIMR     = 0x0007;      /* Enable Int1,2,3 0x0007 */
    iaXINT1CR = 0x0001;      /* Enable XINT1 */


    iaEVAIFRA = 0xFFFF;      /* Clear all Flags */
    iaEVAIMRA = 0x0081;      /* PDPINTA, Timer1 Period Interrupt Enable */
    iaEVAIMRB = 0x0001;      /* Timer2 Period Interrupt Enable */
    iaEVBIMRB = 0x0001;      /* Timer4 Period Interrupt Enable */

}


/*..................................................................
                          Sine Compare
------------------------------------------------------------------*/
void Sin_Comp(void)
{

if((StandbyFlag == 0) && (ShutdownFlag == 0))
{

       static unsigned int cnt1 = 0;
       static unsigned int cnt2 = (64000/3);
       static unsigned int cnt3 = 2*(64000/3);
       static int Ref_A;
       static int Ref_B;
       static int Ref_C;
       static int count2 = 0;
       static unsigned int countSECONDS = 0;


      cnt1 += 649;               /* 64000/640=100 ; 5kHz/100=50Hz */
      cnt2 += 649;
      cnt3 += 649;



/*--------Full cycle switching-------------------*/
/*    if(count2++ == 500)         /* Wait until PWM has completed a full cycle (20ms)*/
/*    {
      iaCOMCONA &= ~ (0x0200);    /* Put PWM Output in High Impedance State */
/*    ShutdownFlag = 1;
      count2 = 0;
      }

/*-----------------------------------------*/
```

```
    if(Ampl >= 1999)              /* Limit the modulation index */
      {
        Ampl = 1999;
      }
      else if(Ampl <= 0)
      {
        Ampl = 0;
      }



    if (cnt1 >= 64000) cnt1 -= 64000;           /* 2^6=64 ; 1000 Pts Sine Tabel */
      Ref_A = (Sin32767(cnt1 >> 6));            /* 64*1000=64000 */
      Ref_A = ((long)Ref_A * (long)Ampl) >> 16; /* Skaal -+ 32767 af na */
      iaCMPR1 = 1000 + (Ref_A);                 /* -+ 1000 */

    if (cnt2 >= 64000) cnt2 -= 64000;           /* 2^6=64 ; 1000 Pts Sine Tabel */
      Ref_B = (Sin32767(cnt2 >> 6));            /* 64*1000=64000 */
      Ref_B = ((long)Ref_B * (long)Ampl) >> 16;
      iaCMPR2 = 1000 + (Ref_B);

    if (cnt3 >= 64000) cnt3 -= 64000;           /* 2^6=64 ; 1000 Pts Sine Tabel */
      Ref_C = (Sin32767(cnt3 >> 6));            /* 64*1000=64000 */
      Ref_C = ((long)Ref_C * (long)Ampl) >> 16;
      iaCMPR3 = 1000 + (Ref_C);

}
}


/*--------------------------------------------------------------------------
                              PROTECTION
--------------------------------------------------------------------------- */
void PROTECTION(void)
{

  static long DCSum =0;
  static int VDCavg = 0;
  static int cnt = 0;

if((StandbyFlag == 0) && (ShutdownFlag == 0))
{
  IDC  = (iaRESULT1 >> 6);              /* Measure DC current */

    for(DCSum = 0,cnt=0;cnt <= 100;cnt++)
    {
    DCValSe   = (iaRESULT0 >> 6);       /* Measure DC-voltage, */
    DCSum = DCSum + DCValSe;
    }

    VDCavg = (DCSum/100);
    VDC = (1000/980)*VDCavg;            /* Scale the DSPmeasured value a a real voltage */

     if(VDC >= 833)                     /* If DCValSe get bigger than 830V then shutdown */
     {
     iaPEDATDIR &= ~(1<<6);             /* IOPE6: EPLD_LED3 Over voltageDC "ON"  */
     ShutdownFlag = 1;                  /* Set flag to trigger Shutdown procedure */
     }

     if(VDC < 730)                      /*If DCValSe gets smaller than 730V then shutdown*/
     {
     iaPEDATDIR &= ~(1<<7);             /* IOPE7: EPLD_LED4 Under voltageDC "ON"  */
     ShutdownFlag = 1;                  /* Set flag to trigger Shutdown procedure */
     }

/*   if(IDC > 1000)                     /* Battery Charge current must be less than 1000,
/*   {                                  /* which corresponds to 12.7ADC."dec=11*IDC*N+520"
```

```
/*   iaPEDATDIR &= ~(1<&lt5);          /* IOPE5: EPLD_LED2 Over currentDC "ON" */
/*   ShutdownFlag = 1;                 /* Set flag to trigger Shutdown procedure */
/*   } */

}
}


/*--.....................................................................--
                          Modulation_Index
--.....................................................................--*/
void Mod_Index(void)
{

  static long k = 5650;      /* Ampl(max) = 1999 = k *230/650   used = 5492*/
  static int count10 = 0;
  static int DCVol[30];      /* Declare a vector of length 50 with name DCVol */
  static int cnt3 = 0;
  static int DCVolSum = 0;
  static int DCVolavg = 0;

if((StandbyFlag == 0) && (ShutdownFlag == 0))
{

    DCValSe = (iaRESULT0 >> 6);/* Measure DC-voltage and current */
    IDC = (iaRESULT1 >> 6);
    cnt3++;                     /* Increment cnt */

  if (cnt3 <= 30)               /* count up to 100 to get a period of 20ms */
  {
  DCVol[cnt3-1] = DCValSe;      /* store values in a vector from IVec[0] to IVec[99] */
  }

    else
    {
    cnt3 = 0;
    }

    DCVolSum = DCVol[0] + DCVol[1] + DCVol[2] + DCVol[3] + DCVol[4] + DCVol[5]
    + DCVol[6] + DCVol[7] + DCVol[8] + DCVol[9] + DCVol[10] + DCVol[11] + DCVol[12]
    + DCVol[13] + DCVol[14] + DCVol[15] + DCVol[16] + DCVol[17] + DCVol[18]
    + DCVol[19] + DCVol[20] + DCVol[21] + DCVol[22] + DCVol[23] + DCVol[24]
    + DCVol[25] + DCVol[26] + DCVol[27] + DCVol[28] + DCVol[29];

    DCVolavg = DCVolSum/30;

/* Insert an if statement to consider volatge drop over inductor when operating */
/* in rectification mode */

/*    if(IDC <= 50)                  /* inverter mode */
/*    {
    Ampl = (k*(220+Vavg)) / DCVolavg; /* ma = Vout/Vd = (Vo + Vdrop)/Vd*/
/*   }
    else {/* if(IDC > 537)           /* rectifier mode */
/*   {
    Ampl = (k*(210-Vavg)) / DCValSe;  /* ma = Vout/Vd = (Vo + (-Vdrop))/Vd*/
/*   }
    else
    {*/

    Ampl = (k*(243)) / DCVolavg;

/* }

  count10++;  */
}
}
```

```
/*--.....................................................................--
                            RMS Calculation
--.....................................................................--   */

void I_RMS(void)
{

  static int cnt = 0;
  static int IVec[100];     /* Declare a vector of length 100 with name IVec */
  static long ISum = 0;

if((StandbyFlag == 0) && (ShutdownFlag == 0))
{

    IDC = (iaRESULT1 >> 6);  /* Measure DC-current */
    Ia = (iaRESULT3 >> 6);   /* Measure AC-current */
    IaAC1 = Ia - 500;        /* subtract offset of 2.6V */
    IaABS = abs(IaAC1);      /* Take absolute value */
    cnt++;                   /* Increment cnt */

    if (cnt <= 100           /* count up to 100 to get a period of 20ms */
    {
    IVec[cnt-1] = IaABS      /* store values in a vector from IVec[0] to IVec[99] */
    }

    else
    {
    cnt = 0;
    }

    ISum = IVec[0] + IVec[1] + IVec[2] + IVec[3] + IVec[4] + IVec[5]
    + IVec[6] + IVec[7] + IVec[8] + IVec[9] + IVec[10] + IVec[11] + IVec[12]
    + IVec[13] + IVec[14] + IVec[15] + IVec[16] + IVec[17] + IVec[18]
    + IVec[19] + IVec[20] + IVec[21] + IVec[22] + IVec[23] + IVec[24]
    + IVec[25] + IVec[26] + IVec[27] + IVec[28] + IVec[29] + IVec[30]
    + IVec[31] + IVec[32] + IVec[33] + IVec[34] + IVec[35] + IVec[36]
    + IVec[37] + IVec[38] + IVec[39] + IVec[40] + IVec[41] + IVec[42]
    + IVec[43] + IVec[44] + IVec[45] + IVec[46] + IVec[47] + IVec[48]
    + IVec[49] + IVec[50] + IVec[51] + IVec[52] + IVec[53] + IVec[54]
    + IVec[55] + IVec[56] + IVec[57] + IVec[58] + IVec[59] + IVec[60]
    + IVec[61] + IVec[62] + IVec[63] + IVec[64] + IVec[65] + IVec[66]
    + IVec[67] + IVec[68] + IVec[69] + IVec[70] + IVec[71] + IVec[72]
    + IVec[73] + IVec[74] + IVec[75] + IVec[76] + IVec[77] + IVec[78]
    + IVec[79] + IVec[80] + IVec[81] + IVec[82] + IVec[83] + IVec[84]
    + IVec[85] + IVec[86] + IVec[87] + IVec[88] + IVec[89] + IVec[90]
    + IVec[91] + IVec[92] + IVec[93] + IVec[94] + IVec[95] + IVec[96]
    + IVec[97] + IVec[98] + IVec[99];

    Vavg = (ISum/800);       /* Vdrop = 18.8V = X*Iavg : and X=18.8/194 = 0.097 */
                             /* where 197 is the dec number of 145 Amperes */
                             /* Vavg = (ISum/100) * 0.097 = (ISum/100) * 1/10.3 */
                             /*      = (ISum/1000) */
    Iavg = ISum/100;

 /*   DCValAverage = Sum/20; */

}
}


/*--.....................................................................--
                            Battery_Charge
--.....................................................................--   */
void BATTERY_CHARGE(void)
{
  static int IDCscale = 0;
  static int IDCscale1A = 0;
```

```
  static int IVecdc[50];     /* Declare a vector of length 10 with name IVec */
  static long ISumdc = 0;
  static int Idcavg = 0;
  static int cnt = 0;

if((StandbyFlag == 0) && (ShutdownFlag == 0))
{

    IDC = (iaRESULT1 >> 6);  /* Measure DC-current and voltage */
    DCValSe = (iaRESULT0 >> 6);
    cnt++;                   /* Increment cnt */

  if (cnt <= 50)             /* count up to 100 to get a period of 20ms */
  {
  IVecdc[cnt-1] = IDC;       /* store values in a vector from IVec[0] to IVec[99] */
  }

    else
    {
    cnt = 0;
    }

    ISumdc = IVecdc[0] + IVecdc[1] + IVecdc[2] + IVecdc[3] + IVecdc[4] + IVecdc[5]
    + IVecdc[6] + IVecdc[7]+IVecdc[8]+IVecdc[9]+IVecdc[10]+IVecdc[11] + IVecdc[12]
    + IVecdc[13] + IVecdc[14] + IVecdc[15] + IVecdc[16] + IVecdc[17] + IVecdc[18]
    + IVecdc[19] + IVecdc[20] + IVecdc[21] + IVecdc[22] + IVecdc[23] + IVecdc[24]
    + IVecdc[25] + IVecdc[26] + IVecdc[27] + IVecdc[28] + IVecdc[29] + IVecdc[30]
    + IVecdc[31] + IVecdc[32] + IVecdc[33] + IVecdc[34] + IVecdc[35] + IVecdc[36]
    + IVecdc[37] + IVecdc[38] + IVecdc[39] + IVecdc[40] + IVecdc[41] + IVecdc[42]
    + IVecdc[43] + IVecdc[44] + IVecdc[45] + IVecdc[46] + IVecdc[47] + IVecdc[48]
    + IVecdc[49];
    Idcavg = ISumdc/50;

/*-------------------Charge at 10A-----------------------------------------*/

if(VDC < 810)
{

    if(Idcavg > 892 && Idcavg <= 1024)
    {

    IDCscale = 27*(Idcavg-893);       /* Scale DC current to get a finer scale */

        if(IDCscale > 0)
        {
        iaT4CMPR = IDCscale/9;        /* Scale down to get pulse width */
        iaPEDATDIR &= ~(1<<3);        /* LED3 ON Thrysistor Dump */
        }

        else
        {
        iaPEDATDIR |=(1<<3);          /* LED3 OFF Thrysistor Dump */
        iaT4CMPR = 0;                 /* When IDC < 10A ==> don't dump */
      }
    }

    else
    {
    iaPEDATDIR |=(1<<3);              /* LED3 OFF Thrysistor Dump */
    iaT4CMPR = 0;                     /* When IDC < 10A ==> don't dump */
    }
}
/*-------------------Charge at 0A------------------------------------------*/

else if(VDC >= 810 && VDC < 830)
{

    if(Idcavg > 517)
```

```
    {
    IDCscale1A = 28*(Idcavg-517);      /* 28Scale DC current to get a finer scale */

        if(IDCscale1A > 0)
        {
        iaT4CMPR = IDCscale1A/5;       /* Scale down to get pulse width */
        iaPEDATDIR &= ~(1<<3);         /* LED3 ON Thrysistor Dump */
        }

        else
        {
        iaPEDATDIR |=(1<<3);           /* LED3 OFF Thrysistor Dump */
        iaT4CMPR = 0;                  /* When IDC < 10A ==> don't dump */
      }
    }

    else
    {
    iaPEDATDIR |=(1<<3);               /* LED3 OFF Thrysistor Dump */
    iaT4CMPR = 0;                      /* When IDC < 10A ==> don't dump */
    }
}
/*-------------------------LED's-------------------------------------*/


  if(IDC > 537)
  {
  iaPEDATDIR &= ~(1<<2);               /* LED2 ON (Rectifier mode ON) */
  iaPEDATDIR |= (1<<1);                /* LED1 OFF (Inverter mode OFF) */
  }

  else if(IDC < 430)
  {
  iaPEDATDIR |= (1<<2);                /* LED2 OFF (Rectifier mode OFF) */
  iaPEDATDIR &= ~ (1<<1);              /* LED1 ON (Inverter mode ON) */
  }

  else
  {
  iaPEDATDIR |= (1<<2);                /* LED2 OFF (Rectifier mode OFF) */
  iaPEDATDIR |= (1<<1);                /* LED1 OFF (Inverter mode OFF) */
  }
}
}


/*--.....................................................................--
                                EMERGENCY
--.....................................................................*/
void EMERGENCY(void)
{
  static int DL_ClkS1 = 0;
  static int wait = 0;

if((StandbyFlag == 0) && (ShutdownFlag == 0))
{

    trip = (iaRESULT6 >> 6);

    if(HaltFlag == 0)
    {
      if ((DL_ClkS1 > 10000))
      {
      trip = (iaRESULT6 >> 6);

        if(trip <= 0x00E8)     /* "if off" 0x00E8 corresponds to 0.75V */
        {
        ShutdownFlag = 1;      /* Set flag to trigger Shutdown procedure */
```

```
        }
      }
      else
      {
      DL_ClkS1++;
      }
    }
}
}


/*--------------------------------------------------------------------
                              SHUTDOWN
--------------------------------------------------------------------*/
void SHUTDOWN(void)
{
  static int DL_ClkS = 0;
  static int count1 = 0;
  static long count2 = 0;

  if ((ShutdownFlag == 1) && (StandbyFlag == 0))
  {
  trip = (iaRESULT6 >> 6);
  iaCOMCONA &= ~ (0x0200);            /* Put PWM Output in High Impedance State */
  iaPFDATDIR |= (2);                  /* S.DC S.AC     10  relay off */
  iaPFDATDIR |= (4);                  /* S.Soft-Start 100  relay off */
  iaPEDATDIR |= (1<<2);               /* LED2 OFF (Rectifier mode OFF) */
  iaPEDATDIR |= (1<<1);               /* LED1 OFF (Inverter mode OFF) */
  iaPEDATDIR |= (1<<3);               /* LED3 OFF Thrysistor Dump */

      if (count1 > 5000)              /* Wait for 1 second before switching S.Dump on */
      {
      iaPFDATDIR &= ~(1);             /* Switch S.Dump on */

        if (count2 > 50000)           /*Wait for 10 seconds to discharge DC-Capacitors */
        {
        iaPFDATDIR |= (1);            /* Switch S.Dump off */
        StandbyFlag = 1;
        }

        else
        {
        count2++;
        }
      }

      else
      {
      count1++;
      }
  }
}




/*--------------------------------------------------------------------
                              STANDBY
--------------------------------------------------------------------*/
void STANDBY(void)
{
trip = (iaRESULT6 >> 6);

if(StandbyFlag == 1)
{
```

```
iaCOMCONA &= ~ (0x0200);                /* Put PWM Output in High Impedance State */
ShutdownFlag = 0;                       /* (compare contr) */
HaltFlag = 1;
iaPEDATDIR |= (1<<3);                   /* LED3 OFF Thrysistor Dump */
iaPEDATDIR |= (1<<2);                   /* LED2 OFF (Rectifier mode OFF) */
iaPEDATDIR |= (1<<1);                   /* LED1 OFF (Inverter mode OFF) */
iaT4CMPR = 0;                           /* When Standby don't dump */

    if((trip >= 0x0340))                /* "if on" 0x0340 = > 832 which corresponds to
                                        /*2.68V*/
    {
        if((trip >= 0x0340) && (EmergencyFlag == 1))
                                        /* "if on" and EmergencyFlag is set */
        {
        while(trip >= 0x0340)           /* 0x0340 = > 832 which corresponds to 2.68V*/
        {
        while(~(iaEVAIFRB)&(1));        /* Wait  for 305Hz Timer2 Period Flag */
        iaEVAIFRB |= 1;                 /* Clear Flag */
        }
      }
      else if(trip <= 0x00E8)           /* "if off" 0x00E8 corresponds to 0.75V */
      {
      EmergencyFlag = 1;
      }
  }
  else
  {
  EmergencyFlag = 1;
  }
}
}


/*--------------------------------------------------------------------
                            Kick Dog
--------------------------------------------------------------------*/
void F2407_Kick_Dog(void)
{
                                /* p-11-9:clears the WDCNTR */
  iaWDKEY = 0x55;
  iaWDKEY = 0xAA;

}

/*--------------------------------------------------------------------*/
```

File: SES_Int.c

```
    project:    Bidirectional converter for Stirling Energy System
    developer:  H.Redecker
    company:    University of Stellenbosch

--.....................................................................--
2004/03/25
/* --.....................................................................-- */

#include "F2407Regs.h"

#define _SES_Int

int IntErrCnt = 0;

/* ------------------------------------------------------------------------*/

interrupt void Int_ERR(void)
{
  IntErrCnt++;
}

/* ------------------------------------------------------------------------*/

interrupt void Int_1()
{
  if ((iaEVAIFRA)&(1))      /* check if power drive protect flag is set */
  {

  iaEVAIFRA |= (1);         /* CLEAR PDP FLAG */
  iaPEDATDIR &= ~(1<<4);    /* IOPE4: EPLD_LED1 Temp|IGBT_ERROR "ON"*/

  while(1) F2407_Kick_Dog();
  }
}
/* ------------------------------------------------------------------------ */

interrupt void Int_2()
{
    if ((iaEVAIFRA)&(1<<7))  /* If GP Timer1 Period interrupt Flag is set*/
    {
    iaADCTRL2 = 0x2000;      /* START A/D */
    iaEVAIFRA |= (1<<7);     /* Clear Timer1 Period Flag */
    F2407_Kick_Dog();        /* Kick Watchdog */
    Mod_Index();             /* Call Mod_Index() to refresh modulation index */
    Sin_Comp();              /* Call Sin_Comp() to Generate Sine PWM */
    PROTECTION();            /* Call PROTECTION() to check for trip values */
    EMERGENCY();             /* Call EMERGENCY() to check if EMERGENCY button is pressed*/
    SHUTDOWN();              /* Call SHUTDOWN() to check if system has to shutdown*/
    I_RMS();                 /* Call I-RMS() to calculate Inductor Voltage drop */
    BATTERY_CHARGE();        /* Call BATTERY_CHARGE() to control Load Management System */
    STANDBY();               /* Call STANDBY() toc check if system needs to halt */
    }
}
/* ------------------------------------------------------------------------*/

interrupt void Int_3()
{
    if ((iaEVAIFRB)&(1))
    {
      iaEVAIFRB |= (1);
    }
}
/* --.....................................................................-- */
```

File: SES_Vec.asm

```
    project:    Bidirectional converter for Stirling Energy System
    developer:  H.Redecker
    company:    University of Stellenbosch

--------------------------------------------------------------------------
2004/03/25
/* ------------------------------------------------------------------------ */


  .sect "vectors" ; map to 0h in program space

  .ref _Int_ERR   ; .ref> defined externally of sourcefile
  .ref _Int_1, _Int_2, _Int_3, _c_int0

  B _c_int0       ; Reset
  B _Int_1        ; Power Drive Protection, XINT1
  B _Int_2        ; Timer1 Period Interrupt
  B _Int_3        ; Timer2 Period Interrupt
  B _Int_ERR      ; INT4 (maskable)
  B _Int_ERR      ; INT5 (maskable)
  B _Int_ERR      ; INT6 (maskable)
  B _Int_ERR      ; Reserved
  B _Int_ERR      ; INT8 (software)
  B _Int_ERR      ; INT9 (software)
  B _Int_ERR      ; INT10 (software)
  B _Int_ERR      ; INT11 (software)
  B _Int_ERR      ; INT12 (software)
  B _Int_ERR      ; INT13 (software)
  B _Int_ERR      ; INT14 (software)
  B _Int_ERR      ; INT15 (software)
  B _Int_ERR      ; INT16 (software)
  B _Int_ERR      ; TRAP instruction
  B _Int_ERR      ; Non Maskable
  B _Int_ERR      ; Reserved
  B _Int_ERR      ; INT20 (software)
  B _Int_ERR      ; INT21 (software)
  B _Int_ERR      ; INT22 (software)
  B _Int_ERR      ; INT23 (software)
  B _Int_ERR      ; INT24 (software)
  B _Int_ERR      ; INT25 (software)
  B _Int_ERR      ; INT26 (software)
  B _Int_ERR      ; INT27 (software)
  B _Int_ERR      ; INT28 (software)
  B _Int_ERR      ; INT29 (software)
  B _Int_ERR      ; INT30 (software)
  B _Int_ERR      ; INT31 (software)

/* ------------------------------------------------------------------------ */
```

APPENDIX B: SCHEMATICS

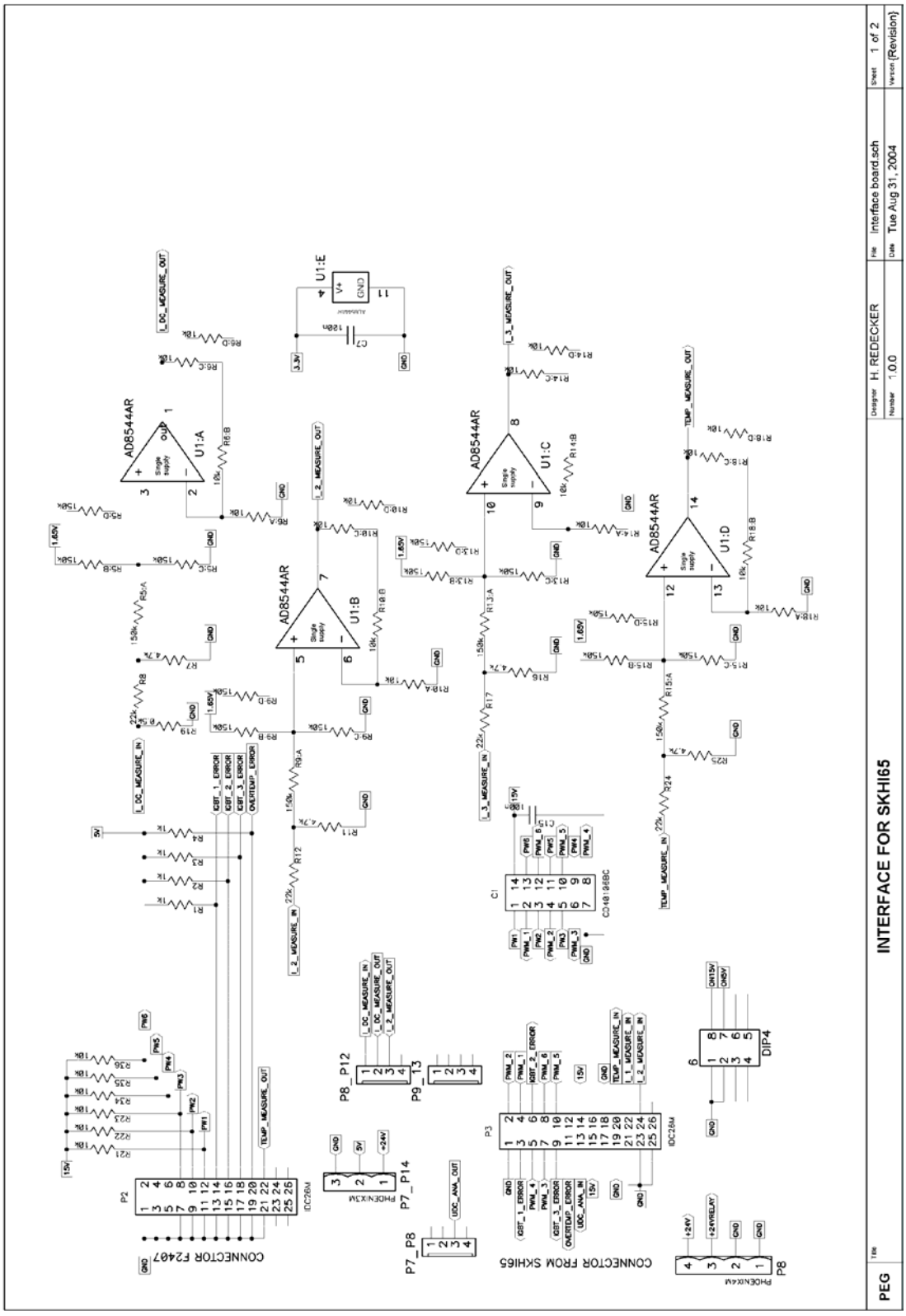


Figure B - 1: Schematic Sheet 1 of Interface Board for SKHI65

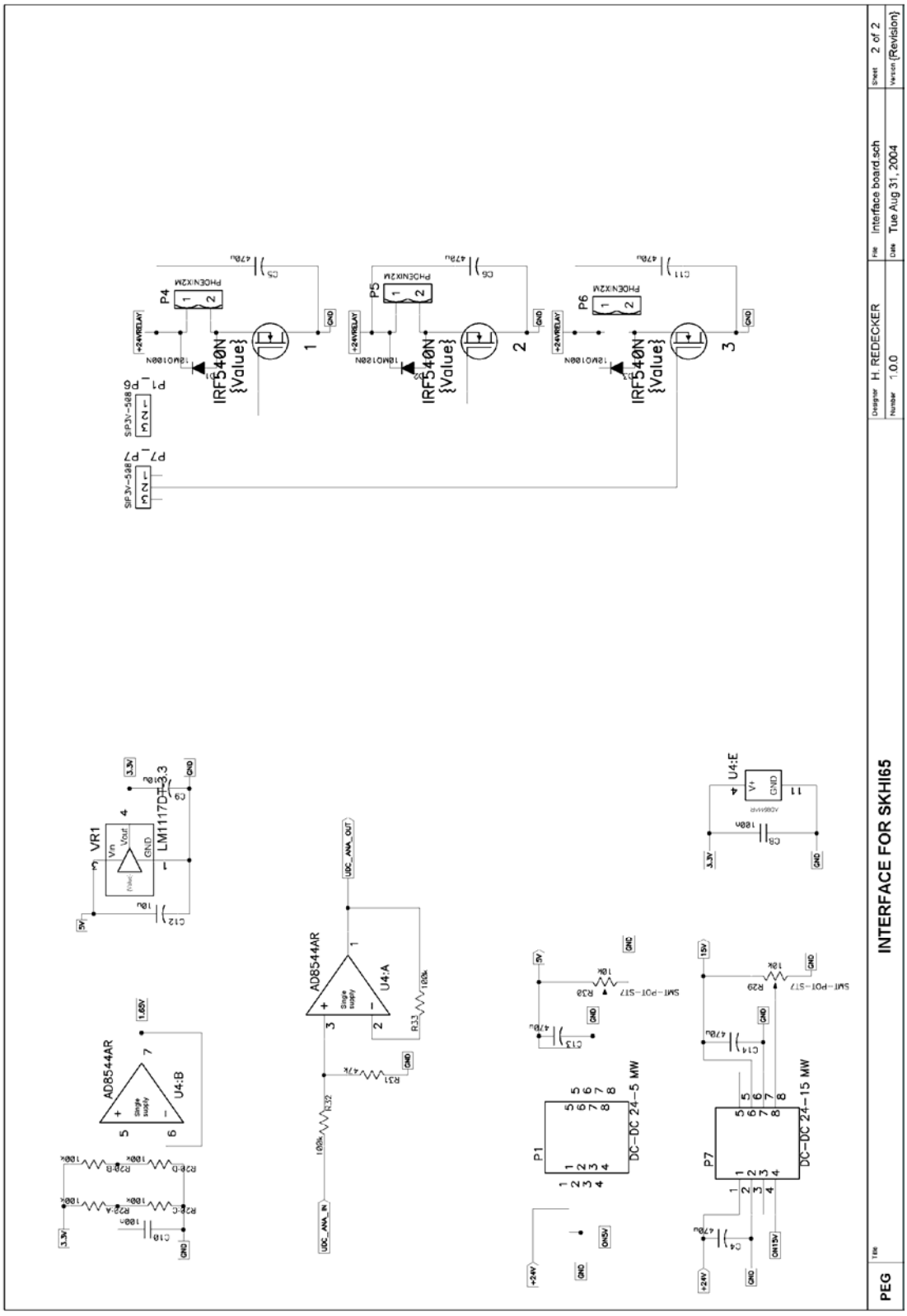


Figure B - 2: Schematic Sheet 2 of Interface Board for SKHI65

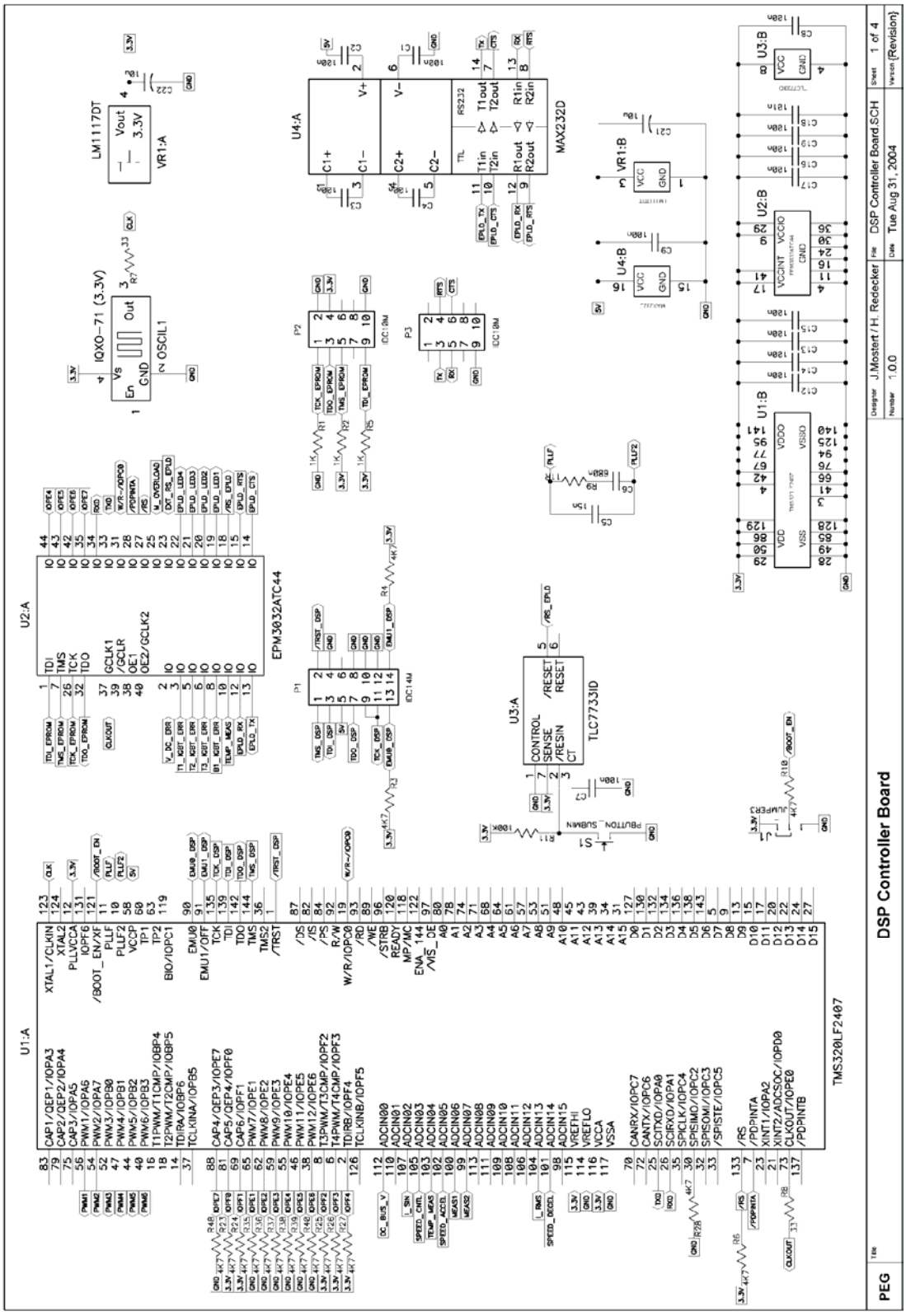


Figure B - 3: Schematic Sheet 1 of DSP Controller Board

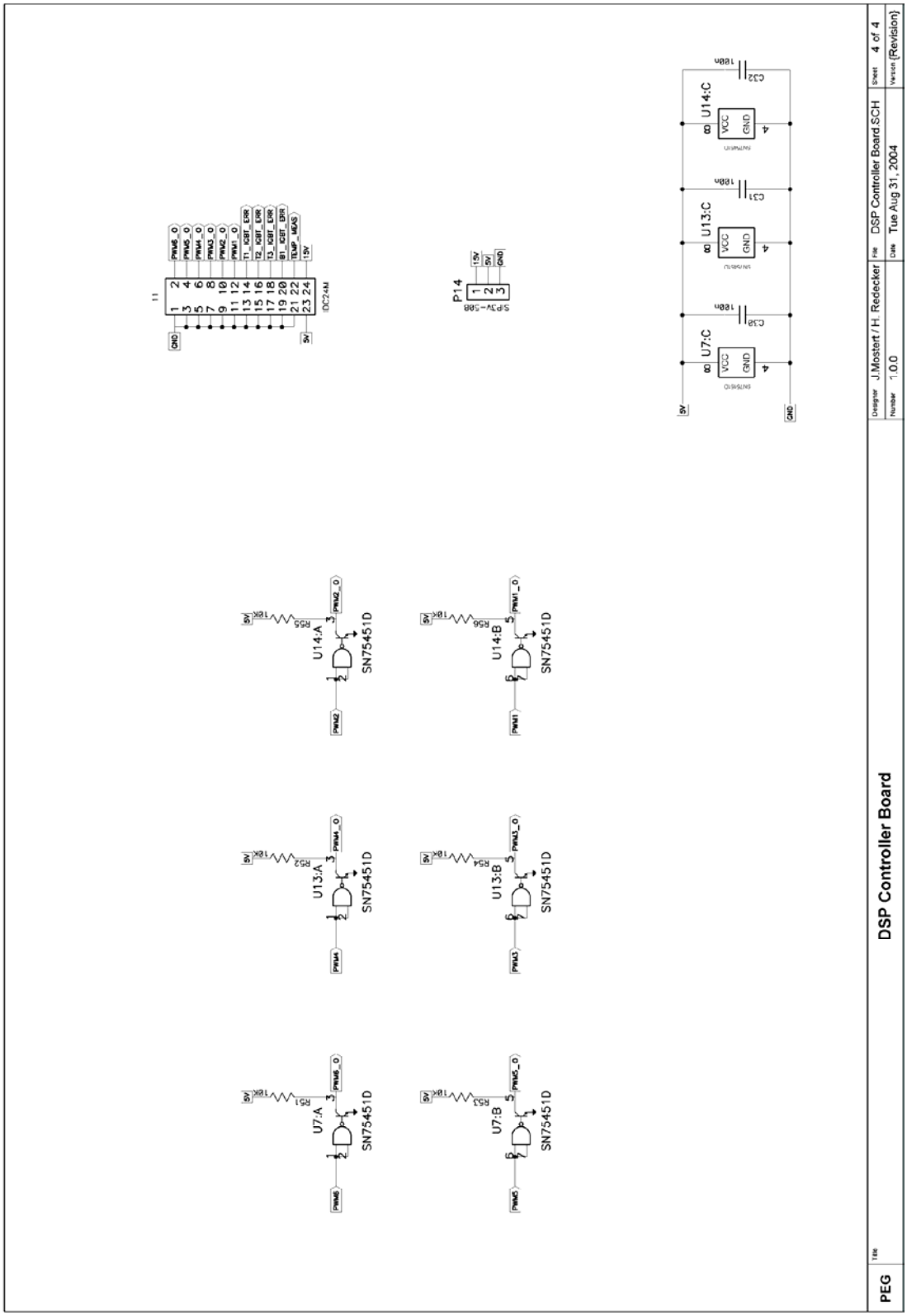


Figure B - 4: Schematic Sheet 2 of DSP Controller Board

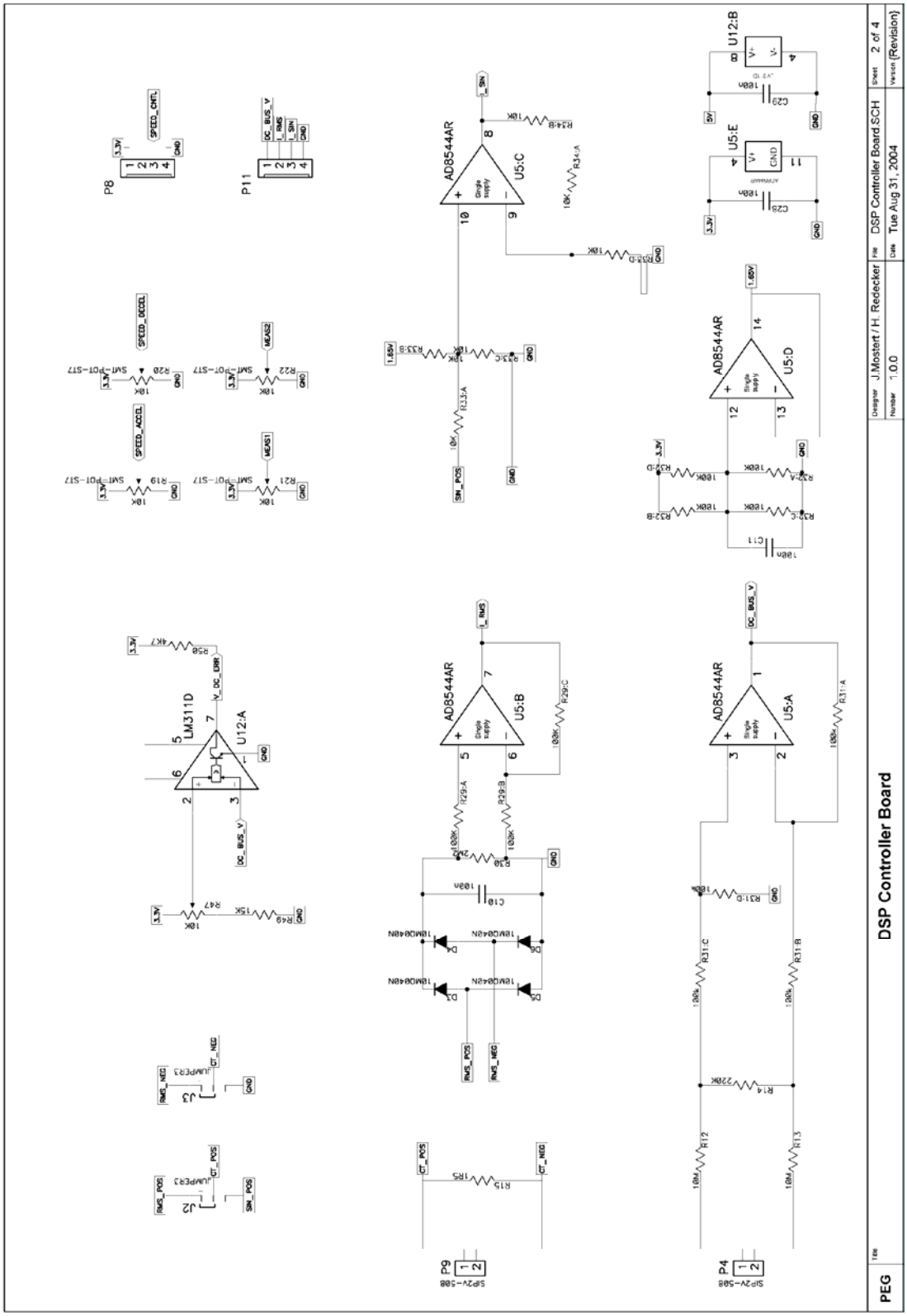


Figure B - 5: Schematic Sheet 3 of DSP Controller Board

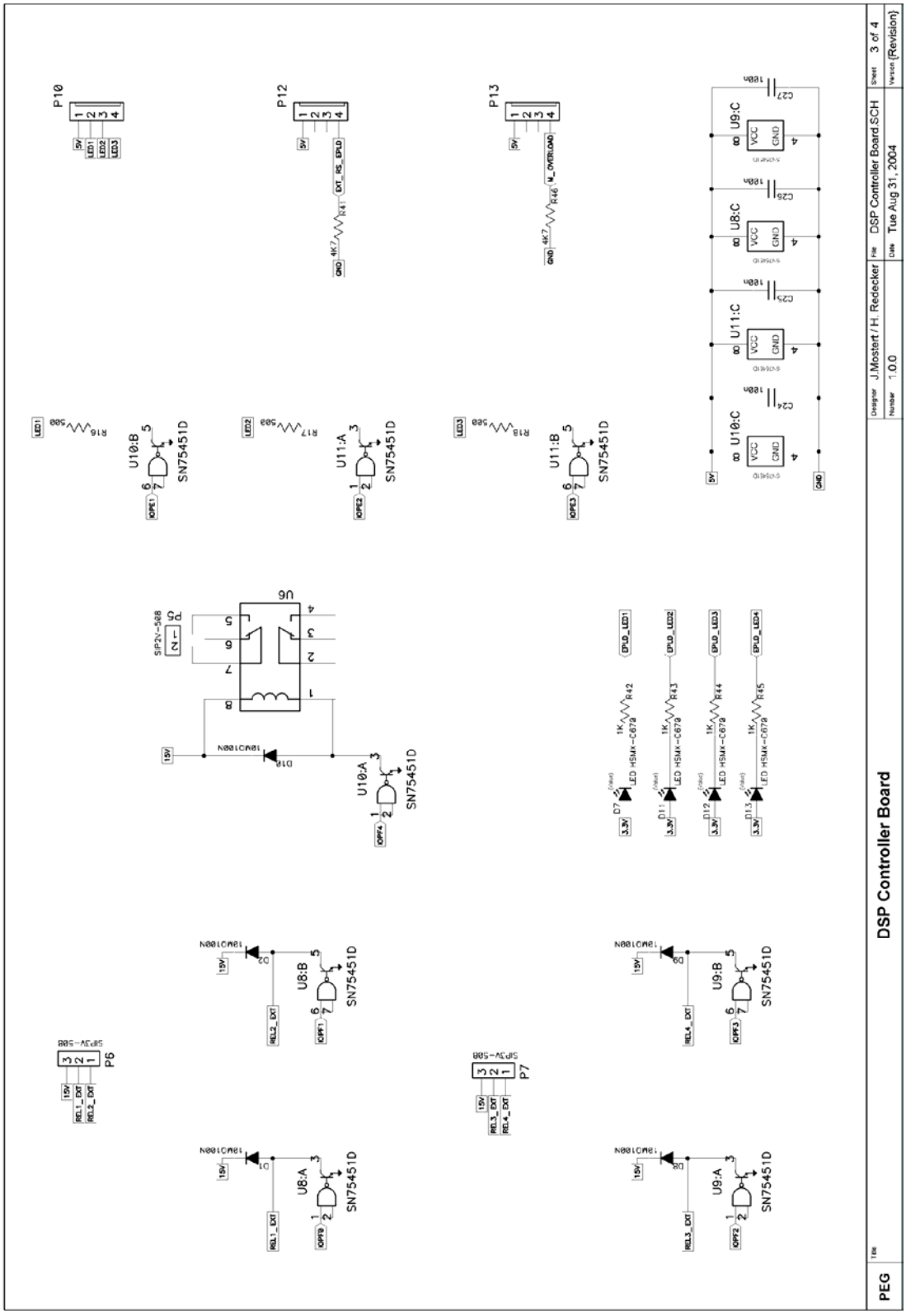
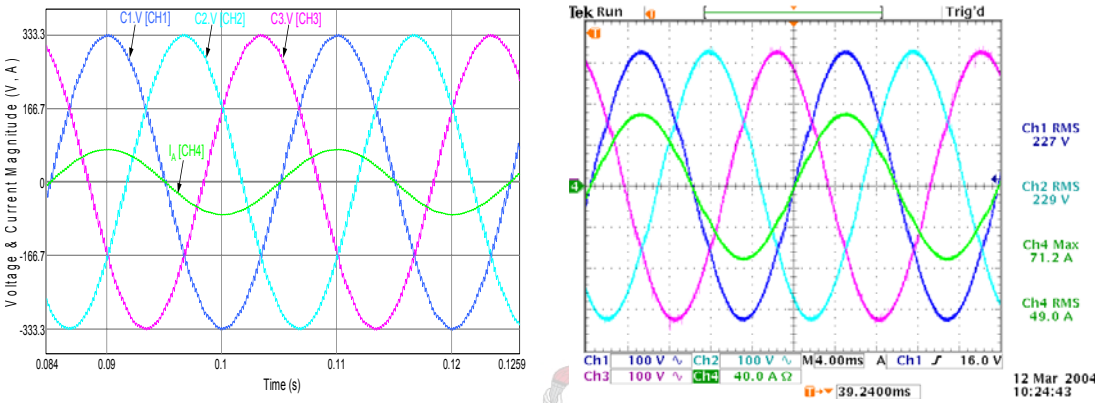


Figure B - 6: Schematic Sheet 4 of DSP Controller Board

APPENDIX C: CONSISTENCY BETWEEN PRACTICAL AND SIMULATED RESULTS

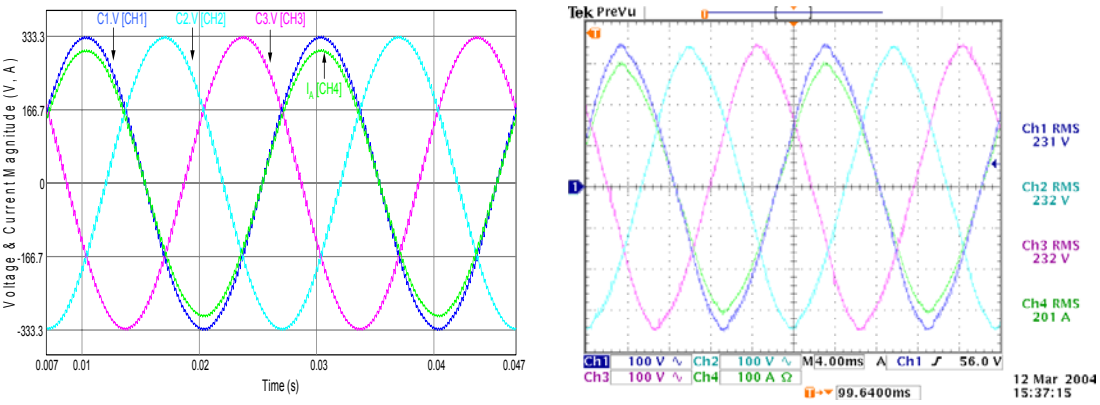
This APPENDIX summarizes the results achieved through simulations and practical experiments. All succeeding results were presented in the main Chapters but are given again to get a better comparison. The following figures reveal the consistency of the simulations over the practical results. Figure C - 1 shows the results of the average-power test.



(a) (b)

Figure C - 1: Average-Power Output: (a) Simulation; (b) Practical

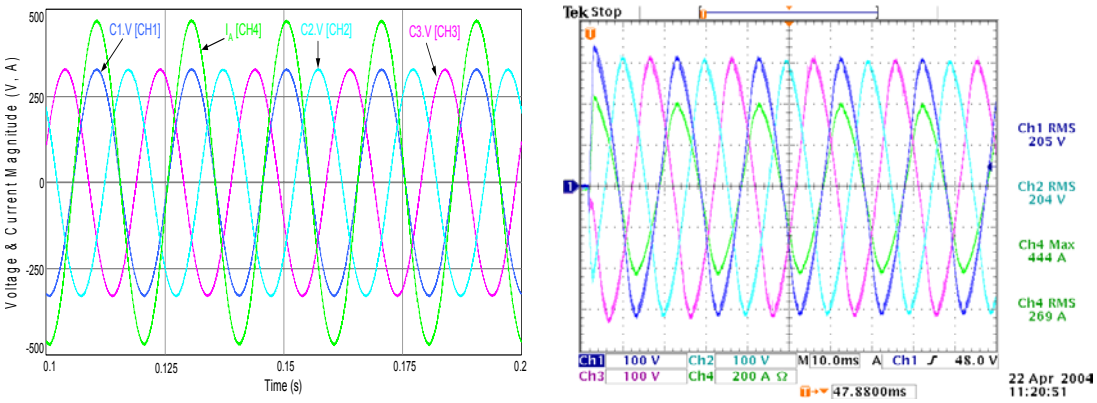
Figure C - 2 presents the waveforms of the high-power test where a power of 144 kW is dissipated in the load.



(a) (b)

Figure C - 2: High-Power Output: (a) Simulation; (b) Practical

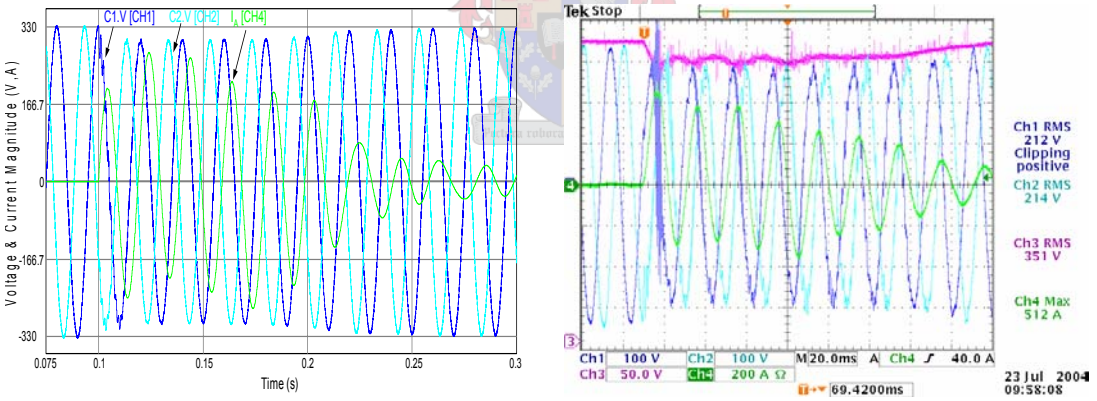
Figure C - 3 shows the peak-current waveform for the simulations and the practical experiment.



(a) (b)

Figure C - 3: Peak-Current Output: (a) Simulation; (b) Practical

The similarities of the start-up waveforms are shown in Figure C - 4. The voltage and current waveforms of the simulations over the practical results are nearly identical.

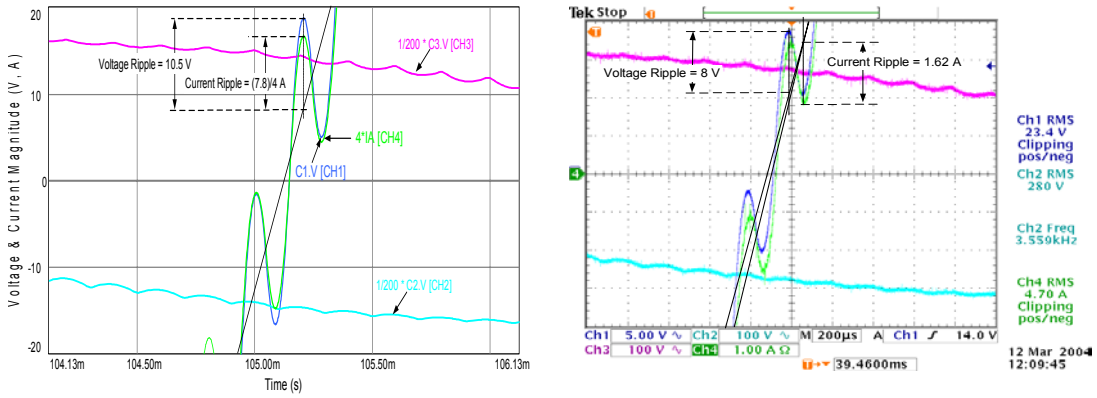


(a) (b)

Figure C - 4: Start-up Waveforms: (a) Simulation; (b) Practical

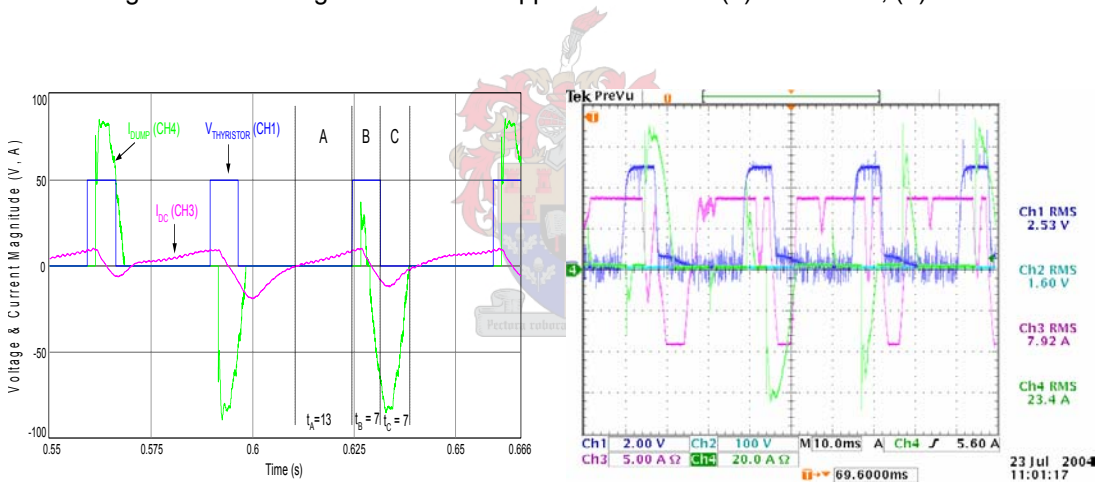
Figure C - 5 represents the voltage and current ripple values of the simulation and of the practical measurement. The voltage and current ripple in the practical results is smaller compared to the ripple in the simulation. Figure C - 6 and Figure C - 7 show the results of

the load management system. The simulations are once again very similar to the practical results.



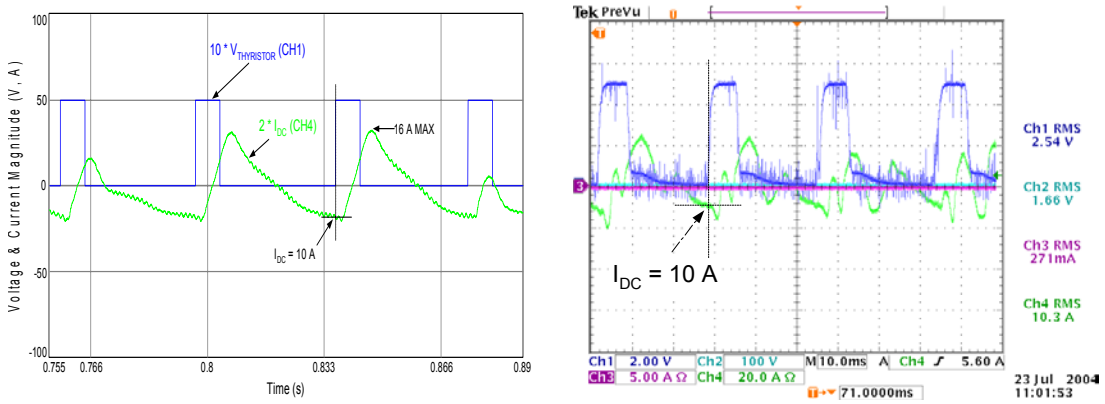
(a) (b)

Figure C - 5: Voltage and Current Ripple Waveforms: (a) Simulation; (b) Practical



(a) (b)

Figure C - 6: Load Management Output: (a) Simulation; (b) Practical



(a) (b)

Figure C - 7: Load Management Output for DC Current: (a) Simulation; (b) Practical