TRANSFORMERLESS SERIES DIP/SAG COMPENSATION WITH ULTRACAPACITORS

by

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DECLARATION

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

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SUMMARY

This thesis covers the development of a transformerless series dip compensator. Of all known power quality problems, voltage dips are the greatest reason for concern. Series injection dip compensators offer the advantage of only having to compensate for the decrease in supply voltage during a dip. This results in significant reduction in converter ratings and energy storage requirements. The aim of this thesis was to take up previous developments and combine them with new technologies to maximize their functionality. The new design was implemented with ultracapacitors to offer a maintenance-free device lifespan of 20 years. As they are very expensive, a new topology was introduced in this thesis to maximize their use so that they become viable for industry. Furthermore, a new method of daisy chaining switches was introduced to minimize costs involved in controlling them. A single-phase compensator, with this new topology and the new way of controlling switches, was designed and built according to specifications stated by Eskom. This ultracapacitor-based dip compensator was tested with a dip generator, developed by the University of Stellenbosch for different load currents. The experimental results confirmed simulations made with identical parameters. This thesis presents a reliable and cost effective solution for dip compensation.

OPSOMMING

Hierdie tesis dek die ontwikkeling van ’n transformatorlose duik kompenseerder. Van al die bekende toevoerkwaliteit probleme wek duike in die spanning die meeste kommer. Serie-injeksie kompenseerders het die voordeel dat hulle net kompenseer vir die verlies in die toevoerspanning tydens die duik. Dit het ’n beduidende vermindering in die omsetterkenwaardes en energiestoorvereistes tot gevolg. Hierdie tesis mik om vorige soortgelyke ontwikkelings op te volg en te verbeter met nuwe tegnologie om die funktionliteit te maksimeer. Die ontwerp is geimplementeer met ultrakapasitore wat die onderhoudsvrye toestel ‘n leeftyd van 20 jaar toelaat. Omdat ultrakapasitore so duur is moes ‘n nuwe topologie onwikkel word om die gebruik van ultrakapasitore meer ekonomies aantreklik te maak. Daar is ook ‘n nuwe manier van skakelaar beheer ontwikkel wat toelaat dat baie skakelaars oor een optise veesel beheer kan word. ‘n Enkel fase dip kompensaeerder is toe onwikkel en gebou volgens Eskom se spesifikasies. Die ultrakapasitor gebaseerde omsetter is getoets met ‘n dip generator wat deur die Universiteit van Stellenbosch ontwikkel is. Die praktiese resultate bevestig die simulasies wat gedoen is met dieselfe parameters. Hierdie tesis lei tot ‘n betroubaare en ekonomiese oplossing vir duik kompensasie.

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LIST OF SYMBOLS

^	Estimate of a variable
ΔV	Voltage difference
$\Delta V_{C(n)(i)}$	Capacitor (n)´s voltage drop after (i) cycles
∞	Infinity
C	Capacitance
C_{ISS}	MOSFET gate capacitance
E_{loss}	Energy lost
f	Frequency in Herz
I	Current
I_C	Charge current
I_D	Discharge current
n	Present voltage step
N	Total number of voltage steps
ø	Phase shift of a input signal
$P_{balance}$	Conduction losses during modules balancing
P_{loss}	Power lost
P_{ON}	Conduction losses during module's 'ON' period
$P_{S(BAL)}$	Switching losses during module's balancing
$P_{S(COND)}$	Switching losses during module's 'ON' period
P_{total}	Total power losses
R	Resistance
$R_{Capacitor}$	Internal capacitor resistance
R_{CS}	Case-to-surface resistance
R_G	MOSFET gate resistance
R_{IH}	Surface-to-ambient thermal resistance
R_{JC}	Junction case resistance
R_{Switch}	Internal switch resistance
t	Time
$t_{(n)n-1->n}$	Time between step (n-1)'s start time and step (n)'s start time
$t_{(n)On}$	Step (n)'s on time
$t_{(n)Start}$	Step (n)'s starting time
$t_{(n)Stop}$	Step (n)'s stopping time
T_A	Ambient temperature
t_C	Charge time

t_D	Discharge time
T_J	Junction temperature
X	Total number of modules
δt	Delta time
δV	Delta voltage
θ	Phase of rotating reference or compensation signal
ω	Radial frequency in radial per second

LIST OF ABBREVIATIONS

A	Ampere
AC	Alternating current
CAD	Computer-assisted drawing
CMLI	Cascaded multilevel inverter
CVT	Magnetic synthesizer transformer
DC	Direct current
DFT	Discrete Fourier transform
EC	Electrochemical
EPLD	Erasable programmable logic device
ESR	Equivalent series resistance
F	Farad – unit of capacitance
FPGA	Field programmable gate array
h	Hour
HV	High voltage
Hz	Herz
IGBT	Isolated gate bipolar transistor
kJ	Kilojoule
kVA	Kilo volt ampere
l	Litre
LV	Low voltage
MMLI	Marxian multilevel inverter
MOSFET	Metal oxide semiconductor field effect transistor
MV	Mega volt
MVA	Mega volt ampere
NPC	Neutral point clamp

ºC	Degrees Celsius
PEC33	Power electronic controller Version 33
PNS	Positive-negative selector
PWM	Pulse width modulation
RMS	Real mean square
s	Second
THD	Total harmonic distortion
V	Volt
VAR	Reactive power component
VRB	Vanadium redox battery
W	Watt
Ω	Unit of resistance

Prototype transformerless series dip/sag compensator with ultracapacitors

17.5 kVA Marxian multilevel inverter – four stacked modules

1 Introduction

1.1 The research initiative

Voltage dips/sags can disrupt the operation of sensitive loads such as computers, adjustable-speed drives (ASDs) and other sophisticated and critical electronic equipment [1-3]. Voltage sags are common in electric power distribution networks and have many causes, including motors starting, fast re-closing of circuit breakers, faults and lightning. More than two thirds of electrical disturbances that caused shut down of equipment were voltage sags. They can be symmetrical or asymmetrical, ranging in magnitude from 10% to 90% and can last from a few milliseconds to several cycles [2].

This study starts with review of a previous Eskom project [4, 5] on voltage dip compensation. Power quality is asserted in terms of voltage dips and their effects. A series multilevel inverter is considered as a transformerless and filterless method to compensate dips in the 50 kVA power range. Several topologies (AC to AC, boost converters and multilevel inverters) are proposed and simulations show their feasibility.

Transient energy storage is required for the multilevel inverters. A recent advance in energy storage (electrochemical or ultracapacitor) eliminates the need for maintenance on these systems.

A more suitable method was required to detect voltage dips for multilevel inverters. A control strategy is developed based on digital signal processing (DSP), which is preferred to the analog control. The proposed series multilevel inverter requires a lower power rating than comparable shunt inverters. There is no voltage range limitation; the system may be used at MV levels. The system has advantages for the utility and the customer; it does not draw more power from the line to increase customer voltage, and it prevents customer equipment shutdown.

The inverter is cost effective. New ultracapacitor technology will be used. Unlike the present lead-acid batteries these energy storage devices have an almost unlimited lifetime. A new development in high-power MOSFET technology for hybrid electric vehicle applications makes it possible to greatly simplify the design and layout of the multilevel converter.

1.1.1 Minimum standards for electricity supply

Electricity supplies must provide reliable bulk power [1, 3, 6]. However, it is difficult for them to provide continuous power of the quality required for sensitive equipment. Quality power does not necessarily mean perfect power. Normal use of electricity generates disturbances, and hence unexpected power system problems, both natural and man-made, will occur. The nature of these disturbances, their severity and their incidence will vary from one location to another.

It is possible to improve the power quality at the user end, but this is only economically feasible for expensive, sensitive equipment.

Power quality may be seen as a combination of voltage quality and current quality, where voltage quality refers to the suitability of the product delivered by the utility and current quality is a measure of how well the customer needs are met [1, 3, 4].

Quality power allows the operation of sensitive equipment. The single most common detractor of power quality is power dips. They cause huge financial losses and are potentially preventable.

1.1.2 Voltage dips/sags

Electronic equipment has become much more sensitive these days than its counterparts 10 or 20 years ago. In countries with reliable power systems, outages are rare and voltage dips are the most costly [1]. The need for improved power quality arises from consumers suffering increased financial losses due to poor quality of supply [7]. In 1996 industrial customers sustained losses in the order of R 1,2 bn as a result of voltage dips [8]. Although this very high figure has been questioned, it is generally accepted that voltage dips are responsible for substantial economic losses in South Africa [9].

Eliminating voltage dips is a difficult, if not impossible, task since the utility does not have control over many of the causes of voltage dips such as lightning strikes, fires, accidental contact, etc. Strengthening the supply by installing additional or redundant feeds may reduce the depth of voltage dips, but this action may increase the occurrence of dips due to increased exposure [9]. Chapter 2 of this report will cover voltage dips more elaborately.

Voltage dip compensation may be achieved by: motor generator sets, tap changing transformers, Ferro resonant transformers, conventional UPS/power conditioners, active filters, shunt compensators and series compensators.

This project develops a series multilevel dip compensator. Costly parallel optic networks are replaced by a serial coupled inverter control chain. High-maintenance components are replaced. There is a significant reduction in the number of components and amount of maintenance compared to previous multilevel inverters or conventional uninterruptible power supplies. Ultracapacitors supply short-term energy. These devices will replace batteries as they need no maintenance.

1.2 Project background

During the last few years extensive research on power-quality compensators, including series compensators, has been done at the University of Stellenbosch [4, 5, 7, 10]. Some of these systems use transformers and large filter components that contribute to size, price and power losses. Their elimination [4] would be a huge advance.

In the past new classes of inverter topologies, the multilevel inverters [11-24], were explored. Their benefits are reduced cost in filter components and overall higher output voltage ratings. Further advances could see their implementation in the future. Prices of semiconductors have dwindled, while transformers and filter inductors remain costly.

This chapter introduces preceding work on series converters and closes with a motivation for the continued study.

1.2.1 **Previous work in this department**

The work on this project builds on a prior assignment [4, 5]. It covers the developed multilevel-cascaded inverter for cost effective and transformerless series dip compensation. Series injection dip compensators offer the advantage of only having to compensate for the decrease in supply voltage during a dip. This means a significant reduction in converter ratings and energy storage requirements compared to conventional uninterruptible power supplies or shunt injection devices. Existing inverter topologies, including multilevel inverters, as possible solutions for cost effective transformerless series dip compensation, were investigated and the conclusion was that the

multilevel-cascaded inverter was the most cost-effective option. The relatively low harmonic content of its unfiltered output voltage eliminates the need for a large output filter. A single-phase dip compensator with this topology was designed and built according to specifications laid down by Eskom, the main utility in South Africa. Batteries for energy storage and automotive MOSFETs as switches were the most cost effective options for the specified power ratings. Figure 1-1 shows the basic diagram of a single-phase multilevel inverter.

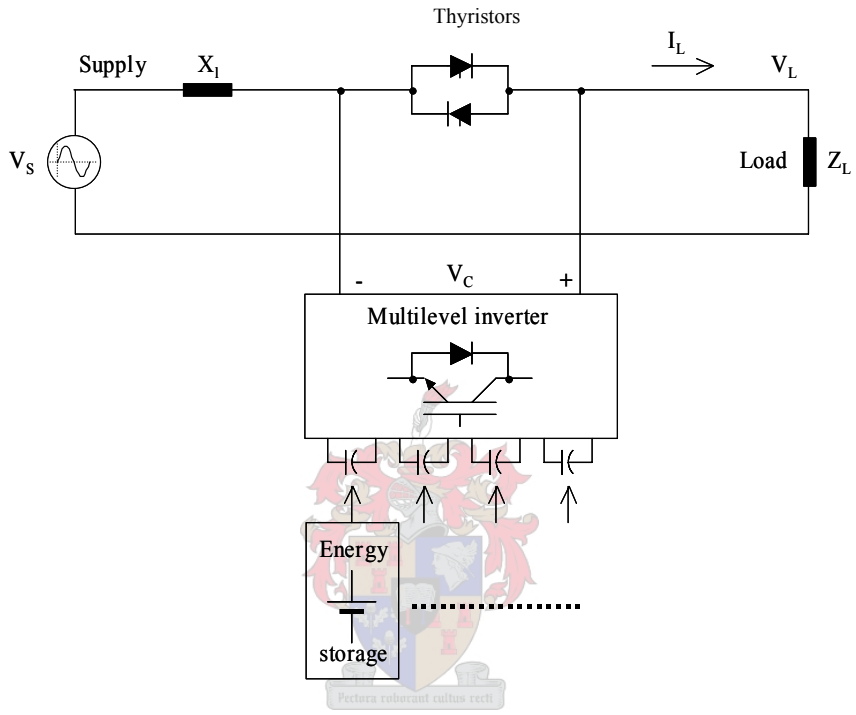


Figure 1-1 Dip compensation with a multilevel inverter in one phase [4, 5]

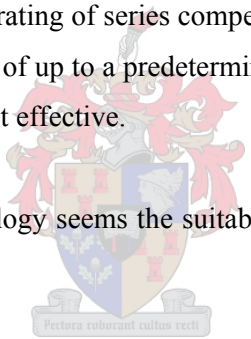
Previous attempts to develop dip compensation schemes at the University of Stellenbosch include the work of D.D. Bester [10] and T. Geyser [7]. Bester's thesis covered the control and implementation of a series compensator for a power-quality conditioner. It combined a series compensator with an active shunt compensator to form a power-quality conditioner. The necessity of the series compensator arouse from functional and financial considerations. Geyer's thesis examined problems associated with the delivery of quality power. It covered extensive research on voltage dips and their origin.

Companies active in this field include DynaCom™ (Singapore) [25] and Dip Proofing Technologies Inc. (USA) [26]. DynaCom™ offers a wide range of dip compensators for single and three phases up to 1 MVA. These are also based on ultracapacitor technology and require low maintenance.

However, their voltage rating is fixed to 400V and may not be interleaved for higher ratings. Dip Proofing Technologies Inc. offers products that compensate for voltage dips on low-power systems. They are transformer based and contain no energy storage.

1.2.2 Earlier literature

The background to voltage dips is a comparison of power conditioners for voltage dip compensation (Table 3-1 [4]). They can be caused by line electrical faults and this is an increasing concern for the industry, because modern technical equipment is becoming more sensitive to dips. Large financial losses can result because shutdowns result in lost production time and damaged products. Compensatory measures can be divided into two main groups, namely utility and customer solutions. Customer solutions in the form of power-conditioning equipment seem to be the most effective way to eliminate dips. A lot of converter technologies (UPS, active filters, AC-AC converters) counteract dips, but they are very expensive. Transformers are the main contributors to the costs of these systems. The power rating of series compensation devices, like series active filters, can be reduced to compensate for dips of up to a predetermined depth. Then series dip compensation without a transformer may become cost effective.



The multilevel cascaded inverter topology seems the suitable inverter for transformerless series dip compensation.

Companies offering dip compensation products include Rainbow Technologies with the “Dip Doctor”, which is a rotating machine operating at 100MVA (132kV). Liebert Corporation produces magnetic synthesizers which consist of blocks of an isolation transformer and inverter to rebuild a new immaculate sinusoidal voltage waveform. Dozens of companies produce online UPSs with energy stored in batteries (Dell, Power Tree and Netsavers). All of these systems convert the input voltage signal to DC and back to AC. This requires an inverter with full-load kVA rating and a large output filter. An offline UPS (PowerCom, UTL Electronics) feeds the input signal directly to the output without first converting it to DC to make the system more energy efficient.

The multilevel cascaded inverter eliminates the output filter and as a result has lower switching losses than the single inverter and it is modular (Table 1-1). The single inverter’s voltage rating will be limited to the rating of available switching components. This topology eliminates extra clamping diodes and voltage-balancing capacitors which are present in the other constructs. This topology compared well with the single transformerless series inverter for cost effectiveness. The cascaded multilevel inverter topology is shown in Figure 1-2.

	Single inverter with an output filter	Direct-coupled multilevel cacaded inverter
Voltage rating	Limited to about 6.5 kV	Limited to the amount of inverters in cascade
Large output filter components	Yes	No
Packaging and layout	Only one inverter per phase	Multiple inverters per phase (modular)
Switching losses	High	Low
Control	Continuous, but PWM control of the voltage loop is difficult with varying loads.	Discrete, but fast.
Compensation for other power quality problems	Yes	No

Table 1-1 Unique properties of the two topologies [4]

1.2.3 **Basic design guidelines arising from this study**

The basic structure of this design is based on three considerations: efficiency, viability and simplicity. The focus is therefore on devices that offer flexibility, i.e. that they will only be 'switched on' on demand by a dip event and bypassed otherwise. This allows for high efficiency during times when the source line voltage is ideal.

A general method to reduce cost is only to compensate fluctuations in source voltage, rather than rebuilding the whole signal to a perfect state. This may be achieved by injecting serial voltage into the line that cancels out the disturbance (Figure 1-1). This reduces cost. An inverter only requires the power rating to match the fault.

A modular design provides customer satisfaction by being adaptable to different requirements. Specifications may be altered by simply adding or removing modules.

1.2.4 **Hardware in previous model**

The compensator shown in Figure 1-2 was designed for a single-phase supply to a typical small industry to compensate for general dips. The inverter is modular in construction. Hence a custom-made converter for a particular dip depth can be created easily.

The major objective was cost effectiveness. Battery energy storage and MOSFETs as switching components proved to be the most cost effective components for the specified ratings. The design of

the DC bus was unique, because of the low voltage and high current ratings. DC bus capacitors were added to stabilize the DC bus voltage and also to compensate for reactive load currents. The anti-parallel Thyristors were designed to conduct the line current continuously and to conduct fault currents of up to twenty times the rated current. A fault current detection circuit was therefore also incorporated [4].

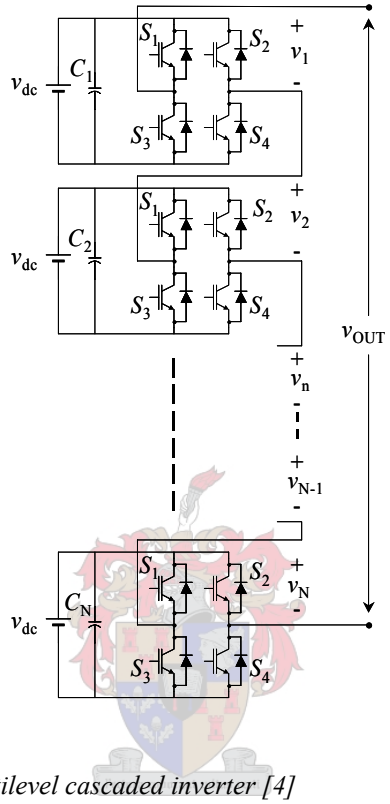


Figure 1-2 Circuit diagram of a multilevel cascaded inverter [4]

Driver circuits able to drive ten MOSFETS in parallel were designed. Digital control was implemented through an established DSP control board. Finally, a gate signal multiplexer worked together with this control in order to implement the 20 gate signals needed for the multilevel inverter.

1.2.5 **Control**

The multilevel inverter's principles of control for series dip compensation can be described as follows (these descriptions are taken verbatim from [4]):

Normal conditions: Under normal conditions, the Thyristors conduct the full load current and all the MOSFETs in the multilevel inverter are switched off [4].

Initiation and termination of compensation: When the line voltage drops below 90% of the nominal RMS voltage, the Thyristors are force commutated by the output of the multilevel inverter. The multilevel inverter then starts to inject a staircase voltage waveform in series with the line. The compensation is terminated when the line voltage rises above 90% of the nominal RMS value or if the energy storage is depleted. The output of the multilevel inverter is first switched to the zero output state and then the Thyristors are switched on. The multilevel inverter is switched off after a sufficient turn-on delay for the Thyristors [4].

Injection of the staircase sine waveform: The generation of this waveform is based on the single-pulse technique. This method can be explained by Figure 2.3. It shows that the voltage pulses contributed by each individual inverter are terminated in the same order that they are initiated. This method is one way to level the duration of discharge for each DC bus, but it will not make it equal. According to [10], the maximum deviation of the discharge values for five inverter units is about 10% if the injected voltage is sinusoidal.

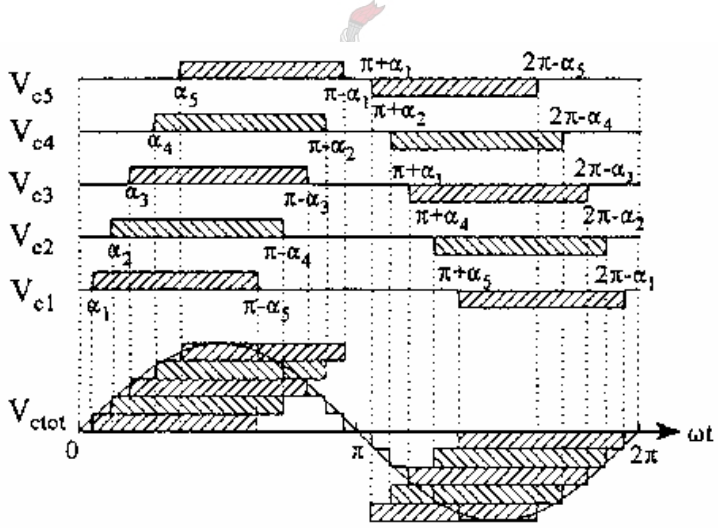


Figure 1-3 Single-pulse technique for the generation of the staircase sine wave [4, 14]

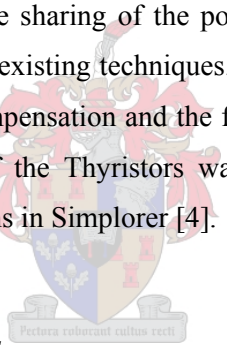
Sharing of the power dissipation: Sharing of the power dissipation in both the switches and the energy storage can be achieved by continuously changing the switching order of the individual inverter units [13] and also by utilizing redundant switching states [4, 24].

Protection: When a fault occurs on the load side of the compensator during a dip, the multilevel inverter must cease its operation as soon as possible and the Thyristors must take over the fault current simultaneously until the necessary circuit breaker is opened [4].

New strategies for voltage dip detection were expanded. The method gives an immediate response in case of a dip. The exact dip depth can be determined after ¼ cycles. The dip detection is done by defining the instantaneous value of the phase voltage at time t_0+T/4 as $A\cos(\omega t_0 + \Phi)$, and at time t_0 as $A\sin(\omega t_0 + \Phi)$. The amplitude of the supply voltage can then be determined by making use of these two values and the identity in equation (1-1) [4].

$$A = \sqrt{\left(A\sin(\omega t_0 + \phi)\right)^2 + \left(A\cos(\omega t_0 + \phi)\right)^2} \qquad (1\text{-}1)$$

The ¼ cycle relationship and the DFT synchronizing techniques were chosen for dip detection and synchronization respectively. In the latter method the reference signal gradually adapts to the phase shifts at the beginning and end of the voltage dip. The way in which voltage steps are added to the supply voltage is based on existing techniques. The existing techniques are based on the assumption of a relative steady-state output voltage, which is not the case for the transient nature of voltage dips. Because of this a new technique for the sharing of the power dissipation in the switches and the batteries had to be developed, based on existing techniques. Finally, the control of the Thyristors in the initiation and termination of dip compensation and the fault current protection was discussed. A new method for force commutation of the Thyristors was also developed. Most of the control methods were confirmed with simulations in Simplorer [4].



1.3 Motivation for the study

This project sought to investigate the possibility of developing a cost effective multilevel dip compensator based on ultracapacitor energy storage. Due to the relative short duration of typical dips in South Africa, ultracapacitors are highly attractive energy storage devices for this application. Unlike the lead-acid batteries that are used in the current system, these energy storage devices have an almost unlimited lifetime. This eliminates the need for short-term maintenance on the system. A new development in Power MOSFET technology for hybrid electric vehicle applications makes it possible to greatly simplify the design and layout of the multilevel converter. A survey of recent MOSFET technologies will be prepared and ultracapacitors technologies will be compared.

Another very important motivation for this project is the need for this sort of technology. Huge financial losses are experienced currently (Chapter 2) and can be prevented with such technology.

1.4 Thesis Outline

This thesis starts by giving a background on power quality and voltage dips in South Africa in Chapter 2. It includes statements made in a recent survey on financial losses caused by dips.

Chapter 3 specifies the requirements for dip compensation and explains why the Marxian multilevel inverter with ultracapacitors is a cost effective method of transformerless series dip compensation. A detailed study of ultracapacitors is included.

The system design of the above-mentioned inverter is explained in Chapter 4. This chapter shows the detailed structure of the complete device used in Chapter 5 for results and measurements. Simulations and practical tests show the working of such a device with ultracapacitors.

2 Supply shortcomings

2.1 Introduction

The rationale behind this project is the need to investigate a number of existing power supply shortcomings, which will be introduced in this chapter. The aim of this project is to offer a simple solution to these problems. The information used in this chapter originates from an Eskom research report on voltage dips in South Africa [8, 9] as well as studies conducted in the USA regarding voltage dips [1, 4, 7, 10, 27].

2.2 Network faults affecting a transmission supply point

One of the main tasks of Eskom is to provide a reliable electricity supply to its customers at reasonable prices. The more reliable the electricity supply, the higher the price. If the system reliability is low, power interruptions and voltage dips tend to occur more often and will result in cost increments for Eskom and in turn for the customers [9].

The relationship between supply reliability and economical viability must be taken into consideration as it is necessary for Eskom to maintain a balanced operation. The optimum reliability level will be the balanced point between the total cost of supply and the benefits to customers. To determine the cost impact, a study [9] presents the costs involved for customers and suppliers in power interruptions and voltage sags. The power disturbance can cause both direct and indirect damage. This means that a loss of production, equipment damage and wastage of materials and labour are a direct result, while environmental, safety and civil unrest, cancellation of goods orders or late deliveries are indirect consequences of power disturbances like voltage dips.

The electric power interruption or dip cost should be estimated in financial terms. Estimating the direct impacts is possible, although often complicated, whilst estimating the indirect impacts is even more difficult. This is because the perspective of each consumer on the impacts of disturbance differs according to his or her objective for the usage of power. Consumer categories, interrupted activities, duration and period of disturbances should be part of the criteria for cost estimation [9].

2.3 General information on voltage dips

Power quality has become an active research field over the past decade as a result of the increased sensitivity of modern electronic equipment to power system disturbances [1, 3, 6-10, 27-39]. Of these disturbances, voltage sags and momentary interruptions are the most disruptive [7]. In order to compensate for voltage dips, they must be well defined in terms of the effects they will have on industries that suffer the greatest losses. Paragraph 2.3.1 and paragraph 2.3.3 describe the causes and effects on industrial plants of voltage dips, paragraph 2.3.4 elaborates on the characteristics of the dips and paragraph 2.3.4.1 discusses phase shifts associated with 3-phase dips. Paragraph 2.4 discusses methodology for determining the costs of dips, and paragraph 2.5 quotes some costs experienced in South Africa due to dips. Paragraph 2.6 concludes with requirements for a dip compensator from information on recorded dips.

2.3.1 Causes of voltage dips

2.3.1.1 Temporary loss of supply

The supply to a plant can be temporarily disconnected for a short duration and the electrical plant can be made to resume operation immediately after the supply recovers, thereby maintaining operation of the process. Sources of this type of voltage dips are usually automatic re-close (ARC) dead times and switch over from one supply to another supply source [3, 9].

2.3.1.2 Short-circuits

The supply voltage to a plant will dip when a short-circuit occurs on the supply side or within the plant distribution medium- or low-voltage system [9].

2.3.1.3 Load switching

Switching of load onto the supply can result in partial voltage dips. Major problems could be experienced when large direct on-line induction motors are being started [9].

2.3.2 Network switching

Switching on either the supply system or the plant internal distribution network can result in various types of voltage dips. Paralleling two supplies running at different load angles will result in a fast transient voltage change followed by a dynamic condition before settling at the new steady-state load angle. The transient changeover is usually fast and it is unlikely to have an effect on normal electrical plant, unless the plant is very sensitive to voltage dips, such as with power electronic equipment [9].

2.3.2.1 Power swings

When the supply network is weakened by the loss of transmission lines or after severe faults on the supply network, power swings between generating stations lasting several seconds can occur on the network [9].

2.3.3 Effects of voltage dips on industrial plant

2.3.3.1 Impact on the plant process

When a voltage dip occurs in the supply of an industrial plant, various parts of the plant process will rapidly approach a point where the process must be discontinued in order to safeguard the plant. It is essential to know the time it takes from the initiation of the voltage dip to the time when the process must be discontinued for a plant, before any counter-measures can be designed. It is also important to arrange the electrical supply equipment in such a manner that its outage time is minimized following a voltage dip. Unsuccessful ARC of transmission lines can result in a second voltage dip. It is thus important to restore the plant process as soon as possible after voltage restoration.

2.3.3.2 Drop-out of contactors

A common problem with low-voltage (LV) switchgear is that the electricity held in contactors falls out during voltage dips. The supply controlling the contactors is normally taken directly from the associated bus-bar supply voltage. When the control voltage falls below 70% [9, 35] of its nominal value, the contactor may open and the seal-in contact will open. LV drives may thus stop when a voltage dip occurs.

2.3.3.3 Variable speed drives

Adjustable speed drives (ASDs) trip due to voltage sags, interfering with production and resulting in financial losses [40]. Smooth operation of ASDs following a voltage dip is not possible on all types of ASDs [4]. The operation of firing circuits controlling power electronics such as thyristors cannot be maintained when the voltage falls to a low level and the drive must therefore be stopped.

2.3.3.4 Control equipment supplies

The application of control equipment such as programmable logic controllers (PLC) in plants is very common. However, this type of control equipment requires a standby supply. Care should be taken such that the supply to such equipment is secure against voltage dips [9].

2.3.3.5 Protection

The setting of protection relays plays a major role in the smooth operation of a plant during voltage dips. The incomer, transformer, MV switchgear and motor protection relay settings must be correctly set in a coordinated manner. The settings of all under-voltage relays and their associated timers on the entire plant should be coordinated to make maximum plant electricity available during a voltage dip without exceeding the capability of the equipment [9].

Any electrical system is vulnerable to short-circuits (some more than others) which lead to voltage dips. If the effect of voltage dips is taken into consideration during the design phase of a plant, the best method can be implemented to ensure the smooth running of the plant. This is not always done and remedial action is taken only when the problem reveals itself during the commissioning phase. A great deal of information on the supply system and the plant process is required before decisions can be made on appropriate counter measures to avoid loss of production during voltage dips.

2.3.4 Characteristics of voltage dips

Preventative actions can be taken to reduce voltage dips, but it is impossible to eliminate them. Voltage dips may occur on more than one phase simultaneously and may repeat themselves more

than once in less than a few seconds. All of these will cause only one process shutdown event, because of an under-voltage trip of an ASD (adjustable speed drive) or a logic controller.

The frequency of dips is another important factor, because it can give an indication of the financial losses that will be incurred at sensitive industrial plants. The performance and expense of present solutions for voltage dips must be considered in order to determine the viability of the solutions [4]. According to IEEE standards [31], the depth of a dip ranges from 10% to 90%. If the depth of a dip is more than 90%, it is defined as a momentary interruption.

IEEE Std 1159 0 defines the duration of a dip as lasting between half a cycle and 1 min. NRS048 [35] defines it as lasting between 20 ms and 3 s. A voltage loss of a longer duration is defined as insufficient voltage regulation. There is no specific definition for the phase shift at the beginning and end of the dip, but it can be defined as the worst phase angle between the generated voltage on the utility grid and the voltage waveform during the dip. According to Eskom [8], phase shifts of up to 30 degrees have been measured on their system.

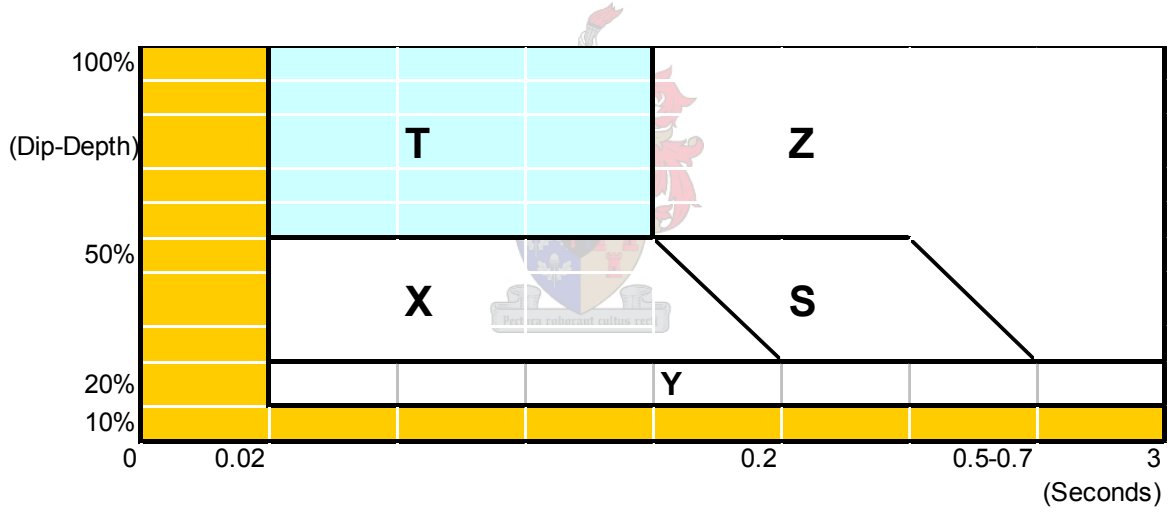


Figure 2-1 Voltage Dip Chart [35]

Dip data in South Africa are represented in the form of a two-dimensional plot of dip depth and duration (Figure 2-1) [8]. The magnitude of the dip is given by the maximum RMS excursion from nominal and the duration of the dip is given by the maximum duration of the worst affected phase in each case. The areas S, T, X, Y and Z have been in use for more than 15 years and originated when observing different performance of protection of interconnected systems. Dips in area X are caused by faults remote from the dip location which are rapidly cleared. Dips in area T resemble large faults local to the dip measurement site. Dips in area S are usually low-level faults cleared slowly by

protection such as backup relays. Z area dips usually represent poor or incorrect protection operation. The dips of interest for this project are dips in area X and Y only (paragraph 2.3.5).

2.3.4.1 **Three-phase voltage dips**

Most industrial equipment requires a balanced three-phase supply voltage. A phase shift on one or more phases on an induction or synchronous machine, for example, would result in unwanted vibrations or high transient currents and eventually causes shut down of the machine. Three-phase thyristor-based equipment would shut down even for small phase shifts. It is therefore important to maintain phase for all three line voltages.

Phase shifts on a three-phase system are even more likely to occur than on a single-phase system [1]. A shift is caused, for example, when a single line-to-ground fault occurs on a high-voltage (HV) line that is then down transformed with a D-Y connected transformer. Depending on dip depth on the HV line, the phases on two of the low-voltage (LV) outputs phase shift drastically. Even if the fault is caused on the (LV) side, the phase of one or more lines may change when a delta connected load is coupled [1]. Figure 2-2 represents the most common relationships between single line-to-ground and line-to-line faults on the primary of the transformer and resulting secondary phase voltages. This clarifies why three-phase dip compensation must include phase compensation as well.

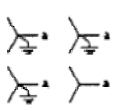
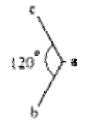
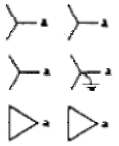
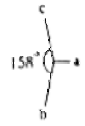
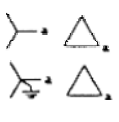
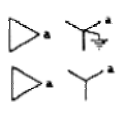
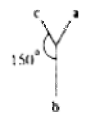
Transformer Connection	Phase to Phase Vab	Vbc	Vca	Phase to Neutral Vab	Vbc	Vca	Phasor Diagram
	0.58	1.00	0.58	0.00	1.00	1.00	
	0.58	1.00	0.58	0.33	0.88	0.88	
	0.33	0.88	0.88	----	----	----	
	0.88	0.88	0.33	0.58	1.00	0.58	

Figure 2-2 Transformer secondary voltages with a fault on the primary [27]

2.3.5 **Requirements for voltage dip compensation**

A decision for the final specifications for the dip compensator was taken after examining available data on voltage dips on several sites graphed in Figure 2-3. These data supplied by the EPRI DPQ [31] Project were obtained from monitoring 222 distribution feeders in the United States from 1993 to 1994.

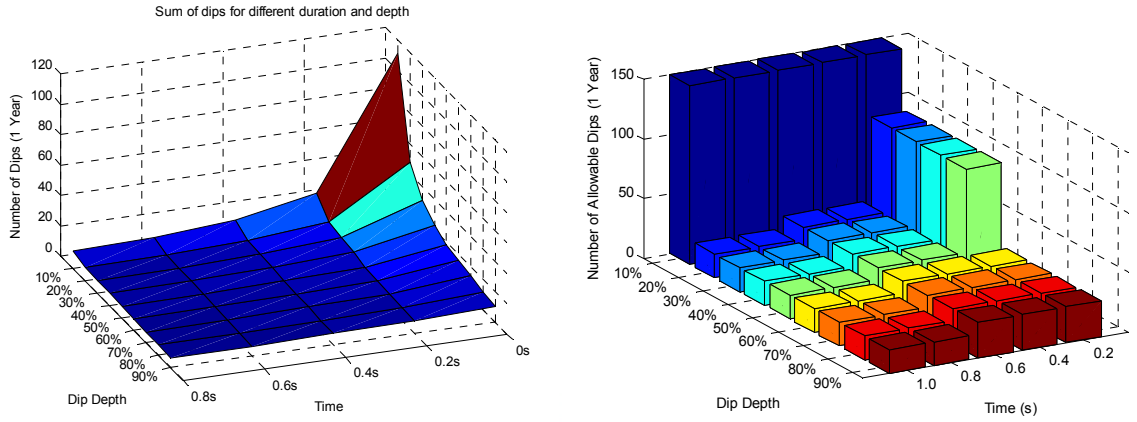


Figure 2-3 Sum of dips (1 year) for different dip depths and dip durations (EPRI DPQ Project) [31]left and supply specifications NRS 048 [35]right

An interesting fact arising from the data used to plot Figure 2-3 is that about 88% of the voltage dips (below 90% in magnitude) had a depth of 10-30% (magnitude 70-90%) and a duration of less than 200 ms. Another one-year survey at a single industrial plant [39] showed that about 79% of all recorded dips (below 90% in magnitude) had a depth of 10-30%. According to yet another survey [41], voltage dips of 10-30% below nominal for 3-30 cycle durations account for the majority of power system disturbances and are the major cause of industry process disruptions. Therefore the probability of small dips (Plane X and Y in paragraph 2.3.4, Figure 2-1) is generally much higher than the probability of large dips because of typical electrical supply configurations [4].

Another consideration to be taken into account is phase shift. At a D-Y transformer connection for example, the worst phase shift occurs when there is a line fault on the primary. There may be phase shifts of up to 30˚ on some lines [8]. In order to compensate for both the dip and the phase shift the dip compensator must add a voltage with much greater amplitude. This phenomenon is shown in Figure 2-4.

This shows that the dip compensator rating, even though it is said to compensate for 30% voltage dip, must be able to inject up to 53% of the phase voltage. At a phase voltage of $230V_{RMS}$

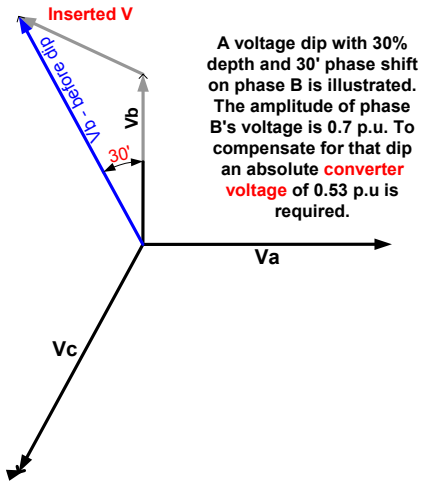


Figure 2-4 Total magnitude required to compensate for voltage dip with phase shift

the dip compensator is required to inject maximum amplitude of 170V. Thus the final design specifications are as follows:

- Three-phase dip compensator with 50 kVA rating;
- Five-step multilevel series inverter per phase (assuming that each step front is 40V. This value is deduced from THD limitations; paragraph 4.4.2.1, Figure 4-7);
- Peak stacked inverter voltage: 170V (5 x 40V = 200V subtract 30V losses => 170V);
- 40V per inverter. At peak current of 110A the total inverter voltage must not drop by more than 30V.

The above-mentioned converter specifications cover the requirements set by Eskom. The dip compensator will be able to compensate for 88% of all dips. Under-voltages as well as over-voltages can be corrected. The range will cover all voltage dips with a magnitude up to 30% of rated voltage and will compensate phase shifts of up to 30˚ from nominal voltage signal.

2.4 Methodology for finding costs of network faults

A debatable issue for years was how much the effects of voltage dips contribute to the financial losses of customer and supplier. Until recently no one could correctly estimate the real contribution of this element of power quality loss. This is the reason why it was difficult to market a product like the dip compensator. The concept was supposedly too difficult to sell, for there was no real evidence of loss and clear financial statistics were non-existent. For Eskom the quality of power delivered to customers is a trade-off between losses experienced due to low-quality power transmission lines and investment or maintenance costs.

An Eskom study [9] (Appendix A) puts values to voltage dip data. This is of great importance to the further proceedings of this technical report, so the methodology used to ascertain financial losses involved with voltage dips is taken verbatim from [9]:

The main emphasis is to attempt to estimate the overall economic impact of a network fault event. Actual load profile measurements just before and after a fault are taken to estimate the amount of energy lost after a fault event (Figure 2-5). By knowing Eskom's internal costs and the approximate cost of unserved energy, it is then possible to estimate the cost impact per fault event [9].

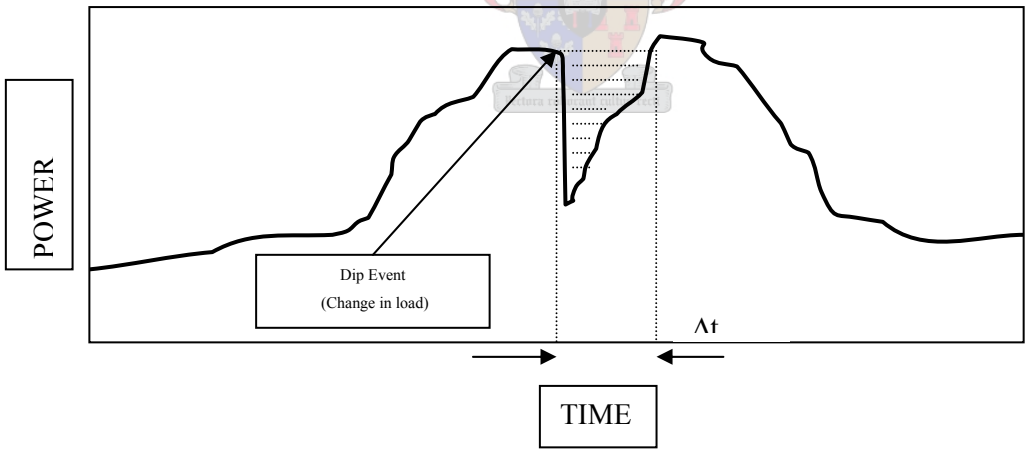


Figure 2-5 Typical load profile of a substation before and after a voltage dip [9]

The estimated load loss after a fault is shown by the shaded area in Figure 3 above. The impact of a fault can be felt at more than one substation; for example, a fault (F1) in the transmission network (see Figure 4 below) will cause a voltage dip for both substations A, B, C and D. It will therefore be necessary to obtain load profiles for all four substations [9].

Just as a stone falls on the water surface and causes ripples, the impact of a fault and the subsequent voltage dip can be felt on different parts of the network. This kind of study will be called Stone On Water Surface. These studies help to identify which customers are affected after a voltage dip or a power interruption event [9]. Normally, all the substations situated closer to the faulty line get affected [9].

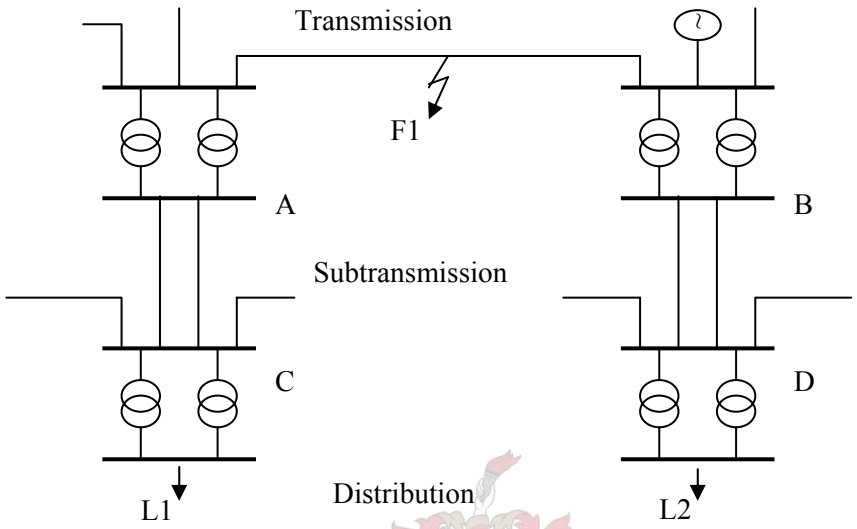


Figure 2-6 A Typical Power System Layout [9]

The voltage dip is then transferred down to all consumers (such as L1 and L2).

The methodology for finding financial losses [9] can be summarized as follows:

- Identify the area which is experiencing dips and power interruptions.
- Refer to quality of supply (QOS) database and transmission and distribution performance database.
- Identify list of faults in and around the specific area or transmission line that is being studied.
- Determine Eskom's internal cost due to each fault. Cost for transformer loss of life, line patrol costs and increased maintenance costs for network equipment must be taken into account.
- For each fault determine impact on customers by studying the load profile at each of the affected feeder substations.
- Estimate the amount of energy lost at each substation affected by the fault.

- Estimate the cost of the unserved energy by identifying affected customers. Then check the database to determine if these customers have been surveyed previously. If no survey information available, arrange for customer surveys utilizing a questionnaire.
- Develop business case to improve performance (e.g.: reinsulation, bird guards, earthing etc.).

2.5 Cost of unserved energy

A voltage dip that affects consumers generally leads to a loss of load and subsequent load recovery. In some cases it is expected that the very smallest load loss may still have a significant impact on the customer. It has been proven that by performing load profile measurements and customer surveys, it is possible to estimate the cost impact per power interruption or dip event.

Year	*Transmission Line*	*Number of major dips*	*Power Lost*	*Cost of Power*	*Main Damage (Supply)*	*Total Cost of faults [9]*
2001	Harvard-Perseus	1	112 MWh	R10/KWh	Transformer loss of life	R1.12m (Power Lost) R0.053m (Other exp.)
2001	Harvard-Merapi	14	0			R46 090 (Other exp.)
2001	Matimba-Witkop-1	19	644 MWh	R10/KWh	Transformer loss of life	R6.44m (Power Lost) R1.01m (Other exp.)
2002	Bighorn-Middelkraal-1	4	403.75 MWh	R21/KWh	transformer loss of life costs and line patrol	R8.478m (Power Lost) R0.213m (Other exp.)
2001	Avon-Impala	3	0		transformer loss of life costs and line patrol	R0.160m (Other exp.)

Table 2-1 Cost of unserved energy [9]

In order to estimate the customer costs for the above studies, it was essential that customer interviews be conducted. The study conducted by [9] also presents customer questionnaires to determine the financial losses experienced by the customers due to voltage dips. These losses were not considered for the purpose of this report due to their complexity and irregularity.

2.6 Summary

Substantial financial losses are experienced as a result of voltage dips. This can be deduced from the study done by Eskom in 2002 [9], which is summarized in paragraph 2.5. The problem with voltage dips is that their existence and causes are still widely debated and usually neglected, because of their complexity and ignorance about their effects. Designing a voltage dip compensator presupposes that dip compensation is a requirement in industry.

This chapter covered the explanation of voltage dips and their causes. In conclusion, a financial study shows that voltage dips cause major losses to Eskom. It was found that 88% of all voltage dips (below 90% of nominal magnitude) had a depth of 10-30% and duration of less than 200 ms. It was thus decided to design the dip compensator to compensate for such dips only and not compensate for other dips as the massive cost increase to compensate for the remaining 12% would not be justified.

3 Viable options

3.1 Introduction

There are some evident solutions with regard to transformerless dip compensation systems. This chapter gives a brief history of existing industry solutions and compares new possibilities for dip compensation.

The objectives of this project are to:

- Re-determine the most cost effective topology for series multilevel inverter for dip compensation;
- Find the more suitable energy storage;
- Develop control strategies and dip detection algorithms for three-phase dip compensation;
- Design and build a 50 kVA three-phase laboratory prototype of a transformerless dip compensator adaptable to high-voltage electric distribution systems.

The overhead requirements for dip compensation are indicated below:

- As was discussed in earlier chapters, the operation is four quadrant if phase compensation is indeed a pre-requirement. For most equipment it is inevitable and logical to compensate for phase as well as amplitude shifts. Very high transient currents come as a result of sudden phase shifts. This possibly causes tripping of breakers resulting in shutdown;
- Adequate protection is another requirement. This is self-evident on a power-quality enhancing device.

3.2 Existing solutions

3.2.1 Introduction

Two very detailed studies on existing solutions [4, 6] will be summarized here for convenience.

3.2.2 **Customer Solutions**

According to [1, 4] customer solutions may involve integrating power-conditioning devices such as:

Technology	*Power rating (p.u.)*	*Trans-former*	*Large filter compo-nents*	*Energy storage compo-nents*	*Other components*	*Performance*	*Compensation for other power-quality problems*	*Commercial/ research*
Tap-changing transformer	1.0	Yes	No	None	Many thyristors	Discrete compensation, slow response	No	Commercial
Ferro-resonant Transformers (CVTs)	4.0	Yes	No	None	Not of significance	Effective for constant low-power loads	No	Commercial
Magnetic synthesizer	1.0	Yes, more than one	No	Capaci-tive storage	Non-linear chokes	Very effective	Yes	Commercial
M-G set	2.0	No	No	Flywheel	A motor and a generator	Effective for dips of up to at least 6 s	No	Commercial
Rotating machine	1.0	No	No	No	Series reactor	Reduce dips only	No	Commercial
UPS	2.0	Yes	Yes	Any type	Many power electronic components	Very effective	Yes	Commercial
Shunt active filter	1.0	No	Yes	Any type	Power electronic components	Very effective	Yes	Commercial
Series active filter	≤ 1.0	Yes	Yes	Any type	Power electronic components	Very effective	Yes	Commercial
UPFC	> 1.0	Yes	Yes	Any type	Many power electronic components	Very effective	Yes	Research
AC-AC converter	1.0	No	Yes	None	Power electronic components	Effective, but limited	No	Research

Table 3-1 Comparison of power conditioner for voltage dip compensation [1, 4]

It may not fall within the scope of this thesis to change the reliability of the utility as regards the problem of dips; this study focuses on a customer-oriented solution with power electronics.

3.2.3 Utility solutions

Utilities can take certain measures to prevent faults that cause dips. There are mainly three options to reduce the number and severity of faults on a power system:

- Preventing faults by routine transmission-line maintenance and attaching lightning grounders to transmission poles;
- Modifying fault-clearing mechanisms and feeder design for optimum power reliability; and
- Reducing dip magnitudes by delta-wye transformer implementation.

While all of these solutions may reduce the frequency or depth of voltage dips, they will not eliminate them.

3.2.4 Total plant solutions

Voltage dips should be treated as a compatibility problem between equipment and supply [31, 42]. Short-circuit simulations determine the plant voltage as a function of fault location throughout the power system [31, 42]. Historical fault performance (faults per year per specified distance) can then be used to estimate the number of dips per year that can be expected below a certain magnitude. From these data the effect of dips on equipment in the plant can be determined. Several things can be done by both the utility and customer to reduce the number and severity of voltage dips. Measures can also be taken to reduce the sensitivity of equipment to voltage dips [4].

3.3 Requirements

This study is restricted in that any solutions considered have to be transformerless. Thus several possibly advantageous solutions may not be considered in depth at all. Other studies [4, 10, 34] have more detailed information on transformer based solutions. They are not reviewed here. This report focuses on a subsection of possible solutions investigated in depth.

3.3.1 Phase shifts and voltage regulation

There is very little data on the phase shifts experienced during dip condition. A typical transmission line undergoes several transformation stages before serving energy to the customer. Figure 2-2

represents the determining three-phase output voltages referred to the output side of the transformer when a fault occurs on the input side. A 30° phase shift is not unusual in the D-Y and Y-D transformation. This is confirmed by Eskom [8]. The phase shifting property of dipped voltages confirms that four-quadrant operation is a necessity.

Any solution encouraged should be capable of keeping the output voltage amplitude constant without emitting excess harmonics and distortion onto the transmission line. In short the following requirements should be met:

- Line independent operation phase [5, 8] Figure 2-2
- Fast response to sudden change in voltage (response time must be half a cycle or less according to [4, 27])
- Dip compensation up to 30% for more than 200ms for compensation of most dips [4, 8, 9, 27, 31, 35]
- Three phase as well as single phase operation
- Prototype operation at 230V, 75A. Possibly upgradeable to high voltage systems
- Adequate protection algorithms must be implemented to protect sensitive loads [23]

3.3.2 Energy storage

Some functional topologies for dip compensation require energy storage. Energy storage has several major advantages over dip compensation without energy storage. The advantages are mainly freedom of four-quadrant operation in single-phase transformerless operation and source current levelling during transient behaviour. The only disadvantages anticipated with energy storage are cost, weight and lifetime of such devices.

The focus is on solutions utilizing energy storage. This is not only because of four-quadrant operation (with any possible output voltage phase), but for reasons of simplicity and practicality. The matrix converter [11, 12], for example, can be made to operate in four quadrants with any possible output phase without energy storage. However, when the input voltage sags, the input power must still equal the output power. This might result in overloading an already unstable dipped line. The matrix converter is a shunt device and has many disadvantages when compared with serial devices.

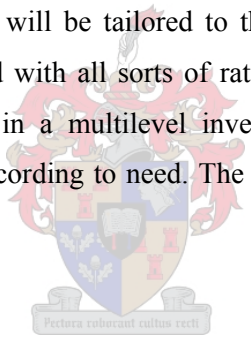
No pure serial devices (four-quadrant operation) able to compensate for dips without energy storage have been described in the literature reviewed. This indicates that at a practical level the most suitable serial inverters involve energy storage.

The requirement for energy storage is that it should contain enough energy to compensate for dips, and that stored energy may be released quickly during a dip. In short, the requirements are:

- High power density;
- Low-cost energy storage;
- Maintenance free;
- Long lifetime (+ 20 years).

3.3.3 Modular design

The final design in a given situation will be tailored to the needs of the customer. A multilevel inverter-based solution can be offered with all sorts of ratings, prices and dimensions. Figure 1-2 shows that there are some sections in a multilevel inverter that are identical. The number of subsections, or modules, may vary according to need. The simplest and most modular design from [4] is reviewed in this study.



3.3.4 Protection

The dip compensator is meant to increase, not degrade the power quality during unreliable operation. In [23] protection issues involved in the multilevel inverter implementation are discussed. The paper mentions that penalty costs are involved with shutdown as a result of device malfunction or protection failure. Adequate procedures need to be implemented to ensure predictable and reliable function.

3.4 Functional topologies – a comparison

Some functional topologies have been simulated with SIMPLORER to verify their working. SIMPLORER is a well-known simulation package widely used for designing power electronic

devices at the University of Stellenbosch. The most promising of all topologies investigated are listed.

3.4.1 AC-to-AC Converters

The AC-to-AC inverter topology is a new method of regulating the AC line voltages. AC-to-AC converters can be produced very cheaply and their operation is reliable as they contain few components and no energy storage. They are shunt devices, which implies that the switching components are exposed to full line-power ratings.

3.4.1.1 Indirect matrix converter

The matrix converter was first introduced in 1980 by M. Venturini [11, 12]. The indirect matrix converter topology [12] is shown in Figure 3-1. With a boost converter on the DC bus the output voltage can be increased. The indirect matrix converter offers a DC bus connection without energy storage. This converter is still classified as an AC-AC converter because it has no DC storage capacitors. The switches in the matrix converter are bidirectional and can block currents in both directions. Compared with the conventional AC/DC/AC converter or back-to-back converter, the matrix converter has the following merits [12]:

- No large energy storage components, such as large DC capacitors or inductors, are needed. As a result, a large-capacity and compact converter system can be designed.
- Four-quadrant operation in the indirect matrix converter is straightforward [11]; both output voltage and input current are sinusoidal only with harmonics around the switching frequency [12].

The indirect matrix converter was investigated and constructed according to Wei and Lipo [12]. All simulations are made by reconstructing their experiments. As the matrix converter traditionally does not boost the voltage threshold, a boost converter addition is added to the proposed topology. There is no change made to the matrix or conventional three-phase converter switching pattern. The boost converter switches at much higher frequency than the other converters to reduce any ruling distortion introduced thereof.

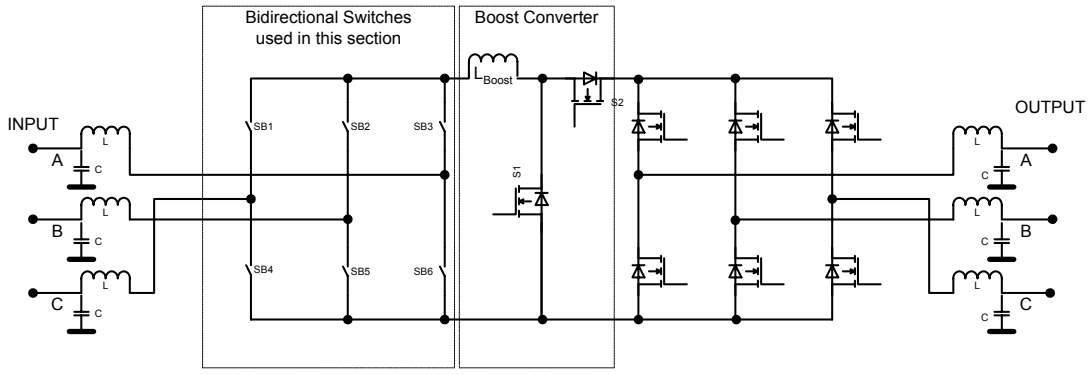


Figure 3-1 Basic topology of the indirect matrix converter [12]with a boost converter.

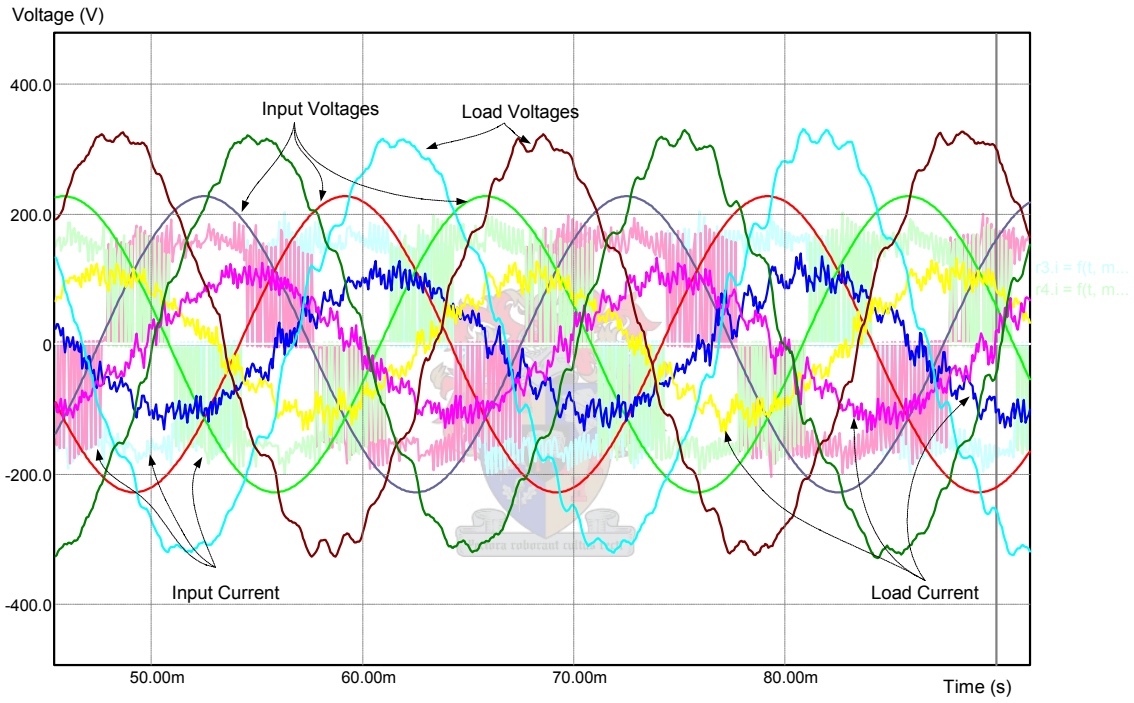


Figure 3-2 Output voltages of the matrix converter.

The Advantages of this topology are:

- It is very cost efficient – high kVA ratings may be achieved with very low component cost. There are no expensive energy storage devices involved;
- It is very versatile: can compensate for any phase shift in a voltage dip;
- It can be manufactured to be small and lightweight. There is no large and heavy energy storage device involved.

The disadvantages of this topology are:

- It requires very large filter components for large current ratings. The voltage drop over a sufficient large filter inductor at 500A can be up to 100V;
- It does not draw sinusoidal current (see Figure 3-2) without large input filter inductors as a result of the boost converter inserted;
- It might cause the network to collapse; the deeper the dip the more current is drawn in order to maintain output voltage;
- The topology can be used only up to a voltage of 6.5kV. No switches with higher rating are available on the market yet;
- High switching frequency is required (5 KHz or more), thus increasing switching losses.
- There are difficulties with safe commutation of bi-directional switches in practical converters (a major disadvantage);
- No modular design is possible.

3.4.1.2 **Boost AC-AC converter**

The three-phase boost converter for unbalanced dip compensation was proposed in [2, 34]. Two bidirectional switches exchange the directional switches in a DC boost converter topology. Most standard AC choppers, such as the one presented here, require four-quadrant switches. The commutation of these four-quadrant switches is critical and their switching pattern is relatively complex. These bidirectional switches may be protected by inserting capacitors at the drain of the two transistor pairs [15].

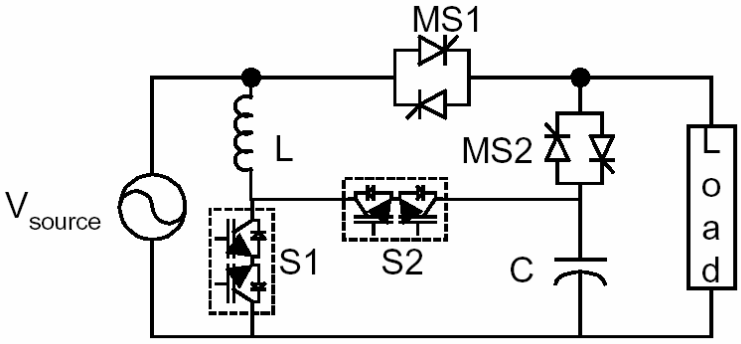


Figure 3-3 Single-phase sag compensator using a boost converter with optional static by-pass switches (MS1, MS2) [2]

With the protection given from the coupling capacitors inserted according to [15], the AC-to-AC converter can be used for high-power industrial applications. A three-phase dip compensator with the required power ratings would thus be realizable.

The advantages of the AC-to-AC converter:

- It is very cost effective; no storage components and very few components needed otherwise;
- It has been proven to work reliably in 250 kVA systems [15].

Disadvantages:

- No output voltage phase shift possible; this means no phase jumps can be compensated for;
- Power In = Power Out. When the line voltage drops, the line current needs to increase to make up for the loss. This might cause instability problems on some lines on deep dips;
- No modular design is possible.
- Switching components limit operating voltage to less than 6.5 KV.

The first disadvantage voids this application. The required dip compensator must compensate for phase jumps.

3.4.2 Other converters with energy storage

Topologies that are neither AC-AC nor multilevel inverters can also be used in dip compensation. Two such inverter topologies are considered.

3.4.2.1 Serial dual boost injector

The boost DC-AC converter was introduced by Caceres and Barbi in 1995 [43] and was improved in 2001 to make it more robust to load variations [44]. Two boost converters are connected to share the same source and ground. The energy source is a 67F, 42V ultracapacitor.

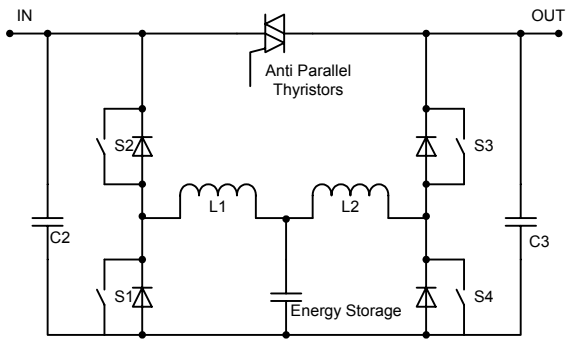


Figure 3-4 Dual boost converter topology [43]

The two positive outputs of the inverter are connected in series with the feeder line (Figure 3-4). The control signals for the two boost converters are given by the following equation (3-1) & (3-2).

$$D_{(left)} = 1 - \frac{1}{1 + F(1 + \sin(\omega t + \phi))} \qquad D_{(right)} = 1 - \frac{1}{1 + F(1 - \sin(\omega t + \phi))} \tag{3-1}$$

$$F = \left| \frac{|V_{nom}| - V_{in}}{2 * V_{ES}} \right| \qquad \phi = a\tan\left(\frac{|V_{in}| \sin\theta}{V_{nom} - |V_{in}| \cos\theta} \right) \tag{3-2}$$

Here D is the duty cycle for the respective inverter arms and F is the desired boost factor that determines the output amplitude (F=1 would give an inverter output sine with amplitude of the twice the energy storage voltage; F = 0 would give a zero output voltage). θ is the input voltages phase and ϕ is the converter voltage phase. V_{in} is the input voltage and V_{nom} is the nominal line voltage.

For a 30% dip with a maximum phase displacement of 30 degrees the maximum compensation voltage must be 250V. This is derived from Figure 2-4, where the compensation voltage must be $0.53*V_{p.u.}$. Another V_{ES} (the voltage on the energy storage) needs to be added to the compensation voltage because of the cancelling minimum output voltages of this topology. Each boost converter has a minimum of 40V output. That is the energy storage or ultracapacitor voltage. However, operating together they have no theoretical minimum voltage output. This means that each boost converter has to boost with a multiplication value of 6.2 (or F = 3.1) to achieve the required 250V output. This is problematic, because usually practical boost converters of this type operate best below a boost factor of 2. Further problems are the losses caused by the high currents on the input of

the boost converters. The internal resistances of the components used cause a further voltage loss, thus the boost factor has to be increased proportionally.

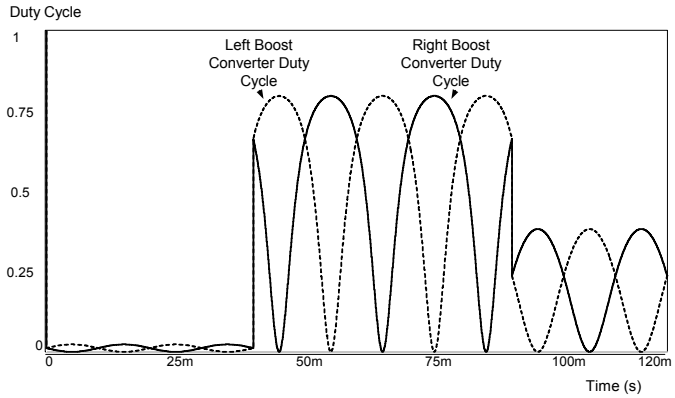


Figure 3-5 Duty cycles for the two inverter halves for the simulated dip at 40 ms

The values of the inductor and capacitor have been calculated for best performance and least current and voltage ripple. The current and voltage ripple reduction come at a cost of response time of this inverter topology. The best response time was achieved with a 5uH inductor with a 1mF capacitor. The inductor ripple current is very high in this case; however response time is absolutely vital.

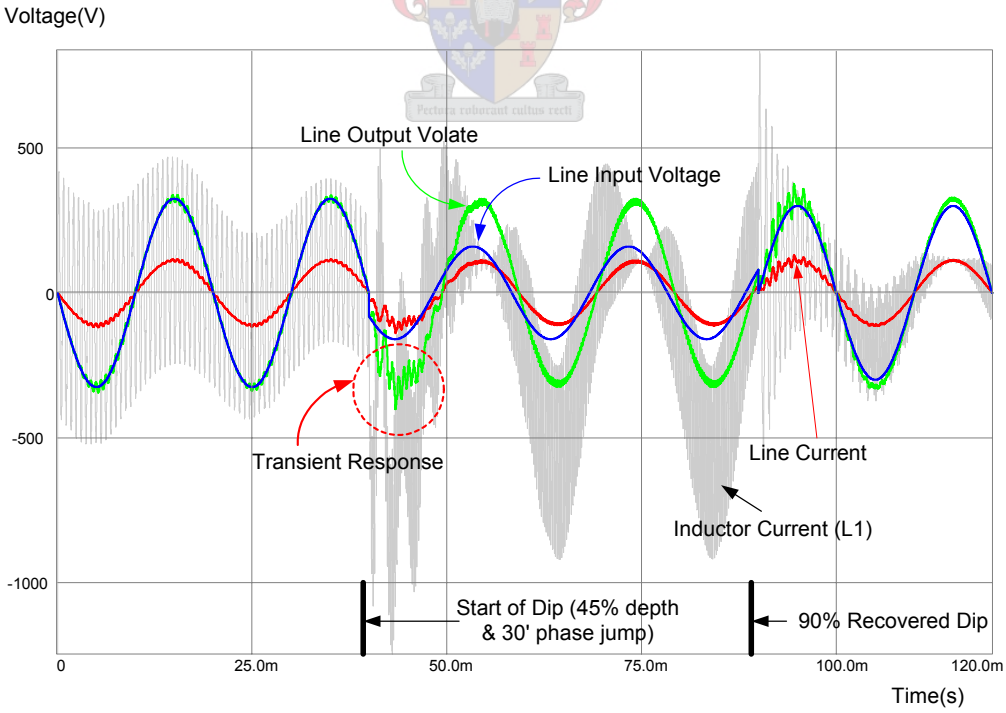


Figure 3-6 Simulation results with a dual boost topology with a single 40V DC storage.

Figure 3-6 shows the simulation results for the dual boost converter with a 75A (RMS) load current. A 45% dip with 30° phase shift is initiated at 40 ms. The dip partly recovers at 90 ms. As can be seen from the simulations, the inductor current and thus also the switch current are very high.

This large current ripple is due to the small size of the inductor used for boosting. This is to keep the losses, cost and response of such a converter optimal. The losses experienced on an inductor increase with the size (inductance) of the inductor.

Advantages of the dual boost method:

- Low component quantity. This reduces the complexity and also space requirement;
- Transformerless. Components only need to handle the serial compensation voltage;
- One energy storage device required per phase (the cost of the low capacitances in each module is much less than that of large ultracapacitors);
- Probably cheaper than multilevel inverters, as powerful IGBT modules are readily available on the market and would be easily integrated in this topology.

Disadvantages:

- Switching modules have to be rated at the peak inductor current and peak compensator output voltage. This is a very high kVA rating per switch. Thus switching losses are great;
- Large losses can be expected in the inductor;
- Transient response is weak compared to multilevel inverter;
- Transient settling time varies from load to load.

The dip compensator needs to operate reliably and rapidly during transient response. The dual boost converter has a sluggish response. This drawback will make the use of the dual boost converter difficult in a dip compensator.

3.4.2.2 **Back-to-back converters**

The back-to-back converter consists of two identical 3-phase AC–DC converters connected together on the DC side. Generally the DC bus voltage is connected to some high-voltage energy storage from which energy can be drawn during a dip. This is the setup of a typical online UPS.

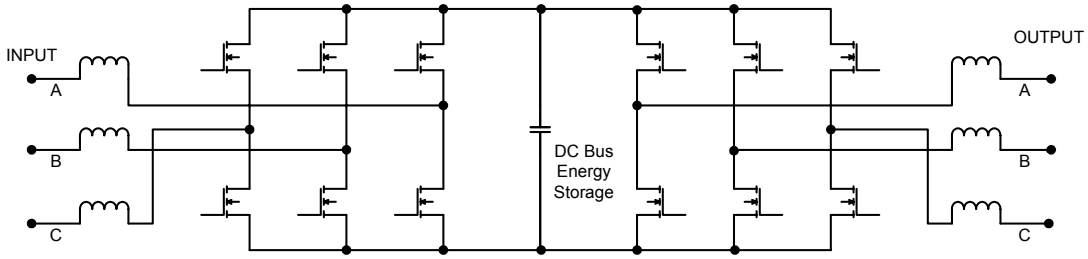


Figure 3-7 Back to back converter

Advantages anticipated with this topology are:

- Dip compensation of up to 100% possible;
- Power-quality improvement easy as output signal is generated from scratch;
- Instant response to dips as output voltage is independent of input.

Disadvantages:

- Low efficiency of converter (generally these converters have about 85% efficiency);
- Switches must handle full line rating;
- Energy storage will be very expensive on high-voltage DC bus.

This device is not suitable for dip compensation for the purposes of this thesis as it is already being widely used in industry. The back-to-back three-phase inverter is an old concept used to compensate for outages and flicker.

3.4.3 **Multilevel inverters**

A multilevel inverter is defined by the number of voltage levels it can produce in half a cycle. Figure 3-8 shows a staircase sine waveform output of a multilevel inverter with 6 voltage levels in half a cycle and 11 voltage levels in total. This inverter is therefore defined as a 6-level inverter. The number of voltage levels depends on the following [14]: 1) the injected voltage and current harmonic distortion requirements; 2) the magnitude of the injected voltage required; and 3) the available power switch voltage ratings. The unfiltered output voltage waveform can obtain a relatively low harmonic content, depending on the number of voltage levels.

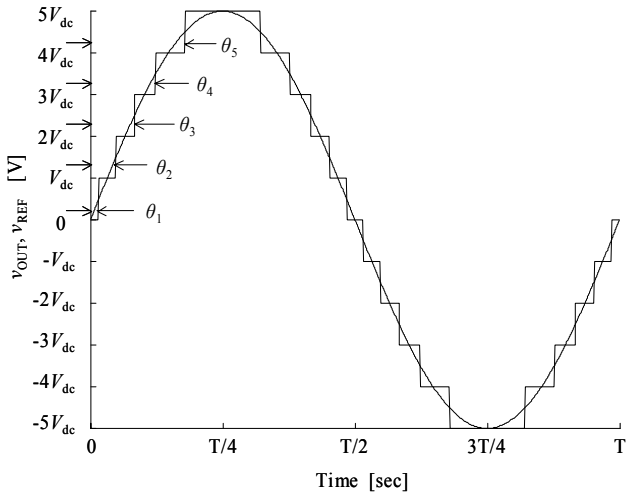


Figure 3-8 Staircase output waveform of a multilevel inverter [14]

3.4.3.1 **Cascaded multilevel inverter (CMLI)**

Cascaded multilevel inverters (Figure 1-2) are a relatively new group of inverters that has attracted many researchers' attention. The applications and control techniques of this category have been well researched [4, 14, 17]. These inverters can reach a high, unfiltered output voltage at multiple voltage levels with reduced harmonics from their own structures without transformers. This property makes it possible to connect these inverters directly in series (Figure 1-1) or shunt with a power line, because the line provides the inductance needed to interface these inverters with the power system [14]. Another virtue of these inverters is their fast dynamic response due to the elimination of large output filter components, which cause delays [17, 43, 44] (See Figure 4-7 for THD emitted from the multilevel inverters).

Figure 1-2 shows the basic structure of cascaded inverters with separated energy storage components, shown in a single-phase configuration. One of the advantages that will make the multilevel inverter more suitable is that it can be used at very high voltages by just adding more converters in cascade. The output of a typical multilevel inverter is shown in an idealized form in Figure 3-8.

Advantages of this topology:

- Modular – there is no limit as to how many modules may be added in series; thus the voltage is limited by the isolation of the gate drivers;

- Overall power rating requirement is less than in matrix converter, because it is a series compensator and only switches a small amount of the total power;
- The control of the switches is low frequency and very simple.

Disadvantages:

- Voltage rating is limited by the number of inverters switched in series;
- Large number of independent isolated DC sources needed for each phase;
- High internal resistance due to long current paths along the series inverters

3.4.3.2 **Marxian multilevel inverter (MMLI)**

A huge drawback of the cascaded multilevel inverter described in paragraph 3.4.3.1 is that a large number of isolated DC supplies are needed for the inverter topology. This makes the design impractical to use with ultracapacitors, as their price is too high. The inverter topology presented here introduces a method to overcome this without the use of a transformer. A solution where only one DC supply can be used is shown by Figure 3-9 [22] per phase. Eliminating the transformer from three-phase systems will still require three different energy sources due to isolation constraints.

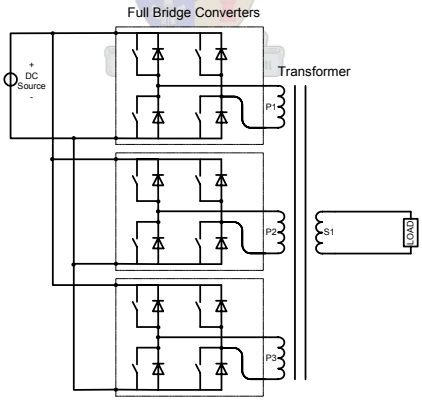


Figure 3-9 Voltage step addition by transformers [22].

A modified topology is transformerless. The combination of several topologies yields another inverter topology that may be used in the dip compensator. These topologies are discussed in [19, 20]. Figure 3-10 shows a generalized multilevel inverter topology. The generalized multilevel inverter topology can balance each voltage level by itself, regardless of inverter control and load characteristics [19].

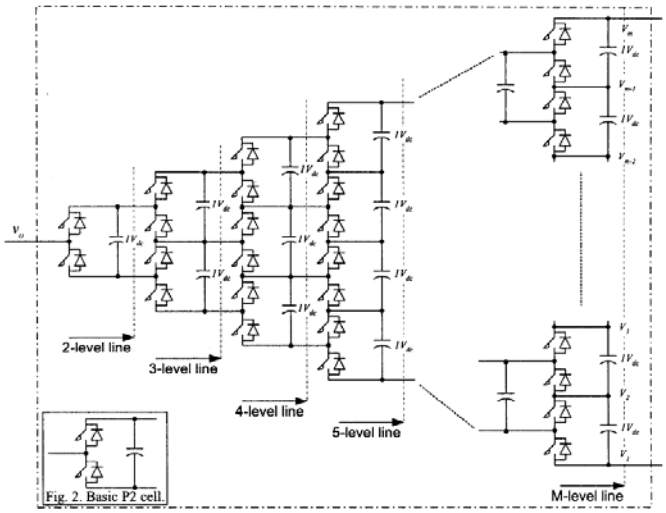


Figure 3-10 Generalized multilevel inverter topology (M - level, one phase leg) [19]

The modified P2 cell topology was introduced by Zheng Peng in 2001 [19]. With this topology a large DC bus voltage can be transformed to AC. The new inverter topology closely relates to this topology, but is also very similar to the Marx generator originally developed by E. Marx in 1924.

The Marx generator is used in high-voltage applications to generate a very high voltage pulse. A single capacitor may be used for voltages up to 200kV [16]. Beyond this voltage, a single capacitor and its charging unit may be too costly. The cost and size of an impulse generator increases at a rate of square or cube of the voltage rating. Hence, for producing very high voltages, a bank of capacitors are charged in parallel and then discharged in series. The capacitors (shown in Figure 3-11) are charged in parallel up to a certain voltage until the spark gaps flash over. Then the capacitors appear in serial because of the smaller resistance of a voltage arc.

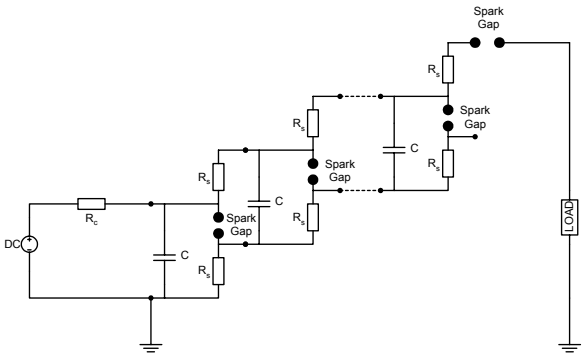


Figure 3-11 Marx generator originally developed by E. Marx in 1924

Because it is so similar to this inverter, the new inverter topology will be called the Marxian multilevel inverter (MMLI) topology. In this adaptation of the Marx generator the recharge resistors and spark gaps in Figure 3-11 are replaced by MOSFETs. The result is that the output voltage can be regulated to take the shape of a sinusoid at a certain frequency, phase and amplitude.

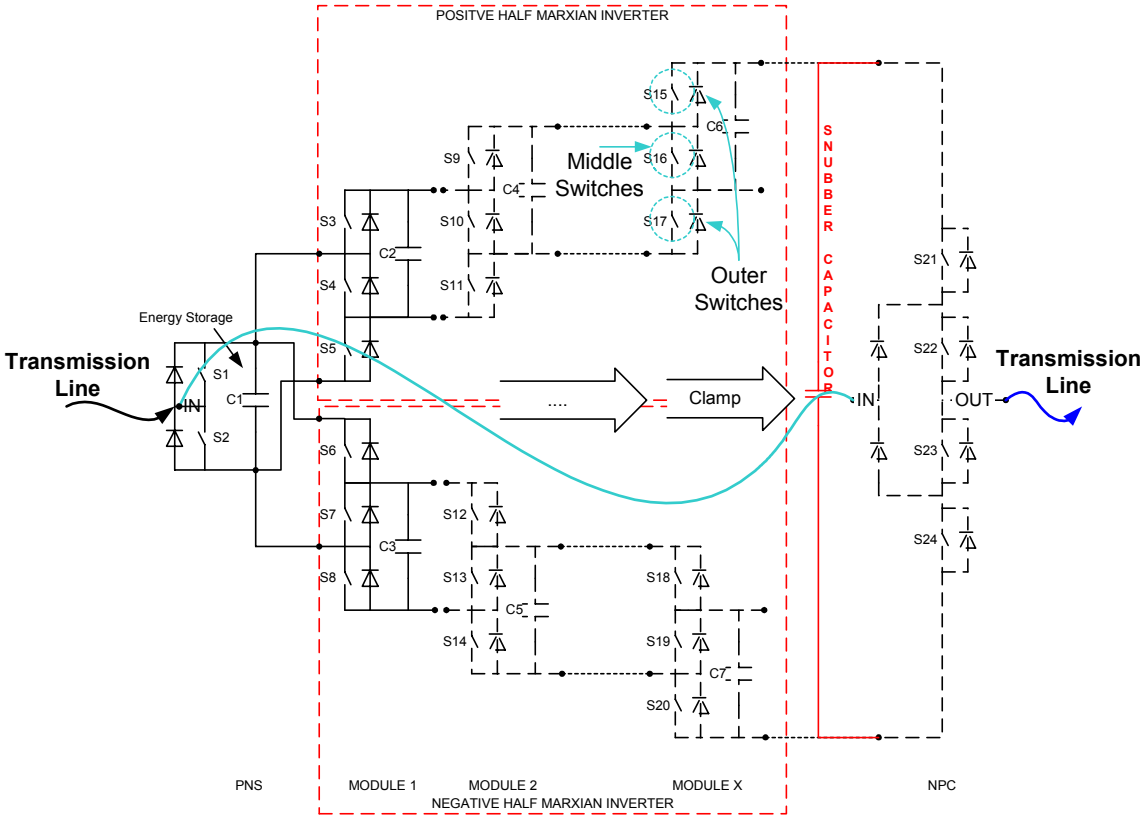


Figure 3-12 Marxian inverter topology

On the left the DC energy storage may be a low-voltage storage device such as a battery or ultracapacitor. In a three-phase converter three insolated energy sources would be needed. Two opposing Marxian inverters are placed in the centre. The upper half delivers the positive half of a sine cycle, while the other half is busy balancing the capacitor voltages with those of the energy source.

The Marxian multilevel inverter topology stacks capacitors in series by switching the middle switch (Figure 3-12) of the three switches on. This way a desired voltage may be added to the current line voltage. The middle and outer switches always operate in alternating mode to allow bidirectional current flow for reactive load currents flowing back into the system.

The reasons for clamping the Marxian MLI's output with a neutral point clamp (NPC) are:

- To switch between the positive and negative half cycles of a sine wave;
- Line currents should not be carried through balancing switches unnecessarily, so during zero output voltage the MMLI is bypassed by the NPC. This will reduce losses during zero injected voltage conditions.

This topology has many of the advantages of the cascaded multilevel inverter. The switching sequence can be chosen to approximately level all capacitor voltages uniformly (Figure 4-16). This way high peak currents due to balancing capacitors may be prevented when the capacitors are connected in parallel. Other capacitors in Figure 3-12 are normal capacitors which have relatively low capacitance, but have the advantage of having even less internal resistance than ultracapacitors. Any capacitor will only hold the energy to supply the system for half a cycle. After that it has to recharge again immediately. Figure 3-13 shows the simulation results. A 47% with 30° dip is initiated at 40 ms.

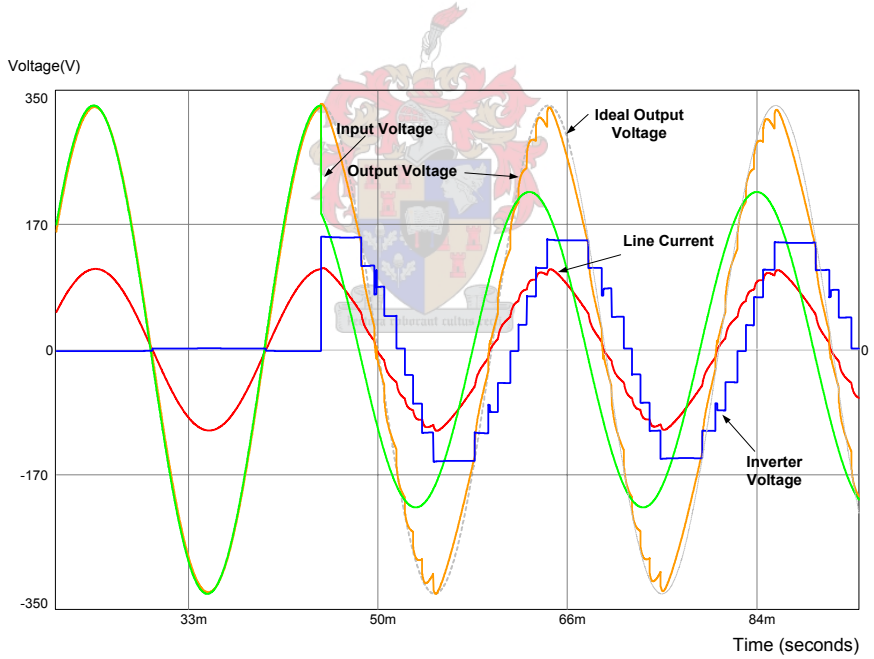


Figure 3-13 Simulated voltage dip response of Marxian multilevel inverter.

Advantages of this topology:

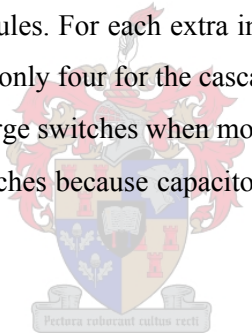
- The output voltage is similar to the conventional cascaded multilevel inverter;
- It is also modular (a large number of inverters may be stacked in series to give higher output voltages). The number of stages is limited to the maximum balancing current the MOSFETS

can handle. However, unlimited voltage output can be reached by coupling many circuits (Figure 3-12) in series, each having isolated energy storage;

- When the dip compensation period needs to be increased, more energy storage can simply be coupled parallel to the existing storage device (this is another advantage over the CMLI);
- One energy storage device required per phase (the cost of the low capacitances in each module is much less than that of large ultracapacitors);
- The losses due to internal resistance are much less than with the cascaded multilevel inverter: the capacitors have an internal resistance of only 3mΩ compared to 20mΩ of the ultracapacitors or batteries. Only half the number of switches conduct line current (compared with the cascaded multilevel inverter) at any time;
- It is cheaper than the cascaded multilevel inverter because fewer isolated energy storage devices are required;
- No filter components required for inverter voltage stages of less than 80V.

Disadvantage of this topology:

- Requires more switching modules. For each extra inverter stage six new MOSFET switches have to be added compared to only four for the cascaded multilevel inverter;
- Higher currents through recharge switches when more modules are added;
- More complex control of switches because capacitor voltages have to be uniform at the end of each cycle.



3.4.4 A comparison of inverter topologies

To determine which topology should be taken for the dip compensator, a comparison table is drawn up. The ratings listed are valid for a 50 kVA three-phase converter. Table 3-2 presents the comparison of switches and other components with their minimum ratings required. A 20% increase was added to the current components for ripple current provision. The transient response is also very important for fast and effective dip compensation and is thus listed.

The best topologies for high-voltage applications with the lowest total VA ratings (for the switching components) listed are: the boost AC-AC, CMLI and MMLI inverter. Others listed are restricted in total voltage rating as they are shunt devices. Of the possible series devices the dual boost converter has a sluggish transient response. The CMLI has very fast transient response and the lowest VA switch ratings; however, it requires a lot of isolated DC power sources. The MMLI has an equally

fast response to the CMLI, but it only requires one energy source per phase. As energy source costs in terms of ultracapacitors are still very high, the MMLI is chosen as the best inverter topology.

Topology for three phase 50kVA Converter	Number of Switches	Minimum Total Switch VA Rating	Number of Inductors	Number of Capacitors	Transient Response	Number of isolated energy storage devices
Indirect Matrix	12+2+6	565V*[(212.2A+20%)*12 + (106.1A + 20%)*6] + 565V*212.2A*20%*2 = 2.444 MVA	6 * 400uH * 75A + 3 * 40uH * 150A	3 * 1mF (for boost converter) + Filter Caps	Very Fast	0
Boost AC-AC	6	325V*(212.2A+20%)*6 = 497 kVA	3 * 40uH * 150A	Filter Caps	Limited by LC components	0
Dual Boost	12	250V * (1000A+20%)*4 = 1.2 MVA	6 * 5 uH * 750A	6* 1mF	Limited by LC components	1 * 42V * 67F
Back to Back Converter	12	800V*(106.A+20%)*6 = 1.222 MVA	6 * 400uH * 75A	Filter Caps	Very Fast	Bus Storage Capacitance 1 * 1F * 600V
CMLI	60	40V*(106.1A+20%)*60 = 305 kVA	0	0	Very Fast	5 * 42V * 67F
MMLI	90	40V*(106.1A+20%)*30 + 40V*(220A+20%)*48 + 250V*(106.1A+20%)*12= 1. 04 MVA	0	24*250mF*40V	Very Fast	1 * 42V * 67F

Table 3-2 Component ratings for the compared topologies

3.5 Energy storage

3.5.1 The energy storage solution

Energy storage technologies may be employed in a wide range of useful electric power system applications, including storage of intermittent energy from solar and wind resources, load levelling on the electric power system, and various power-quality and backup power-related uses such as UPS systems and power stabilization. For large-scale storage at the bulk power system level, only pumped hydroelectric storage has been widely used. For smaller storage applications at the distribution or customer-utilization levels of the system, batteries have been used. This is not

because batteries are ideal performers of these functions or inexpensive, but because the other energy storage options were either not technically available or were too expensive to be justified. Thus, batteries were the only real, albeit imperfect, option available. Batteries have some serious drawbacks, including their limited cycle life, the hazardous materials that are in many designs, high maintenance, sensitivity to temperature, and other issues. Given the disadvantages of batteries, the industry has been searching for a superior energy-storage technology that can outperform batteries from both a cost and electrical performance perspective and be widely used at the distribution and customer utilization levels of the power system.

3.5.2 **Ultra/super capacitors**

Double-layer electrochemical capacitors (EC), also known as ultra-capacitors or super-capacitors, are an emerging storage technology already being used for applications such as DC motor drives, UPS systems and electric vehicles. The latest EC store enough energy to rival a lead-acid battery and can outperform batteries in several key performance parameters such as power density, cycle life and temperature sensitivity. Many EC designs are also more efficient and can be manufactured with metals such as nickel and carbon that are environmentally benign relative to the metals in lead-acid or nickel-cadmium batteries. As the EC technology improves further, an impressive world of applications should emerge. These applications include intermittent renewable energy storage, bulk power system peak shaving, load levelling, and various other distributed resource possibilities [45].

At the University of Stellenbosch research and tests are conducted on EC technology for short-term energy storage for dip compensation on high-voltage power lines. The technology used is manufactured by EPCOS, a subdivision of Siemens. Figure 3-14 shows a 67F, 42V ultracapacitor ("ultracapacitor" is an informal description of EC or electro-chemical capacitors).

Figure 3-14 Ultracapacitor tested at the University of Stellenbosch (dimensions (mm) 240x225x195)

3.5.2.1 What is an ultracapacitor?

Ultracapacitors are compared to electrolytic capacitors below.

A standard capacitor consists of two conductive plates separated by a dielectric (Figure 3-15). Electrical charge is stored on the plates and energy is stored in the electric field within the dielectric that separates the plates. The capacitance of a standard capacitor is determined by the area of the plates multiplied by the dielectric constant of the insulating medium between the plates and divided by the distance between the plates. With a standard capacitor, the key to increasing capacitance is to increase the area of the plates, reduce the distance between the plates and/or increase the dielectric constant (use a different dielectric material) [45, 46].

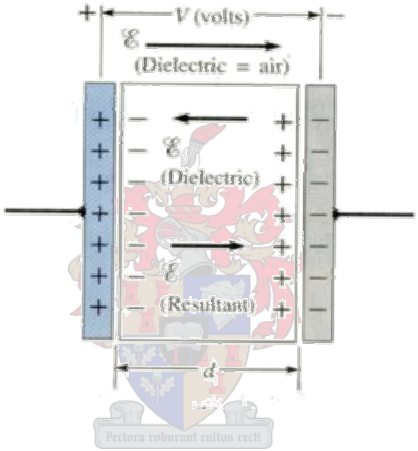


Figure 3-15 Electric field components between the plates of a capacitor with a dielectric present [45]

An ultracapacitor is an electrochemical device consisting of two porous electrodes immersed in an electrolyte solution that stores charge electrostatically. In many ways an ultracapacitor is subject to the same physics as a standard capacitor. That is, the capacitance is determined by the effective area of the plates and the dielectric constant of the separating medium. However, the key difference of the ultracapacitor is that with its liquid electrolytic structure and porous electrodes, this gives it a very high effective surface area compared to a conventional plate structure. It also ensures a minimal distance between the "plates." These two factors lead to a very high capacitance compared to a conventional electrolytic capacitor [45, 46]. Ultracapacitors can have 100 to 1000 times the capacitance per unit volume compared to a conventional electrolytic capacitor [45, 46]. The electrolytic solution of the ultracapacitor is typically potassium hydroxide or sulfuric acid. This structure effectively creates two capacitors (one at each carbon electrode) connected in series. No lead, cadmium or other dangerous metals are used in this design, which makes it relatively benign

from an environmental perspective. The simplified electrical equivalent model of the ultracapacitor consists of a small series and parallel resistance. This is a DC model that does not consider dynamic response [46].

Ultracapacitors, like batteries, have cells that can be connected in series and parallel combinations to achieve the appropriate voltage level and capacitance desired. Typical cell voltages range from about 0.8 volts per cell up to over 2 volts per cell, depending on the materials used in the cell. Ultracapacitors share some of the chemistry of batteries, but the approach is to operate them at a cell voltage range that leads to only electrostatic storage of charge. If the charge becomes excessive, chemical reactions begin to occur and the cell behaves more like a battery. Ultracapacitors are operated over a working voltage range and removing half the voltage removes about 75% of the energy from the capacitor. This is because the energy stored in a capacitor in joules is equal to 50% of the product of the voltage squared multiplied by the capacitance (that is 1/2CV2) [46].

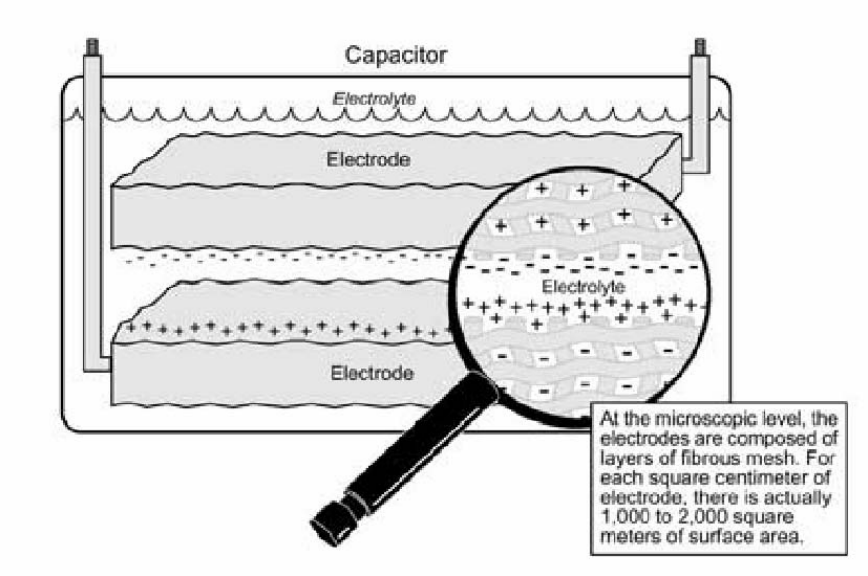


Figure 3-16 Construction of the electrochemical capacitor (ultracapacitor) – a single cell is shown [45].

The electrolytic solution in the capacitor serves two functions. First, it is the conductive path linking the two capacitors together. Second, it also serves as an "effective conductive plate" for one side of each capacitor that is formed at the liquid electrolyte/electrode interface. This is because an electrical charge layer forms between the carbon electrode surface and the electrolytic solution. The ultracapacitor structure really is equivalent to two capacitors in series connected by the resistance of the electrolyte. This resistance is much lower than the effective internal resistance of a typical battery, so ultracapacitors can achieve much higher power density than batteries (by a factor of 10 or more). But their energy density at low discharge rates is still less than batteries [46, 47].

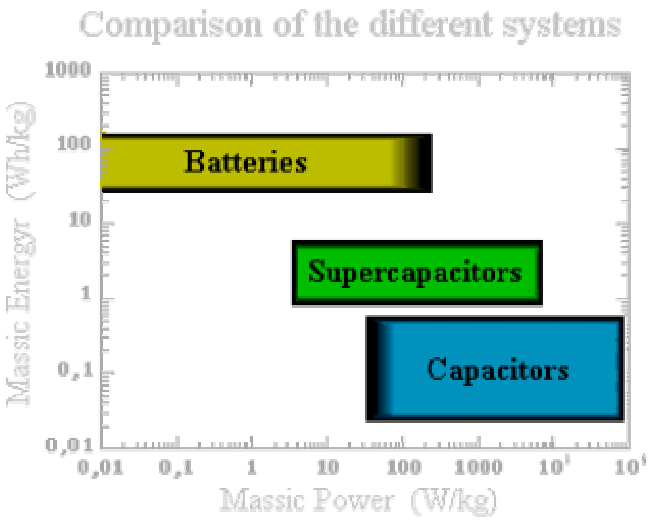


Figure 3-17 Market segments of ultracapacitors, batteries and capacitors [47].

The capacitor design discussed so far is known as a symmetrical ultracapacitor, where both electrodes are the same type of material (activated carbon). However, there are also asymmetrical capacitors [46] (the newest type), which show more promise for high-energy applications and have minimal electrical leakage. They use a carbon electrode on one side and a NiOOH (nickel-hydroxide) electrode on the other side. This approach creates an asymmetrical distribution of voltage between the two capacitors within the cell, since the capacitance is not the same on each side; however, this approach can increase the energy density by about a factor of 5 compared to a symmetric ultracapacitor design. Asymmetric designs also have very low leakage and, depending on the voltage level of charging, can be left charged for months, self-discharging only a few percent over this period [46, 47].

The use of non-aqueous electrolytes, some of which attain a specific electrode capacitance of 1/3 the value found in aqueous systems, allows a unit-cell to be charged to 4V instead of 1.2V [48]. The specific electrode capacitance of the ultracapacitor increases with the ceramic loading. This is a result of three-dimensional micro-porosity in the coating, which is accessible throughout its thickness, providing increased surface area for charge storage [46]. The availability of this surface area can be verified by BET surface area measurements. This increase in capacitance with ceramic loading, or thickness, is unlike the behaviour of the capacitance due to the dielectric films in electrolytic capacitors [45]. In such devices the capacitance is inversely proportional to the film thickness [45]. Since thinner films, however, result in lower breakdown voltages, there is a trade-off between high voltages and high capacitances. This trade-off does not exist in the ultra-capacitor

technology; charging voltage is only restricted by the type of electrolyte and is unaffected by ceramic loading [45].

Ultracapacitors are compared to lead-acid batteries below.

Currently, the lead-acid battery is the leading energy storage technology for UPS systems, DC telecommunications equipment and renewable energy storage applications. So how does the lead-acid battery compare with the current state of the art for ultracapacitors? Table 3-3 lists some of the key characteristics of batteries and ultracapacitors, showing that in many areas the ultracapacitor outperforms the battery. It is only in initial cost (discussed later) and energy density that lead-acid batteries are currently superior.

Whether or not use of an ultracapacitor makes practical sense over the use of a battery depends on the application. Broadly speaking, applications can be divided into long-duration energy storage and short-duration energy storage applications. Power quality-related applications that need seconds or minutes of energy are examples of short-duration applications. A long-duration application would be charging a capacitor at night (off peak) and then dispatching it in the daytime for 3-4 hours during peak utility system loading. Another long-duration application is storing enough energy from a PV system to power loads at night.

Other interesting comparisons are also possible.

An important transitional element between electrochemical capacitors and batteries arises with processes involving Li+ intercalation into layer-lattice host cathode materials, e.g., MoS_2, TiS_2, V_6O_{13}, and CoO_2. Normally these materials, coupled with an Li anode or a Li-C anode, would be regarded as battery cathode materials. However, the forms of the charge and discharge curves and associated pseudocapacitance, and even the cyclic voltammetry profiles, are similar to those for two-dimensional electrosorption. Hence this class of materials exhibits properties intermediate between those of bulk-phase battery reagents and quasi-two-dimensional pseudocapacitor electrodes [46].

However, the Li+ battery is still classified as a battery [46] and not a capacitor, because it is Faradaic – this means a chemical reaction takes place while charging and discharging the capacitor. The opposite would be non-Faradaic. In this case no reactions take place. Only charge is stored.

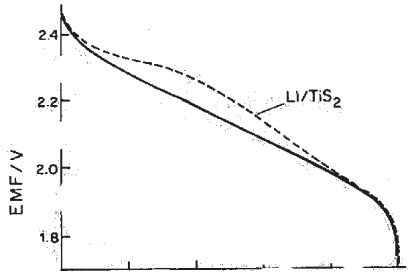


Figure 3-18 Discharge curve for Li+ intercalation into TiS_2 showing voltage versus time [46]

3.5.2.2 **Use of ultracapacitors for long-duration distributed resource (DR) applications**

The ultracapacitor is currently not as well suited for long-duration applications as it is for short-duration applications [47]. This is due to its lower energy density (compared with batteries [48-53]) and higher capital cost. The energy density of the ultracapacitor is only about 15-20% that of the battery [48, 51-53] for long-duration applications. Despite the poorer energy density, the ultracapacitor does have a number of characteristics that can make it ideal for energy storage for long-duration applications once its cost becomes a bit less. For example, off-grid wind and PV systems can cycle on a daily basis every day of the year – leading to 365 discharges per year. Since ultracapacitors have a very high cycle life compared to batteries, they should last much longer than batteries in this role. In most renewable energy storage applications such as a remote home-powered by PV or remote supply for instruments, the batteries are replaced every 3-7 years depending on the system design, whereas ultracapacitors, because of their very long cycle life, should be able to last for 20 years or longer – as long as the PV panels. Cycle life tests have determined that some products can greatly exceed 100,000 cycles [48, 51-53] without significant degradation.

The performance advantages of ultracapacitors include the following:

Charging efficiency: a lead-acid battery system can lose a significant amount of energy (20-30%) during the charge/discharge cycle [48, 54] (including inverter losses), the ultracapacitor system (including inverter losses) may lose only 10% of the energy[48].

Temperature performance: ultracapacitors can operate over a broad temperature range (-50 to +50^{o}C) [48, 53] without much change in performance and, therefore, don't need to be oversized to handle low temperatures – such as at very cold remote power sites at polar regions or on mountaintops.

Despite the performance advantages above, the high capital cost of ultracapacitors compared to batteries prevents them from being used in many long-duration applications. The capital cost of ultracapacitors is currently in the range of R50.00 – R500.00 per kJ depending on the capacitor type and application. The capital cost for batteries is one tenth of that of ultracapacitors, in the range of about R0.30 – R2.00 per kJ. Of course, initial capital cost is not the whole story. Since capacitors are more efficient, have a much longer cycle life and lower maintenance, ultracapacitors will compete with batteries in long-duration type applications. As further improvements in the cost and energy density of this technology are made (and are expected to occur within the next 5-10 years) they may eventually displace batteries for these applications.

3.5.2.3 **Ultracapacitors for short-duration storage applications**

Short-duration applications of energy storage are characterized by the need for high power but for short periods of time. These include power-quality ride-through applications, power stabilization, and adjustable speed-drive support, temporary support of DR during load steps, voltage flicker mitigation and many other applications. Most of these involve energy storage capacity ranging from a few seconds up to 20 minutes [48, 53].

The ultracapacitor is ideally suited to these applications (especially in situations lasting less than a few minutes) because it has a much higher power density than batteries and can be very quickly recharged. By contrast at very fast discharge rates, significant internal power dissipation within the battery occurs – wasting much of the energy and lowering the effective energy density. Also, chemical reaction rates in the battery limit the speed of discharge. Ultracapacitors do not have these limitations. This means that, at a rapid discharge rate, the ultracapacitor can actually deliver more joules of energy per rand of capital cost than a battery. This is why for short-duration UPS systems of a few minutes or less, the ultracapacitor is the better option. Ultracapacitors used in most short-duration applications should cost less than batteries in the long term. This is an emerging technology and industry will take some time to recognize the ultracapacitor's advantages.

3.5.3 **Vanadium redox flow battery (VRB)**

VRBs are widely used for peak-power shaving in large office environments [49, 50]. Their operation is reliable and very long term. The VRB promises environmentally friendly operation and a very long lifetime. The configuration of a redox flow battery is comparatively more complicated that that

of lead-acid batteries. Pumps and piping need to be installed. They are widely available structures because they are also used in chemical plants.

3.5.3.1 Life time of vanadium redox flow batteries

When compared with the typical lead-acid battery the VRB allows two or three times the depth of discharge capability without damaging the battery structure [49]. There are none of the factors which reduce battery service life seen in other batteries that use a solid active substance, such as loss or electrodesposition of the active substance. Furthermore, operation at normal temperatures ensures less deterioration of the battery materials due to temperature [50].

A lifespan of up to 40 years or 10000 cycles is promised by some redox flow battery manufacturers [49]. This could be longer than the lifespan of the ultracapacitor. However, regular maintenance on the pumps and polymer membranes is needed. This factor is a disadvantage and places the VRB in direct competition with a motor generator set in terms of its performance with motor generator sets. Motor generator sets can actively compensate for many dips very reliably. They run at high efficiency and their initial costs are low [6]. They require regular maintenance.

3.5.3.2 Vanadium redox flow batteries for short and long-duration storage applications

Regarding power density (Watts/kg), the lead-acid battery still outperforms the redox flow battery by two to three times. This, however, is only true for very short times as the depth of discharge of the lead-acid battery is crucial for its lifespan. The VRB has higher internal resistance than the lead-acid battery, so that in terms of active dip compensation for high-power applications this battery is not suitable.

The energy density of redox flow batteries (~33 W-h/litre) is higher than the lead-acid battery. While this is not apparent from the manufacturer's specification, research [50] has shown that the practical measured energy density can be twice that of a lead-acid battery over the specified lifespan. This property makes the VRB very attractive for long-term energy storage applications.

3.5.4 Lead-acid batteries

There are two types of lead-acid battery; flooded lead-acids and sealed cell. Lead-acid batteries contain lead electrodes which is a pollutant [50]. Hydrogen is produced during discharge of the cell and the designer must make provision for this. Controlled disposal of the lead electrodes is a legal requirement.

3.5.4.1 Lifetime of a lead-acid battery

The sales literature provided for lead-acid batteries is well developed. Battery life, depth of discharge, discharge rate, state of charge and recharging rate need all be considered when estimating battery lifetime. Lead-acid batteries are quoted as having lives of 5 or 10 years. This is a conditional statement [49, 54]. What this means is that if the battery is kept within a specified temperature range and is kept at a specific float voltage within very limited usage periods, the battery may last for the specified period. In dip compensation the use is very random and battery usage may at any time fall outside specified operating conditions. This will drastically reduce the lifetime. So for active dip compensation a lifetime not exceeding three years is taken as a rule of thumb.

3.5.4.2 Lead-acid batteries for short- and long-duration storage applications

There is a wide range of lead-acid batteries available on the market today. The user may typically choose the lead-acid battery for its application. One can chose from a deep-cycle, long-life or high-current battery. The main use of lead-acid batteries is for long-duration, low-discharge application. This is the converse of the qualities in a dip compensator, where high power is required for very short times.

In practice the lead-acid battery usable energy density for storage applications is about 12 W-h/litre [48, 54] – based on several factors such as gassing, heat and the primary issue of deep discharges. With regard to power density basis, the lead-acid battery is generally better to alternative batteries such as VRB batteries.

In the specific case study using the Willard Solar 105Ah battery (South Africa) it was found that it has 3 times less power density than the EPCOS ultracapacitor module range. The energy density

was found to be almost 10 times higher in Willard Solar 105Ah batteries than in EPCOS ultracapacitors [4, 50].

3.5.5 Energy storage comparison

Table 3-3 shows the ultracapacitor compared to the vanadium redox flow and lead-acid battery.

Characteristic	Asymmetrical Ultracapacitor	Vanadium Redox Flow Batteries	Deep-Cycle Lead-Acid Battery
Deep Discharge Cycle Life	10,000 - 100,000+	13, 000 +	1000-2000
Charge/discharge cycle efficiency	90% +	85% +	70-90%
Charging time	Seconds to minutes	Many hours	Many hours
Temperature Range	-50 to +50 C little impact on life or performance	0 – 40 ° Celsius	Must be kept near room temperature to optimize life and performance
Typical Maximum Energy Density (kJ/kg)(W-h/litre) – long-time use (3 - 5 years)	5.9 – 10 (kJ/kg) 1.71 (W-h/litre)	120 (kJ/kg) 33 (W-h/litre)	50 (kJ/kg) 12(W-h/litre)
Typical Maximum Power Density (kW/kg)	2-5 (kW/kg)	~ 0.16 (kW/kg)	0.3-0.5 (kW/kg)

Table 3-3 Comparison of lead-acid battery, VRB and ultracapacitor [47, 50].

3.6 Summary

The Marxian multilevel inverter (MMLI) topology as a dip compensator was found to be the most appropriate transformerless series compensation. It only requires one energy source per phase and has relatively low component power ratings. This is low-cost and low-maintenance operation. The remainder of this thesis will be a study on the MMLI topology for dip compensation.

4 Analysis and Design

4.1 Introduction

This thesis shows the practical implementation of a new topology, the MMLI as a dip compensator. The concept is practical and lends itself to usage over a range of applications. However a major factor in developing a working prototype was the selection of components of the device. It became apparent that the internal resistance of the components plays a major role. This factor is often overlooked, but in this calculation it was pivotal. The data obtained during developing the device are presented.

This chapter gives a detailed analysis of the topology chosen for the final dip compensator. Chapter 4.2 will elaborate on the specifications and functions of the final product. Chapter 4.3 will explain the new Marxian multilevel inverter (MMLI) topology and Chapter 4.4 will explain all considerations involved in the hardware design. Chapter 4.5 will cover the software and firmware design.

4.2 Specifications and functions

The device's primary goal is dip compensation. However, a series dip compensation device has the infrastructure of many other power-quality-enhancing devices such as active serial VAR compensators [14] and harmonic compensators [10]. In both cases no real energy is required. All the functions are described in more detail in the control section (paragraph 4.5.2).

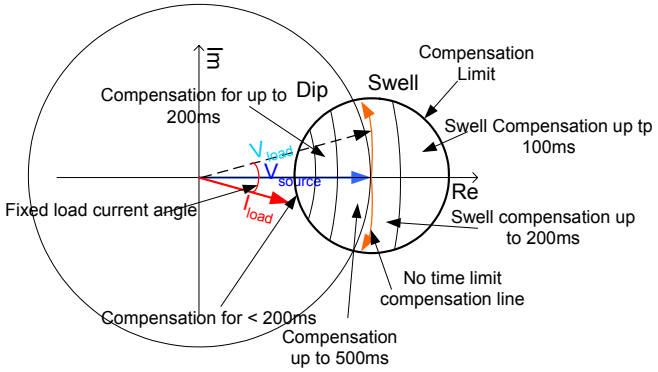


Figure 4-1 Vector diagram showing operation potential for one phase

4.2.1 Dip\sag and swell compensation

The device is designed to compensate for 30% dips with 30° phase shift or 50% dips with no phase shift. The swell can be 30% more than rated voltage. The compensation minimum time is 200ms for 50% dips on resistive loads.

4.2.2 VAR compensation

The device can compensate for up to 16° current phase shift due to unwanted line inductance. The load would then appear resistive instead of inductive.

4.2.3 Harmonic filter

By controlling the switching angles and output frequency of the inverter, certain odd harmonics can be eliminated [14]. The staircase sine waveform can then be used for various types of power line compensation. Transformerless series compensation with these multilevel inverters also requires three single-phase units, each with its own energy storage.

4.2.4 Total specifications

The full specifications of the prototype design are:

- 50 kVA three phase (230V, 75A, 50 or 60Hz ± 15%);
- Series compensation device with a 140V (RMS) peak output voltage;
- Dip compensation:
    - Up to 50% dips – no phase compensation for 200 ms
    - Up to 30% dips – up to 30º phase jumps during dip for 300 ms
    - Up to 20% dips – up to 45º phase jumps during dip for 500 ms

      (Compensation times more with smaller loads);
- Swell compensation:
    - Up to 20% swell for 200 ms or less – 45º phase jumps;
    - Up to 30% swell for 100 ms or less – 30º phase jumps;
    - Swells up to 50% for two cycles or less – no phase jumps;

      (Compensation times more with smaller loads);

- Harmonic compensation:
  - 3rd, 5th or 7th harmonic up to 50% of fundamental can be compensated;
- VAR compensation:
  - Phase shifts of up to 16º due to line inductance can be compensated.

4.3 Marxian multilevel inverter topology

This section will detail the operation of the MMLI. This should provide a clearer understanding of the topology that is being introduced. The MMLI is designed to generate an AC voltage many times the amplitude of the DC source voltage. This can be achieved by alternatively discharging capacitors (that have been previously charged to the DC source threshold) by inserting them in series with the line.

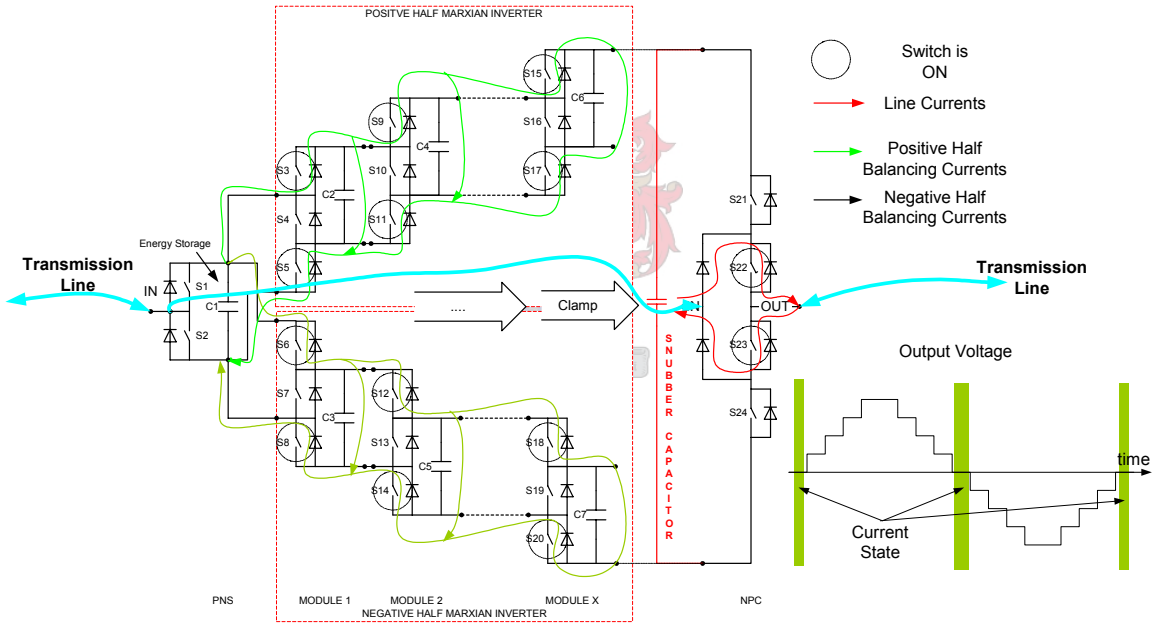


Figure 4-2 Zero output voltage state – The inverter is in balancing mode

In Figure 4-2 the inverter is in bypass mode. There is no output voltage (as can be seen on the lower right in Figure 4-2). Here the shaded area indicates the momentary output voltage and position in the wave cycle. The line current is bypassed through the NPC. In this mode the capacitors are all connected in parallel. This means that the voltage across every capacitor is equal to the voltage on the energy source seen on the left. To switch all capacitors in parallel the top and bottom switches of each module (encircled in Figure 4-2) are closed. The current from the energy source is split to flow through S3, S9, S15, S17, S11 and S5 to charge capacitors in the positive half inverter. S6, S12, S18,

S20, S14 and S8 are closed to allow the balancing of the negative half inverter. The forced balancing of capacitors (by switching them in parallel) is permitted under conditions explained in paragraph 4.4.3.1.

In the event of a dip, for example, the inverter changes from bypass mode to dip compensation mode. Here the NPC's top and bottom two switches are used to select between positive or negative injection voltages. Figure 4-3 shows that the top two switches in the NPC are closed to allow currents to flow in and out of the positive half inverter. On the input side the bottom switch of the PNS is closed to effectively add the energy source's voltage to the output voltage. In this mode the modular capacitors are not discharged as they remain coupled parallel to the energy source.

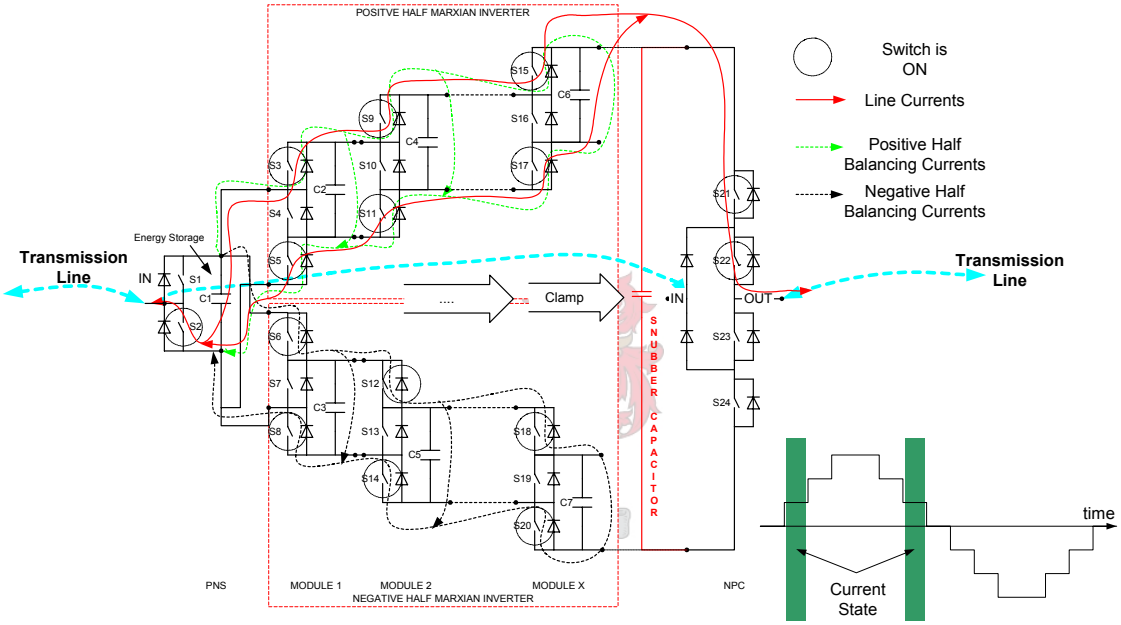


Figure 4-3 First positive output voltage level – The source voltage is added

In Figure 4-4 the output voltage is increased to double the energy storage voltage. Here one of the previously charged modular capacitors is coupled in series with the energy source and the rest of the inverter. While the rest of the inverter remains in balancing mode, this module is discharged or charged depending on the line current direction. The module's voltage is added to the output voltage by closing its middle switch while the outer balancing switches are opened. In Figure 4-4 S16 is closed to insert the voltage of the last module (Module X).

It does not matter which module is switched on first (Module 1, Module 2 or Module X) (Figure 4-4) - simulation results show that there is no difference in terms of voltage balancing. When the last Module X is switched as the first module the discharge rate on its capacitor is quicker than if

Module 1 is switched on. When Module 1 is switched on initially, the capacitors of Module 2 to Module X will appear in parallel with it thus reducing the discharge rate. The resulting recharge times for the two approaches differ little.

As a result of these small balancing time differences different sequences have been simulated and the best was taken as the switching sequence to be used with this specific Marxian inverter. The optimal sequence (Figure 4-44) differs when different total numbers of stacked modules are used. Thus no generalizations or guidelines are given here.

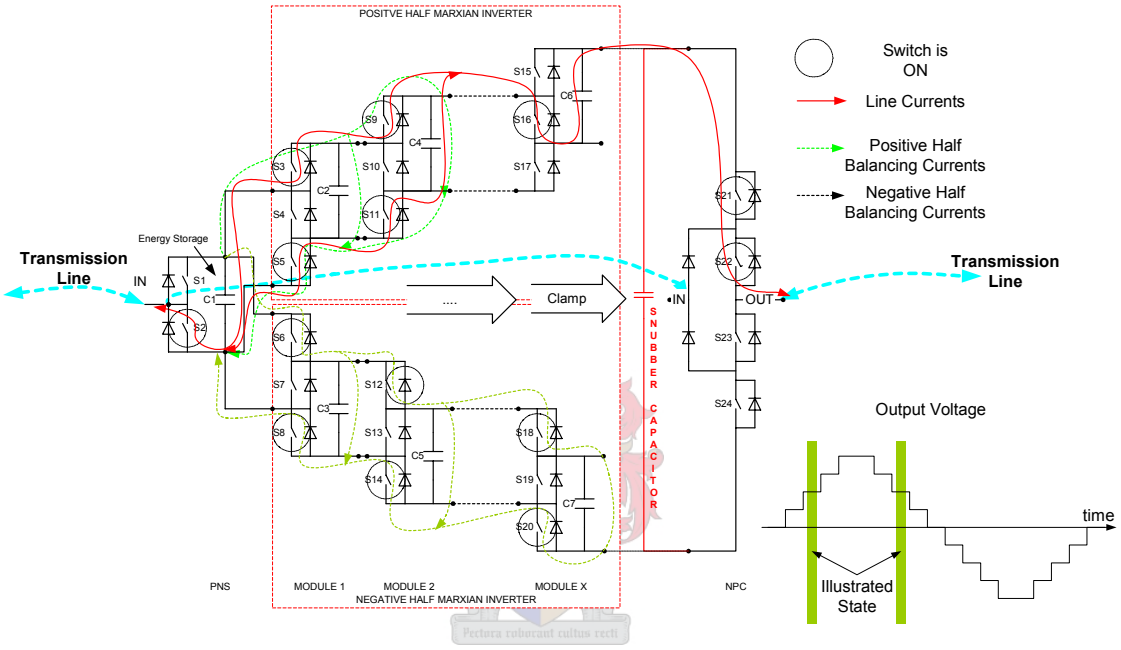


Figure 4-4 Second positive voltage level – the source plus last capacitor voltage are added

From Figure 4-4 it can also be seen that the balancing switches (S3, S9, S15, S17, S11 and S5) have to carry the line current as well as the balancing current. This can result in high peak currents experienced on the switches. Due to the control method used (Figure 4-16) to balance the capacitors, these high peak currents only exist for only a very short time. These peak currents may be prevented by using another control method or by assuring that no balancing of capacitors takes place during an inverter halves active or conducting period. To make sure that no balancing takes place in conduction mode the lower switches in the positive inverter are kept open while conducting line currents. The opposite strategy is used for the negative half. Line currents are only conducted through the balancing switches during the times a half Marxian converter is active – that means that the NPC is switched to select that specific converter section. MOSFET switches are used throughout the Marxian inverter sections, due to these high peak currents on the switches. These MOSFET

switches can handle very high peak currents for a short time. (The MOSFET's voltage rating in this design is 75V and the current rating is 140 A (RMS))

A higher output voltage level is achieved by simply closing another module's middle switch while its outer switches are open. When maximum rated output voltage is required all modular voltages are added by switching all capacitors in series (as seen in Figure 4-5 indicated by the red line).

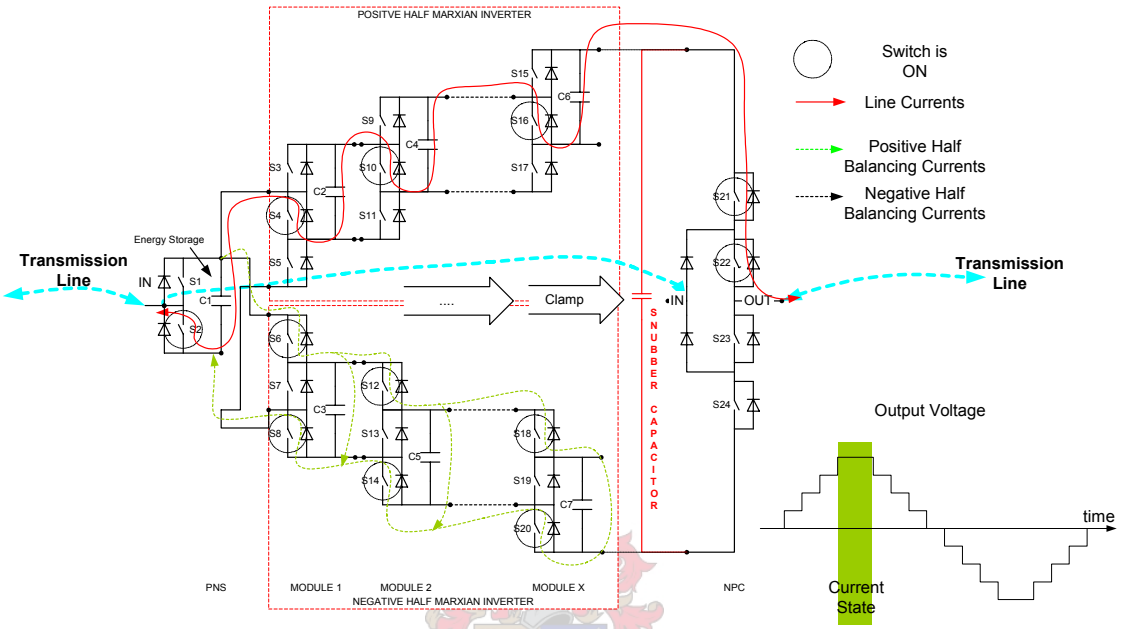


Figure 4-5 All capacitors appear in series – maximum output voltage

The opposite of what was explained in the above figures occurs when a negative output signal is required. A negative output voltage is generated using the lower half Marxian inverter. During the negative half cycle of a sine wave no line currents flow through the positive half inverter. Then the positive half is in balancing mode.

Once the voltage dip recovers the inverter is switched back to bypass mode (Figure 4-2). However, when the energy source needs be recharged the inverter is switched on again. Here several ways of recharging the energy source exist. These are elaborated in paragraph 4.5.6. One way of recharging the energy source is by generating a small sine wave with only one step's amplitude in a ~ 90° phase shift from the line's current signal. By slightly increasing or decreasing this angle, power can be absorbed or released from the energy source.

This concludes the explanation of the MMLI topology. More detail on the balancing currents and voltages are included in the voltage balancing paragraph (4.4.3.1).

4.4 Hardware design

4.4.1 Overview

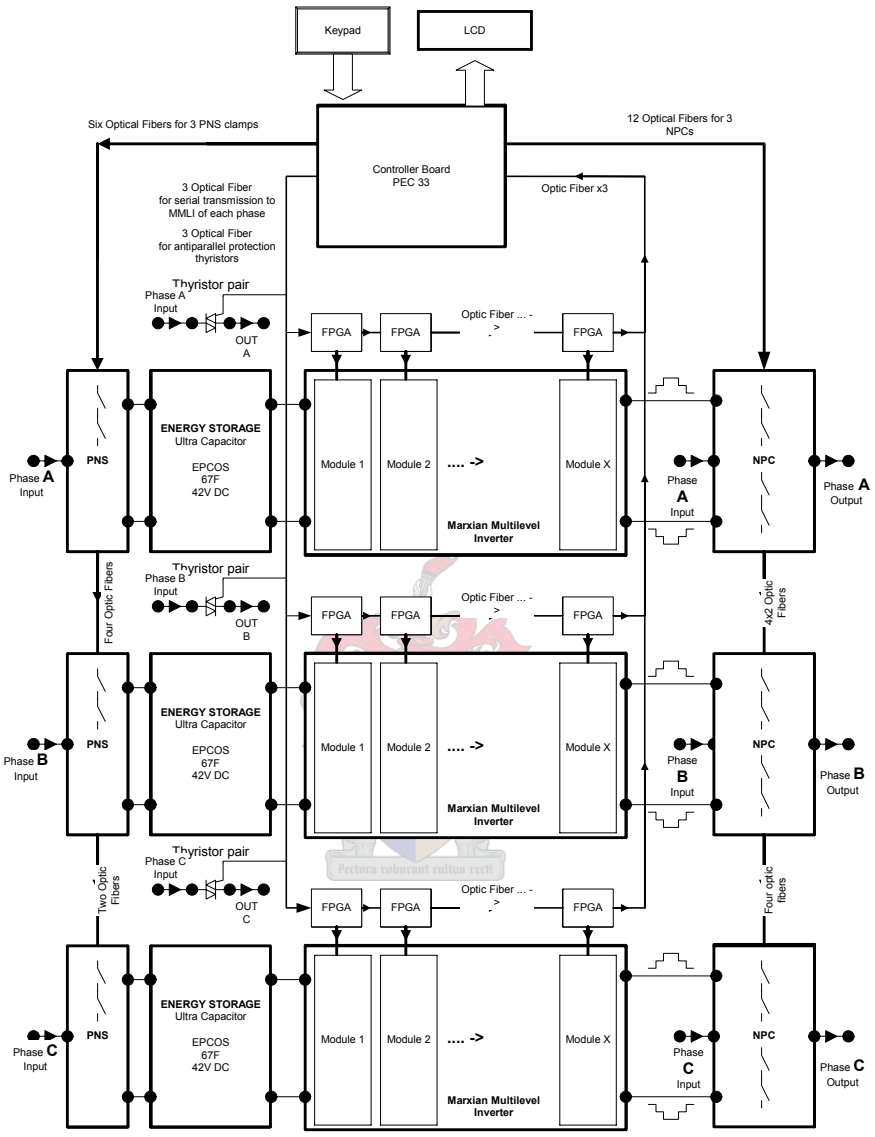


Figure 4-6 Block diagram showing hardware setup of complete three-phase Marxian inverter

Figure 4-6 shows a block diagram of the 3 phase compensator. The key design of the setup lies in the blocks labelled Marxian multiplier modules. The rating is user specific and may be altered according to need (see paragraph 4.4.3). Each of these consists of a custom number of identical modules. This is what makes the design modular. The customer may demand individual maximum compensation of a whole three-phase inverter or just selected phases.

On the right a block labelled NPC contains the neutral point clamp. This block feeds the outputs of the Marxian Multilevel Inverter back into the power line. When the inverter is off or has no momentary voltage output, the NPC will redirect the input to the output directly. The NPC is used as line currents should not be lead through MMLI unnecessarily.

On the left is a block labeled PNS. This is the positive-negative voltage injection selector. In the event of a zero voltage being injected into the system both top and bottom switches are open. In the event of a negative voltage being injected into the line the top switch will close. The process is done vice versa for positive injected voltages.

As the switch count inside the Marxian MLI is high, a new method for controlling these is introduced. All gate signals must be isolated from each other because gate signal voltages may differ as much as 60% of the rated line voltage in a five-level MLI. The solution is thus to daisy chain all the modules within one phase. That means that only one optical fibre signal for each phase is required to control the Marxian MLI. The other optical fibre connections shown in the diagram feed the IGBT modules which are needed for the NPC and the PNS.

The control is done digitally by a newly developed controller board (PEC33) [55]. This controller board was developed by the University of Stellenbosch specifically for use in power electronics applications. Analogue control of such a system would be inadequate because of the systems added complexity through daisy chaining switches and sharing of capacitor voltages on the modules.

This section deals with the design of hardware. This includes: energy storage, Marxian MLI, the use of a neutral point clamp and the design of the switch chain.

4.4.2 Energy storage

Ultracapacitors were chosen for this project because of their many advantages over other means of electro chemical energy storage. The most important advantages of ultracapacitors are their very high power density and extremely long lifespan. The dip compensator is maintenance free.

4.4.2.1 Allowable capacitor voltages

On deciding on which type of ultracapacitor to use in this project it is important to know how much distortion is emitted onto the power line by the multilevel inverter. According to the NRS 048 a

maximum of 8% total harmonic distortion (THD) may be induced by any power conditioner [35]. Figure 4-7 shows a graph of the THD plotted for different capacitor voltages. Each stage of the multilevel inverter will thus add a voltage equivalent to the capacitor voltage to the line voltage. The graph shows results for dip depths up to 60%. It also indicates the different stages that are used to compensate for the dip.

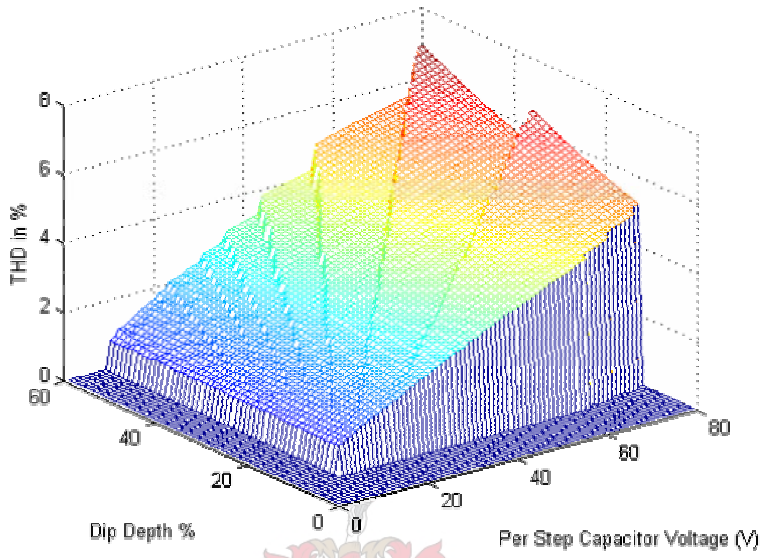


Figure 4-7 THD plotted for different capacitor voltages and dip depths

This figure indicates that a capacitor voltage and thus also inverter voltage as high an 80V will not emit excess distortion on a 230V AC line. The highest voltage-rated ultracapacitor modules (30 – 56V) were thus considered to reduce the number of stages required to compensate for a voltage dip. The THD was calculated with a method suggested by [3].

4.4.2.2 Choosing an ultracapacitor

The main reason ultracapacitor are introduced into power electronics is that their price per Farad at very high capacitance values is approximately ten times cheaper than ordinary electrolytic capacitors. (Communica South Africa sells 220mF, 25V capacitors at R 220.-; this is R4000/F at 42V compared to R400/F at 42V for an ultracapacitor.)

Some technical information on ultracapacitors has been obtained directly from companies currently active in the field. Companies contacted are, amongst others: Maxwell, Evans and NessCap. However these companies produce only small current ultracapacitors that are of little use in power electronics. The only companies that currently manufacture suitable ultracapacitors are Epcos

(Siemens, Germany), Esma (Russia) and Tavrima (Canada). The requirements of a suitable electrochemical capacitor are:

- The maximum rated current must be in the order of 280A or more;
- The internal resistance is low (less than 30 mΩ for 40V or more rated caps);
- The rated voltage is high enough to be used directly without cascading many units;
- The capacitance is high enough to hold enough energy for sufficient dip compensation;

	EPCOS (Ultracapacitor)	ESMA (Ultracapacitor)	Electrolytic Capacitor	Battery (Lead Acid)
Available in South Africa	Yes	No	Yes	Yes
Suitable Products	67F, 42V -> R 26,750.- pp 150F, 42V -> R 39,000.- pp 100F, 56V -> R 56,625.-pp	107F, 45V -> $2,200.- 150F, 32V -> $1,300.- 330F, 45V -> $2,900.- 700F, 30V -> $1,300.- 300F, 32V -> $1,550.-	220mF, 25V -> R 220.- 1mF, 50V -> R 4.50	Willard Solar 105, 12V -> R 345.-
Internal Resistance	<20mΩ	8 < .. < 27mΩ	4 mΩ	50 mΩ
Lifecycles	500 000	300 000	> 1Million	< 1000
Technology	Carbon & Aluminum Electrodes, Non Aqueous	Carbon & Nickel Hydroxide Electrodes, Aqueous	Aluminium Thin Film	Lead Acid
Temperature Range	-30˚ to +70˚	-50˚ to +50˚	-50˚ to 70˚	Room Temp
Toxic – Ecologically Unfriendly	Yes (Organic Toxic Substrate used - toxic)	No (Aqueous Substrate used – non -toxic)	No	Yes (Lead Acid)
Sensitive to Moisture	Yes	No	No	-
Topology to be used in	Marxian	Marxian	Cascaded MLI	Cascaded MLI
Percentage of Total Price of 50 kVA system (No MOSFET Modules used)	80% Total Cost of Comp.: ~R 120 000.-	75% Total Cost of Comp.: ~R 100 000	96% Total Cost: ~R 500 000.-	10% Total Cost: ~R 50 000.-
Percentage of Total Price of 50 kVA system (MOSFET Modules used)	67% Total Cost of Comp.: ~R 190 000.-	65% Total Cost of Comp.: ~R 160 000.-	90% Total Cost: ~R 570 000.-	6.8% Total Cost: ~R 110 000.-

Table 4-1 Comparison of unique features of EPCOS and ESMA ultracapacitors.

Table 4-1 compares the cost of using ultracapacitors in the system to using batteries or standard capacitors. Both ultracapacitor brands offer a maintenance-free lifetime of more than 10 years. Although the ESMA ultracapacitor is generally cheaper, the decision was made to focus on EPCOS ultracapacitors because they are available in South Africa (all components used on this prototype are listed in Appendix C).

The amount of capacitance required in this converter topology is calculated by balancing the energy the inverter releases during a dip. As most dips last up to 200ms the capacitor voltage should only drop by about 10% during this time. In the event of the compensating voltage being a maximum, the output power of the compensator is 75A*140V RMS = 10.5KW (purely resistive loads).

$$P = \frac{1}{2}VC^2 - \frac{1}{2}(0.9V)C^2 \qquad (4\text{-}1)$$

Solving for capacitance gives C = 32.40F. This is the absolute minimum capacitance that would be sufficient for compensating for the worst dips.

4.4.3 Modular inverter design

There is a limit as to how many modules may be stacked in parallel (for reasons that will be explained in the next paragraph on voltage balancing). For the purpose of this study it was necessary to stack 4 modules plus the ultracapacitor module for specified voltage dip compensation. This will allow a total of 11 output voltage levels or 5 steps to be switched.

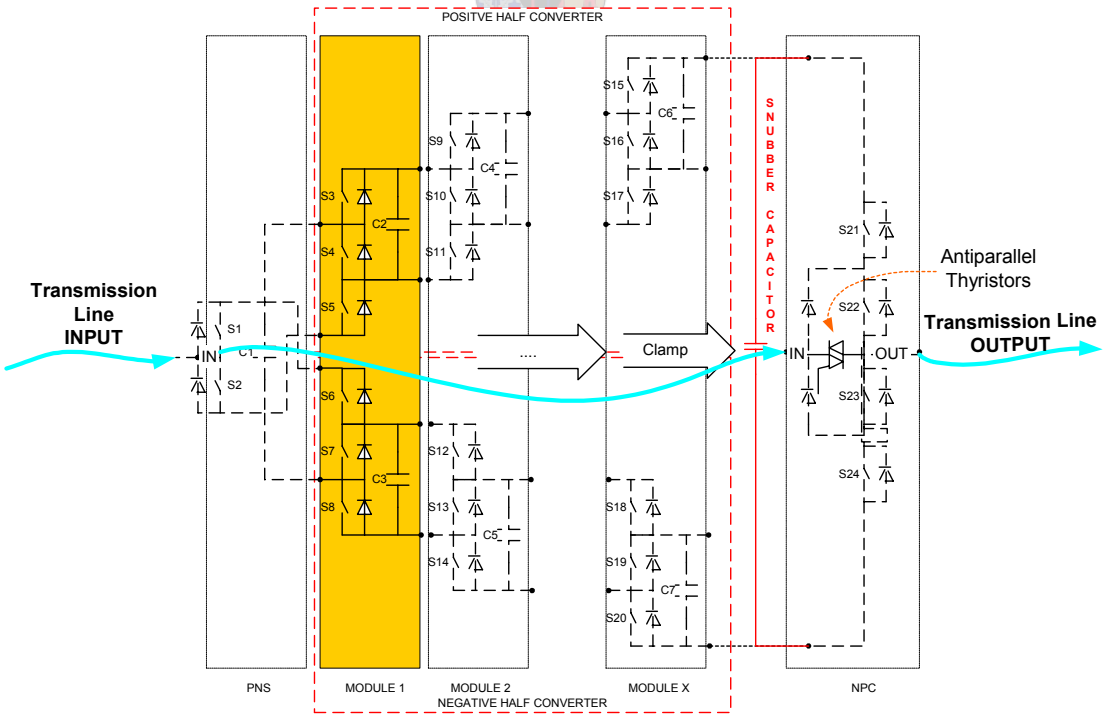


Figure 4-8 Modular design

Multilevel inverters output a stepped wave-signal where the voltage from one level to the next is generally kept small enough so that the harmonic distortion injected onto the line is below international restrictions. This way no output filter is required. Multilevel inverters have a pre-determined output voltage range which is not linear but also stepped.

It is crucial to keep the total harmonic distortion emitted by any power-quality enhancing-device low. This factor limits the maximum voltage allowed per step at a certain switching frequency. For this study switching at line frequency was considered to simplify the control. Switching at line frequency is desirable as losses are kept low and capacitor banks' size cannot be reduced by increasing switching frequency because low ESR is required. This shows that the maximum allowable step voltage is around 80V for less than 8% THD and 45V for a less than 5% THD on a 325V line. Figure 4-7 also shows that the THD will remain relatively constant for more than just one level. The figure shows the THD for up to 4 steps at 40V.

These modules have to satisfy the following criteria:

- High current rating. They must be able to conduct rated load current (75 A_{RMS}) for a long time, because the compensator operates in series with the power line
- Low voltage rating. This will be approximately 50 V, because of the low bus voltage (40 V)
- Low losses. They must have a low on-state resistance in order to minimize the voltage loss across them
- They must be cost effective
- For practical reasons they must be robust and compact. They must not generate excess heat and must be low cost

To satisfy all these criteria each module is designed for high current capabilities. The components are placed very close to each other, thus reducing stray inductances that can be caused by long conductors.

4.4.3.1 **Voltage balancing between two modules**

At each state change the Marxian multilevel converter connects two different groups of capacitors either in series or in parallel. As described in paragraph 4.3, all capacitor voltages are clamped (equalized) as the multilevel converter switches into capacitor balancing mode where capacitors are switched in parallel. Voltage balancing between capacitors occurs in the latter case. Figure 4-9 shows a circuit that is illustrating the transition. The two capacitors have a voltage difference ΔV,

power loss will occur at each transition when the switch closes. To investigate such power loss, a MOSFET-based circuit is used as an example (Figure 4-9). When turned on a MOSFET switch can be equivalently expressed as a resistance. The energy loss (E_{loss}) in the resistor can be expressed as the following at each transition:

$$E_{loss} = R\int_0^\infty {i_R}^2 dt = R\int_0^\infty {i_C}^2 dt \tag{4-2}$$

$$= R\int_0^\infty \left(\frac{\Delta V}{R} e^{-\frac{t}{R(C/2)}}\right)^2 dt = \frac{\Delta V^2}{R}\int_0^\infty e^{-4t/RC} dt \tag{4-3}$$

$$= \frac{\Delta V^2}{R*(-4/RC)}\left(e^{-\infty} - e^{-0}\right) \tag{4-4}$$

$$E_{loss} = \frac{1}{4} C \cdot (\Delta V)^2 \tag{4-5}$$

Here R is the series resistance shown in Figure 4-9. C is the capacitance of each module and t is the time which is integrated to infinity. In equation (4-3) the capacitance is divided in two because two capacitors appear in series on the balancing path. (Equation (4-5) is taken from [19].)

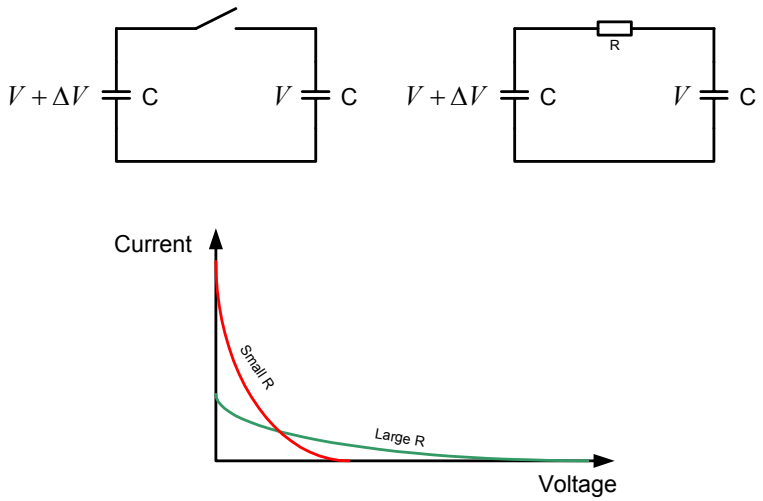


Figure 4-9 Balancing capacitor voltages by switching them in parallel

The energy loss is proportional to the voltage difference and capacitance but independent of resistance (this is also explained in Figure 4-9). The resistance only affects the charging/discharging current and duration, but has no effect on the loss. Thus in choosing the relevant resistance the designer would only consider the maximum currents weighed out over the maximum time given for balancing the voltages. This design consideration will be dealt with further later in this paragraph.

The voltage difference is caused by charging or discharging current during each switching state; this can be expressed as:

$$\Delta V = \frac{I_C \cdot t_C}{C} \quad \text{OR} \qquad \Delta V = \frac{I_D \cdot t_D}{C} \tag{4-6}$$

I_C and I_D are the respective average charging or discharging currents during one switching state and t_C and t_D are the relevant times that this state is active. From equations (4-5) and (4-6), the energy loss at each switching-over instant can be rewritten as (4-7) and the power loss (P_{loss}) is thus expressed as equation (4-8):

$$E_{loss} = \frac{I_C^{\,2} \cdot t_C^{\,2}}{4C} \tag{4-7}$$

$$P_{loss} = \frac{I_C^{\,2} \cdot t_C}{4C} \tag{4-8}$$

Therefore, the power loss is inversely proportional to the capacitance and switching frequency. This confronts the designer with another trade-off between the material cost involved in increasing the capacitance and the efficiency experienced. Another consideration, though, is that the stress on the switches also increases inversely with the capacitance. However, the dip compensator will only run for a very short time span and will be less efficient during the time of the dip. This proposes that the device does not need ultimately high efficiency because of its infrequent and short operation times. For this reason the capacitance may ultimately be lowered.

Calculations and graphs were used to investigate the exact trade-off between the internal resistance of components and the capacitance chosen for the prototype converter. The primary goal is to find out how much current will flow for a certain type of R and C chosen. R is the sum of all resistances along the voltage balancing path. This resistance contains the internal resistance of the switches and

capacitors. The capacitance is of concern in this consideration as the voltage difference ΔV changes inversely to the capacitance (Equation (4-6)). Thus the maximum balancing current (I_{max}) is inversely proportional to the capacitance (Equation (4-9)).

$$I_{\max} = \frac{\Delta V}{R} \quad => \quad I_{\max} = \frac{I_D * t_D}{RC} \tag{4-9}$$

A few generalizations have been made to simplify the analysis of the multilevel inverter:

- All calculations are based on worst-case scenarios. This means that the system will be functional in less extreme conditions.

- As the inverter is rated for 75A RMS current the peak current through all modules would be 106.1 A. This would be the worst-case scenario and all further calculations assume a discharge current on the capacitors of 106.1 A. This discharge current would occur during conditions not lasting longer than 10 ms (half a cycle at 50Hz line frequency). Usually a discharge state would be much less than 10 ms because of implementation of capacitor sharing control (Figure 4-16 and Figure 1-3). As the load current is AC most of the time and only contains extreme harmonics for some loads, the peak current of 106.1A would only persist for a fraction of the 'on' time of a module.

- The minimum recharge and voltage balancing time would be 10ms. This is the time of the half cycle in which the specific module would be in 'recharge' state. Usually the recharge and voltage balancing times exceed 10 ms because of capacitor sharing control (Figure 4-16 and Figure 1-3). Figure 4-10 shows the balancing current for different internal resistances and module capacitances. These balancing currents represent I_{max} from equation (4-9) for different R and C values.

Figure 4-10 suggests that a higher internal resistance in components is preferred as a solution to minimizing high recharging currents. This is not entirely true as the voltage balancing may generally not take longer than half a cycle which at a 50Hz line frequency would be 10ms. As the balancing of the capacitors occurs through a resistor, the perfect balance between the capacitors voltages would only be achieved at times equals to infinity. As the voltages are not perfectly balanced after only 10 ms, there would be an ever decreasing average voltage on the capacitors. This can clearly be seen on the simulations of the inverter. After two or three cycles the total output voltage of the inverter is

considerably lower than what it was originally. However, this decreasing tendency does not continue for long before it stabilizes to continue even dip compensation (Figure 4-11).

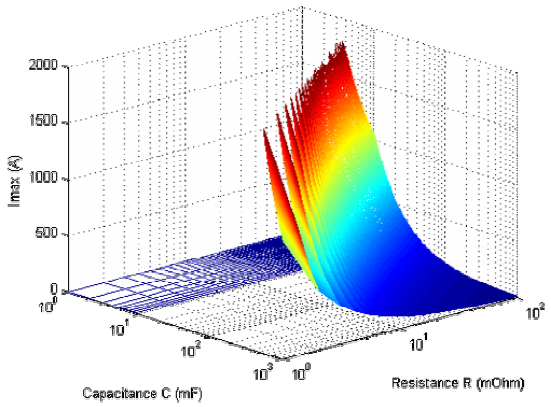


Figure 4-10 Stress (I_{max}) on switches on balancing capacitor voltages as a function of resistance and capacitance

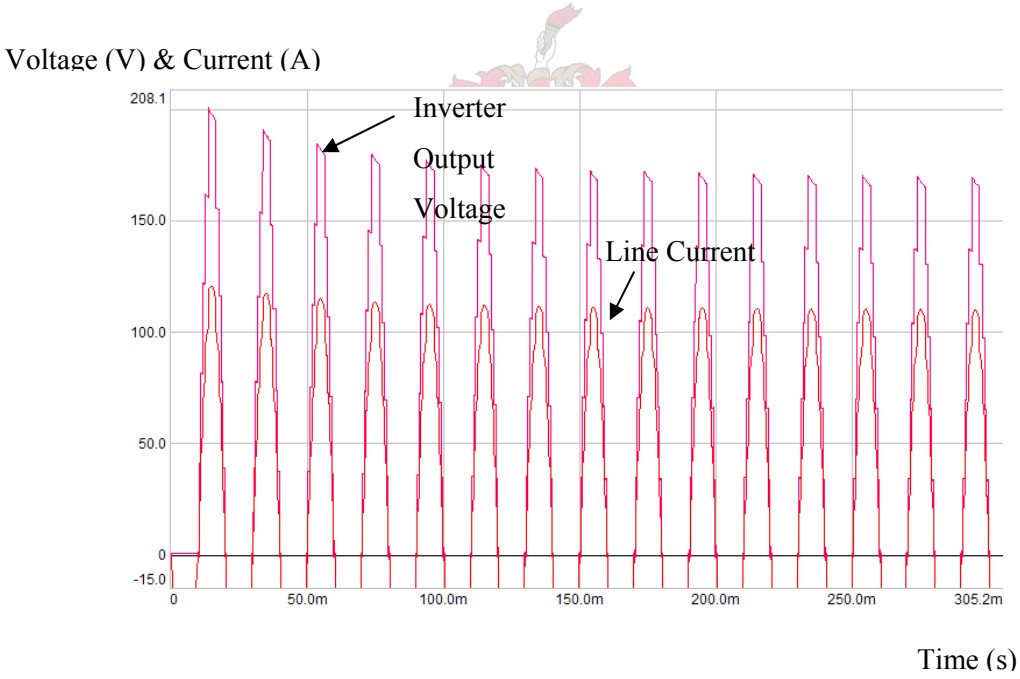


Figure 4-11 Simulation of MMLI at full load – drop in output voltage after few cycles

The new balance is established as the recharge time given is sufficient to recharge the capacitor to a certain percentage of its final voltage once again. This additional loss in voltage over the capacitor that can no longer be recharged due to insufficient balancing duration was calculated with the following iterative equation (4-10). Here $\Delta V_C(1)$ is the voltage drop attained after the first cycle. $\Delta V_C(i)$ is the voltage drop after 'i' cycles. Every cycle the voltage drop increases slightly as the capacitor has insufficient time to balance to its final (infinite time balancing) voltage.

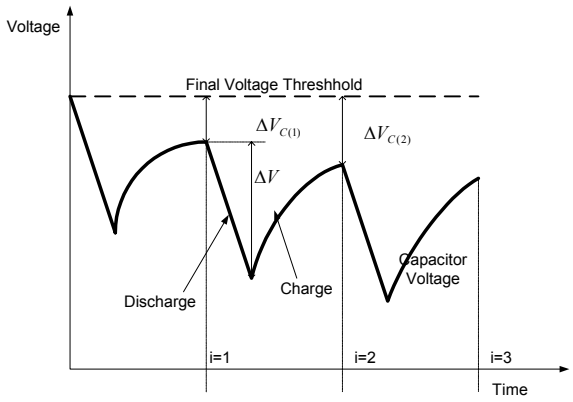


Figure 4-12 Explanation to voltage drop experienced due to insufficient balancing times

$$\Delta V_{C(i)} = (\Delta V_{C(i-1)} + \Delta V)e^{(-t/RC)} \qquad \Delta V_{C(0)} = 0 \tag{4-10}$$

Here ΔV is the voltage drop attained during discharge according to equation (4-6). (A constant discharge current of 106.1A for 10 ms results in ΔV.) After ten cycles the new voltage difference is taken to show the new voltage drop across each module that can no longer be balanced out. Figure 4-13 shows this information graphically as a function of R and C.

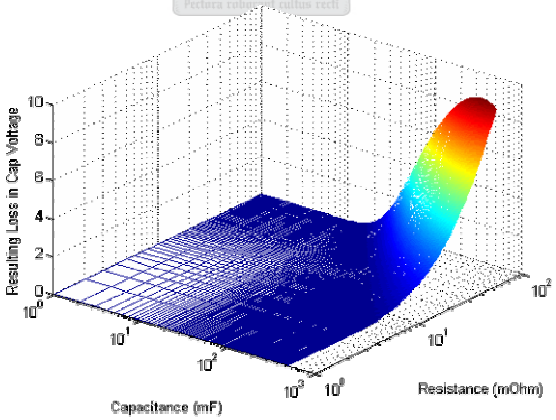


Figure 4-13 Drop in capacitor voltage $\Delta V_C(10)$ as a result of too high internal resistance or too high module capacitance.

By combining the results of the two graphs shown in Figure 4-10 and Figure 4-13 one may clearly see that there is a definite guideline on the choice of components that should be taken for the modules (Figure 4-14). The intersection of the two graphs shows a line on which component values

may be chosen to allow good functionality and performance at the lowest cost. Usually the internal resistance is the given variable. From that perspective only the capacitance may be read from the intersection line.

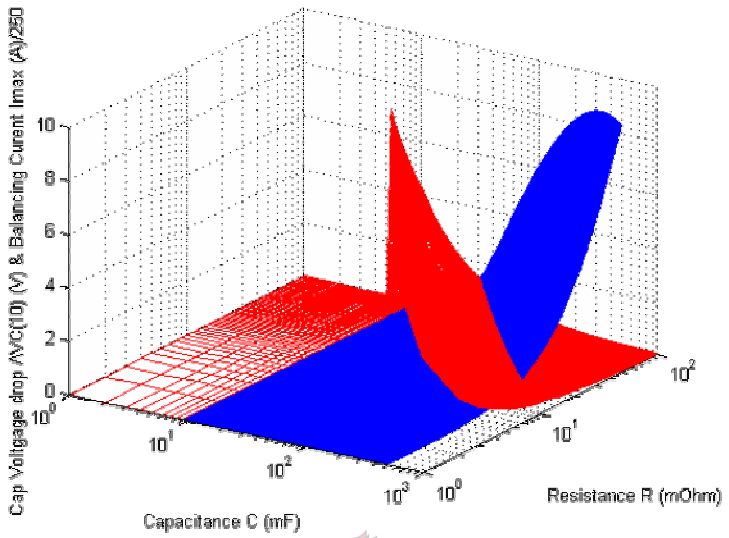


Figure 4-14 Combined graph of stresses on switch and voltage loss as a function of internal resistance and capacitors in multilevel inverter

Thus with the capacitor and switch type selected for this project the total internal resistance on the balancing path is given in equation (4-11)(Along the balancing path there are two switches and two capacitors) (Paragraph 4.4.3.5 discusses the main components choices and Appendix C contains a table of components used for the prototype; MOSFET datasheet [56]; Capacitor datasheet [57]):

$$R = 2* R_{Switch} + 2* R_{Capacitor} = 2* ½*4\ m\Omega + 2 * 3.8m\Omega = 11.6m\ \Omega \quad (4\text{-}11)$$

Reading the capacitance from Figure 4-14 C should be around 250mF to 300mF

Another important issue now is whether the device still meets its specifications with the selected components. The inverter starts inserting a voltage when the line voltage has dropped 10% or more from its nominal value. The smallest step that may be inserted into the line has a 40V front. This corresponds to 12.3% of the nominal line voltage amplitude. Thus the output will be 2.3% higher than nominal when a 10% voltage dip is compensated. Now the line voltage drops even further. So at around 85% of nominal voltage the second level of the multilevel will switch on. The second level may not be switched on beforehand as the output would overshoot the nominal by more than 10%. However, just before this the line input voltage plus the inserted voltage still only makes up for 97.3% of nominal voltage. The device is not allowed to drop the output voltage more than 10%

which leaves a 7.3% slack. This is plenty buffer as the first level is a direct contribution of the ultracapacitors voltage. Its voltage does not drop significantly during a small dip under investigation here.

Under full load conditions (50% dip with no phase shift) the drop across all internal components may not be more than 40V. The voltage required to compensate for a 50% dip is 160V which corresponds to 80% of maximum inverter output voltage which is 200V. Figure 4-15 shows the current path under full load and full dip conditions.

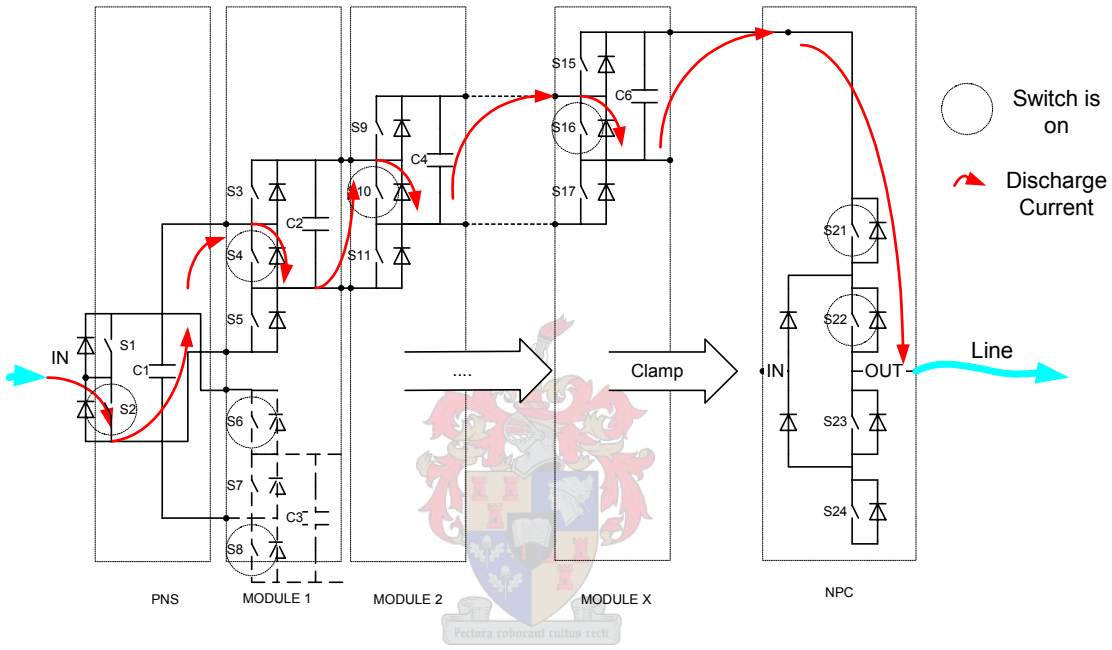


Figure 4-15 Current path when all levels are switched on; all capacitor voltages are stacked in series

Under condition where the ultracapacitor voltage has dropped overall conditions are no longer so critical. A step front will thus have lower amplitude and thus another level may be switched on way ahead of the above-mentioned limitations. The number of levels added into the supply line is a function of supply line voltage and ultracapacitor voltage. By doing so the capacitor voltage drop after a certain time is taken into account.

When adding the entire voltage drop across the currents path at a full load current, the voltage drop will be equal to 5V. The internal resistance of the ultracapacitor, switches and capacitors is 20m Ω [53], ½*4m Ω [56] and 3.8m Ω [57] respectively.

The voltage drop across the capacitors is at its peak on purely resistive loads. It was previously noted that the voltage drop from one module to the next will be less than 2V after 10 cycles or 200ms

according to Figure 4-14. This means that the foreseeable voltage drop because of internal resistances and of improper balancing would be 5V + 4*2V. There is thus still enough remaining buffer to compensate for other voltage drops discussed in the next paragraph.

4.4.3.2 **Voltage balancing throughout the inverter**

Another worst-case scenario needs to be tested before concluding. Can the energy be transferred fast enough from the ultracapacitor to the capacitor bank? This question needs to be asked although basic voltage balancing has been shown (above). This voltage balancing theorem proves that two equal modules may be switched in parallel. This aspect of voltage balancing investigates how the interconnection of several modules in parallel with one ultracapacitor influences the overall voltage balancing. It is clear that the energy transfer duration would be too long if all discharged capacitors were connected in parallel to the ultracapacitor for only 10 ms.

What should now be shown is how the capacitors' voltages behave under the control strategy proposed in Figure 1-3. This control strategy should help equalize the flow of energy over a longer duration, thus enabling larger total energy transfer from the ultracapacitor to the shunted capacitor bank. As the middle switches in the topology (Figure 4-8), (S4, S10, S16, S7, S13, S19) are complementary to the two outer switches (S3, S5, S6, S8, S9, S11, S12, S14, S15, S17, S18, S20), one may clearly read all the balancing times from Figure 1-3 and Figure 4-16. The balancing times would be the times when the modules voltage would not be added to the output signal; the non-shaded areas in Figure 1-3, or the shaded area in the Figure 4-16. The 'on' times would be shown by the non-shaded area in Figure 4-16.

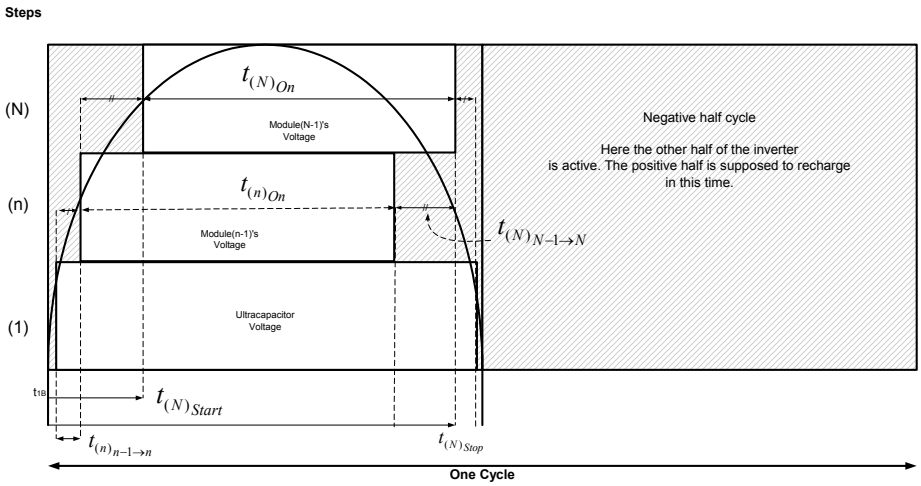


Figure 4-16 Capacitor balancing control – shaded areas are balancing times

The times shown in Figure 4-16 may be given by equation (4-12) to (4-17). Equation (4-12) gives the starting time of an 'on' state of a module 'n'. Equation (4-13) gives the stopping time. Equation (4-15) gives the total 'on' time for a module 'n' and Equation (4-17) gives the times between the starting and stopping times of a step. The radial frequency ω is 2πf where f is the line frequency.

$$t_{(n)Start} = \frac{\sin^{-1}\left(\left(2n-1\right)/2N\right)}{\omega} \tag{4-12}$$

$$t_{(n)Stop} = \frac{\left(\pi - \sin^{-1}\left(\left(N-n-1/2\right)/N\right)\right)}{\omega} \qquad n \neq 1 \tag{4-13}$$

$$t_{(n)Stop} = \frac{\left(\pi - \sin^{-1}\left(\left(2n-1\right)/2N\right)\right)}{\omega} \qquad n = 1 \tag{4-14}$$

$$t_{(n)On} = \frac{\pi - \sin^{-1}\left(\left(N-n-1/2\right)/N\right) - \sin^{-1}\left(\left(2n-1\right)/2N\right)}{\omega} \qquad n \neq 1 \tag{4-15}$$

$$t_{(n)On} = \frac{\pi - 2\sin^{-1}\left(\left(2n-1\right)/2N\right)}{\omega} \qquad n = 1 \tag{4-16}$$

$$t_{(n)n-1\rightarrow n} = \frac{\sin^{-1}\left(\left(2n-1\right)/2N\right) - \sin^{-1}\left(\left(N-n-1/2\right)/N\right)}{\omega} \tag{4-17}$$

The notation used in equation (4-17) can be explained as follows: The subscript in brackets following the symbol 't' is the step number (n) of (N) total steps to which the specific time difference from switching the previous 'n-1' step to switching the present step 'n' refers. That this is a time difference between previous and present state is indicated by the notation following the brackets being 'n-1→ n' for example (See Figure 4-16). This notation will be used throughout this thesis.

Another worst-case scenario should be analyzed here. Most energy is drawn from the inverter under maximum dip conditions. This would mean that all modules would be switched 'on' at some time during one cycle. Fortunately the time a module is 'on' or in discharge mode is inversely proportional to the dip depth. More recharge or balancing time is thus given at greater dip depth. The 'on' times of all modules are kept close to equal. This helps to divide power drawn across all modules, the ultracapacitors unbalancing time would be equal to that specific 'on' time of the first module or 'step 2'.

The circuit in Figure 4-17 shows the network to be analyzed to establish the exact conditions during dip compensation. The output of the dip compensator is connected to an ideal current source I_A with 50Hz, 106A block output (this is done for consistency and simplicity of the calculations in this report). It was previously noted that all calculations are for worst-case scenarios only. The calculations continue only for the balancing times of the ultracapacitor to the rest of the capacitor bank. Each time a switch closes at time $t_{(n)}$ to balance a capacitor, it is assumed that a maximum current of I_A = 106.1A previously discharged the capacitor for not longer than half a cycle (absolutely worst-case scenario).

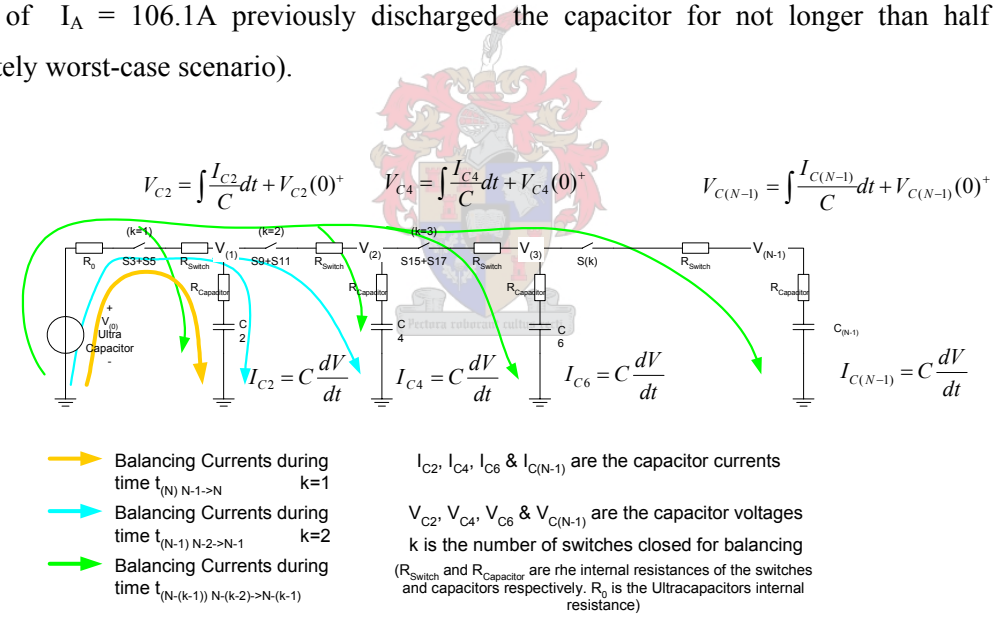


Figure 4-17 Actual balancing paths for different times – serial resistances have already been merged in this figure.

After balancing (according to Figure 4-16), the calculation at each capacitor voltage (Figure 4-17) would require solving very complex differential equations. The author suggests another method that can be used to give a linearized function of the capacitor voltages. Precise calculations are probably not necessary as these results serve as guidelines as whether the design parameters lead to successful

dip compensation at rated current or not. Simulations show that the method may be used to approximate capacitor voltages with sufficient precision.

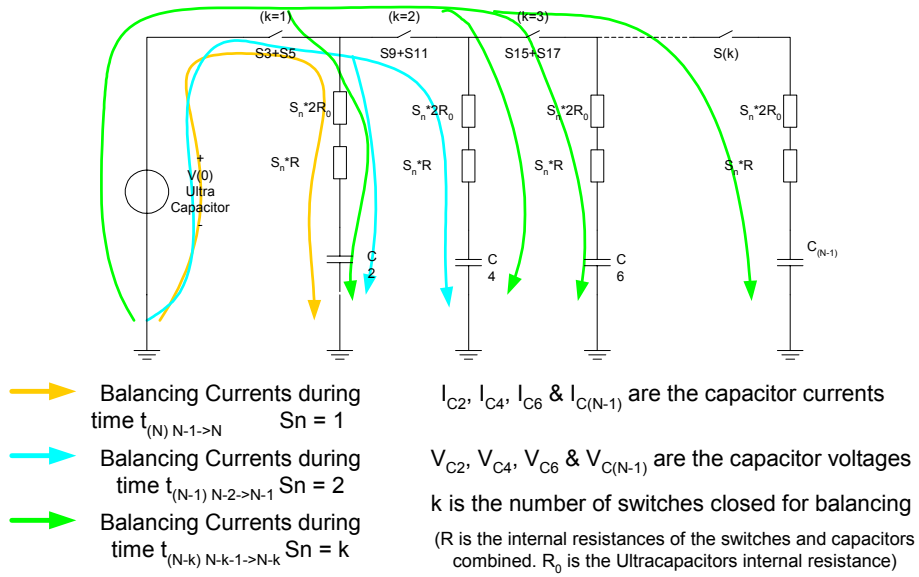


Figure 4-18 Simplified balancing current paths for different times – This will give an approximation of the balancing currents.

Finding the capacitor voltages for the circuit shown in (Figure 4-18) requires finding a solution to (4-18). This is an iterative equation and should be iterated at least ten times for acceptable precision in terms of total capacitor voltage lost. (The number of iterations strongly depends on the component values chosen.) One iteration resembles the completion of one complete cycle. Thus after 10 cycles one would know what the individual capacitor voltage would be after 200 ms (on a 50Hz system).

$$\Delta V_{C_{(n-1)}(i)} = -\Delta V - \sum_{i_t=1}^{i-1} \Delta V_{C_{(n-1)}(i_t)} + \sum_{m=3}^{N} V_{inc}(m)_{(i)} \qquad (4\text{-}18)$$

In this equation $\Delta V_{C_{(n-1)}(i)}$ is the capacitor voltage drop (from initial threshold) after (i) cycles that can no longer be balanced to threshold voltage. ΔV is the change or decrease in capacitor voltage due to discharge. $V_{inc}(n)_{(i)}$ is the change or increase in capacitor voltage after balancing in the (i)th cycle.

Equation (4-18) originates from the following deduction:

The voltage drop across the capacitors after they have been discharged with a constant current for half a cycle ($t_{1/2cycle}$) is given by equation (4-19).

$$\Delta V = \frac{I_D \cdot t_D}{C} \qquad (4\text{-}19)$$

Thereafter they will be charged again. However, the charging does not proceed as simply as in the previous paragraph 4.4.3.1. Balancing is initiated by closing switch (S3+S5) (k=1) in Figure 4-18. Then for a short time ($t_{(N)\ N\text{-}1\text{->}N}$) (Equation (4-17)) the first capacitor C2 is balanced with the source voltage V(0). After this time has passed, another switch (S9 + S11) (k=2) is closed for a time ($t_{(N\text{-}1)\ N\text{-}2\text{->}N\text{-}1}$). The difference between the circuit shown in Figure 4-17 and Figure 4-18 is that the internal resistances R are split up in Figure 4-18. When two switches are closed for balancing the resistances along the path are split up by two ($S_n = 2$) to balance the two capacitors separately with the voltage source V(0). This is the equivalent of charging two capacitors in parallel through one resistance R or charging them from the same source but through two separate resistors with each having double the resistance (2*R).

According to this simplified principle (after C2 has been discharged once by ΔV and balanced for a certain time) C2's voltage drop $\Delta V_{C2(1)}$ from initial voltage threshold is given by equation (4-21) (In the equation n starts at value 2 as the first capacitor C2 or C3 is only used for step two in the inverter) (Figure 4-12 shows the origin of this value graphically.)

In order to get to equation (4-27)(this gives each capacitor voltages) all the transitions need to be analyzed. Each time a step is removed from the output voltage, a new capacitor is connected and balanced with the source V(0). In the transition from one step removed to the next step removed, the resistance seen from a capacitor to the source changes. Due to this the recharge rate changes as well. It is not only the recharge rate that changes, but the initial voltage the capacitor is at, when another step is removed, does not comply with the original voltage before balancing is started. Equation (4-20) gives the voltage increase ($V_{inc}(n)$) on the capacitor C2 from recharge transition (n-1) to the next (n) (n always represents a step number. A certain capacitor will always contribute to the same step as shown in Figure 4-16). $V_{inc}(2) = 0$ as no balancing took place before step n = 2 was removed from the output voltage. Thus the increase in voltage towards balancing this step would be zero. $V_{inc}(n)$ would typically give a positive value only after and including n = 3 (Step 3 shown in Figure 4-16). This means that $V_{inc}(3)$ is the increase in capacitor voltage from when step n=2 was removed to when step n=3 is removed from the inverter output voltage.

$$V_{inc}(n)_{(1)} = \left(\Delta V - V_{inc}(n-1)_{(1)}\right)\left(1 - e^{\left(\frac{-t_{(N-(n-2))N-(n-1)\to N-(n-2)}}{(n-1)RC}\right)}\right) \tag{4-20}$$

The notation used here for the time inside the exponent was explained earlier underneath Figure 4-16. The total voltage of C2 after one cycle would thus be the sum of all voltage increases $V_{inc}(n)$ [sum of $V_{inc}(3)$ to $V_{inc}(N)$] minus the initial voltage drop ΔV:

$$\Delta V_{C2(1)} = -\Delta V + \sum_{m=2}^{N} V_{inc}(m) \tag{4-21}$$

After the second cycle the initial voltage drop $\Delta V_{C2(1)}$ after the first cycle needs to be considered as well to calculate $\Delta V_{C2(2)}$. So $\Delta V_{C2(2)}$ would then be calculated as in equations (4-22) and (4-23):

$$V_{inc}(n)_{(2)} = \left(\Delta V + \Delta V_{C2(1)} - V_{inc}(n-1)_{(2)}\right)\left(1 - e^{\left(\frac{-t_{(N-(n-2))N-(n-1)\to N-(n-2)}}{(n-1)RC}\right)}\right) \tag{4-22}$$

$$\Delta V_{C2(2)} = -\Delta V - \Delta V_{C2(1)} + \sum_{m=2}^{N} V_{inc}(m)_{(2)} \tag{4-23}$$

After 'i' cycles the voltage drop $\Delta V_{C2(i)}$ on capacitor C2 would thus be given by:

$$V_{inc}(n)_{(i)} = \left(\Delta V + \sum_{i_t=1}^{i-1} \Delta V_{C2(i_t)} - V_{inc}(n-1)_{(i)}\right)\left(1 - e^{\left(\frac{-t_{(N-(n-2))N-(n-1)\to N-(n-2)}}{(n-1)RC}\right)}\right) \tag{4-24}$$

$$\Delta V_{C2(i)} = -\Delta V - \sum_{i_t=1}^{i-1} \Delta V_{C2(i_t)} + \sum_{m=3}^{N} V_{inc}(m)_{(i)} \tag{4-25}$$

This can be expanded to give voltage drops for any capacitor within the circuit shown in Figure 4-18. The capacitors in the next equations are not labelled according to previous circuit diagrams but rather to step number. So the capacitor responsible for adding step two's voltage is labelled $C_{(n-1)}$ where n = 2 for example.

$$V_{inc}(n)_{(i)} = \left(\Delta V + \sum_{i_t=1}^{i-1} \Delta V_{C_{(n-1)}(i_t)} - V_{inc}(n-1)_{(i)} \right) \left(1 - e^{\left(\frac{-t_{(N-(n-2))_{N-(n-1)\to N-(n-2)}}}{(n-1)RC} \right)} \right) \qquad (4\text{-}26)$$

$$\Delta V_{C_{(n-1)}(i)} = -\Delta V - \sum_{i_t=1}^{i-1} \Delta V_{C_{(n-1)}(i_t)} + \sum_{m=3}^{N} V_{inc}(m)_{(i)} \qquad (4\text{-}27)$$

Here $\Delta V_{C_{(n-1)}(i)}$ is $C_{(n-1)}$'s voltage drop after 'i' cycles. R is the total series resistance consisting of $R_{Switch} + R_{Capacitor} + 2*R_0$ (R_0 is multiplied by two as there are both positive and negative module arrays connected to the same ultracapacitor. This simplification is valid according to the approximation principle introduced in Figure 4-18).

To give an indication of the accuracy of this equation, the results of several simulations with the same component values are used to compare the results obtained with equations (4-26) and (4-27). These types of graphs are used throughout this thesis to show the voltage drops $\Delta V_{C_{(n-1)}(i)}$ for many combinations of 'N' which is the maximum number of steps the inverter may output.

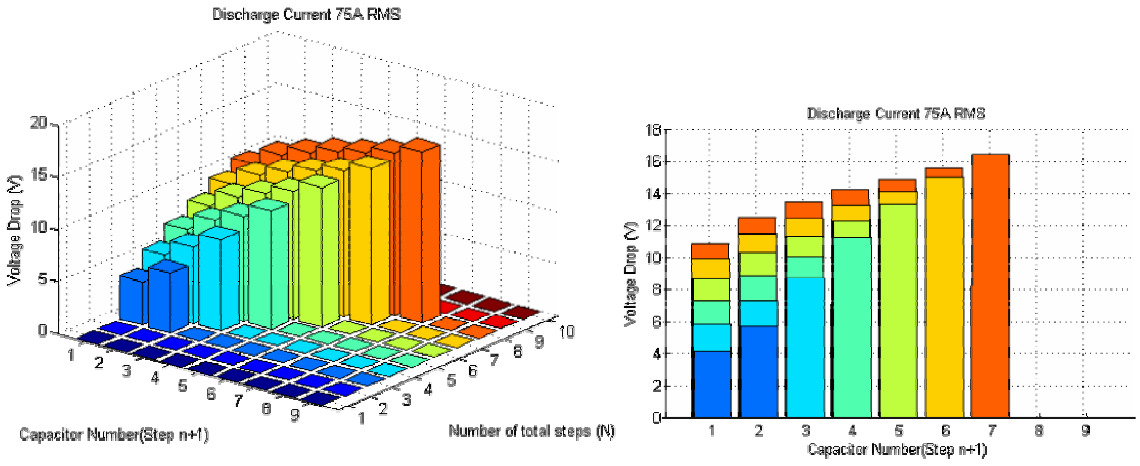


Figure 4-19 Results obtained from equations (4-26) and (4-27) for a discharge current of 75A (RMS)

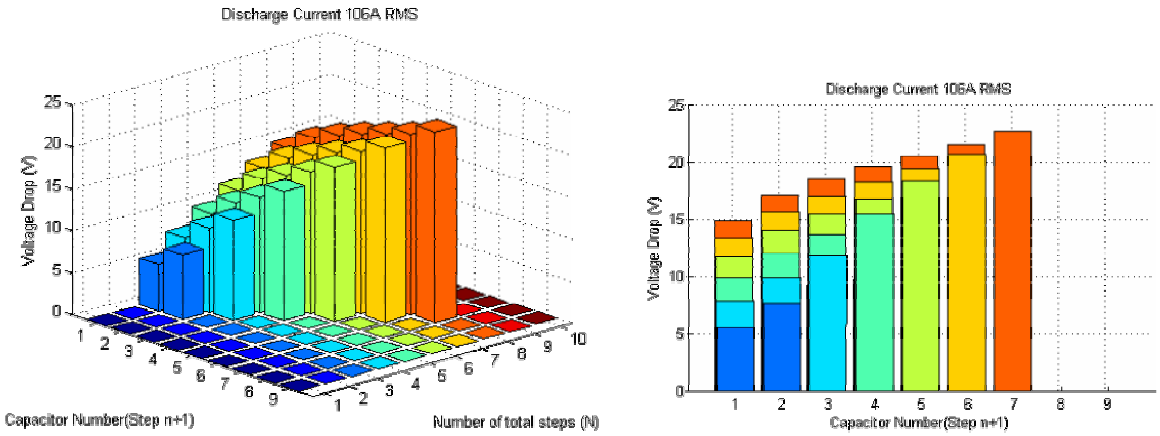


Figure 4-20 Results obtained from equations (4-26) and (4-27) for a discharge current of 106.1A (RMS)

These figures show that for a five-step inverter (which has 4 modules and one energy storage device, thus N = 5) the voltage drop from the energy source to the first module (At step n=2) is about 7.5V for a 75A load. Thereafter the voltage drop from subsequent modules increases by less than 2V with each further module.

The graphs also show that the more modules are stacked in parallel, the higher the voltage drop will be. For example, when 7 modules (this would allow 8 steps or 17 levels) are stacked, a voltage drop of 16 V is experienced on the furthest parted module form the source.

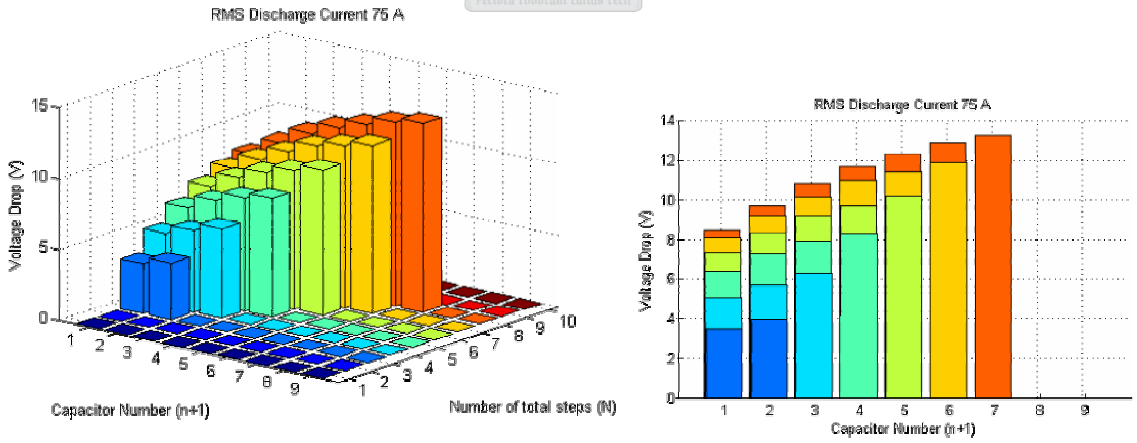


Figure 4-21 Results obtained from simulations for a discharge current of 75A (RMS)

Figure 4-23 shows the voltage drop on the capacitors of a five step inverter. The voltage across these modules drops very quickly during the first few cycles. After about 200 ms the drop stabilizes around 7V below the nominal source threshold. There will still be a decreasing slope as shown in

Figure 4-23, but that is mainly as a result of the energy source also being a capacitor that is slowly discharging.

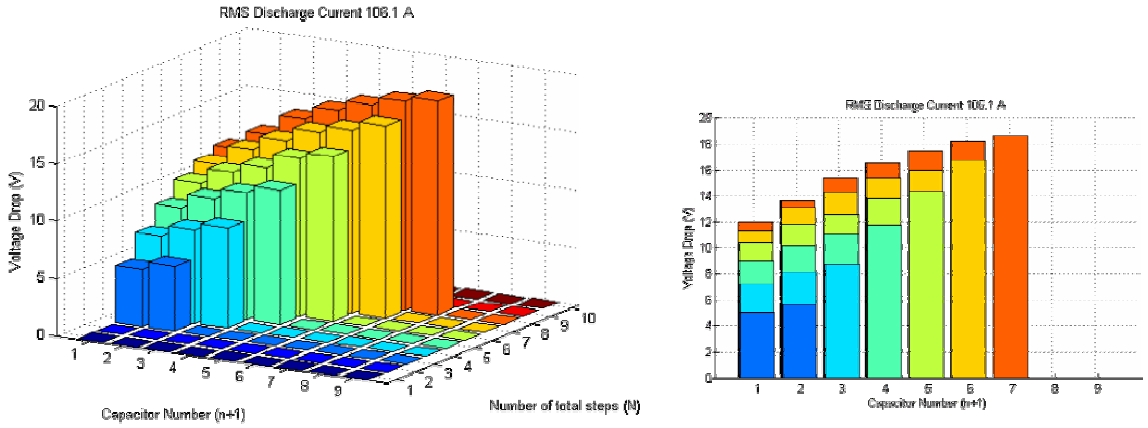


Figure 4-22 Results obtained from simulations for a discharge current of 106.1A (RMS)

Figure 4-21 and Figure 4-22 show the data obtained from simulations results such as shown in Figure 4-23 graphically as a function of N and n.

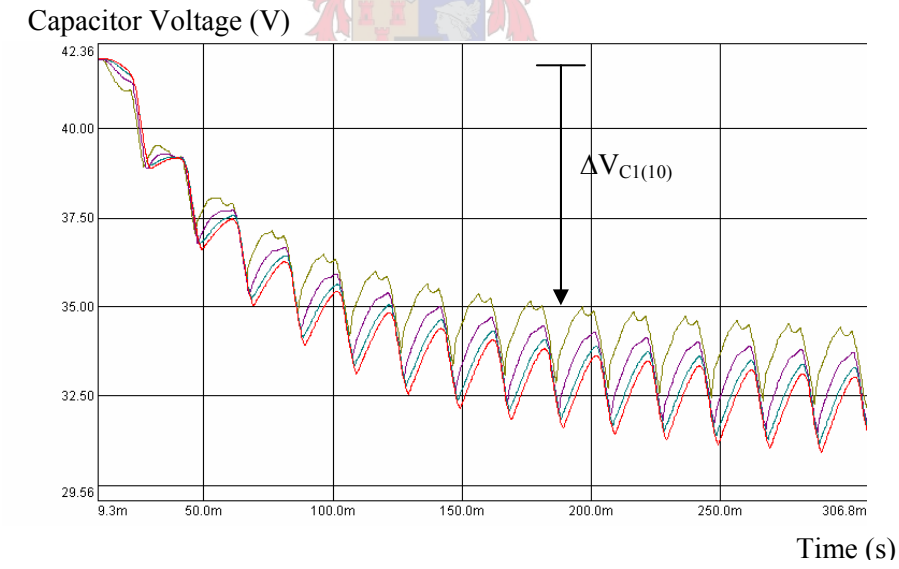


Figure 4-23 Respective capacitor voltages for full-scale simulation on a 5-step (4 capacitor module) inverter topology (75A RMS)

From the above figure the voltage drop from one module to the next is also shown to be less than 2V as is the case from Figure 4-14. The prototype inverter of interest here has five steps – four capacitor modules: With an average discharge current of 75A, the voltage drop from ultracapacitor voltage to the first capacitor C1 is about 7V after 10 cycles. This translates to a balancing current on the first

switches S3 + S5 to be 140A (knowing that the internal resistances along the path remain constant within tolerable range). Both the positive and the negative module array draw such currents from the ultracapacitor. Thus the balancing current seen by the ultracapacitor would be around 280A. This suggests that the voltage drop on the internal resistor of the ultracapacitor would be 20mΩ * 280A = 5.6V. The difference between 7V and 5.6V is the voltage difference seen from the input terminals to the output terminals of a module. This is given as 1.4V and again corresponds to the allowable voltage drop according to Figure 4-14).

Consider the simple 'power in' must equal 'power out' principle. When the inverter draws an average current of 75A on the output at a peak voltage of 200V (141V RMS) the current on the input (40V) side cannot be less than 265.2 A. This corresponds to the simulations where the input current is less than 280 A (as in above paragraph).

In the case of Figure 4-20 and Figure 4-22 the final inverters peak output current is taken as the average current in the simulations and calculations. The voltage drop from ultracapacitor and first capacitance C1 is less than 11V (Figure 4-20). This translates to a current of 220A through switches S2+S5. Thus the current rating of the balancing switches should be about double the peak output current of the inverter for a five-step topology.

It was previously mentioned (paragraph 4.3) that the balancing switches need to carry line currents as well as balancing currents for a very brief moment. Thus the components were chosen so that they may handle brief current peaks like these. Simulations show that these current peaks are way below 250A for full load currents.

In conclusion all voltages and currents in this topology can be analyzed for different internal properties of components. It was found that the voltage drop of the inverter is significantly high and must not be ignored. For this reason the software must take the voltage drop after a few cycles into consideration and has to compensate for that by inserting more steps to keep the line voltage steady.

4.4.3.3 **Improvement of voltage balancing by modular expansion**

The performance of the proposed topology can be greatly improved by reducing the voltage drop across the capacitors (this problem occurs as a result of insufficient balancing). This addition does not require extra ultracapacitor storage, thus only minimally increasing the price and complexity. It would be helpful when the inverter is expected to compensate for up to 100% voltage drops.

The problem with the topology analyzed here is the drop in capacitor voltage as a result of insufficient balancing times. The balancing times can be greatly increased by increasing the number of modules inside and converter. There are two ways of modifying the converter for better balancing and larger output voltage rating as discussed below.

4.4.3.3.1 Sharing of power consumption by more modules

The discharge path is thus rotated through all modules. Each discharge period is thus followed by a (K-1) time longer charge period before a discharge will occur on a module again. This charging time will increase by $2(K-1)/T_s$ where K is the number of identical inverters inserted and T_s is the cycle period.

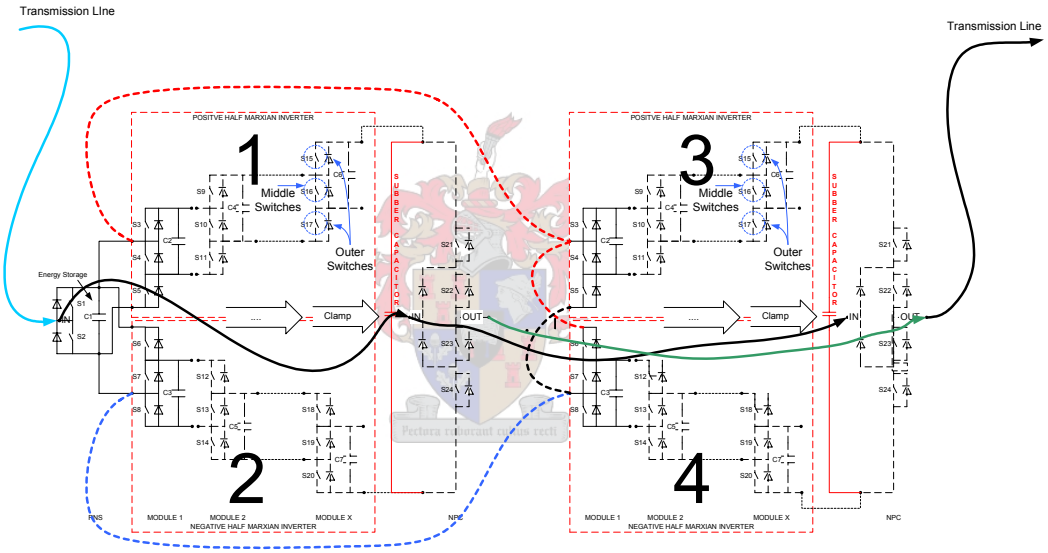


Figure 4-24 Rotating the use of the modules (ultracapacitor and PNS not shown)

Figure 4-24 shows two superimposed stacked inverter modules sharing the same input, output, energy storage and PNS (the figure does not show the PNS or the energy storage).

Figure 4-25 shows the irreversible voltage drop for the same inverter as in paragraph 4.4.3.1 but with two inverters superimposed. The active operation duration of each inverter half is distributed equally from inverter to inverter during dip compensation. During each half cycle a shift takes place. When two inverters are combined each module will only activate every second cycle.

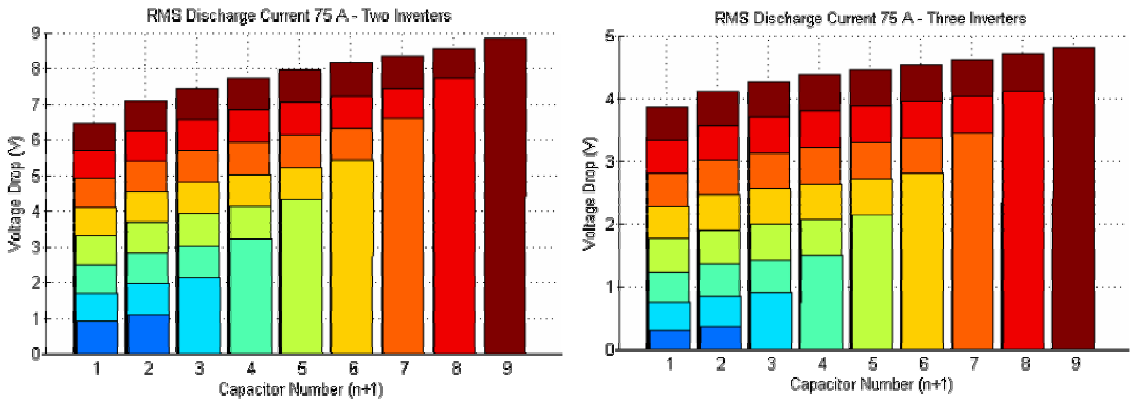


Figure 4-25 Matlab results showing capacitor voltages for two and three single-phase 17 kVA superimposed inverters

From these graphs one may see that the balancing dramatically improves as less voltage drop is experienced on the capacitors. This also reduces the balancing currents so that smaller MOSFETs may be taken for the converter.

4.4.3.3.2 Back- to-back Marxian MLI

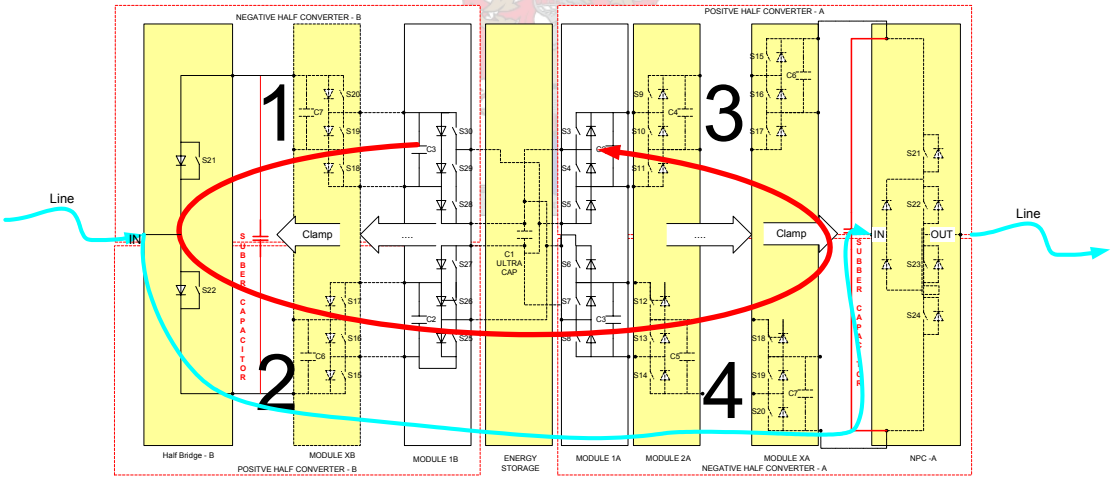


Figure 4-26 Back-to-back Marxian MLI

This method of improving the voltage balancing is similar to the above mentioned procedure. However this method yields some more advantages in terms of versatility. Two identical Marxian MLI blocks are connected back to back as shown in Figure 4-26, without using the PNS clamp. Under normal working conditions the boost operation is rotated around the inverter as is the case above. The voltage balancing is improved in the same manner as in paragraph 4.4.3.3.1. However this topology has the option of doubling its output voltage by engaging operation without improved

voltage balancing. This way the left and right side of the inverter are not switched alternatively but at the same time. Voltage balancing will proceed as in paragraph 4.4.3.1 (Figure 4-19 to Figure 4-22) in this case.

This method would be useful in dip compensators designed to compensate for occasional large dips or even outages. The NPC would have to handle half the total inverter output voltage, as well as the half bridge clamp on the left.

4.4.3.4 **Current density**

This paragraph explains the design of the circuit board. The main concern here was to minimize the current path lengths between the modules to reduce ringing on switching capacitors in parallel and to design for high-current conduction. However, ideally the design should be kept modular. This means that the number of modules inside an inverter should still be optional. From the previous paragraph the maximum current on a module is 220A.

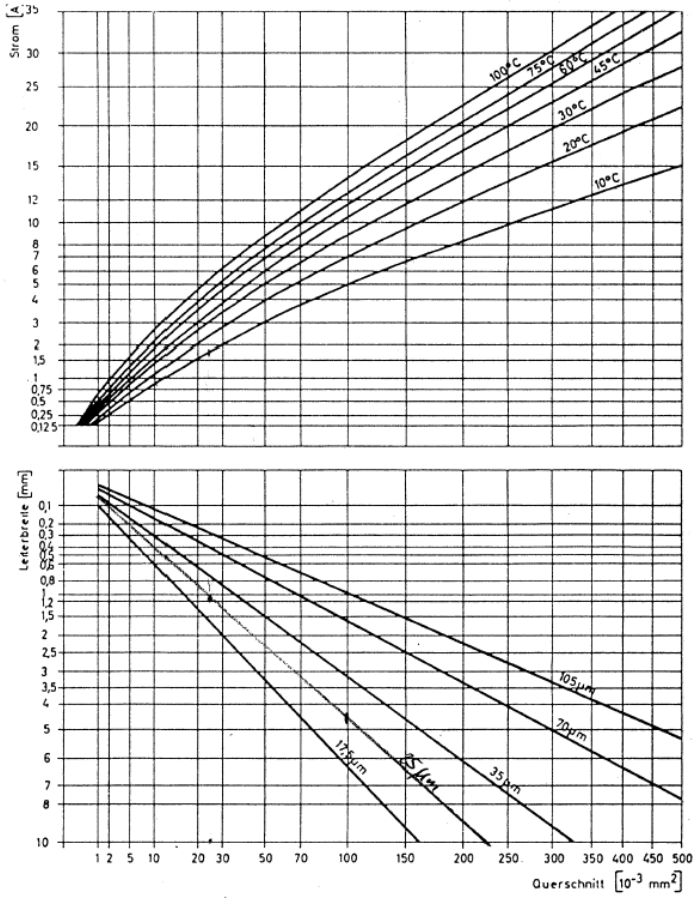


Figure 4-27 Design chart from NBS Report 4283 [58]

According to the NBS Report 4283 [52], a copper conductor on a PCB should be 5 mm wide (70µm thickness) for a current of 25A and a maximum temperature increase to 60°C. In Figure 4-27 it can be read that the conductor width increases approximately logarithmically with current. Thus the average conductor width for 220A current should be 45mm.

Track copper thicknesses of 70µm are readily available from most PCB manufacturers. Although the thickest possible copper track for the design would be ideal for such high current PCBs, the costs involved for 105µm were proportionally too high to consider. Thus 70µm copper thickness was chosen. This is practical as the components took up a good amount of board space. Board space may be utilized for conductors and components at the same time. To make sure each component has optimal connection to the copper layer, two PCBs are placed on top of each other. Each PCB has two layers of which the layer pours over the whole surface on both sides. This implies that one surface would be one pole of the four poles required for one half modules (Figure 4-8).

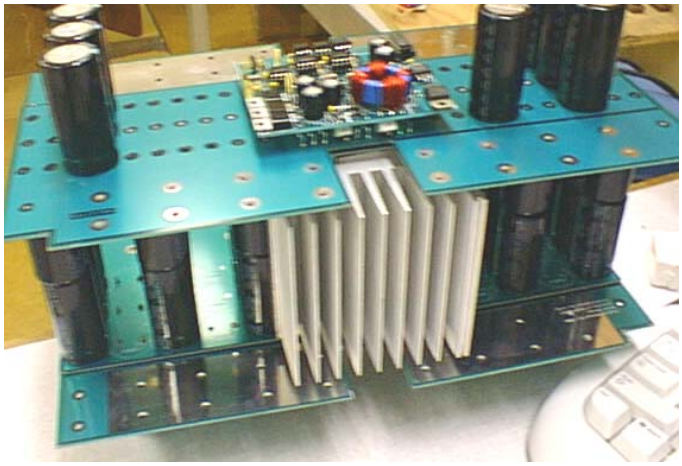


Figure 4-28 One module with both positive and negative sides is shown with the MOSFETS in the middle.

The MOSFETS are placed in the centre so that they may still be easily accessed when they need to be replaced. The heat sink can also be used for both the negative and positive side. Another added benefit of this design is mechanical strength and compactness.

4.4.3.5 **Internal properties of components**

Choice of components for the practical setup: The main components of interest here are the switching components and the capacitors for energy storage. (A complete list of components is attached in Appendix C.)

Ideally one should use few components in any system. This would increase reliability. However in some cases the price of a single unit exceeds the price of combined units. The choice is to use cheaper, smaller, more readily available units. Another factor contributing to this choice is that the practical model is designed for laboratory evaluation. In devices for field operation more focus is put onto the reliability of components.

A survey of recent MOSFET technologies was done for the purpose of this project. (Table 4-2). The aim was to find a switch that operates at low voltage (< 150V) and very high current (more than 220A). There are several MOSFET modules with suitable ratings available on the market; however they are still very expensive. Another solution would be to take lower current rated MOSFETs and switch them in parallel, so that they may switch at rated current.

Company & Type	*Rating*	*Price*	*MOSFET Module*	*Internal Resistance*	*Finding*
International Rectifier IRFP064M	90A, 55V	R 11.50	No	5.5mΩ	Too low voltage rating
International Rectifier IRFS3810	170A, 100V	R39.49	No	9mΩ	Suitable when stacked parallel
International Rectifier IRFP2907	209A, 75V	R25.00	No	4mΩ	Suitable when stacked parallel
International Rectifier IRF8010L	80A, 100V	R15.50	No	12mΩ	Suitable when stacked parallel
International Rectifier IRF8010S	80A, 100V	R10.20	No	12mΩ	Suitable when stacked parallel
Toshiba S2Z49-MG600A2YM80	600A, 100V	R1419.67	Yes	1.1mΩ	Suitable but expensive
Semikron SKM 111 AR	200A, 100V	R 795.00	Yes	4mΩ	Suitable but expensive
Semikron SKM 313B010	400A, 100V	R 2700.-	Yes	2mΩ	Suitable but expensive
IXYS VMK 165-007T	2x165A, 70V	R 515.-	Yes	7mΩ	Too low voltage rating
IXYS VMO 650 -01F	650A, 100V	R 1865.-	Yes	1.1mΩ	Suitable but expensive
IXYS VMM 650-01F	2x680A, 100V	R 3234.-	Yes	1.1mΩ	Suitable but expensive

Table 4-2 MOSFET comparison table (currents are given in peak allowable currents)

As the MOSFET modules are very expensive, it was decided to make use of ordinary MOSFETs and stack them in parallel. The IRFP2907 from International Rectifier seems appropriate (2x 200A = 400A peak or 140A average).

Another survey of electrolytic capacitors was made (Table 4-3). The capacitors must be able to carry the line current, balancing current and have a very low ESR. The listed capacitors are able to carry the line current when connected in parallel.

The electrolytic capacitor from HITANO was preferred because it has the lowest ESR. The allowable ripple current per unit is 5.6A. This gives a total allowable ripple current of 140A when 25 units are stacked in parallel. This is adequate when the load current is 75A (RMS).

Company	*Code*	*Rating*	*Internal Resistance (ESR – DC)*	*ESR at 250mF, 50V*	*Price* Total price ~250mF, 50V*
	ALS30A684RT025	680000uF, 25V	4mΩ	8mΩ	R1238.00
	ALS31A684RT025	680000uF, 25V	4mΩ	8mΩ	R1238.00
BHC	ALS40A684RT025	680000uF, 25V	3.9mΩ	7.8mΩ	R1238.00
	ALS41A684RT025	680000uF, 25V	3.9mΩ	7.8mΩ	R1238.00
	B41456-B4680-M	680K uF, 16V MOQ 12	5.6mΩ	11.2mΩ	R 3720.00
EPCOS	B41456-B5470-M	470K uF, 25V MOQ 12	6.0mΩ	12mΩ	R1038.00
	B41456-B5150-M	150K uF, 25V MOQ 15	8.0mΩ	8.0mΩ	R1743.04
	B41456-B7220-M	220K uF, 40V MOQ 12	6.5mΩ	6.5mΩ	R 1753.00
BHC/Aerovox	See RS catalogue	220000uF, 40V	6mΩ	6mΩ	R1069.00
Kendeil	Type K01	220000uF,25V	9mΩ	9mΩ	R 880.00
Hitano	ECR Series	10000uF, 50V	40mΩ	3.8mΩ	R 325.50

Table 4-3 Capacitor comparison table

4.4.3.6 **Heat sink design**

This part of the design deals with the heat expulsion throughout the system. Heat is generated in the switching components such as the IGBTs and the MOSFETs. The IGBTs are packaged inside the module with the built-in heat sink. No design needs to be done on those. The MOSFETs are PCB-mount components in a TO 247 package. This is undesirable as the performance is known to improve on packages with better layout, like screw-mount MOSFET modules. Even though the internal MOSFET is rated at 200 A, the package only permits 80A continuous conduction. The heat sink design must thus satisfy the following conditions:

- Each switch consists of 2-3 MOSFETs in parallel that all have to be mounted on the PCB (see paragraph 4.4.3.4);

- For practical purposes one heat sink is used per module. This includes the top and bottom half of each module that needs to be mounted onto one heat sink;
- The heat sink should be large enough to allow continuous operation such as during harmonic, VAR or power factor compensation;

In order to minimize losses, the MOSFETS are controlled to conduct minimum possible current for balancing and compensation by making use of the phase shift control technique (Figure 4-16).
The calculations made are for all MOSFETs on one heat sink. Thus the power is doubled as two halves share a heat sink. As conduction times vary during different dip situations, the worst-case scenario is again investigated here. Thus the conduction time is 10 ms in a 20 ms cycle.

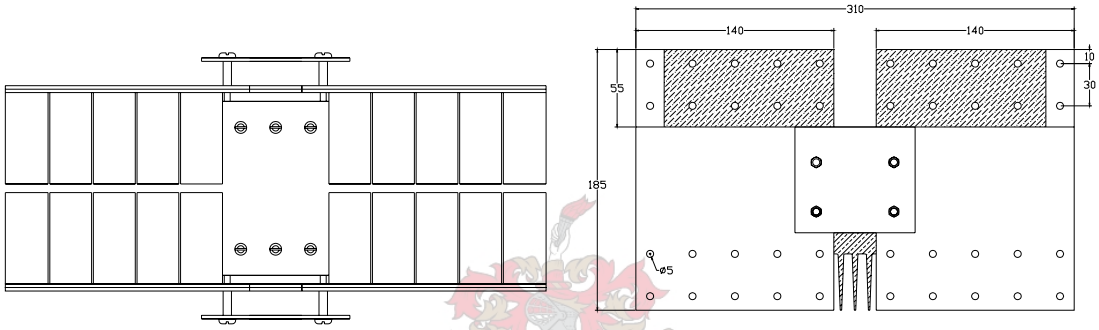


Figure 4-29 Cad drawing of front and top view of a module

Conduction Losses:

$$P_{on} = 2I^2 R_{on} \frac{t_{on}}{Ts} = 11.25W \qquad (4\text{-}28)$$

P_{on} is the time during which a module is in conduction mode. The current I is known to be 75 A_{RMS} (power is doubled for two sets of MOSFETs on the heat sink). The maximum time a module is in conduction mode is 10ms and R_{on} is 4mΩ * 0.5 as two MOSFETs are in parallel.

$$P_{balance} = 4I_C{}^2 R_{on} \frac{t_{on}}{Ts} = 78.4W \qquad (4\text{-}29)$$

$P_{balance}$ is the power consumed during balancing times. The average balancing current I_C through a MOSFET pair is 140A in the lower rank modules in the 5-step inverter. There are 4 switch pairs on

one heat sink, thus the power absorbed by the heat sink must be 4 times the power generated in one switch.

Switching losses:

$$P_{s(Cond)} = 2\left(1/2V_{dc}If_s(t_{c(on)} + t_{c(off)})\right) = 1.2W \quad (4\text{-}30)$$

$$P_{s(Bal)} = 4\left(1/2V_{dc}I_c f_s(t_{c(on)} + t_{c(off)})\right) = 4.48W \quad (4\text{-}31)$$

where $t_{c(on)}$ and $t_{c(off)}$ are both 4us (paragraph 4.4.3.7)

Here $P_{s(Cond)}$ and $P_{s(Bal)}$ are the switching losses in the conduction mode switches and the balancing switches respectively. V_{dc} is the modular voltage (40V) and f_s is the switching frequency (50 Hz).

Total losses on one module:

$$P_{total} = P_{on} + P_{balance} + P_{s(Cond)} + P_{s(Bal)} = 95.33W \quad (4\text{-}32)$$

The heat sink used in this setup has a thermal resistance to air of 0.5°C/W. The isolation pads used between the MOSFETs and the heat sink have thermal resistance of 0.65°C/W. These pads have a breakdown voltage of 4 kV and a 2 kV breakdown voltage under very moist conditions.

With $R_{\theta JC}$ + $R_{\theta CS}$ = 0.56 ˚C/W on each MOSFET, the average $R_{\theta JC}$ + $R_{\theta CS}$ + R_{IH} would be the calculation of the paralleled thermal resistance of each MOSFET (junction case and isolation pad).

There is a total of 12 MOSFETs attached to the heat sink each having their separate isolation pads. The total thermal resistance (junction to heat sink) would thus be:

$$R_{JC} + R_{CS} + R_{IH} = (R_{\theta JC} + R_{\theta CS} + R_{IS})/12 = \sim 0.1\ ^\circ C/W \quad (4\text{-}33)$$

The resulting junction temperature, showing a total power consumption of P_{total}, is given in equation (4-34).

$$T_J = P_{total} (R_{JC} + R_{CS} + R_{IH}) + T_A = 82.2\ ^\circ C \qquad (4\text{-}34)$$

T_A is the ambient temperature, which is taken to be 25˚C for most normal circumstances. This shows that the heat sink chosen for the cooling of the modules is sufficient. For practical field installations the device should be equipped with better cooling for increased reliability and lifetime of components. Each MOSFET can still conduct 148 A when the junction is at 100˚C [56]. This allows for proper function to 82.2˚C.

4.4.3.7 **MOSFET drivers**

According to [59] MOSFETs can be paralleled very easily, because of the positive temperature coefficient of their on-state resistance. For the same junction temperature, if $r_{DS(on)}$ of MOSFET 2 exceeds that of MOSFET 1, then during the on state, MOSFET 1 will have a higher current and thus higher power loss compared to MOSFET 2. Therefore the temperature of MOSFET 1 will increase along with its 'on' resistance. This will cause its share of current to stabilize.

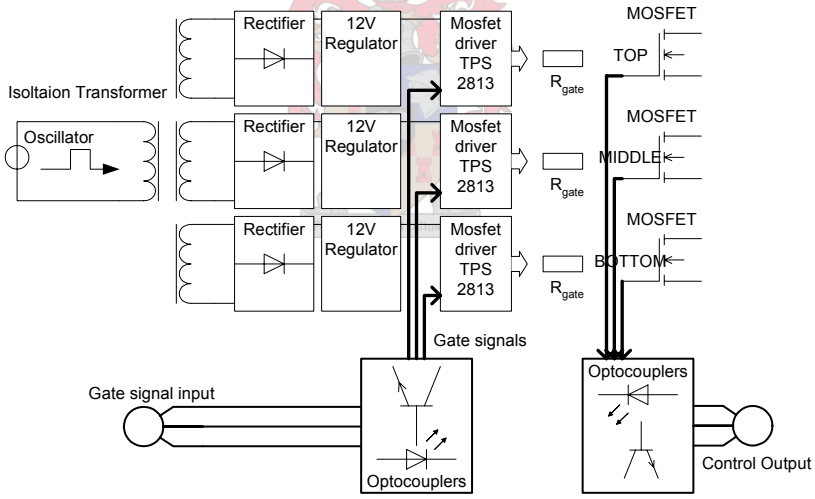


Figure 4-30 Block diagram of the isolated supply and driver circuits of the MOSFETs.

A block diagram representation of these circuits is shown in Figure 4-30. (The complete circuit diagrams of these circuits and the rest of the new circuits are available in Appendix C.)

Power supply:

Each individual inverter module needs an isolated power supply with six isolated 12V outputs. For better isolation the positive and negative halves of each module have individual isolation transformers. Thus every module has two separate driver boards driving three switches each. The driver board consists of a 50 kHz oscillator, with its output on the primary side of a pulse transformer, and three secondary windings that supply the necessary voltage for the driver circuits of each switch. This is a very standard design for driving MOSFETs.

Driver circuits:

The main aim of this part of the design is to achieve the following:

- The MOSFETs must be switched in pairs of three in parallel, simultaneously;
- The turn-on and turn-off times must be minimized, but that will keep the voltage overshoot across the MOSFETs within limits; and keep the transition currents low. The turn-on times must be slow enough to allow the snubber capacitor shown in Figure 4-31 to charge or discharge without exceeding the current limits of the inverter switches.

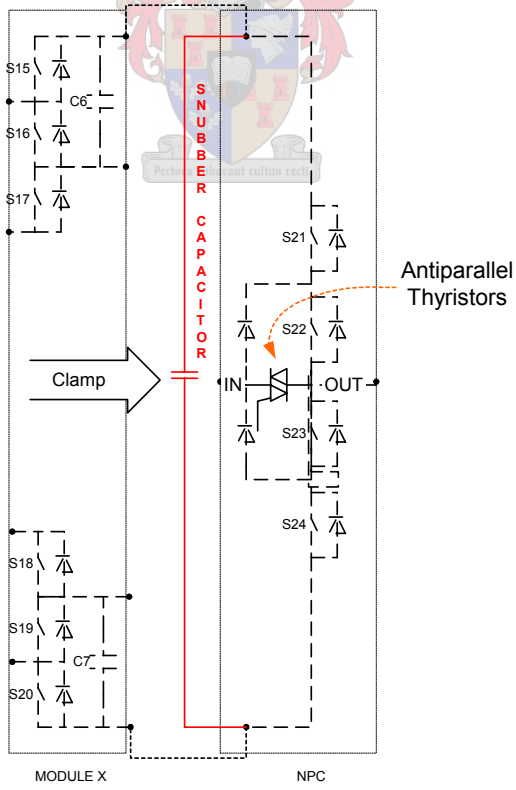


Figure 4-31 Location of the snubber capacitor

It is best to keep the gate-source voltage of the paralleled transistors the same during switching so that they share approximately equal currents. However, the gates cannot be connected together, but rather a small resistance must be used in series with the individual gate connections [59] (Chapter 22-6-3). The minimum turn-on and turn-off times of the MOSFETs which are specified on the datasheets are as follows:

$$tc(on) = tr = 213 \text{ ns}$$
$$tc(off) = tf = 260 \text{ ns}.$$

In this design these times must be longer in order to minimize the voltage overshoot at turn-off. The gate signals are transmitted serially through an optical link. The minimum time between one state to the next is thus limited to 70 μs. The minimum time in which a MOSFET can be turned on and turned off is therefore 70 μs. It will be therefore a safe practice if the turn-on and turn-off times of these MOSFETs are chosen as tc(on) = tc(off) = 4.0 μs.

With this turn-on and turn-off time it is necessary to verify that the turn-on and turn-off currents, because of the snubber capacitor shown in Figure 4-31, do not exceed the rated switch current. The snubber capacitor has a capacitance of 0.47 μF. The worst-case voltage change across this capacitor within turn-on and turn-off time is equivalent to five steps voltage (200V).

$$I = C\frac{\delta V}{\delta t} \qquad \therefore I = 23.5A \qquad (4\text{-}35)$$

The rated continuous current of three paralleled MOSFETs is 240A. The peak current is 600A. Thus the turn-on and turn-off currents as a result of the snubber capacitor plus balancing currents are still within limits (maximum balancing current estimated to be 220A, Paragraph 4.4.3.1).

The gate input capacitance of one MOSFETs is specified as C_{iss} = 13nF. From figures 22-11 and 22-14 in [59] it seems reasonable to assume that the turn-on/turn-off times are more or less equal to four times the time constant of the gate resistance (R_G) and C_{iss}. The gate resistance can therefore be designed according to the following equation:

$$4\mu s = 4R_G C_{ISS} \qquad (4\text{-}36)$$

From this equation, the gate resistance is calculated as:

$$R_G = 76.92\ \Omega \approx 100\ \Omega$$

According to paragraph 22-6-2 in [59], the bias voltage of the MOSFETs must be high enough to minimize the 'on' resistance ($R_{DS(on)}$), but not too high for specifications stated in the datasheets. The bias voltage was chosen as V_{GS} = 12 V. It will cause a peak current of I_G = 12 V/ (100 Ω/3) = 0.36 A. The TPS 2813 driver chip of Texas Instruments, with a 2 A peak output current rating, was chosen as the most cost-effective option.

To assist in protecting the inverter, the gate signal from the MOSFET is fed back to the controller board again. In the event of a MOSFET failing to switch on (this might be because it was previously damaged) the controller will call an error condition in which case the inverter will shut down. As the balancing of the capacitors is a crucial component of the design, potential damage caused by an unbalanced inverter would be prevented.

The current drawn by the optical couplers is around 10 mA. This will reduce the final gate voltage on the MOSFET by 1 Volt. The MOSFET switches on completely at 8V already. Thus the MOSFET will still be fully switched on at 12V-1V. The effect of the additional optical driver on the gate can thus be neglected for the calculations of R_G.

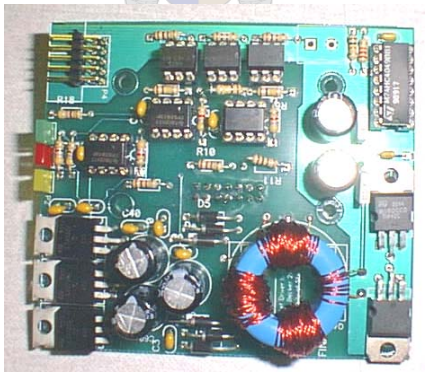


Figure 4-32 Picture of the driver circuit for each half module

4.4.4 **Neutral point clamp**

A simple neutral point clamp is used in MMLI topology to combine the positive and negative output waveforms to one MMLI-based converter output. The reason a neutal point clamp is used here is so

that the line current can be bypassed during zero voltage emission phases. Unnecessary conduction of line currents through the inverter would introduce unwanted zero voltage losses.

4.4.4.1 Power ratings

The power rating of the NPC depends on the number of modules inserted in the MMLI. Generally the NPC carries a current not exceeding the line current and a voltage not exceeding (X + 2) V(0) (Here V(0) is the energy sources voltage and X = N-1 is the number of modules in an inverter. The prototype has four modules).

In the 50 kVA 3 phase converter tested in this study, the voltage rating of the switches should be more than 240V (seen during voltage dump) and current rating of more than 75A (RMS).

This proves the performance benefit of this type of serial topology over similar shunt topologies where in three-phase systems the switch rating should be 650V or more. Both system current ratings are equal.

4.4.4.2 Snubber capacitor

The snubber capacitor across the NPC is used to reduce some stresses. The NPC will handle a maximum of 240V (or 252V during swell compensation) across its terminals. Due to the switching property and stray inductance from the MMLI, the NPC needs a snubber capacitor as protection because the MMLI's voltage may drastically overshoot the specified voltage.

The snubber capacitor has multiple voltage levels across its terminals within one cycle. In Figure 4-31 the snubber capacitor is shown as a purely capacitive snubber. A purely capacitive snubber in this case would be impractical as currents inside the MMLI would peak. Thus virtual snubber resistance is added by reducing dV/dt on the gate drives of the MOSFET as is explained in paragraph 4.4.3.7.

4.4.4.3 Elimination of the NPC, PNS and snubber capacitor – an alternative

The use of additional high-voltage switching components in the MMLI topology is not entirely necessary. There is, however, a trade-off as usual. The addition of the high voltage switches allows the use of improved voltage balancing techniques introduced in paragraph 4.4.3.3. If only two module arms with limited voltage balancing capability are used, the following topology allows complete elimination of a snubber capacitor, PNS or NPC.

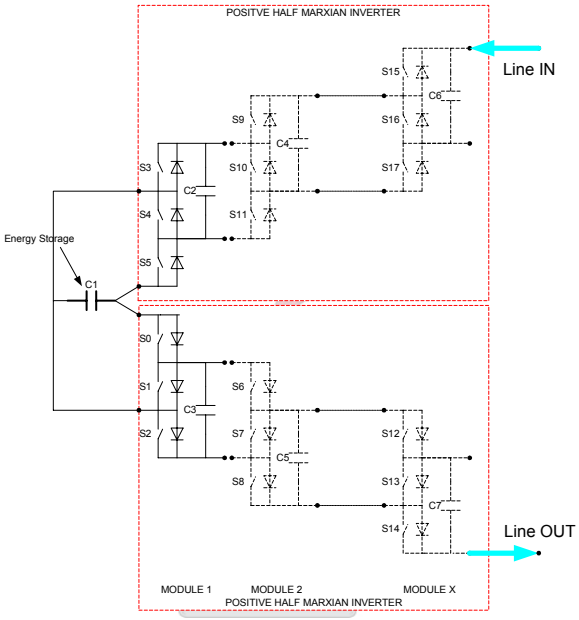


Figure 4-33 Marxian MLI without NPC, PNS and snubber capacitor

This topology also conforms to the voltage balancing theorem of paragraph 4.4.3.1.

Advantages of this topology:

- No expensive high-voltage components required such as IGBTs;
- Simpler than other suggested MMLI topologies;
- Both sides' modules (upper and lower) are the same. No negative modules are required;
- No additional snubber capacitors needed.

Disadvantages:

- The peak output voltage is $(X)V_{C1}$ as opposed to $(X+1)V_{C1}$ of MMLIs with NPCs and PNS's. (X is the number of modules in the inverter);

- Following from this the voltage balancing is even worse for the same amount of possible steps.

4.4.5 Daisy chaining of switches

The solution to multiple switches:

The solution used for the device in this project is a combined switch chain and switch multiplexing technique. As an indication of the number of switch signals required, a three-phase compensator with 5 steps uses 90 switch signals. Each gate drives at a different voltage, so isolated gate signals would be needed. Isolation is required for protection of the controller circuit. To implement 90 signals individually isolated by optic fibre would cost about R 18 000. (EBV Electrolink currently sells optical senders and receivers for about R100 each.) Another problem is purely mechanical. The number of optic fibres going to the controller would be too large to manipulate.

The solution to this is to daisy chain all the switches. This reduces the number of optical fibres going to the controller board to only one. However the number of optical transmitters and receivers remains the same. Thus a purely daisy chained switching does not reduce the cost.

A better solution is to mix optical fibre with other, cheaper optical isolators. As the gate voltage difference on one module will not increase to more than $V_{Module} + V_{gate}$ cheap low voltage isolation optical couplers can be used. Common optical couplers have a 1 to 2KV isolation. The cheapest optical coupler found in South Africa has 5KV isolation (4N25). This is more than enough isolation for the inverter, which is only rated at 230V AC or maximum gate difference voltage of 240V (zero common mode voltage).

However, it must be remembered that most dips occur on HV transmission lines (Chapter 2 and Appendix A). The effort and expense of daisy chained switches for a 230V inverter as the final product is unduly complicated. In this event, as prototype for larger systems the complication of daisy chaining switches would be allowed.

Time spent on daisy chaining switches probably works out to be approximately 80% of the total time spent on designing such a compensator. Daisy chaining requires a certain serial protocol to which all the switches respond. The disadvantage of any readily available serial communication devices such as those communicating on I2C, SPI or 1Wire protocol from Maxim is that the signal-delay times vary from one instant to the next.

Another option would be to use standard UART protocol. This, however, still requires multiplexing the signal with an EPLD or FPGA.

A new protocol was developed for this project. This protocol is much simpler than a standard UART protocol and is very reliable (this protocol is explained in the software section). The delay times are always fixed. Even though the delay is fixed, another major difficulty remains. Serial transmission and interpretation of data take time. In this design all information of the states of 90 switches may be sent via a 16 bit string. This serial transmission over a 1Mbaud optical serial link would take 70µs. This is almost a 2° delay on a 50 Hz signal. More delay would be introduced through the DSP, analogue to digital converters, and filters. The total delay would then be around 10°. Due to this a special dip detection algorithm is required that determines all the properties of the dip at the dip's start. So initially there would be a delay on the dip compensation, but as the dip properties remain constant, the dip compensator's phase stays as desired and would not be delayed at all.

This is in contrast to a simple non-daisy chained system. Here the desired output signal may just be subtracted from the actual and as a result would deliver the compensation voltage. However, this requires instantaneous response from the switches. In serial gate signal transmission this is difficult.

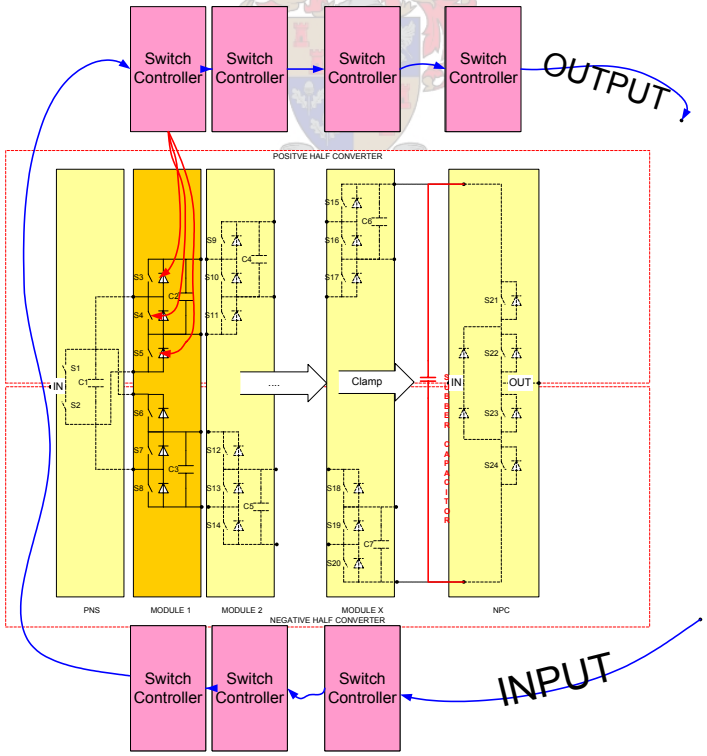


Figure 4-34 Daisy chaining HV modules.

In designing the daisy chain system two major possibilities exist. Either all intelligence and switch control is done on the controller board, or the switch control is done by the PLD needed for serial communication. In the first event the switch signals to each switch would be sent in advance to overcome the delay. In the latter case the controller only determines the dip properties, which are phase and magnitude of the compensation signal. This signal is then sent to the PLD and only there is it interpreted into gate signals.

The second case has the advantage that a safe switching method can be easily implemented to ensure that two complementing switches are not turned on at the same time through the inverter. This may be important in an error event. When all legal switch states are stored inside the receiving PLD, the probability of an error may be reduced. This, however, requires more logic power as all legal switch states need to be pre-programmed into the device.

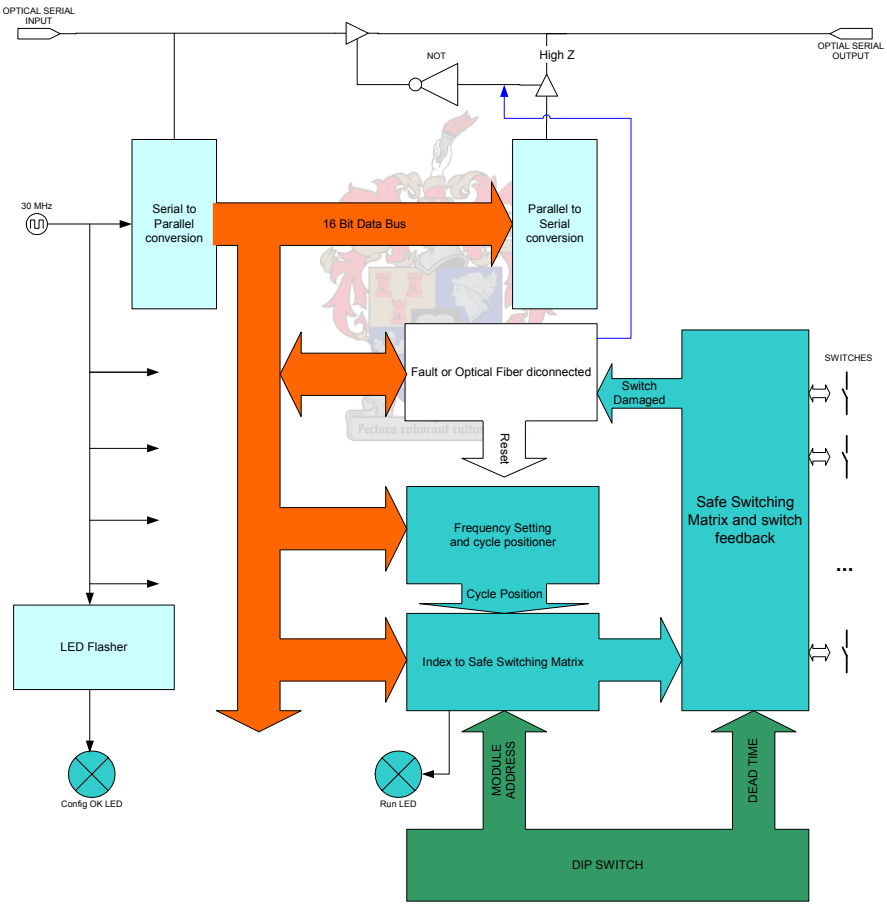


Figure 4-35 Block diagram of serial to switch multiplexing

For the purpose of this study the latter option was taken. A complete matrix of all possible switch states is stored inside. Each row resembles a complete switch state across the whole inverter. Each

new column is a new state at a different instant in a cycle. Another algorithm converts the information from a counter into an index. The index gives the column number of the switch matrix. The counter is also connected to the data bus inside the FPGA. Advantages anticipated through this are that line frequency and compensation phase may also be sent through the serial optical link.

The software design of this switch multiplexer will be discussed further in the software and firmware section of this report.

4.4.6 **Protection**

Anti-parallel thyristors will only switch on during a fault or over-current. Otherwise all current is carried through neutral point clamp. This is how this project differs from the previous dip compensator developed at the University of Stellenbosch. In an over-current event the inverter will switch to zero voltage conduction (both middle switches of the neutral point clamp will switch on) before the thyristors are fired a split second later. The over-current will be conducted through the thyristors for the period before the breaker opens. The system must then restart. On start-up the thyristors are switched off again.

The output voltage of the MMLI is constantly monitored to grant added protection. When the output voltage falls below allowable limits, one of two things could have occurred: too much current is drawn from the inverter, causing voltage balancing to improperly function, or MOSFET failure inside the inverter caused improper output voltage.

Along with the output voltage of the inverter, the ultracapacitor's voltage is measured with high precision. According to [51], the ultracapacitor is insensitive to short-circuits or pulsed currents; however, an over-voltage will quickly cause permanent damage. As the ultracapacitor is charged up to 40V and its maximum allowed voltage is 42V, little slack is left for voltage swells on the capacitor. In addition to that, the compensator is designed to compensate for swells as well as for dips. During a voltage swell the ultracapacitor voltage is allowed to rise up to 42V. Thereafter an error condition is launched where the swell compensation is terminated and the compensator proceeds by discharging the ultracapacitor to 40V by using the reverse charging mechanisms suggested in paragraph 4.5.6. The user is informed of the above actions via the LCD.

4.4.6.1 Fault current detection

A LEM current probe is connected directly into the line. The probe reading is fed separately to a comparator and the controller board. The current waveform is required by the controller board for ultracapacitor charging, harmonic filtering, power-factor correction and additional over-current protection. The comparator simply triggers a turn-off switch to the NPC. On an over-current event the DSP is not necessarily involved in handling the over-currents as this might delay the operation. An automatic shutdown is triggered after which the controller is informed of the occurrence. The controller then shuts down the MMLI. The user is informed of this action via the LCD.

4.4.6.2 Start-up and shut-down procedures

The system startup requires knowledge of the individual capacitor voltages before closing any switches that might cause large balancing currents to occur. As the individual modular voltages are not monitored, the only way to know the capacitor voltages is to zero them first. This is done by individually switching on module stacks to full potential voltage (serial alignment of all capacitors) and then adding a dump load across. After the dump load has been connected for some time, the inverter is activated and controlled ultracapacitor charging may follow.

Shutting the inverter down is rather tricky. When all switches are suddenly opened, the internal inverter diodes act as a rectifier charging the modules to destruction. Thus on shut-down the NPC or the thyristors must still carry the line current. Only after load disconnection may the inverter's power be taken off.

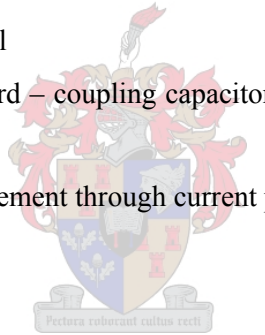
In a pure serial compensation device without any shunt connected power supplies, this rectifying property may prove very useful. The power that is involuntarily redirected into the inverter from the line can charge up the modules. This can proceed uncontrolled until the last module reaches a voltage sufficiently large to power the controller boards. Then active controlled recharging may follow up to rated voltage. The influence of this uncontrolled charging on startup is negligible as this will reduce the line voltage on the load by less than 10 V. This is all that is required until the controller switches in.

4.4.7 Voltage and current measurement for the controller

A high-voltage measurement board was designed to be used with the PEC 33 controller [55] board. It is designed for minimum noise and low cost. It fits directly onto the controller board thus eliminating long conductors introducing more noise. It has several adjustment taps including common mode rejection and gain control for each of the eight channels and reference offset control. The PEC 33 uses a reference voltage generator that sets the maximum voltage for 10-bit resolution on the analog to digital converters. The board has shotkey diodes protecting the sensitive analog–digital converters on the controller board.

In short, the specifications for one voltage measurement board are:

- ± 5V supply with supply voltage noise filter (250 mW power consumption)
- ± 1kV input measurement range
- 8 channels per board (compatible connectors for interfacing with the PEC 33 controller)
- Common mode rejection adjusters on each channel
- Gain adjusters on each channel
- Reference adjustment per board – coupling capacitors on each channel reference to prevent noise pickup.
- Modifiable for current measurement through current probes
- Low cost.



4.5 Software and firmware design

4.5.1 Overview

Several innovative techniques for multilevel inverter control have been introduced in recent years. Some of these conform closely to the control applicable in this design [14, 17]. One of these papers discusses series reactive current compensation [14]. This paper introduces two important design building blocks that are also used during this design. The one is the control strategy introduced in Figure 1-3 and Figure 4-16 and the other giving insight into the VAR compensator function of this design. Another paper gets close to the actual balancing control strategy implemented in this design [19]. Most of the papers on multilevel inverters discuss control principles in steady state or close to steady state. Most dips are transient phenomena that can change continually in depth. These control strategies may be combined with dip detection methods introduced by Fitzer and Mutschler [60, 61] to serve as a suitable method of control for this application.

The requirements for control of the Marxian MLI with a serial switch chain are as follows:

- Fast response in small voltage steps that adapt quickly to changing circumstances. This can be achieved, because there are no delays introduced by large filter components. The low switching frequency makes the control relatively simple. The transitions within a cycle are few in comparison with fast switching multilevel inverters;
- Power dissipation sharing across all inverter modules is necessary for sufficient voltage balancing. The control must ensure that modules deliver approximately same power;

This paragraph will discuss the control principles used in this design. Paragraph 4.5.2 will give a general overview, paragraph 4.5.3 will elaborate on the usage of the phase shift method presented in [14] and paragraph 4.5.4 will debate the need for accurate dip detection in any system operating on a switch chain. Paragraph 4.5.5 will go into the detail of the design of such a switch chain. The last paragraph in this chapter will introduce a software charging strategy for the ultracapacitor. This eliminates the need of a separate capacitor charger.

4.5.2 Control principles

To give a general overview of principles and techniques used to control this system for single phase dip compensation Figure 4-36 shows a functional block diagram of all the software elements. The measured voltages and currents are sampled at 12.8 kHz (256 samples per cycle at 50Hz).

The control is designed to operate the inverter in different modes. The principal modes are described below:

Start-up mode: In this mode the inverter must be made ready for compensation. This involves balancing and charging all capacitor voltages. After start-up each module may have a different voltage. To engage balancing or charging now would damage the switches. Thus all modules must be discharged first. This is done by closing the middle switches of the positive half and then adding a discharge resistance across the snubber capacitor shown in Figure 4-31. After all capacitors in the positive half are discharged (including the ultracapacitor), the same discharging has to be done to the negative half compensator. The positive and negative compensators may not be discharged at the same time, as this might surpass neutral point clamp voltage ratings. Before engaging to a different mode, the capacitors are charged and line frequency is sent to the switch controllers. It is assumed that the line frequency does not vary dramatically during operation. In the event that the thyristors

have not yet disengaged from conduction state, the capacitors will not charge and the inverter may not be switched into a different mode. In this event a shutdown and re-start must commence.

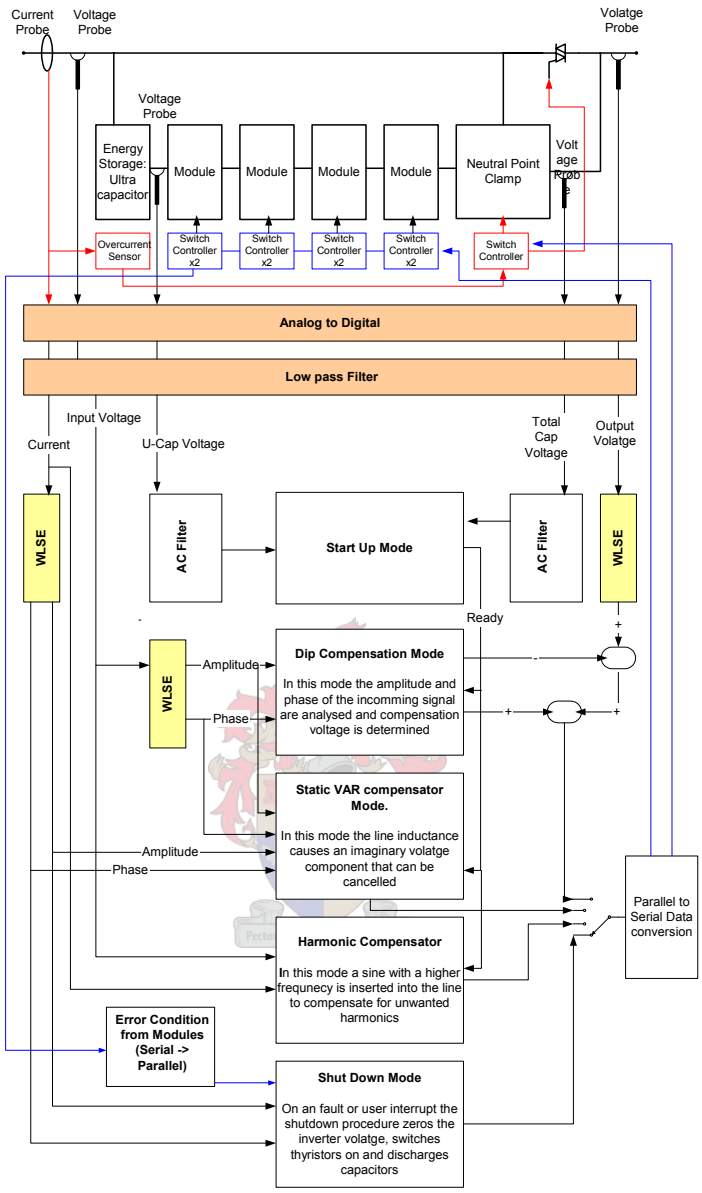


Figure 4-36 Block diagram of the control of the multilevel inverter with a serial switch chain (only one phase shown in diagram).

Dip compensation mode: In this mode the amplitude and phase are interpreted coming from the WLSE (Weighted Least Squares Estimation) blocks (Paragraph 4.5.4.2). These amplitude and phase values are updated very quickly on dip occasion and thus simplify the calculation of the compensation voltage to be injected. During a dip event the calculated compensation data are transmitted serially to the switch controller. This delays the dip compensation by another 70 µs. The greatest delay is introduced by the A/Ds, input filters and DSP calculation times. After a dip occurs,

the delay time is expected to be 500 µs before compensation is started. Each time the characteristics of the dip change, the new calculated compensation data are transmitted immediately. Otherwise at each cycle start the compensation data is resent, to make sure that the switch control modules are still synchronized.

VAR compensation mode: In this mode the user may specify that an imaginary voltage component caused by the line inductance, for example, can be reduced by inserting an imaginary opposing voltage into the line. The principle originates from [14]. Ideally no real power is drawn or released from the converter in this mode.

Harmonic compensation mode: This mode is dedicated to enhance the current quality drawn from the supply as non-linear loads like computers would lower the current quality. The leading harmonics are detected with the help of a fast Fourier transform. The user must then dictate which harmonic should be compensated for. Only one harmonic can be compensated for at a time. (For example: Only 3rd harmonic can be reduced by 15% for loads such as computers.)

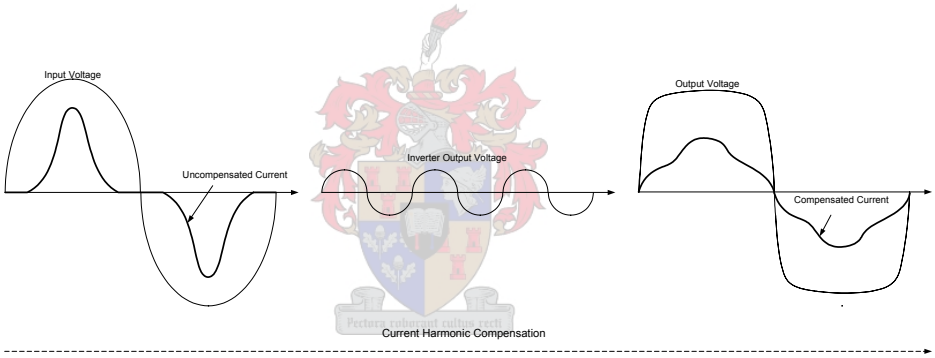


Figure 4-37 Current harmonics compensation – ove- exemplified in this figure

Over-current protection mode: The inverter cannot be switched manually into this mode. This mode is called an over-current event. The current is picked up by a LEM current probe. Its signal is then sent to a comparator circuit (paragraph 4.4.6.1 on fault current detection) as well as to the controller board. When an over-current is detected, the inverter voltage is zeroed. After this the bypass thyristors are fired to handle the over-currents (the thyristors are shown in Figure 4-2 to Figure 4-6). This is done without the help of the controller board as its response might be too slow. Then the inverter is put into shut-down mode by the controller.

Shut-down mode: In shut-down mode the same procedure is followed as in a fault or over-current event. Here the controller is in full command of the thyristors and other switches. The difference to

over-current protection mode is that all modules are also discharged here. This mode can be activated by the user.

It is clear that a system like this would be most easily attainable with digital control. Analog control was not considered. No detailed study of different controllers is included in this thesis. The Power Electronics Group has designed and manufactured some outstanding digital controllers specialized for controlling complex inverters. The latest and most advanced model developed is the PEC 33 [55] controller board. It was chosen for this project because of its versatility and high performance.

The sampling frequency of the analog to digital converters was chosen to be 12.8 kHz. This gives an 8-bit resolution on a cycle at 50Hz. This is partly beneficial as 8 of the 16 bits transmitted via the optical serial link hold information on the cycle location. The other 8 bits hold information about various controller modes. Although not deliberately chosen systematically for this reason, it gives a good tradeoff between the processing power of the PEC33 and the desired infinite sample frequency. The PEC33 is capable of sampling at 25 kHz across all 32 channels. This means that at a sample rate of 12.8 kHz, when reading the present sample from the A/D, the new sample will be readily available in the next sample period after giving the sample command. The delay introduced through this is 78µs. Another sample period is given to complete the calculations. This includes the WLSE and the different mode blocks, thus allowing for a total of 5859 instruction cycles for all functions that need to be completed at the end of the sampling period. Only about 3000 cycles are required. Choosing a higher sampling rate would possibly reduce the allowable instruction cycles too much.

4.5.3 Power dissipation sharing

It needs to be verified whether the balancing technique suggested in Figure 1-3 and Figure 4-16 is optimal for the use in the MMLI. The upper diagram in Figure 4-38 shows how the output waveform can be generated by simply switching the steps on or off by comparing the required output voltage amplitude to the level at which a step may be switched on or off.

The module closest to the energy source is chosen to be closest to the zero voltage axes. This way the modules with the lowest number rank need to deliver most energy. It may prove better to draw most energy from the module closest to the energy source (ultracapacitor), thus using a simpler control technique. The different techniques are shown again for comparison in Figure 4-38. In the middle of Figure 4-38, where capacitor sharing control is implemented, the control approximately equals the operating time across all modules. This ensures that modules are discharged about

equally. The balancing current is expected to be kept lowest as all modules should have roughly the same voltage when they are connected in parallel.

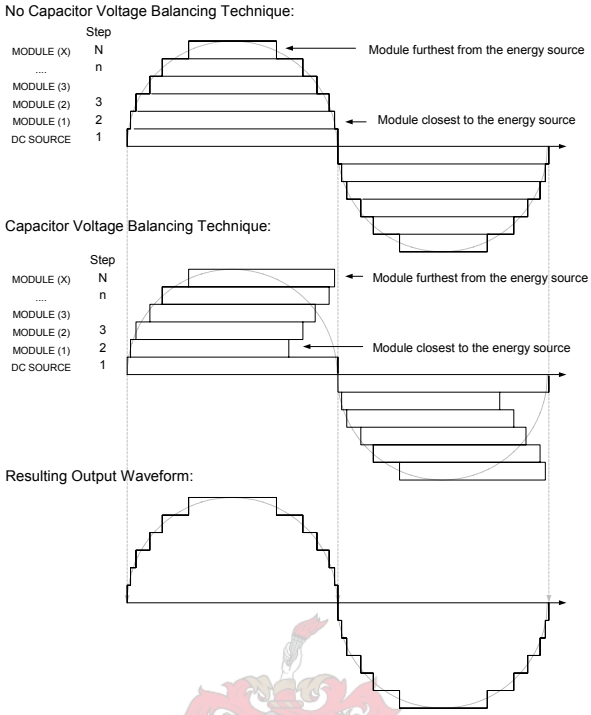


Figure 4-38 Two possible control techniques compared (normal and capacitor balancing respectively)

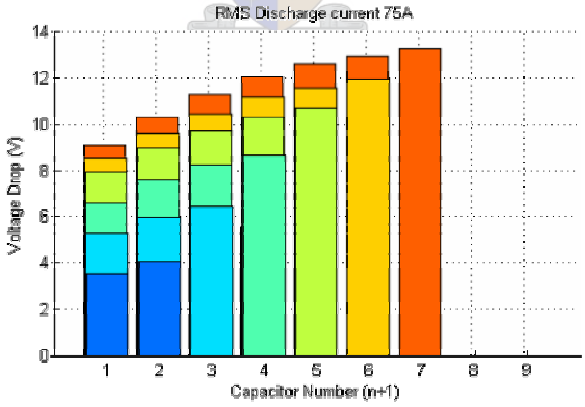


Figure 4-39 Voltage drop experienced with normal control technique

Simulations have been done with these two techniques to show their balancing capabilities. The results these simulations give are represented in the same manner that the results from paragraph 4.4.3.2 are displayed. Here the voltage drop $\Delta V_{C_{(n-1)}(i)}$ is plotted for different n and N values (n is

the module at step = n and N is the total number of steps the inverter can output). (Simulations are done with Simplorer on full-scale circuit with a 75A (RMS) resistive load.)

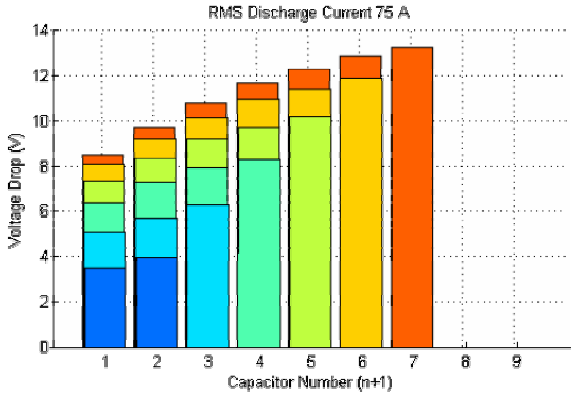


Figure 4-40 Voltage drop experienced with capacitor balancing control technique

It can be seen from this figure is that the advanced control technique for module usage improves the balancing slightly. This can be seen by comparing the voltage drop experienced by the last module in a five-step inverter (Capacitor #4) for example. The voltage drop experienced with capacitor balancing control is about 8V. Without balancing control the voltage drop is almost 9V. This is due to the reduced period the energy source is connected to the MMLI.

4.5.4 Need for accurate dip detection

Accurate function of such a device is essential, because more damage may be caused to subsequent devices if the function of a dip compensator is unreliable than is currently experienced without. Low power quality and voltage spikes could trigger the device due to compensator failure to distinguish proper dips. Therefore initiation of dip compensation must only be triggered by a dip that can cause shutdown.

One way to make the system more resistant to non-dip fluctuations is by low-pass filtering of the input signal. A more refined signal with less noise is thus analyzed by the dip detection algorithm. The algorithm itself must still be robust and immune to harmonics and other power-quality issues.

However, a filter introduces a delay. Yet another delay is introduced by the serial switch chain. In total the delay was measured to be around 10 degrees on a 50 Hz signal or 500 µs. With a delay of this magnitude it would be almost impossible to succeed in dip detection by simply comparing the

input signal to a reference. Each time the difference between the two dictates that another level must be inserted by the MLI, it would take 500 µs to respond. By that time the added level might not be necessary any longer.

A way needs to be found to instantly determine what the signal's new phase and amplitude are and send this data to the switch controller. The switch controller will then have the MLI insert a sine wave moulded for the specifications, which are the amplitude and phase of the compensation signal. The switch controller can then be updated on demand without causing the signal to lag.

A lot of dip detection strategies have been explored in previous work mentioned in paragraph 1.2. These will not be repeated here, but rather an addition to the newer methods is introduced. One of these methods anticipates all the advantages of other dip detection methods without using a lot of controller memory or a long processing time. The best processing time so far was introduced by the ¼ cycle method [4]. This method requires a ¼ cycle to accurately determine the dip's properties. Also samples of the last ¼ cycle need to be stored in the memory. This method was tested again in the 1 kVA prototype Marxian MLI developed for this project. The method proved very good for detecting the amplitude but not the phase.

(All dip detection algorithms are simulated in MATLAB. This software package allows the simulation of many complex and iterative algorithms later implemented into the DSP. MATLAB is widely used at the University of Stellenbosch.)

4.5.4.1 **Numerical matrix sag detection method**

A numerical dip detection method [61] has been developed that, unlike the previous methods, has small time latency when implemented and returns results that are directly interpretable. The method is applied to each supply phase independently and as such can monitor the start or end of a dip, dip depth and any phase jump. The method involves sampling the supply and storing the data in a matrix format.

Provided bands of dominant supply frequency components are known, a set of equations can be developed. Here $V_{present}$ is the present voltage sample, $V_{past1\text{-}3}$ are the past voltage samples and ω_1 is the radial line frequency, $\omega 5$ is the fifth's harmonic frequency. The line signals phase is $ø_1$, and the fifth harmonics phase is $ø_5$.

$$V_{(present)} = |V_1|\cos(\omega_1 t + \phi_1) + |V_5|\cos(\omega_5 t + \phi_5) \quad (4\text{-}37)$$

$$V_{(past-1)} = |V_1|\cos(\omega_1 t - \omega_1 T + \phi_1) + |V_5|\cos(\omega_5 t - \omega_5 T + \phi_5) \quad (4\text{-}38)$$

$$V_{(past-2)} = |V_1|\cos(\omega_1 t - 2\omega_1 T + \phi_1) + |V_5|\cos(\omega_5 t - 2\omega_5 T + \phi_5) \quad (4\text{-}39)$$

$$V_{(past-3)} = |V_1|\cos(\omega_1 t - 3\omega_1 T + \phi_1) + |V_5|\cos(\omega_5 t - 3\omega_5 T + \phi_5) \quad (4\text{-}40)$$

If dominant harmonics are not included in the equations, the solution can contain errors, with the size of the errors referred to as the 'sensitivity of the matrix to unknown harmonics'. Typically the sensitivity of the matrix increases for a given sampling rate with the order of the unknown harmonics, for example, a small amount of 20th harmonic may give the same errors as a large amount of 5th harmonic.

Expanding and re-arranging equation (4-37) to equation (4-40) into a standard matrix format, with equations (4-41) and (4-42) decomposing the frequency components into pairs of solvable simultaneous equations, effectively converts the problem into a more readily analyzable "state-space".

$$\begin{bmatrix} V\sup plypresent \\ V\sup plypast1 \\ V\sup plypast2 \\ V\sup plypast3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ \cos w_1 T & \sin w_1 T & \cos w_5 T & \sin w_5 T \\ \cos 2w_1 T & \sin 2w_1 T & \cos 2w_5 T & \sin 2w_5 T \\ \cos 3w_1 T & \sin 3w_1 T & \cos 3w_5 T & \sin 3w_5 T \end{bmatrix} \begin{bmatrix} |V_1|\cos\phi_1 \\ |V_1|\sin\phi_1 \\ |V_5|\cos\phi_5 \\ |V_5|\sin\phi_5 \end{bmatrix} \quad (4\text{-}41)$$

$$\begin{bmatrix} u \\ v \\ w \\ x \end{bmatrix} = \begin{bmatrix} |V_1|\cos\phi_1 \\ |V_1|\sin\phi_1 \\ |V_5|\cos\phi_5 \\ |V_5|\sin\phi_5 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ \cos w_1 T & \sin w_1 T & \cos w_5 T & \sin w_5 T \\ \cos 2w_1 T & \sin 2w_1 T & \cos 2w_5 T & \sin 2w_5 T \\ \cos 3w_1 T & \sin 3w_1 T & \cos 3w_5 T & \sin 3w_5 T \end{bmatrix}^{-1} \begin{bmatrix} V_{\sup\, plypresent} \\ V_{\sup\, plypast1} \\ V_{\sup\, plypast2} \\ V_{\sup\, plypast3} \end{bmatrix} \quad (4\text{-}42)$$

As the sampling period T, the angular frequencies w_1 and w_5 are known the inverse of matrix 'A' and the variables x, w, v, u can be evaluated. The magnitude and phase of each harmonic component included in the matrix can now be found. The ability of this method to decouple the individual frequency components in the supply is a key feature when the strong voltage harmonics are present.

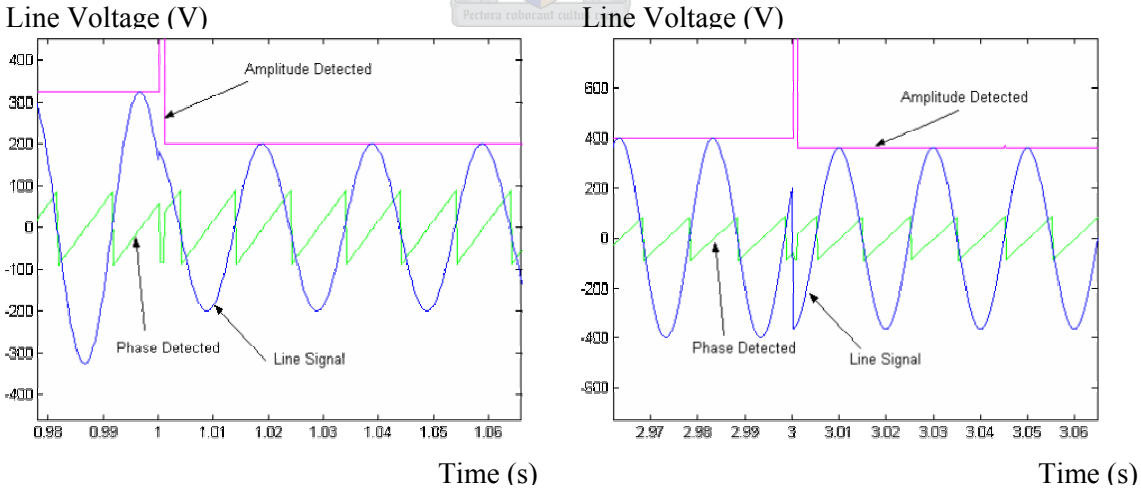
To give an indication of the speed and precision of this method a few simulation results are shown below. Figure 4-41 shows the response to a dip on a pure 50Hz signal without noise and only little 5th harmonic.

Advantages projected with this method are:

- Fast response time. At a 5 kHz sampling rate the accurate signal properties may be known after only 2 ms;
- The harmonic components may be easily determined as well:
- May be used on single- and three-phase systems.

Disadvantages:

- A small amount of Gaussian noise may perturb the measurements greatly;
- As all know harmonics have to be included, the number of calculations needs to increase exponentially with sampling frequency.



38% Dip, 40° shift.

10% Dip, 120° phase shift.

Figure 4-41 Matlab simulation results of matrix dip detection method

4.5.4.2 **Weighted least squares estimation algorithm**

The method introduced here is based on a paper published in 2002 [60]. This work proposes a very fast and robust phase angle estimation algorithm that operates well even under transient conditions. Ultimately this is what is desirable in dip detection algorithms. As a side product the algorithm returns amplitude and frequency of the line signal.

In this paragraph the phase angle estimator for a single-phase system is developed based on the weighted least squares estimation (WLSE) method [60, 62]. A frequency estimation algorithm is also used [60] to track the line frequency. The ideal single phase line voltage is given by [60]:

$$E_s(t) = \overline{E}\cos(\omega t + \phi) = E_d \cos\omega t - E_q \sin\omega t \qquad (4\text{-}43)$$

where $\overline{E}$ is the voltage amplitude, ω is the angular frequency; ø is the phase angle, t is the time, $E_d = \overline{E}\cos\phi$ and $E_q = \overline{E}\sin\phi$. E_d, E_q and ø are constant under steady state [60].

Equation (4-43) can be expressed in matrix format [60]:

$$y(t_i) = \mathrm{H}(t_i)x(t_i) \qquad (4\text{-}44)$$

where $\mathrm{H}(t_i)$ is:

$$\mathrm{H}(t_i) = \begin{bmatrix}\cos\omega t_i & -\sin\omega t_i\end{bmatrix} \qquad (4\text{-}45)$$

$$x(t_i) = \begin{bmatrix}Ed(t_i) & Eq(t_i)\end{bmatrix} \qquad (4\text{-}46)$$

$$y(t_i) = E_s(t_i) \qquad (4\text{-}47)$$

The cost function is given as:

$$J\left[x(t_i)\right] = \sum_{j=0}^{i} \lambda^{i-j}\left(y(t_i) - \mathrm{H}(t_j)\hat{x}(t_j)\right)^2 \qquad (4\text{-}48)$$

Where $\hat{x}(t_j)$ is the estimated value for the actual $x(t_i)$ that satisfies equation (4-44).

Now the challenge lies in minimizing this cost function by minimizing $y(t_i) - \mathrm{H}(t_j)\hat{x}(t_j)$. According to [60] λ E (0, 1) is the forgetting factor chosen to be 0.99 from the application example [60]. The solution $\hat{x}(t_j)$ that minimizes the cost function is obtained from the least squares algorithm [60]:

$$\hat{x}(t_j) = \hat{x}(t_{j-1}) + \mathrm{K}(t_i)\left(y(t_i) - \mathrm{H}(t_i)\hat{x}(t_{j-1})\right) \tag{4-49}$$

$$r(t_j) = 1 + \mathrm{H}(t_i)P(t_{i-1})\mathrm{H}(t_i)^T \tag{4-50}$$

$$\mathrm{K}(t_j) = \mathrm{P}(t_{j-1})\mathrm{H}(t_i)^T r(t_i)^{-1} \tag{4-51}$$

$$\mathrm{P}(t_j) = \lambda^{-1}\mathrm{P}(t_{j-1}) - \lambda^{-1}\mathrm{K}(t_i)\mathrm{H}(t_i)\mathrm{P}(t_{j-1}) \tag{4-52}$$

in which $\hat{x}(t_{-1}) = 0$, $\mathrm{P}(t_{-1}) = \pi_0 * \mathrm{I}$ where $\mathrm{I} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ and $\pi_0 > 0$ is the initial covariance constant. When $\hat{x}(t_j)$ is known, the phase and amplitude can be easily derived from equation (4-44).

The frequency estimator suggested in [60] uses a PI controller to track the frequency by simply integrating the phase difference to zero. When no phase difference occurs after each calculation the selected reference angular frequency ω is said to be selected correctly. This type of control is only stable in steady state and may cause serious disturbance in transient conditions. Thus another factor q is introduced that is reset to a relatively high value in a transient condition. After each sample period q is reduced. Only when q reaches zero may the frequency may be updated. Values for K_p and K_i were directly taken from the application example in [60].

To be useful for this dip compensator application the author suggests slightly modifying the frequency detection mechanism in [60] by adding another feedback path to the frequency detection loop (indicated in red in Figure 4-42). This path allows for phase resetting and converter adjustment in case the dip does not recover to a zero-phase condition. In such an event the converter continues switching for a few seconds slowly adapting the load to the same phase as the source. Little real power is absorbed (see Figure 4-1) in this operation. To prevent any further disturbance or instability the constant K_w was chosen so that the effect of this phase adjustment is much slower than the PI

controller. The PI controller's cut-off frequency is in the order of 1.2 kHz, where the phase adjustment path would generally cause the phase to zero after only about a few seconds.

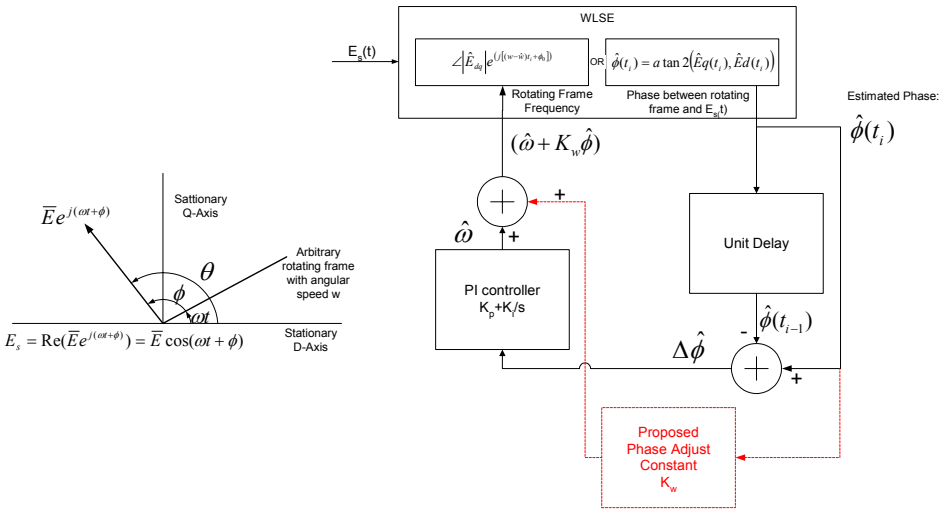


Figure 4-42 Vector diagram of line voltage Es(t), rotating vector and control diagram of angular frequency tracking [60] with additional automated phase adoption.

The working of this added feedback path can be explained very simply. When the estimated phase is non-zero the reference frequency is increased slightly from ideal line frequency till the phase is zero. Thus the reference vector will rotate at slightly faster speed than actual line frequency until it catches up with the actual line signal vector. The approach speed is linear with distance from the designated zero-phase condition.

To show the response of the complete dip detection algorithm a Matlab simulation with all necessary variables has been included to this study (Figure 4-43). A line signal was generated with some fundamental harmonics and some Gaussian noise. This noise is likely to be present under practical conditions as the voltage measuring probes are low-cost, but adequate precision devices. Harmonics might be introduced by the load.

Advantages of the WLSE method:

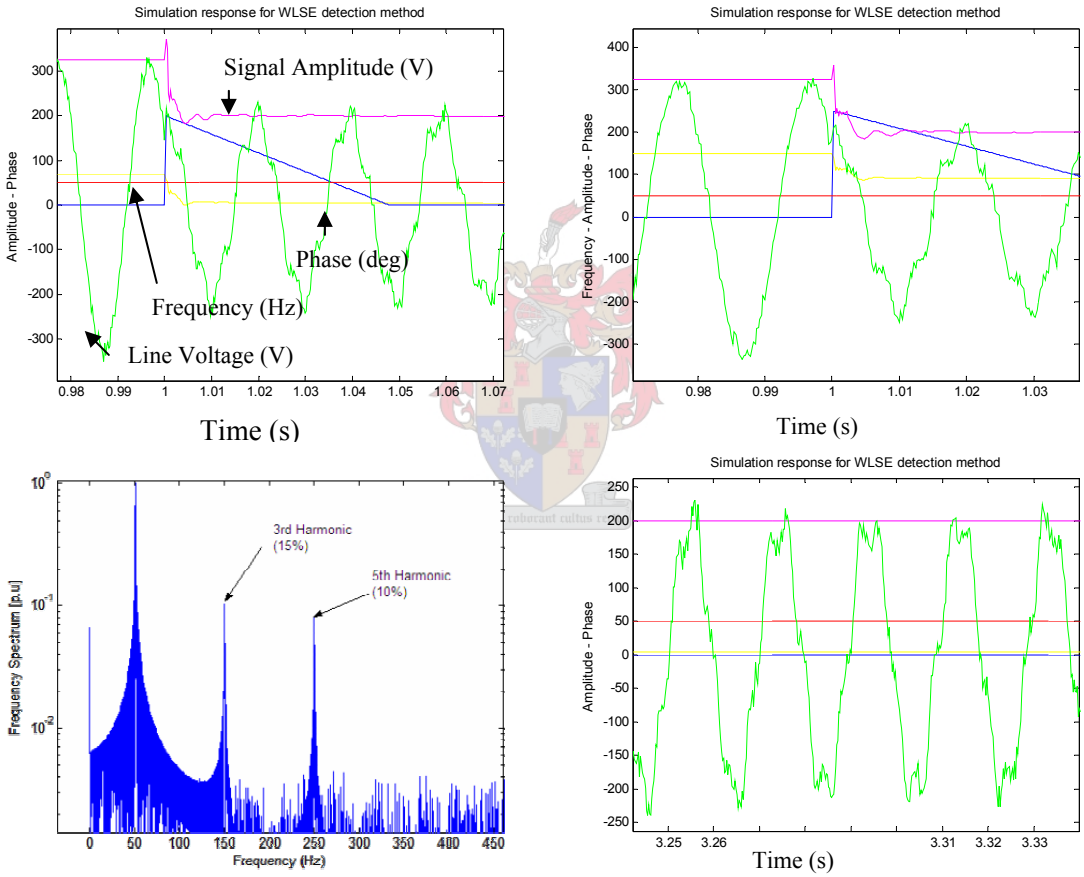
- Fast response time. Within 1 ms detected phase comes close to actual phase. After 3 ms seconds detected phase stabilizes;
- Relatively high distortion component allowed. Method is robust and insensitive to normal grade harmonics;
- Little computational power required. When using a lookup table for the "arctangent" function, the process may be completed in only 91 clock cycles;

- Only 7 float variables need to be stored in memory after sampling.

Disadvantages:

- Too large harmonic components cause unreliable results and total instability;
- Slower that the numerical matrix dip detection method.

For the purpose of this study the WLSE method is adequate because of its ability to function under noise and harmonic conditions. The computational power is also relatively low, making it easy to use on several measured signals in one sample period. Another advantage is that it may be used on single-phase systems as well as three-phase systems.



Top shows response on dip. Bottom left shows frequency spectrum of line signal. Bottom right shows steady state with zero phase.

Figure 4-43 Matlab simulation examples testing the WLSE method.

4.5.5 **Reliable serial switching chain**

This paragraph will discuss the possibility of using a safe switching matrix. The advantage of this safe switching matrix is the exclusion of illegal switch combinations throughout the inverter. By damaging one switch the whole inverter might collapse because too much energy that is stored may be released.

Figure 4-35 shows the firmware implemented into the receiving end PLD. The serial data are directly relayed to the optical transmitter without delay. This means that all daisy chained modules get the same stream at approximately the same time. A 16-bit serial string is decoded onto the data bus in each module. On this string several components are connected. According to contents of the data each block decides if it should use or reject the current bus data. Four blocks read the bus data: The parallel-to-serial encoder, the error feedback block, the frequency and phase adjustment block, and the index block for the switching matrix.

The serial to parallel protocol is based on a Morse code principle. As the sending and receiving end clocks are not synchronized and may run at slightly different speeds, drift may occur during transmission of a serial stream. To overcome this problem Morse code introduces encoding that is reliably understood even though clocks may differ. A zero is simply represented by a long zero pulse, while a digital ‘1’ is represented by a short pulse. The two may easily be distinguished on the receiving end. When no data are transmitted a continuous ‘1’ can be read off the optical fibre. In the event that the optical fibre is unplugged or is faulty a ‘0’ is read for a time span exceeding the maximum allowable ‘0’ transmitting pulse. As a result an error condition is launched and the PLD is reset.

Under normal operation the line frequency is sent to the frequency setting block in the startup procedure. After that another 16-bit string is sent to tell the inverter what amplitude sine and at what phase it should generate it. The disadvantage of using a safe switching matrix is that the types of signal waveforms have to be preprogrammed. In this case only a sine waveform has been programmed into the PLD. Other waveforms may be easily be added later.

Still under normal operation with the internal waveform frequency set, the frequency and phase block dictates the current phase angle (0 to 2π). The index block also reads the data bus for information on amplitude and then combines these elements to generate a row index to the switching matrix.

It should still be mentioned that there are two modes in which the compensator may operate. This is a purely experimental approach and is not necessary for finalizing this project. Mode A makes use of both top and bottom switches in each module half to balance capacitors, while Mode B only uses one switch for balancing. Mode B's operation is not bidirectional. This means that the energy storage cannot be charged from the line. In this mode only 66 switches are used instead of 90 in Mode A for a three-phase converter.

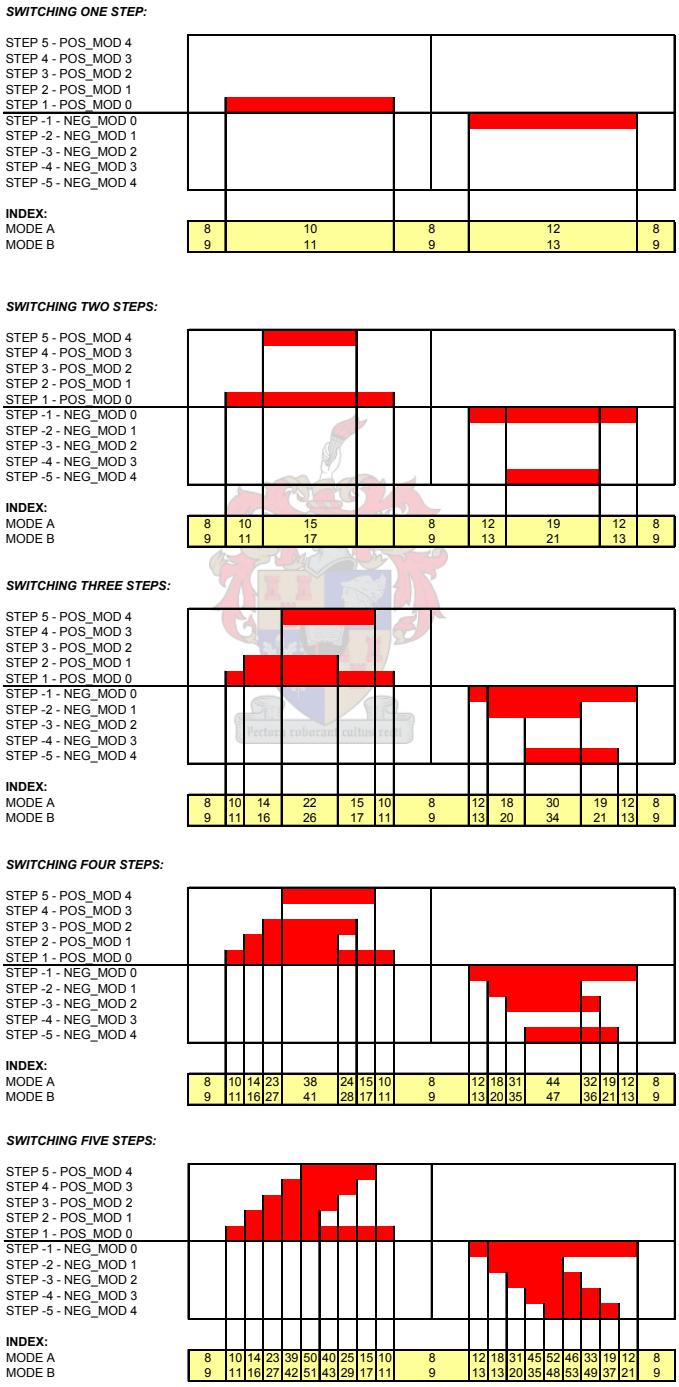


Figure 4-44 Visual explanation of index selection for different compensation levels

The complete safe switching matrix is listed inside Appendix B.

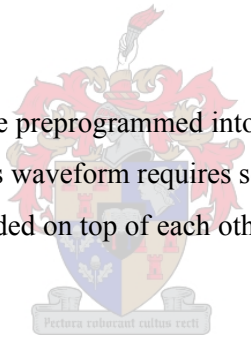
The index (Figure 4-44) is then sent to the safe switching matrix block. Each index refers to a certain row in the switching matrix. Each switch in the inverter has a column holding possible states respective to the row index selected. To implement dead time between switch states the new row pointed to by the index is "AND" gated with the previously selected row for the duration of the dead time. This makes it possible to easily change the dead time on demand. Each modules dead time may thus be set manually with external dip switches.

Advantages of a safe switching matrix stored inside the receiving end PLD:

- No illegal switching states are possible, as all states are manually programmed into the PLD. A valid switching state is stored in one row of a matrix. At any instant in time the switches will have gated according to this row information;
- No phase delay. When the initial compensator information is received the module will always introduce new steps at the precise time required.

Disadvantages:

- The output waveform has to be preprogrammed into the PLD. This requires a lot of memory space as each amplitude of this waveform requires separate memory space;
- No two waveforms may be added on top of each other. This is a drawback, especially during harmonic compensation.



4.5.6 Charging of ultracapacitors

To make a device truly a serial compensation device no shunt connection should exist. This means that all power used by the device should be drawn from the line without making use of a neutral wire or second phase. In high-voltage applications especially this is a matter of concern as special isolation would be required if one were to make use of a shunt driven controlling or charging unit.

It is easy to power up the control circuit once the device is coupled into the line. This is because all switches contain diodes that act as rectifiers when the device is off. Enough power can be taken up initially for 'booting' the control system. More challenging is the charging and balancing of the ultracapacitor without disturbing the line voltage unduly. A small amount of real power needs to be drawn from the device in serial configuration at all times to compensate for the losses inside the

inverter. The topic of the next paragraphs is how to charge the capacitors and keep them charged at all times under different operation modes.

Under pure dip compensator mode the device is not expected to draw any power under non-dip condition. The input voltage and phase must correspond to that of the output. Thus one is forced to introduce something new to the multilevel dip compensator with energy storage concept. As the device is expected to have an equal input and output amplitude under normal conditions, the power can be drawn by introducing a phase shift between input and output signal. To make the user believe he is not being robbed of power, the phase shift could mean something positive (like active VAR compensation, for example).

Active VAR compensation would mean that the inverter tries to cancel the phase shift introduced by the line inductance. The only difference this model would have with this type of active VAR compensation is that the compensation vector would have a slight real power component to it, assuring that the capacitors remain charged at all times.

Another possibility to draw some real power is to offer harmonic compensation on the line current. Normally harmonic compensation does not inject or absorb real power. When the magnitude of the compensation signal is strategically varied over time, however, some real power may be absorbed through this method. This type of compensation would only be minimal, because during a dip occurrence no more harmonic compensation is permitted for the time of the dip. It would still be effective for some computer or non-linear loads. The limiting harmonic compensation can be changed by pre-programming more waveforms into the PLD. (Only a sine wave has been programmed into the PLD for this project.) During a dip the inverter output waveform is a 50Hz sine with as little as possible low-order harmonics. When the user requires maximum harmonic compensation, the dip compensation capabilities of the device are disabled. For less sensitive equipment both dip compensation and harmonic compensation may be enabled.

4.5.6.1 **Normal operation – little power factor compensation**

In this mode the output signals phase is only shifted by the absolute minimum: A fixed 7°. This is done by injecting a voltage in such a way that its output signal leads or lags the line signals phase by roughly ± 90°. By slightly changing this angle, power may be drawn or released from the inverter. The signal injected into the line has 40V amplitude. When no power factor compensation is needed (because the load draws perfect power) the device will introduce a slight imperfection to this power

factor. The only way to prevent this is by introducing a shunt connection to this setup or by using the harmonic compensation mode instead.

The converter is using some of its potential for dip compensation to inject a small voltage vector. When a voltage dip occurs, however, almost all the inverter scores are available in this mode. If the compensator has to insert a vector into the same direction as the vector of the power factor compensation, only 80% of the converter voltage would be available, where in the opposite case 120% would be available. Assuming that the dip introduces no phase shift 99% of the inverter voltage would still be available under dip condition as a result of combined power factor compensation.

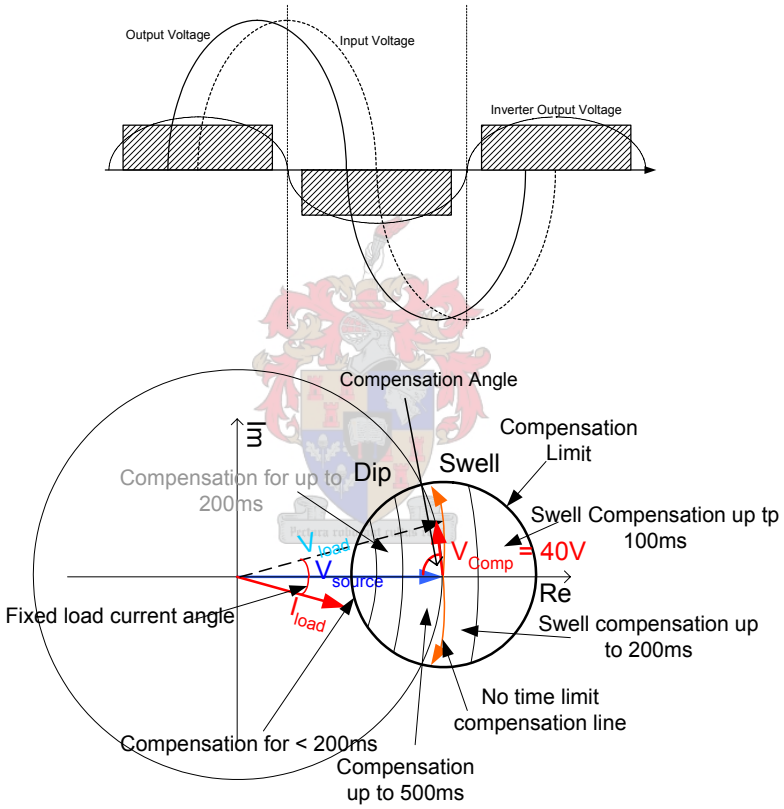


Figure 4-45 Vector diagram showing normal operation with phase shifting the output signal slightly

This mode is optimal for maximum dip compensation capability. The inverter would be able to compensate up to 30% dips with up to 30° phase shift for longer than 200ms.

4.5.6.2 **VAR compensation mode**

VAR compensation mode may be explained most easily with reference to Figure 4-46. The idea originates from [14]. In this the compensator injects a sinusoidal waveform at 50 Hz 90º to the line voltages phase and opposing (180º) the phase shift introduced by a high line inductance. To benefit the powering of the system simultaneously, the vector injected is not purely opposing the line inductance vector, but also introduces a slight real power component. This is done by keeping the input voltage equal to the output voltage and introducing a difference in the magnitude between the load current angle and the source current angle (Figure 4-46). Under pure VAR compensation mode these angles would be the same, as would be required if one needed equal voltage amplitudes on both sides of the inverter.(δ is the phase shift between the input and the output voltages introduced by the compensator. Θ_{load} is the current phase as seen at the load and Θ_{source} is the current phase as seen at the source or input side of the compensator. V_{load} is the load voltage, V_{source} is the source voltage and I_{load} is the load current in Figure 4-46)

In this mode the ability to compensate for dips depends mostly on the level of VAR compensation chosen. If, for example, a vector with a 100V (RMS) amplitude is injected to compensate for a large line inductance, only 28% of the inverters rating is left to compensate in that same direction. This means that a dip with no phase shift may not exceed the inverter boundaries shown in Figure 4-1. For this example it would translate to a maximum dip compensation capability for only up to 25% dipped voltages.

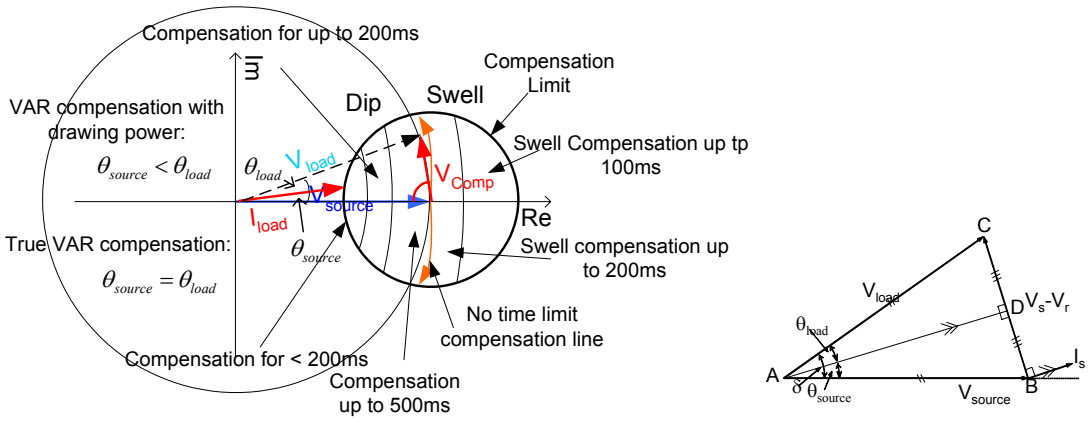


Figure 4-46 Vector diagram showing switching under VAR compensation mode.

During a dip the voltage phase on the load must be maintained to prevent strong over-currents and possible shutdown of equipment.

4.5.6.3 **Harmonics compensation mode**

As it is relatively easy to compensate for load current and source voltage harmonics with a series device, this option is included in the current design. The difficulty with compensating for harmonics with this specific type of inverter lies in the daisy chaining of the switches. Currently a safe switching matrix is used together with the serial switching chain. The working of this safe switching chain dictates that a waveform needs to be pre-programmed into the PLD on the receiving end. In other words the voltage that the series inverter can currently inject into the line has to take the shape of a sinusoid.

When compensating for harmonics only one harmonic element can be reduced or taken out of the frequency spectrum. This is done by detecting the phase and amplitude of that specific harmonic and then inserting an opposing signal into the line. An example of this is a diode rectifier connected onto a single-phase network. It causes a strong 3rd, 5th and 7th harmonic. Finding the properties of one harmonic component the load current may be drastically improved through shaping the load voltage signal so that the load current comes close to a sinusoid.

In the event of a dip the inverter voltage can only compensate for the dip by generating a sinusoidal voltage at line frequency as this means that for the duration of the dip no harmonic compensation can be attempted. This may cause problems to the utility or the load. The user must thus first verify if such disturbance can be tolerated or not. Should such transient behaviour be problematic, the harmonic compensation must be very little or another mode must be selected.

The device draws power in harmonic compensation mode by slightly varying the compensation amplitude with a 50 Hz rate of recurrence. This introduces new high-order harmonics into the line. Thus the recurring compensation amplitude should be minimal. Figure 4-47 visually explains how this is done.

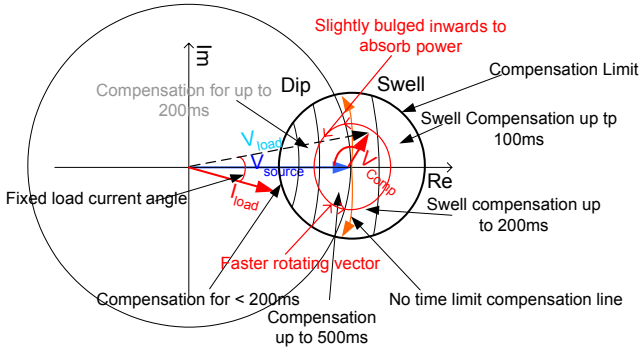


Figure 4-47 Drawing power in harmonic compensation mode

4.6 Summary

This chapter covered the detailed design of the final dip compensator for laboratory evaluation. The dip compensator is built with a Marxian multilevel inverter topology. Voltage balancing and switch control have been the focus on this section. The second half of this chapter goes on to discuss software design and operating principles. The concepts of daisy chaining and accurate signal tracking are dealt with here.

The final step to making a pure serial device would come by removing all the shunt connections. By enabling energy storage charging through power-quality management, the device moves closer to that goal.

5 Results

5.1 Introduction

In this chapter simulation results are compared with practical results. Both were produced on a 50 kVA Marxian multilevel inverter. In paragraph 5.2 simulations are done for various dips with different loads. These same conditions are applied to the practical setup. This chapter concludes with a summary in which the results are discussed.

5.2 Simulated results of the Marxian multilevel inverter

A simulation study was done with the Simplorer simulation package to verify the control techniques for dip compensation with a multilevel inverter developed in the previous chapter. Simulations of dip compensation at dips with different depths and at different load resistances are discussed here.

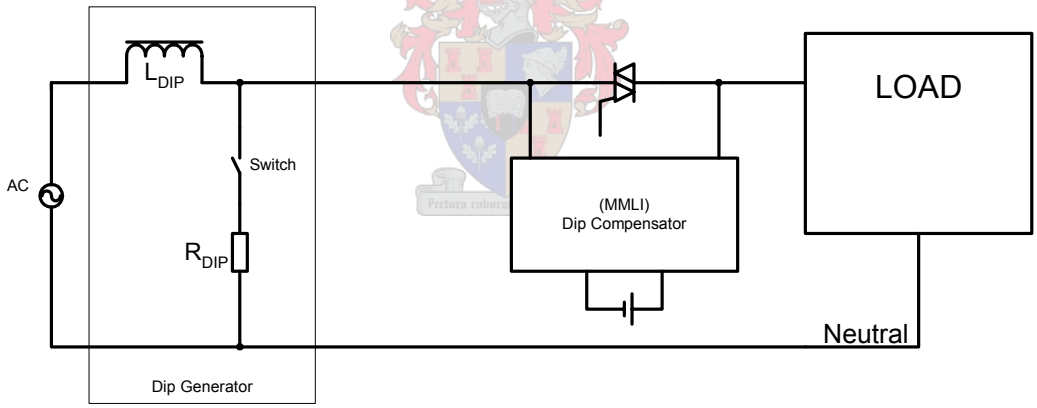


Figure 5-1 Simulation Setup

Parameter	*Value*
Supply Voltage	230 V (RMS)
Line Frequency	50 Hz
Dip Duration	200ms or 10 cycles
Line Inductance (L_{DIP})	400µH, 800µH, 1200µH
Short circuit resistance (R_{DIP})	0.4 Ω
Load Resistance (Line to Neutral)	4.6 Ω, 3.2Ω, 2.5Ω

Table 5-1 Basic parameters for the simulated resistive load tests

The basic simulation setup was done according to Figure 5-1. The parameters used in these simulations are given in Table 5-1. When the switch above R_{DIP} is closed a dip is generated with a certain depth and phase jump depending on the values used for R_{DIP} and L_{DIP}. After 200 ms the switch opens again. This restores the original source voltage.

5.2.1 Simulation of dip compensation

The first simulation is done on a 50A (RMS) resistive load. The values for R_{DIP} and L_{DIP} are 0.4Ω and 1200µH respectively. This will cause a 27% voltage dip with a 43º phase shift on a 50Hz line signal. The simulations are done with all internal resistances and component values also used in the practical setup. The complete circuit as it was designed for theoretically is implemented in the simulations and later built practically in exact proportions.

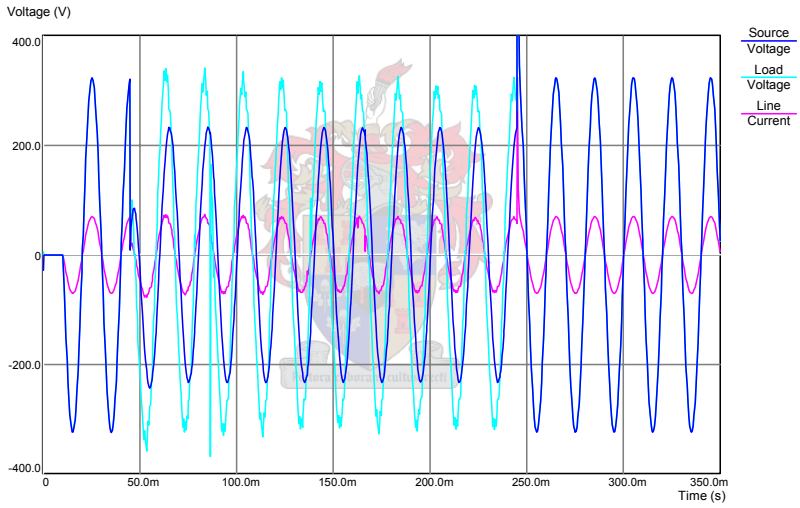


Figure 5-2 Dip compensation on a 27% dip for a 50A resistive load.

Figure 5-2 and Figure 5-3 show the simulated results for a 27% voltage dip. The output voltage remains level at 230V (RMS) while the input voltage dips. The original signal phase is also maintained so that loads like rotating machines do not draw excess current on sudden phase shifts. Figure 5-3 shows that on termination of the dip compensation a voltage spike can be seen on the load's voltage. This is due to the line inductance. The current on the line is very high for the duration of a dip. So after the dip recovers some of that current is quickly released on the load causing the voltage to spike.

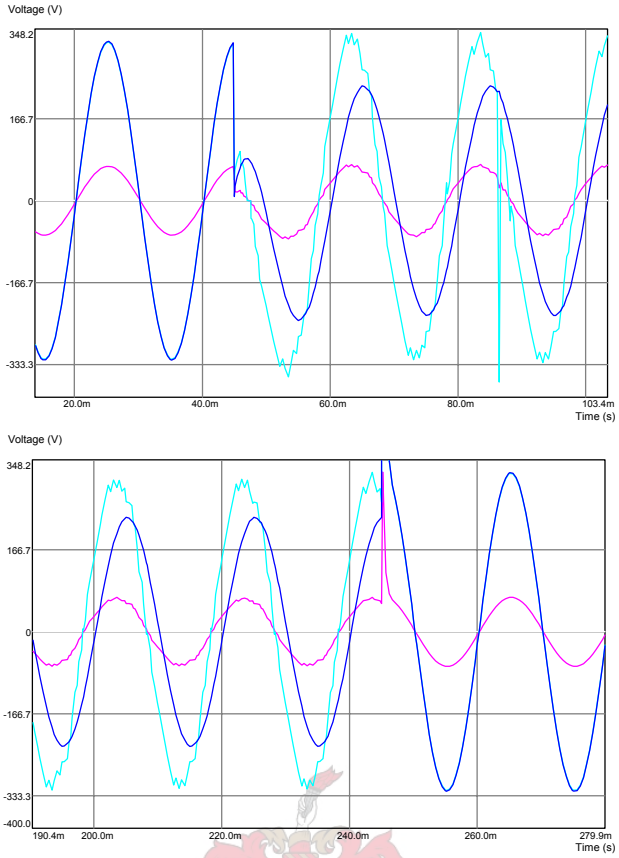


Figure 5-3 Start and stop of the 27% dip with 43° phase jumps on a 50A (RMS)

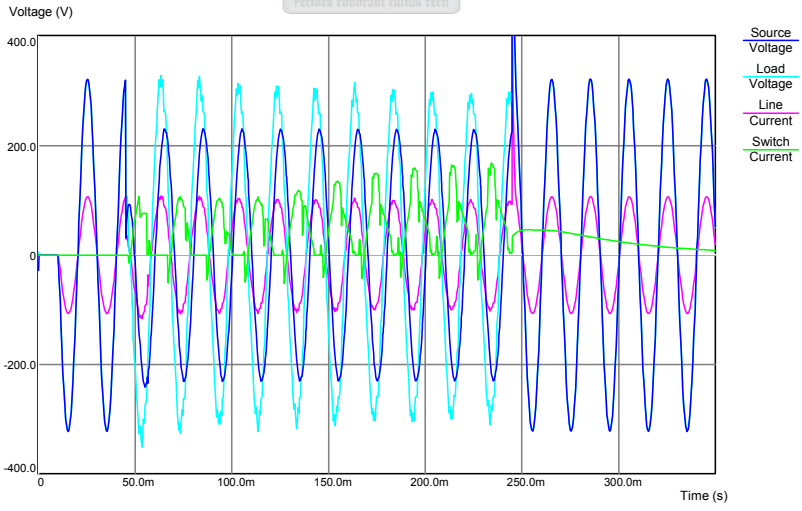


Figure 5-4 Dip compensation on a 27% dip for a 70A resistive load.

The same simulations are done on a 70A (RMS) load. Very similar results are obtained. These are shown in Figure 5-4 and Figure 5-5. Under these load conditions the energy stored in the ultracapacitor are sufficient to maintain the load voltage within limits.

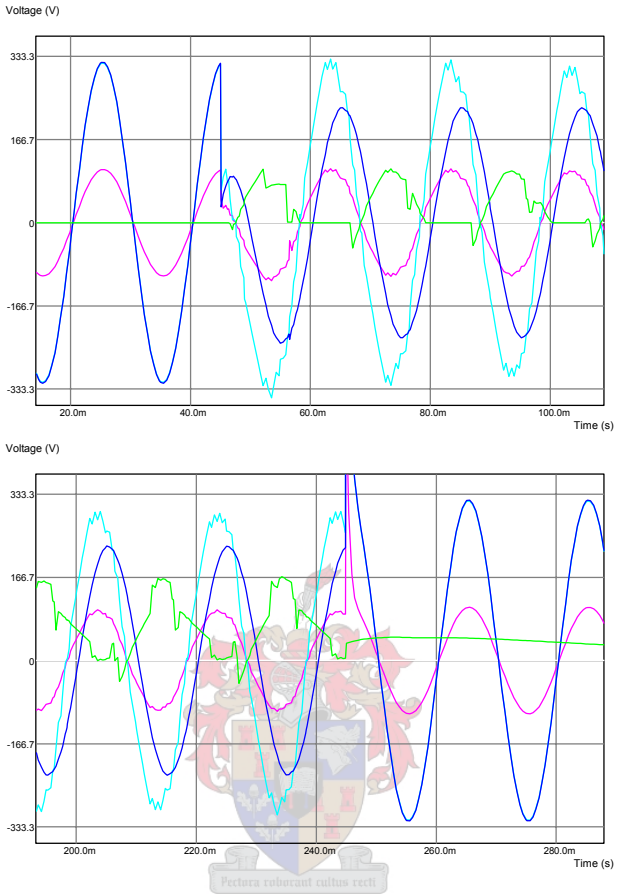


Figure 5-5 Start and stop of the 27% dip with 43° phase jumps on a 70A (RMS)

To verify that the inverter can operate up to its specifications, the load is increased to 90A (RMS). This is more than its rated current of 75A. Even here the load voltage can be maintained throughout the dip. In Figure 5-6 and Figure 5-7 the inverter output voltage is also shown. One can clearly see the voltage drop experienced after some time. This is due to the ultracapacitor discharging and due to the improper balancing of capacitors on the modules. This is as discussed in paragraph 4.4.3.2.

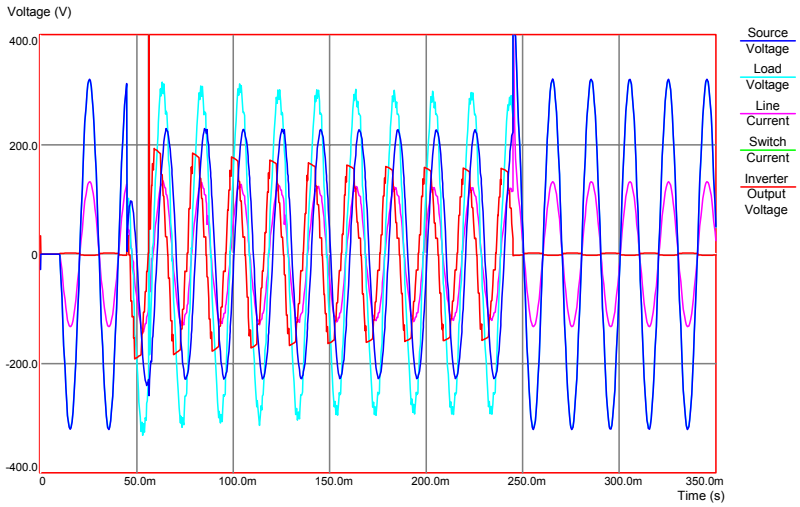


Figure 5-6 Dip compensation on a 27% dip for a 90A resistive load.

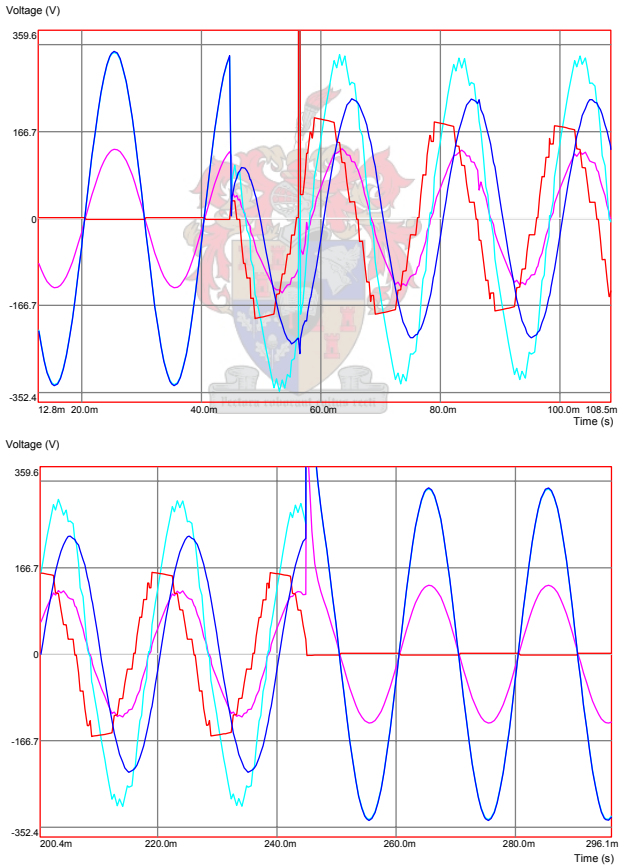


Figure 5-7 Start and stop of the 27% dip with 43° phase jumps on a 90A (RMS)

On the right of Figure 5-7 the inverter's output voltage is much lower in amplitude than it is on the left. After the dip terminates, the inverter's output voltage is zero and the input voltage to the series compensator equals the output voltage.

Different dip conditions are simulated for a 70A (RMS) load. Figure 5-8 shows the response to a 16% voltage dip with a 32º sudden phase jump. As can be seen here the output voltage is once again kept stable for the duration of the dip.

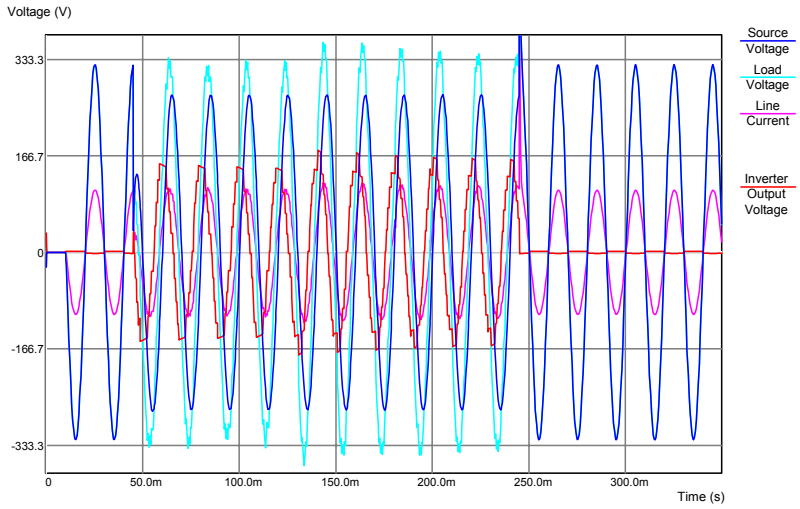


Figure 5-8 Dip compensation on a 16% dip with 32ºphase jump for a 70A resistive load.

Figure 5-9 shows the response to a 6% voltage dip with an 18º phase jump. The source voltage is still within its allowable range; however, an 18º sudden phase jump can be prevented by inserting a small voltage to compensate for that dip.

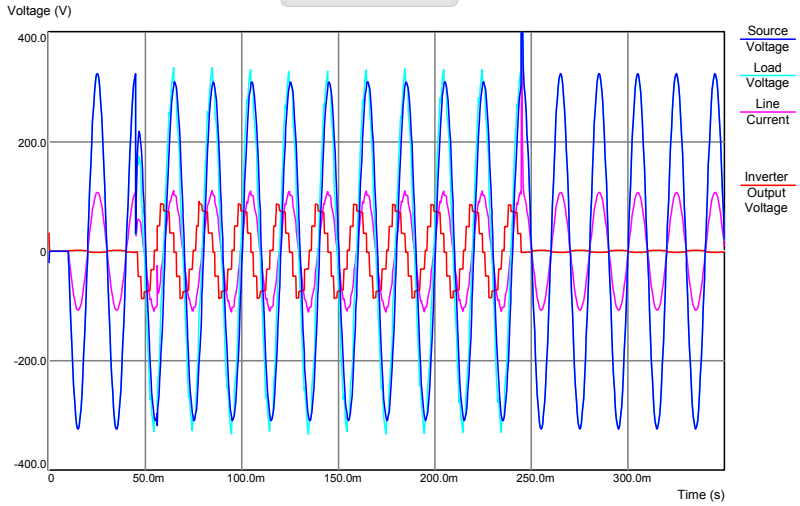


Figure 5-9 Dip compensation on a 16% dip with 32ºphase jump for a 70A resistive load.

The simulations prove that the dip compensator can compensate for dips within its specification range. Dips that fall outside of this specification range are compensated for in the best possible way the inverter can provide.

5.3 Practical results of the Marxian multilevel inverter

The simulation results in the previous section verify the working and theory of the Marxian multilevel inverter for three-phase dip compensation. To verify the theoretical results obtained, a single phase of the 50 kVA inverter was built. The practical results included in this section were taken from testing the single phase of the 50 kVA converter under various dip conditions. This section includes results of the voltage overshoot experienced on the MOSFTEs at turn off. The dip compensation results on resistive loads are represented in almost the same way as the simulations in paragraph 5.2. To conclude, the dip detection control principle is verified by monitoring DSP variables through the digital to analog ports on the PEC 33 controller board.

5.3.1 MOSFET overshoot at turn off

To minimize component ratings the overshoot on transient state from its nominal operating condition should be minimal. This is especially true when a system serves as a prototype for much larger rated successors. The switches inside many power electronic devices are the most sensitive and most difficult to protect against damage caused by transient overshoot. When using a MOSFET switch tiny parasitic inductances on the PCB layout can cause large voltage overshoot when it is switched off.

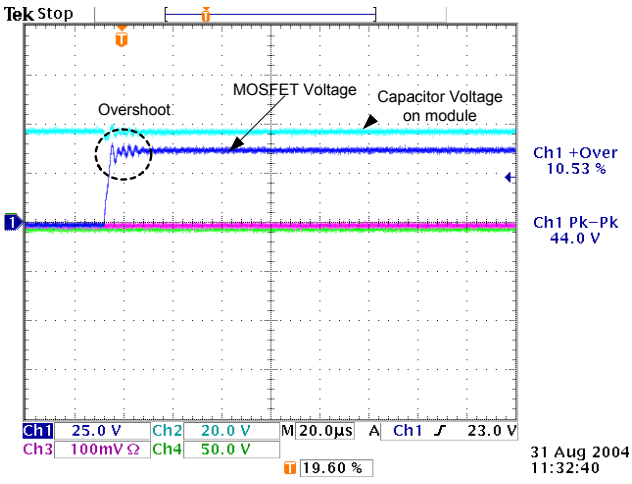


Figure 5-10 Worst overshoot measured on S3 (S3, S5, S6 and S8 carry most current. See Figure 4-2)

To prevent large overshoot in the MMLI the components are placed very close to each other. Each module's PCB's is designed for minimum conductor lengths. Each module has two opposite inverter halves, of which each has only four ports (Two input and two output ports). The PCB has four layers; this means that each port is assigned to one layer, thus eliminating the possibility of lengthy conductors that can cause large stray inductances.

Overshoot was measured on the MOSFETs carrying most current. Other MOSFETS show less overshoot during switching. The load draws a 90A (RMS) current. Measurements were done with a voltage differential probe with a 100 MHz cut-off frequency. As can be seen from Figure 5-10 the overshoot is about 10% for above-specification loads. The rated voltage of the MOSFETs is 75V. At 44V peak voltage (Figure 5-10) there is thus no danger of damaging the switches as a result of voltage overshoot.

5.3.2 Dip compensation with resistive loads

These results were taken for various resistive loads with different load currents. 50A, 70A and 90A loads were tested. This would clearly enssure that resistive loads up to rated current should not cause problems to the dip compensator. The experimental setup, including the dip generator is shown in Figure 5-11. For each load, L_{DIP} and R_{DIP} three identical dips were generated. The worst of the three responses in each case is exemplified here to illustrate the transient responses that may be expected during dip compensation.

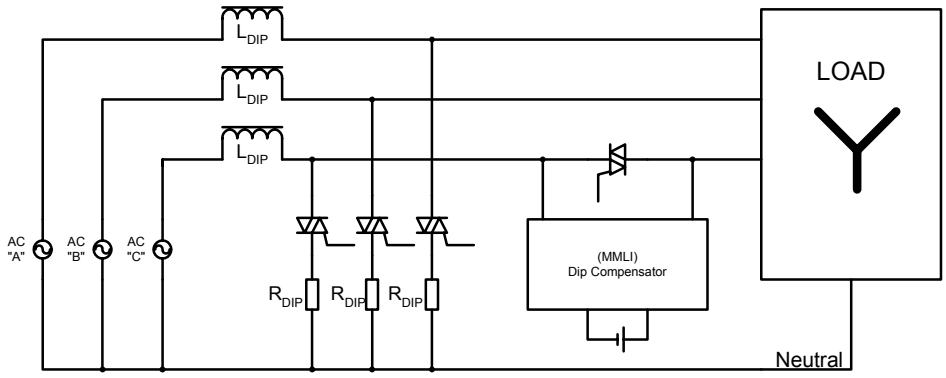


Figure 5-11 Experimental setup for the dip compensation results

The loads and dip settings are listed in Table 5-2.

The first tests were done on a small 50A load on a 27% dip with a 43º phase jump. The line inductance is 1200µH and the short-circuit resistance is 0.4Ω. In this case full potential voltage of the dip compensator is required. 140V (RMS) is injected into the line to compensate for the dip.

Parameter	Value
Supply Voltage	230 V (RMS)
Line Frequency	50 Hz
Dip Duration	200ms or 10 cycles
Line Inductance (L_{DIP})	400µH, 800µH, 1200µH
Short-circuit resistance (R_{DIP})	0.4 Ω
Load Resistance (Line to Neutral)	4.6 Ω, 3.2Ω, 2.5Ω

Table 5-2 Basic parameters for the practical resistive load tests

During all practical measurements CH1 (Channel 1) on the oscilloscope shows the input voltage before compensation. CH2 shows the load voltage after compensation and CH3 shows the line current. CH4 shows the peak current experienced in the switches.

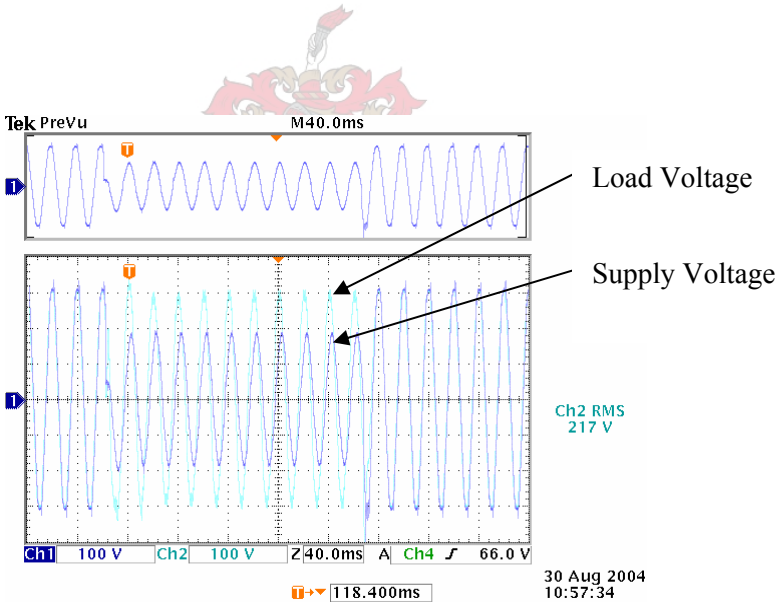


Figure 5-12 Dip compensation on a 27% dip for a 50A resistive load.

Figure 5-13 shows that the converter perfectly compensates for both voltage dip and sudden phase jump. On the oscilloscope channel 1 (CH1) is connected to the input and (CH2) is connected to the load terminals. Channel 3 (CH3) shows the line current. The compensators output voltage is also shown as the red line in Figure 5-13. The amplitude of the load voltage keeps steady while the input voltage dips. There is a ripple on the output voltage that is introduced by the multilevel inverter that

switches in steps and does not have a continuous voltage signal. This ripple can be also be seen on the simulations.

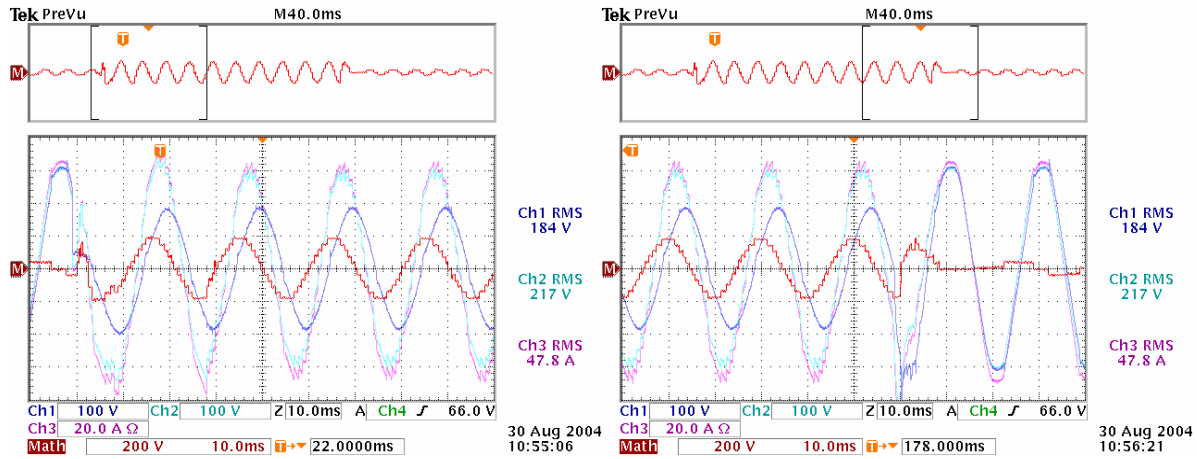


Figure 5-13 Start and stop of the 27% dip with 43° phase jumps on a 50A (RMS)

The difference between the practical results and the simulations is that some transient exists on starting and termination of the dip. There is a 1 ms delay before compensation is started in the practical result. This delay is introduced by the DSP's analog to digital conversion but is mainly because of the serial gate signal transmission, which causes most of the delay. No delay is simulated. The compensation signal also shows some irregularities during the first cycle after the dip occurred. This is due to the response of the weighted least squares estimator (Paragraph 4.5.4.2). When a dip is detected its properties are immediately sent to the switch controllers. The information is updated only after each cycle. This means that the initial overshoot measured on the estimated signal properties is read by the switch controller. As the correct signal estimate is only available after 2ms and the switch controller responds after just 1ms the correct compensation parameters are only interpreted in the next cycle.

There is some overshoot in load voltage when dip compensation is terminated. This is as result of the delay of the compensator and the line inductance. When the dip ends the compensator still continues compensation in the previous fashion for another 1-2ms before compensation terminates. The main contribution to such a high overshoot however is the sudden fault clearing. When the fault resistance RDIP is removed, high currents in the line inductance cause the voltage on the load to overshoot. This effect is self-explanatory and cannot be easily prevented. The controller is designed to dampen this effect however, the response is too slow so that by the time this overshoot has passed the converter starts compensating for it causing the voltage to drop for a few milliseconds. This

effect can be clearly seen on the right of Figure 5-13 which shows the termination of the dip compensation.

Similar results can be seen when the load is increased to 70A (RMS) (Figure 5-14 and Figure 5-15). Figure 5-15 is a zoomed window of the dip initialization. From it can be seen that, after the dip occurs the load voltage drops for 1-2 ms before it is recovered to original. Most loads should be insensitive to 1-2ms dips.

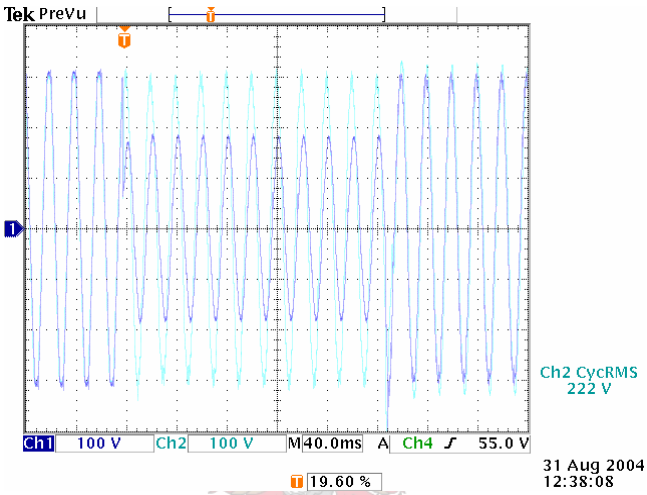


Figure 5-14 Dip compensation on a 27% dip for a 70A resistive load.

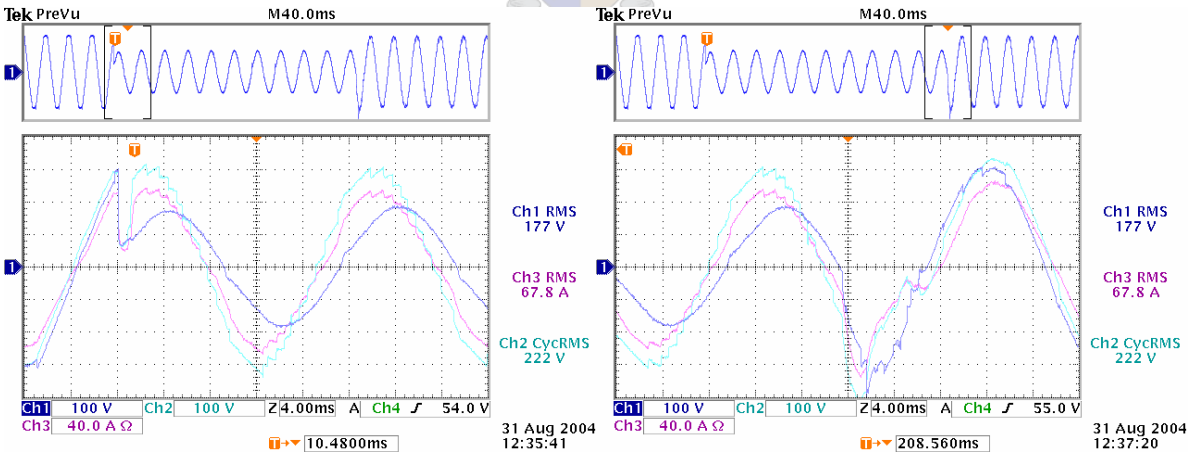


Figure 5-15 Start and stop of the 27% dip with 43° phase jumps on a 70A (RMS) load

Figure 5-15 also shows the current of S3. It can be seen that its current does not exceed 140A (Here a Tektronix DC current probe is used with an amplifier. The units are thus shown in Voltage and not Ampere in Figure 5-15.)

To verify the operation of the dip compensator at rated current a load with 90A (RMS) is connected and tested with a 27% dip and 43º phase jump.

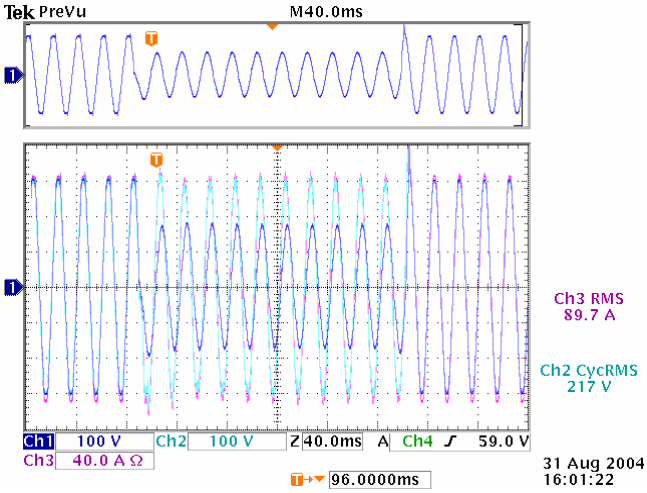


Figure 5-16 Dip compensation on a 27% dip for a 90A resistive load.

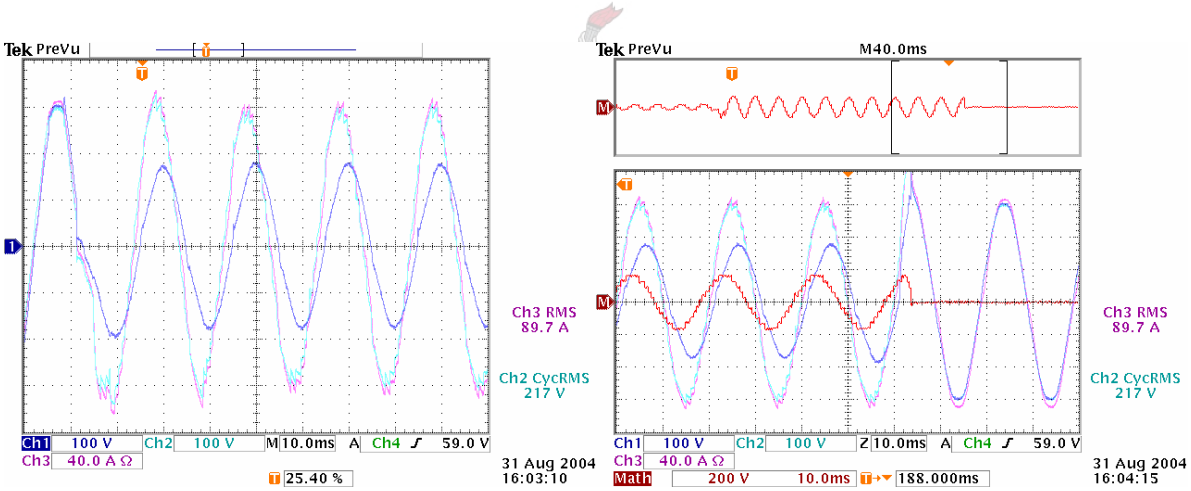


Figure 5-17 Start and stop of the 27% dip with 43° phase jumps on a 90A (RMS) load

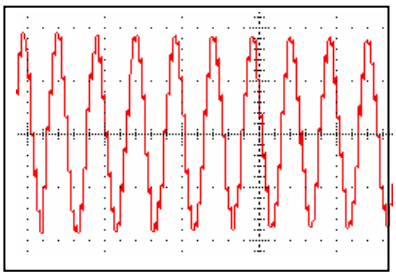


Figure 5-18 Converter output voltage dropping (zoomed) because of improper balancing (90A (RMS) load)

The dip compensator compensates even for larger loads without dropping the output voltage beyond specifications. The loss in ultracapacitor voltage and capacitor voltage drop due to improper voltage balancing (as discussed in paragraph 4.4.3.2) can be seen on the inverter output voltage, which is shown in Figure 5-18 for a 90A (RMS) load.

Other dips are also tested in this experiment. This is done by reducing the line inductance from 1200µH to 800µH. The resulting dip can be classified to be a 16% dip with a 32º phase jump. This experiment was conducted on a 70A (RMS) load.

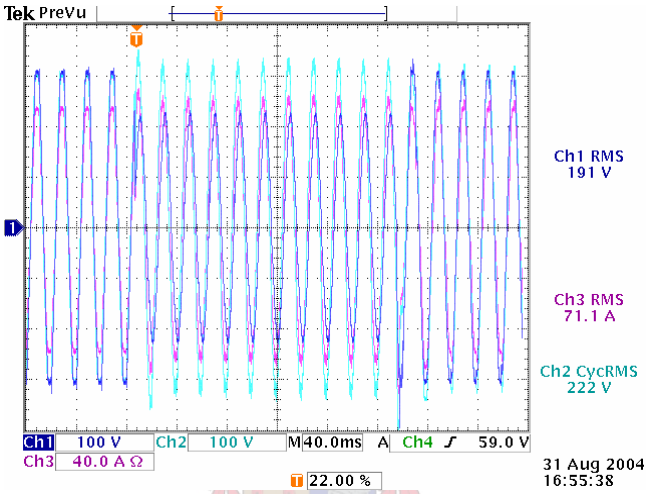


Figure 5-19 Dip compensation on a 16% dip for a 70A resistive load.

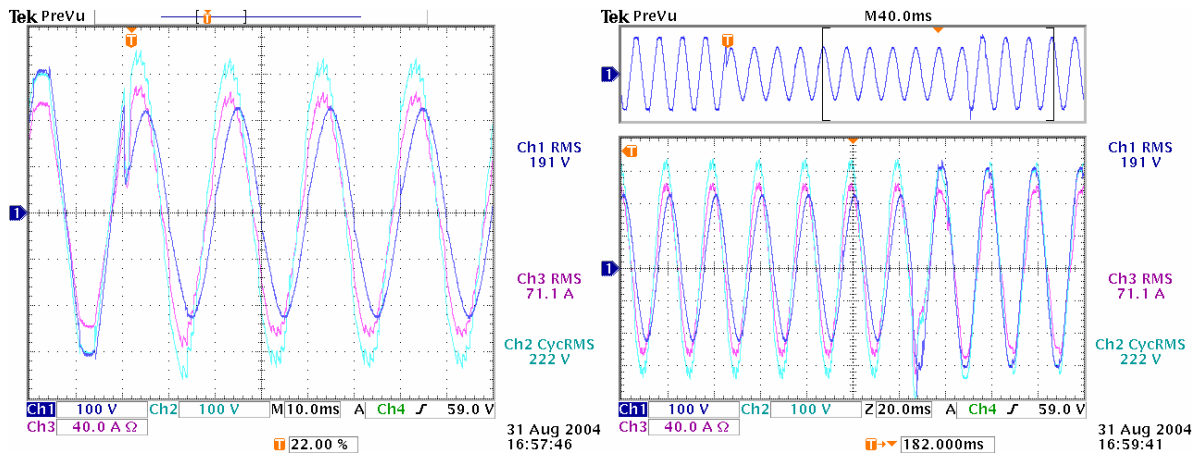


Figure 5-20 Start and stop of the 16% dip with 32° phase jumps on a 70A (RMS) load

Even smaller dips can be compensated for successfully. To generate an even smaller dip, the line inductance is reduced to 400µH. This will result in a 6% dip a 18º phase jump. The results are shown in Figure 5-22 and Figure 5-21.

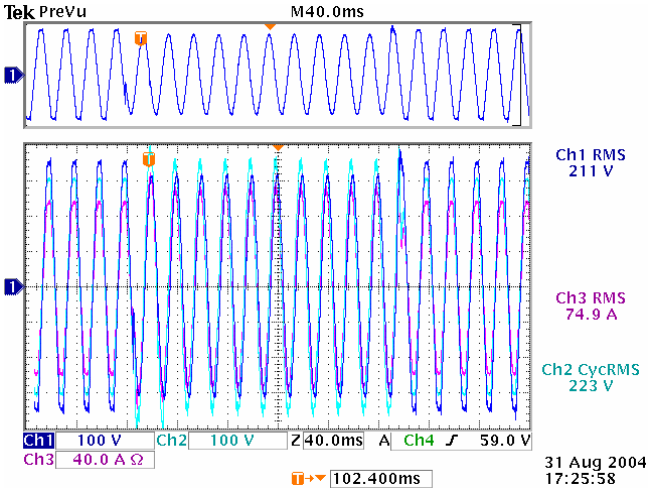


Figure 5-21 Dip compensation on a 6% dip for a 70A resistive load.

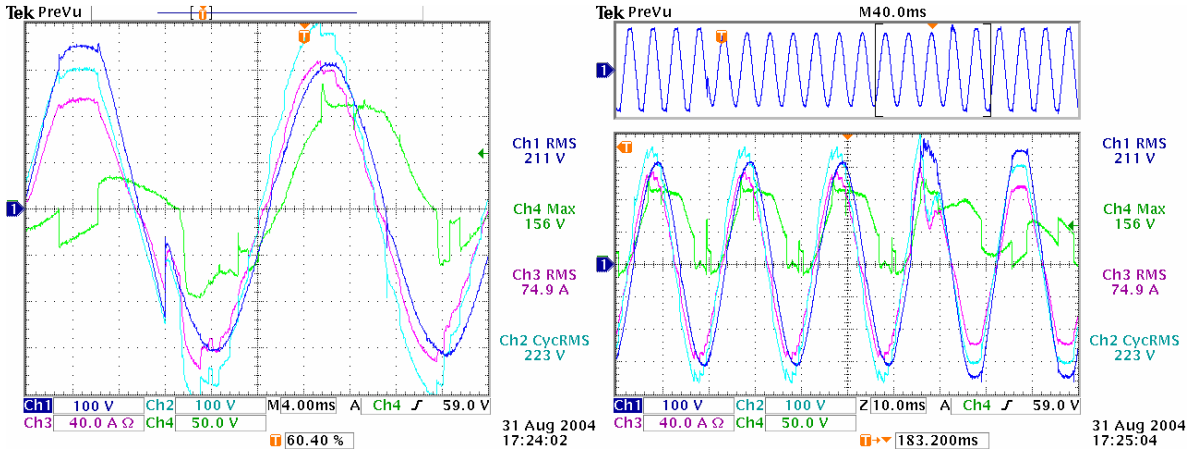


Figure 5-22 Start and stop of the 6% dip with 18° phase jumps on a 70A (RMS) load

5.3.3 Verification of control principles

5.3.3.1 Dip Detection

The control principles under discussion here are the dip detection algorithms. To monitor the algorithm variables inside the DSP, the digital to analog ports were used to output the compensation phase and compensation amplitude for a 27%, 43º dip.

Figure 5-23 shows that after a dip occurs the algorithm (Paragraph 4.5.4.2) quickly picks up such disturbance and starts estimating the parameters needed for compensation. The stable compensation

phase and amplitude are only available after a few milliseconds howeve,r acceptable estimation of the actual compensation parameters can be read after only 1 millisecond. This is exactly what can be seen from simulated results shown in paragraph 4.5.4.2 (Figure 4-43).

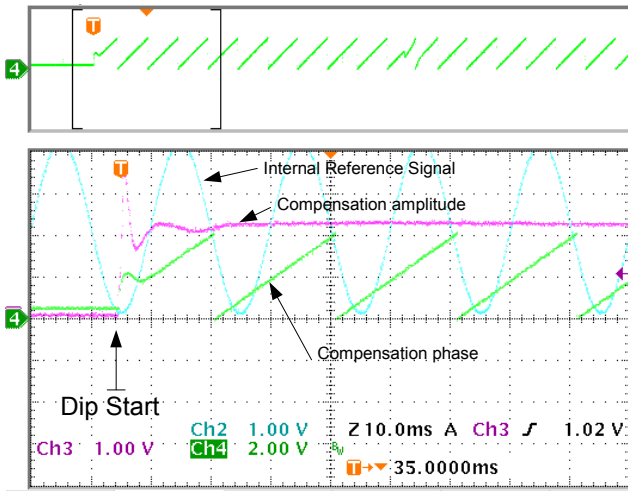


Figure 5-23 DSP internal variables for compensation amplitude and phase

5.3.3.2 **Ultracapacitor Charging**

Another control algorithm implemented into the practical system is the charging of the ultracapacitor by using power factor correction. This mode was chosen for the practical system as it introduces the least interference with the actual dip compensation ability. The phase of the output voltage is shifted by 7 degrees in such a direction as to improve the power factor seen by the supply or compensator input. The amplitudes of the input and output voltages are the same. When this mode is used for ultracapacitor charging 99% of the inverters maximum dip compensation rating is still available. (See paragraph 4.5.6.1).

In Figure 5-24 the converter is in charging mode with the ultracapacitor fully charged before a dip occurs. The inverter automatically switches to dip compensation mode for the duration of the dip before it switches to charging mode again. As the capacitor is fully charged the converters output signal phase shift from nominal line voltage is 90°. This means no power is taken up any more. If the capacitor would need charging again this phase angle would slightly increase to absorb power. The phase shift causes the output voltage to slightly lead the input voltage. This is because the load was found to be slightly inductive causing a lagging line current. By charging the ultracapacitor in such manner as described above the load current would also be shifted by +7°.

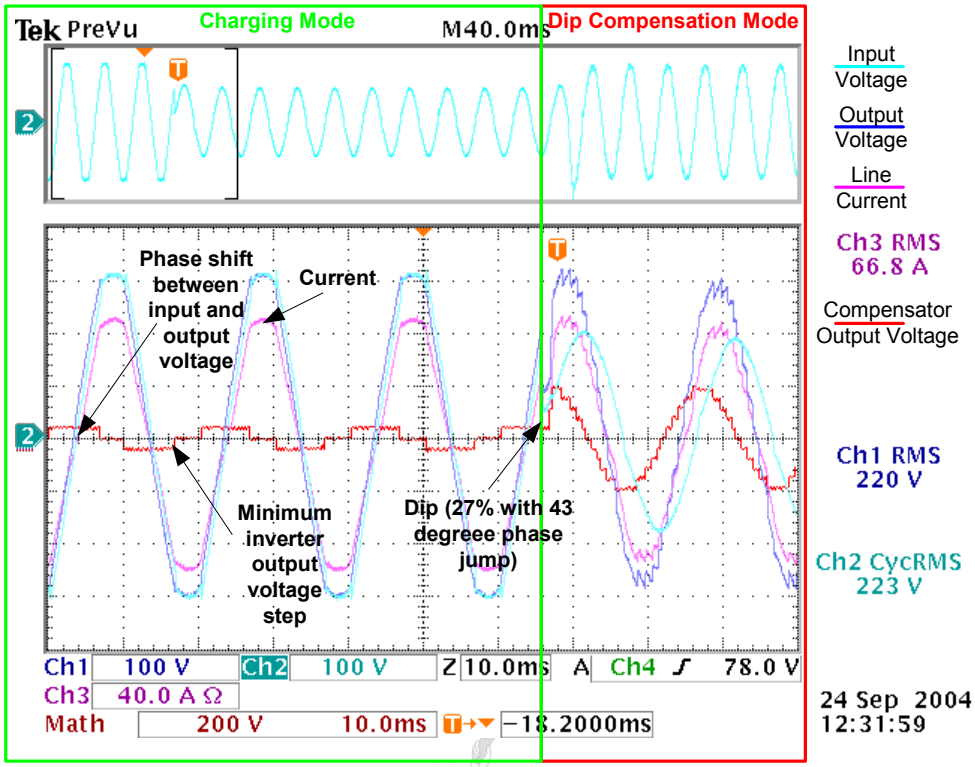


Figure 5-24 Ultracapacitor charging with little power factor correction

5.4 Summary

The Marxian multilevel inverter topology was found suitable in performance for the use in dip compensation for small-scale and larger-scale power-quality enhancing. The new concept was implemented practically and the results show good capability to compensate for most regular dips. The results obtained in the practical system under several dip conditions closely correspond to the simulations completed with the same conditions. The simulated and practical results also show a voltage drop on the inverter's output voltage after some compensation time. This was already predicted and analyzed in paragraphs 4.4.3.1 and 4.4.3.2. The dip detection algorithm used also proves to be successful and reliable.

This chapter proved that ultracapacitors can be used for maintenance-free dip compensators. It also proved that the Marxian multilevel inverter topology can be used with ultracapacitors to drastically reduce the costs by reducing the number of ultracapacitors in the system. It was proved that low-cost automotive MOSFETs can be used in the application together with other low-cost capacitors. The MOSFETs do not experience large overshoot and thus the application concept is safe to proceed to greater kVA rated devices.

Overall the results compare favourably to the simulation results shown in Chapter 5.2; thus the workings of the dip compensator are verified.

6 Conclusion

The aim of this thesis was to investigate and develop a cost effective dip compensator that is based on ultracapacitors. Ultracapacitor technology promises a brand-new method of storing energy effectively and economically. It promises gigantic power ratings and long lifespans (more than 20 years). As this technology is new and has not yet established its superior properties amongst power electronics experts, it is still expensive and scarcely available. Being successful in using ultracapacitor technology puts South Africa on par with international developments in that field.

Benefits of such an upgrade include the extension of system lifespans, reduction of maintenance intervals and reduction of optic fibre connections inside the system, thus reducing complexity.

6.1 Outcome of this thesis

Over the past five years the Power Electronics Group at the University of Stellenbosch has developed a number of state-of-the-art power-quality devices. One of these devices, a low-cost transformerless dip compensator [4], provides significant benefits in terms of cost and performance. Unlike conventional dip compensators this device does not use costly filter components and injection transformers. The modular structure of the converter makes it possible to customize its design for a variety of different applications.

The aim of this project was to take up previous developments and combine them with new technologies to maximize their functionality. The system was proven to have a fast and reliable response to voltage dips. General features include cost efficiency, low maintenance and high reliability. (The ultracapacitor is a powerful but costly device that can operate without maintenance. Development with new technology has always been expensive; however, the past has taught that prices decrease rapidly once the technology has established its market share.)

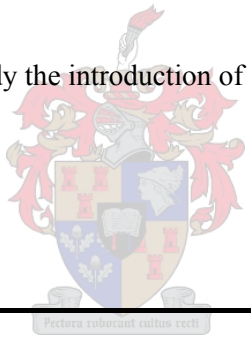
As a result of this expensive and new ultracapacitor technology, new ways were found to realize a very efficient use of ultracapacitors. The new Marxian multilevel inverter (MMLI) topology allows the use of a single low-voltage ultracapacitor to compensate for voltage dips many times the amplitude of its maximum rated voltage. The MMLI is a DC-to-AC boost converter with the advantage of only using low-voltage switches.

The converter was implemented with a dip detection strategy that proved reliable in detecting both the phase and the amplitude of the line voltage quickly and accurately. Control of the switches inside the inverter is done through a daisy chain. The advantages of using a daisy chain for switching are that costs can be reduced further as only few optical fibres are needed for isolation. All switch gates are controlled through a single optical fibre coming from the main controller board. This method does not limit the maximum number of switches that can be used and proves to be very fast and reliable.

6.2 Thesis contribution

Substantial financial losses are experienced as a result of voltage dips. This can be deduced from the study done by Eskom in 2002 [9] and that is summarized in paragraph 2.5. The problem with voltage dips is that their existence and causes are widely debated and usually neglected because of their complexity and their ignorance surrounding their effects.

However, on the basis of Eskom's study the introduction of a voltage dip compensator could become viable to industry.



6.3 Future work

The focus should be directed towards addressing the following aspects:

6.3.1 **Hardware:**

The device should be able to operate without extra power supplies for the controller. This can be achieved by drawing power from energy storage such as the ultracapacitor during operation. The need for extra ultracapacitor chargers has already been eliminated as it draws its power from the supply by various power-quality-enhancing abilities of the converter.

The concept of using ultracapacitors with the MMLI topology should be upgraded and tested for larger rated systems. This should include both voltage and current increase. The device is not limited to a maximum line operating voltage as it has no neutral point connection.

6.3.2 **Control:**

After the fault condition is removed, the line inductance causes the load voltage to overshoot its maximum operating voltage. The present control reacts to this overshoot by absorbing some of this overshoot current. However these peak currents only exist only briefly. As the controller has a certain sluggishness, the resulting load voltage may then be too low once the inverter is still actively compensating the peak after it has subsided. This property needs to be removed from the control.

The controller has full error condition detection and correction capabilities implemented already. The device can thus still compensate for dips after one module has failed. The selected module is thus deactivated from the chain. No further reliability improvements on the control need to be made.

6.4 Final Conclusion

In this thesis detailed research showed that the Marxian multilevel inverter can be used with ultracapacitors for transformerless dip compensation. The topology is best suited to using ultracapacitors, although the cost of ultracapacitors is still high. Ultracapacitors are the most expensive component in the inverter. The Marxian multilevel inverter reduces the number of required ultracapacitors to a minimum.

7 References

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APPENDIX A Power Quality

Transmission network fault data in South Africa – Section from Eskom report RES/RR/03/20237

A.1 Case study 1:

Stone on Water Surface Study for Harvard-Perseus No.2 275 kV line and Harvard-Merapi No.1 275 kV line.

A.1.1 List of faults for 2002

Harvard-Merapi No.1 275 kV line had 14 faults and Harvard-Perseus No.2 275 kV line had 1 fault in 2002. These are listed in the table below.

1	2	3	4	5	6	7
START_DT	EQUIP_DESCRIPTION	REASON	REGION	kV	Actual Month	Year
Thursday 21 February 2002 05:04:00	Harvard - Perseus No2 275kV Line	Bird Streamer	North Western	275	2002.02	2002
Monday 10 April 2000 21:50:00	Harvard - Merapi No1 275kV Line	Unknown	North Western	275	2000.04	2000
Monday 29 October 2001 00:47:00	Harvard - Merapi No1 275kV Line	Under Investigation	North Western	275	2001.10	2001
Saturday 12 January 2002 23:35:00	Harvard - Merapi No1 275kV Line	Unknown	North Western	275	2002.01	2002
Friday 08 March 2002 21:45:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.03	2002
Saturday 09 March 2002 01:17:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.03	2002
Saturday 09 March 2002 02:43:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.03	2002
Monday 11 March 2002 02:16:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.03	2002
Tuesday 19 March 2002 23:29:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.03	2002
Tuesday 26 March 2002 19:19:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.03	2002
Thursday 04 April 2002 05:12:00	Harvard - Merapi No1 275kV Line	Unknown	North Western	275	2002.04	2002
Thursday 04 April 2002 13:12:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.04	2002
Thursday 04 April 2002 20:10:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.04	2002
Saturday 06 April 2002 04:40:00	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.04	2002
5/5/02 14:01	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.05	2002
5/24/02 3:22	Harvard - Merapi No1 275kV Line	Bird Streamer	North Western	275	2002.05	2002
5/30/02 0:42	Harvard – Merapi No1 275kV Line	Under Investigation	North Western	275	2002.05	2002

Table A-1 Transmission Performance Information for Harvard-Perseus No.2. 275 kV line and for Harvard-Merapi No.1 275 kV line Load profiles for the highlighted data are included below.

A.1.2 Quality Of Supply (QOS) Information FOR AFFECTED SUBSTATIONS

The information which follows includes the QOS data for each substation. Note:

The highlighted QOS information in the table below indicates which faults were studied.

1	2	3	4	5	6	7	8
Name	Dip Date	Dip Time	Max Depth (%)	Max Duration (ms)	Class	Cause	Effect on Load Profile
QOS Information for Harvard Substation							
Harvard 275/132kV	21-Feb-02	5:03	84.6	980	Z	Bird Pollution	78 MWH lost
Harvard 275/132kV	12-Jan-02	23:36	31.8	70	X	Unknown	Assumed no effect
Harvard 275/132kV	08-Mar-02	21:45	31.1	60	X	Unknown	Checked - no effect
Harvard 275/132kV	09-Mar-02	1:17	33.8	70	X	Unknown	Assumed no effect
Harvard 275/132kV	09-Mar-02	2:42	32	60	X	Unknown	Assumed no effect
Harvard 275/132kV	19-Mar-02	23:30	33.7	70	X	Other	Assumed no effect
Harvard 275/132kV	26-Mar-02	19:19	32.3	80	X	Bird Pollution	Checked - no effect
Harvard 275/132kV	04-Apr-02	5:11	50.6	70	X	Unknown	Checked - no effect
Harvard 275/132kV	04-Apr-02	13:10	33.1	80	X	Bird Pollution	Assumed no effect
Harvard 275/132kV	04-Apr-02	20:09	34.9	70	X	Bird Pollution	Assumed no effect
Harvard 275/132kV	06-Apr-02	4:39	36.3	80	X	Bird Pollution	Checked - no effect
Harvard 275/132kV	05-May-02	1:42	51.3	70	X	Bird Pollution	Checked - no effect
Harvard 275/132kV	24-May-02	3:21	48.7	70	X	Bird Pollution	Checked - no effect
Harvard 275/132kV	30-May-02	0:42	48.7	70	X	Bird Pollution	Checked - no effect
Merapi 275/132kV	12-Jan-02	23:36	70.4	80	T	Unknown	Assumed no effect

Table Continued…							
Merapi 275/132k V	16-Jan-02	21:24	26.3	80	X	Unknown	Assumed no effect
Merapi 275/132k	21-Feb-02	5:03	66.3	90	T	Bird Pollution	Assumed no effect
Table continued…							
Merapi 275/132k V	21-Feb-02	5:03	17	310	Y	Bird Pollution	34 MWH lost
Merapi 275/132k V	21-Feb-02	5:03	13.2	110	Y	Bird Pollution	Assumed no effect
Merapi 275/132k V	08-Mar-02	21:44	78.7	60	T	Unknown	Checked - no effect
Merapi 275/132k V	09-Mar-02	1:16	69.8	60	T	Unknown	Assumed no effect
Merapi 275/132k V	09-Mar-02	2:42	79.7	60	T	Unknown	Assumed no effect
Merapi 275/132k V	11-Mar-02	2:16	80	70	T	Unknown	Assumed no effect
Merapi 275/132k V	19-Mar-02	23:29	64.5	80	T	Other	Assumed no effect
Merapi 275/132k V	26-Mar-02	19:19	66.8	60	T	Bird Pollution	Checked - no effect
Merapi 275/132k V	04-Apr-02	5:10	60.2	70	T	Unknown	Checked - no effect
Merapi 275/132k V	04-Apr-02	13:09	67.1	70	T	Bird Pollution	Assumed no effect
Merapi 275/132k V	04-Apr-02	20:08	64.8	70	T	Bird Pollution	Assumed no effect
Merapi 275/132k V	06-Apr-02	4:39	64.2	70	T	Bird Pollution	Checked - no effect
Merapi 275/132k V	05-May-02	1:41	58.5	70	X	Bird Pollution	Checked - no effect
Merapi 275/132k V	24-May-02	3:20	58.5	70	X	Bird Pollution	Assumed no effect

Table Continued…							
Merapi 275/132kV	30-May-02	0:41	59.6	70	X	Bird Pollution	Checked - no effect
QOS Information for Perseus Substation No QOS data was available for Perseus Substation. However, the load profile for the fault resulting in unserved energy has been included in the report.							
QOS Information for Theseus Substation For the fault on Harvard-Perseus 275kV line and Harvard-Merapi 275 kV line, there were no QOS data recorded for these faults at Theseus Substation. However, the load profiles (at the time of these faults) were obtained from Encor.							

Table A-2 Quality of Supply Information for Harvard and Merapi Substations

A.1.3 QOS information for Merapi substation

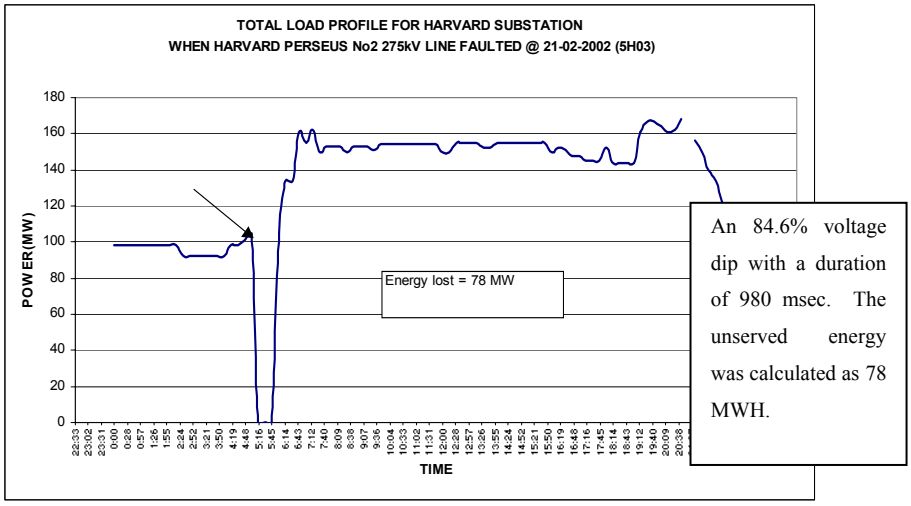
At this substation, 93 dips were experienced thus far in 2002 ranging from a depth of 11.8% to 99.1%, and duration of 30msec to 1.17 seconds. The table below only lists data for the line faults of interest.

A.1.4 Load profiles for affected substations

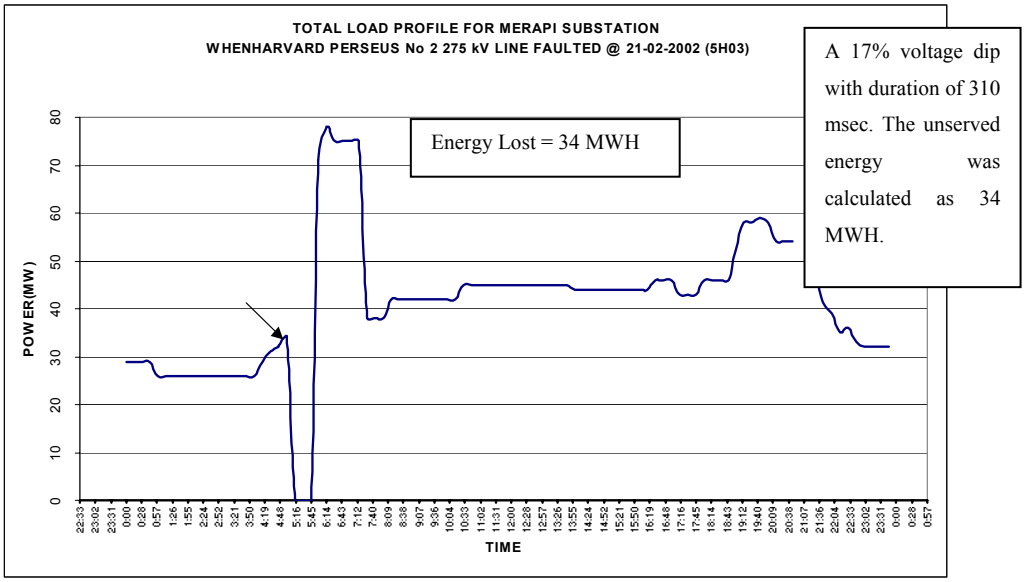
The ENCOR database keeps records of the instantaneous snapshots (taken every 15 minutes) of the real time network. The results stored in this database are used to generate load profiles of the network at specific locations as shown below.

A.1.5 Fault on Harvard-Perseus No.2 275 kV line (on 21 February 2002 at 5:04:00)

This fault caused a dip on several substations. The load profiles for these substations are shown below.



P.T.O.



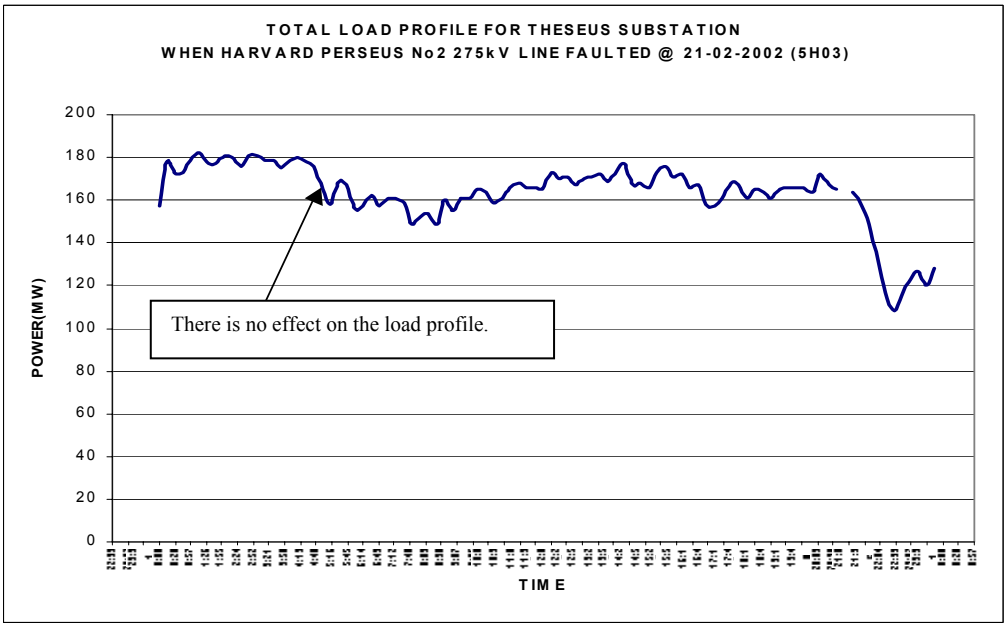


Figure A-1-1 fault on Harvard-Perseus No.2 275 kV line

The above load profiles indicate that for the fault on Harvard-Perseus No.2 275kV line (on 21 February 2002 at 05:04:00), there was no effect on the load profile at Theseus Substation; however there was a total of 112 MWH unserved energy at Perseus Substation (that is, the 78 MWH unserved energy at Harvard Substation, and 34 MWH unserved energy at Merapi Substation). The unserved energy for each load profile was calculated using the method outlined in section 1.4 of this report.

A.1.6 Fault on Harvard-Merapi No.1 275 kV line (on 08 March 2002 at 21:45:00)

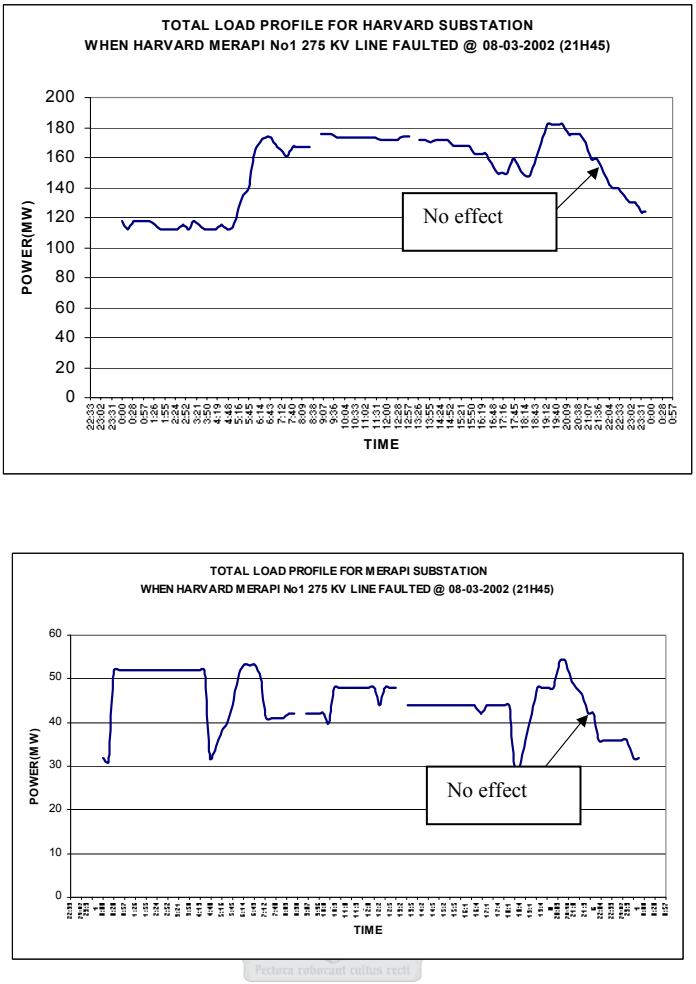


Figure A-1-2 Load profile on the Harvard-Merapi No.1

For the fault on Harvard-Merapi No.1 275 kV line on 08 March 2002 at 21:45:00, the load profiles for Perseus and Theseus Substations were not available. The load profiles for Harvard and Merapi Substations indicated that there was no effect on the load profiles and thus there was no unserved energy. Thus, it can be seen that not all faults lead to an unserved energy situation. The severity and duration of the fault, as well as the type of customer/load, will determine whether or not an unserved energy situation will eventually arise.

The load profiles for the other highlighted faults on the Harvard-Merapi 275 kV line were also studied and the results were similar to that above (that is, there were no effect on the load profiles, and hence no unserved energy in these cases).

A.1.7 Estimation of the cost of unserved energy

1 Fault on Harvard-Perseus No.2 275 kV line		
Customer Costs		
Cost of Unserved Energy		Amount:
Substation	MWH lost	
Harvard	78	R 780 000.00
Merapi	34	R 340 000.00
Perseus	112	R 1 120 000.00
= >Total MWH lost	112	R1 120 000.00
1Total Customer Costs (@ R10000/MWH)		R1 120 000
14 Faults on Harvard-Merapi No.1 275 kV line		
Customer Costs		
Cost of Unserved Energy		Amount:
Substation	MWH lost	
Harvard	0	0
Merapi	0	0
Perseus	0	0
= >Total MWH lost	0	0
1Total Customer Costs (@ R10000/MWH)		R0

Table A-3 Faults on Harvard-Merapi & Harvard-Perseus line

The rate of R10000/MWH (average COUE) was assumed for now. Further analysis of the customer surveys would reveal a more accurate calculation rate (i.e. no customer interviews were conducted for this network).

A.1.8 Eskom Costs

Effect of Through-Faults on Transmission Transformers:

The contribution of through-faults to transformer failure is evidenced by loose and deformed transformer windings. Although transformers do not fail as a result of a single fault under normal operating conditions, loose and deformed windings do occur as a result of faults. Any further faults on an already fault-damaged transformer exacerbate the damage and eventually transformer failure occurs. In some cases this damage is irreparable. Although transformer windings are designed with a measure of elasticity, the windings are weakened by continuous faulting and do not return to their original shape. The number of faults required to cause transformer failure are largely dependent on three factors:

- Magnitude of faults;
- Duration of faults; and
- Number of faults.

It is assumed that after 10 severe through faults, a transformer fails. It is also assumed that 1 out of every 30 through faults which occur, are of the severe type. The position of the fault on the line has the most impact on fault current. Hence, we can conclude that after 300 through faults, a transformer failure will result. However, more research needs to be carried out in 2003 in order to confirm these figures.

1 Fault on Harvard-Perseus No.2 275 kV line	
Eskom Costs	
Helicopter Patrol	R2 000
Ground Patrol	R329.40
Travel and Subsistence	R900
2 Breaker Maintenance Costs	R0
2 CT Maintenance Costs	R0
Transformer Damage Costs	R50 000
Total Eskom Costs	R53 229.40
Total Cost of Fault (i.e. Customer & Eskom costs)	R1 173 229.40
14 Faults on Harvard-Merapi No.1 275 kV line	
Eskom Costs	
Helicopter Patrol	R26 460
Ground Patrol	R7 030
Travel and Subsistence	R12 600
2 Breaker Maintenance Costs	R0
2 CT Maintenance Costs	R0
Transformer Damage Costs (distance away from source)	R0
Total Eskom Costs	R46 090
Total Cost of Fault (i.e. Customer & Eskom costs)	R46 090

Table A-4 Faults on Harvard-Merapi & Harvard-Perseus line

These costs are assumed low pending further research.

A.2 Case study 2:

Stone on Water Surface Study for a fault on the matimba-witkop 400kv line.

A.2.1 List of faults for 2001

Matimba - Witkop No1 400kV Line had 18 faults reported in 2001. These are listed in the table below.

1	2	3	4	5	6
START_DT	REASON	REGION	kV	Actual Month	Year
4/1/01 22:50	Bird Streamer	Northern	400	2001.04	2001
6/7/01 12:34	Fire Veld	Northern	400	2001.06	2001
6/7/01 12:35	Fire Veld	Northern	400	2001.06	2001
6/10/01 13:41	Fire Veld	Northern	400	2001.06	2001
6/18/01 15:07	Fire Veld	Northern	400	2001.06	2001
6/18/01 15:08	Fire Veld	Northern	400	2001.06	2001
6/18/01 15:09	Fire Veld	Northern	400	2001.06	2001
6/18/01 15:10	Fire Veld	Northern	400	2001.06	2001
6/18/01 18:15	Fire Veld	Northern	400	2001.06	2001
6/18/01 18:16	Fire Veld	Northern	400	2001.06	2001
7/11/01 12:41	Fire Veld	Northern	400	2001.07	2001
7/12/01 6:24	Bird Streamer	Northern	400	2001.07	2001
7/19/01 15:19	Fire Veld	Northern	400	2001.07	2001
7/20/01 11:53	Fire Veld	Northern	400	2001.07	2001
7/20/01 12:10	Fire Veld	Northern	400	2001.07	2001
8/16/01 15:27	Fire Veld	Northern	400	2001.08	2001
9/22/01 3:15	Bird	Northern	400	2001.09	2001
11/15/01 14:28	Rain	Northern	400	2001.11	2001
5/13/02 0:22	Unknown	Northern	400	2002.05	2002

Table A-5 Transmission Line Performance information for Matimba-Witkop No.1 400kV

Load profiles for the highlighted data are included below.

A.2.2 Quality of supply (QOS) Information for affected substations

The information which follows includes the QOS data for each substation. Note: The highlighted QOS information in the table below indicates which faults were studied.

1	2	3	4	5	6	7	8
Name	Dip Date	Dip Time	Max Depth (%)	Max duration (ms)	Class	Cause	Effect on Load Profile
QOS Information for Witkop Substation							
Witkop 400/132 kV	01-Apr-01	22:50	79.3	90	T	Bird Pollution	Checked - no effect
Witkop 400/132 kV	07-Jun-01	12:34	40.6	60	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	10-Jun-01	13:40	37.1	60	X	Veld Fire	Assumed no effect

Table Continued…							
Witkop 400/132 kV	18-Jun-01	15:06	44.6	60	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	18-Jun-01	15:08	33.4	60	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	18-Jun-01	15:10	35.7	60	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	18-Jun-01	15:11	44.3	60	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	18-Jun-01	18:14	34	60	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	18-Jun-01	18:15	35	60	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	18-Jun-01	18:16	45.6	90	X	Veld Fire	Checked - no effect
Witkop 400/132 kV	11-Jul-01	12:41	36	50	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	11-Jul-01	12:42	43.2	60	X	Veld Fire	Checked - no effect
Witkop 400/132 kV	12-Jul-01	6:24	36.5	60	X	Birds	Assumed no effect
Witkop 400/132 kV	19-Jul-01	15:19	49.6	60	X	Veld Fire	232 MWH lost
Witkop 400/132 kV	20-Jul-01	11:52	34.5	60	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	20-Jul-01	12:10	38.5	50	X	Veld Fire	Checked - no effect
Witkop 400/132 kV	16-Aug-01	15:26	28.9	80	X	Veld Fire	Assumed no effect
Witkop 400/132 kV	22-Sep-01	3:14	42.9	60	X	Bird Pollution	Assumed no effect
Witkop 400/132 kV	15-Nov-01	14:27	56.8	90	X	Storm Related	Assumed no effect
QOS information for Matimba Substation No other QOS data was available for Matimba Substation.							
Matimba 400/132kV	13-May-02	0:21	12.8	40	Y	Unknown	Assumed no effect

Table Continued…

QOS information for Merensky Substation

Merensky 275/132kV	01-Apr-01	22:50	25.4	50	X	Bird Pollution	Assumed no effect
Merensky 275/132kV	13-May-02	0:21	15.5	60	Y	Unknown	Assumed no effect
Merensky 275/132kV	07-Jun-01	12:34	12.5	30	Y	Veld Fire	Assumed no effect
Merensky 275/132kV	18-Jun-01	15:06	14.8	40	Y	Veld Fire	Assumed no effect
Merensky 275/132kV	18-Jun-01	15:10	14.2	40	Y	Veld Fire	Assumed no effect
Merensky 275/132kV	18-Jun-01	18:15	16.4	70	Y	Veld Fire	Assumed no effect
Merensky 275/132kV	19-Jul-01	15:18	15.9	40	Y	Veld Fire	100 MWH

QOS information for Spencer Substation

Spencer 275/132kV	01-Apr-01	22:50	57.2	50	X	Bird Pollution	Assumed no effect
Spencer 275/132kV	01-Apr-01	22:50	64.4	90	T	Bird Pollution	Assumed no effect
Spencer 275/132kV	13-May-02	0:21	27.8	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	07-Jun-01	12:34	28.5	50	X	Veld Fire	Assumed no effect
Spencer 275/132kV	10-Jun-01	13:40	27.7	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	10-Jun-01	13:40	27	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	15:06	26.1	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	15:06	26.4	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	15:06	32.7	50	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	15:08	22	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	15:10	24.6	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	15:10	24.5	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	15:10	24.1	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	15:10	31.9	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	18:14	24.5	50	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	18:15	25.4	50	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	18:16	23.2	50	X	Veld Fire	Assumed no effect
Spencer 275/132kV	18-Jun-01	18:16	35	110	X	Veld Fire	Checked - no effect

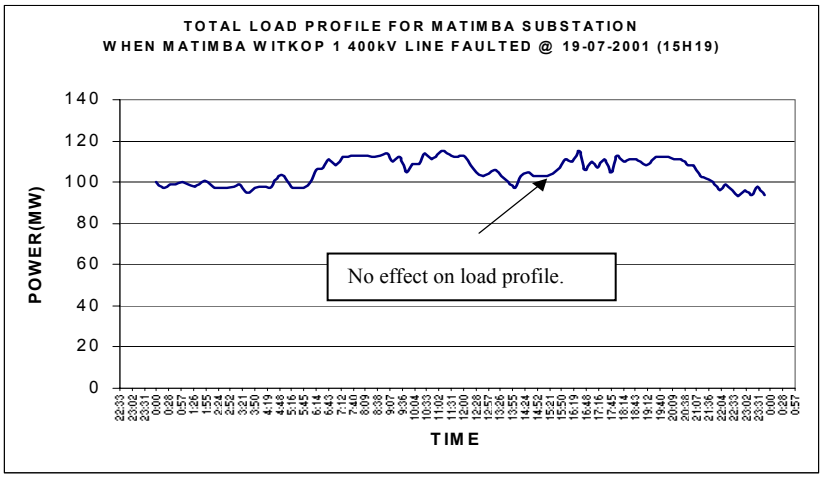
Table Continued…							
Spencer 275/132kV	11-Jul-01	12:42	25.2	50	X	Veld Fire	Assumed no effect
Spencer 275/132kV	11-Jul-01	12:42	32.2	60	X	Veld Fire	Checked - no effect
Spencer 275/132kV	12-Jul-01	6:24	27.6	60	X	Birds	Assumed no effect
Spencer 275/132kV	19-Jul-01	15:19	30.1	50	X	Veld Fire	Assumed no effect
Spencer 275/132kV	19-Jul-01	15:19	29.9	60	X	Veld Fire	Checked - no effect
Spencer 275/132kV	20-Jul-01	11:52	24.1	60	X	Veld Fire	Assumed no effect
Spencer 275/132kV	20-Jul-01	12:10	26.4	60	X	Veld Fire	Checked - no effect
Spencer 275/132kV	16-Aug-01	15:26	21.7	80	X	Veld Fire	Assumed no effect
Spencer 275/132kV	22-Sep-01	3:14	30.5	60	X	Bird Pollution	Assumed no effect
QOS information for Tabor Substation							
Tabor 275/132kV	01-Apr-01	22:50	63.6	90	T	Bird Pollution	Assumed no effect
Tabor 275/132kV	07-Jun-01	12:33	26.3	50	X	Veld Fire	Assumed no effect
Tabor 275/132kV	07-Jun-01	12:34	28.5	50	X	Veld Fire	Assumed no effect
Tabor 275/132kV	10-Jun-01	13:40	25.5	60	X	Veld Fire	Assumed no effect
Tabor 275/132kV	18-Jun-01	15:06	32.6	50	X	Veld Fire	Assumed no effect
Tabor 275/132kV	18-Jun-01	15:08	21.8	60	X	Veld Fire	Assumed no effect
Tabor 275/132kV	18-Jun-01	15:10	31.3	60	X	Veld Fire	Assumed no effect
Tabor 275/132kV	18-Jun-01	18:14	24.6	50	X	Veld Fire	Assumed no effect
Tabor 275/132kV	18-Jun-01	18:15	25.5	50	X	Veld Fire	Assumed no effect
Tabor 275/132kV	18-Jun-01	18:16	35.4	90	X	Veld Fire	Checked - no effect
Tabor 275/132kV	11-Jul-01	12:42	30.7	60	X	Veld Fire	Checked - no effect
Tabor 275/132kV	12-Jul-01	6:24	27.1	60	X	Birds	Assumed no effect
Tabor 275/132kV	19-Jul-01	15:19	29.5	60	X	Veld Fire	Checked - no effect
Tabor 275/132kV	20-Jul-01	11:52	23	60	X	Veld Fire	Assumed no effect
Tabor 275/132kV	20-Jul-01	12:10	25	50	X	Veld Fire	Checked - no effect
Tabor 275/132kV	16-Aug-01	15:26	18.9	80	Y	Veld Fire	Assumed no effect
Tabor 275/132kV	22-Sep-01	3:14	29.5	60	X	Bird Pollution	Assumed no effect
Tabor 275/132kV	15-Nov-01	14:27	49.1	90	X	Storm Related	Assumed no effect
QOS information for Warmbad Substation							
Warmbad 275/132kV	01-Apr-01	22:50	37.2	90	X	Bird Pollution	Assumed no effect
Warmbad 275/132kV	07-Jun-01	12:33	19.1	50	Y	Veld Fire	Assumed no effect
Warmbad 275/132kV	07-Jun-01	12:34	20.1	40	X	Veld Fire	Assumed no effect
Warmbad 275/132kV	10-Jun-01	13:40	19.5	50	Y	Veld Fire	Assumed no effect
Warmbad 275/132kV	18-Jun-01	15:06	22.4	50	X	Veld Fire	Assumed no effect
Warmbad 275/132kV	18-Jun-01	15:08	17.3	40	Y	Veld Fire	Assumed no effect

Table Continued…							
Warmbad 275/132kV	18-Jun-01	15:10	18.5	50	Y	Veld Fire	Assumed no effect
Warmbad 275/132kV	18-Jun-01	18:14	18.5	40	Y	Veld Fire	Assumed no effect
Warmbad 275/132kV	18-Jun-01	18:15	18.9	50	Y	Veld Fire	Assumed no effect
Warmbad 275/132kV	18-Jun-01	18:16	24.6	90	X	Veld Fire	Checked - no effect
Warmbad 275/132kV	11-Jul-01	12:42	21.6	50	X	Veld Fire	Assumed no effect
Warmbad 275/132kV	19-Jul-01	15:19	20.4	60	X	Veld Fire	Checked - no effect
Warmbad 275/132kV	20-Jul-01	12:10	19.5	40	Y	Veld Fire	Checked - no effect
Warmbad 275/132kV	16-Aug-01	15:26	15.7	40	Y	Veld Fire	Assumed no effect
Warmbad 275/132kV	22-Sep-01	3:14	20.1	50	X	Bird Pollution	Assumed no effect
Warmbad 275/132kV	15-Nov-01	14:27	31.8	70	X	Storm Related	Assumed no effect

Table A-6 Quality of Supply Information for affected Substations

A.2.3 Load profiles for affected substations

The ENCOR database keeps records of the instantaneous snapshots (taken every 15 minutes) of the real time network. The results stored in this database is used to generate load profiles of the network at specific locations as shown below.



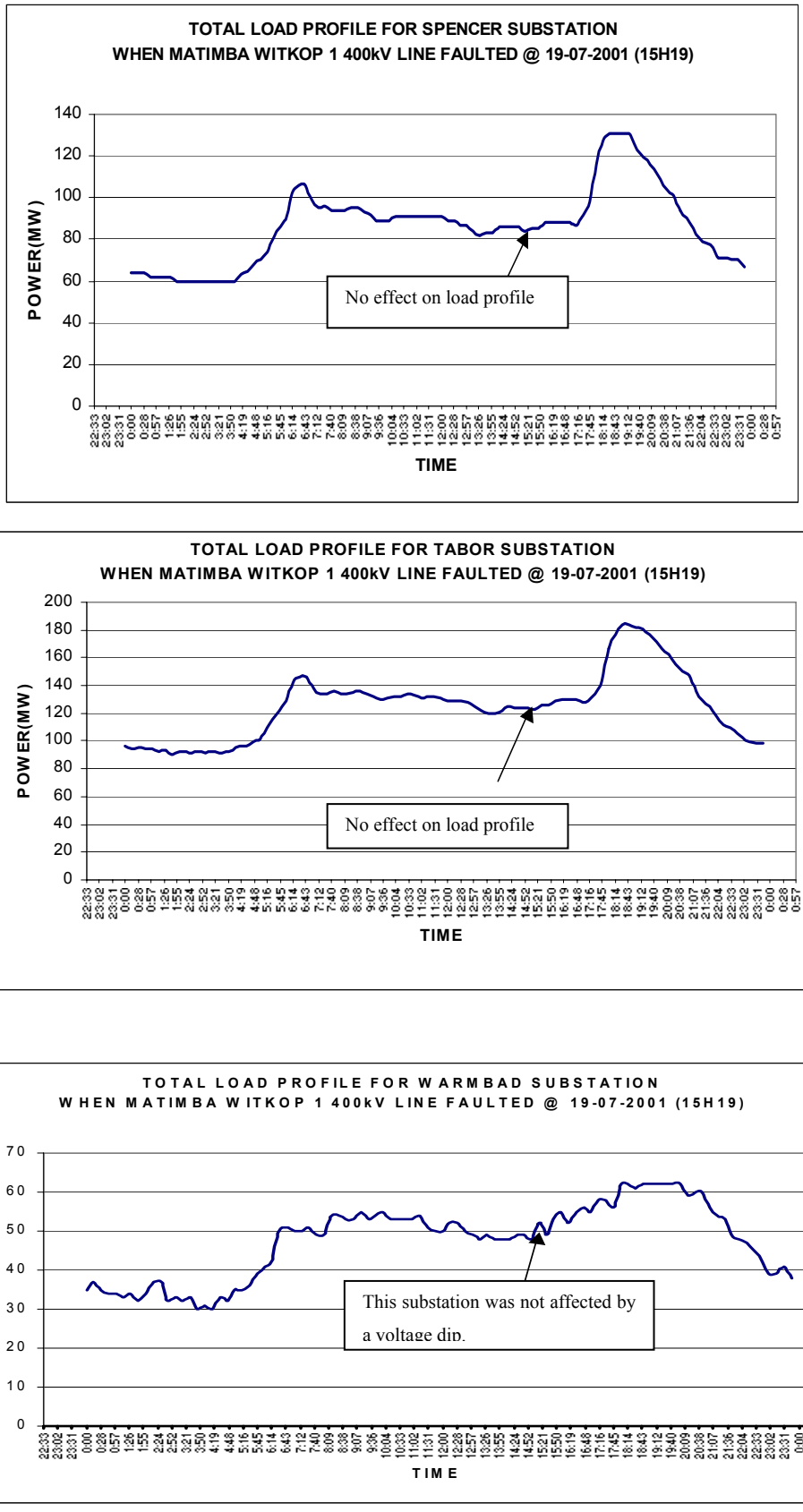
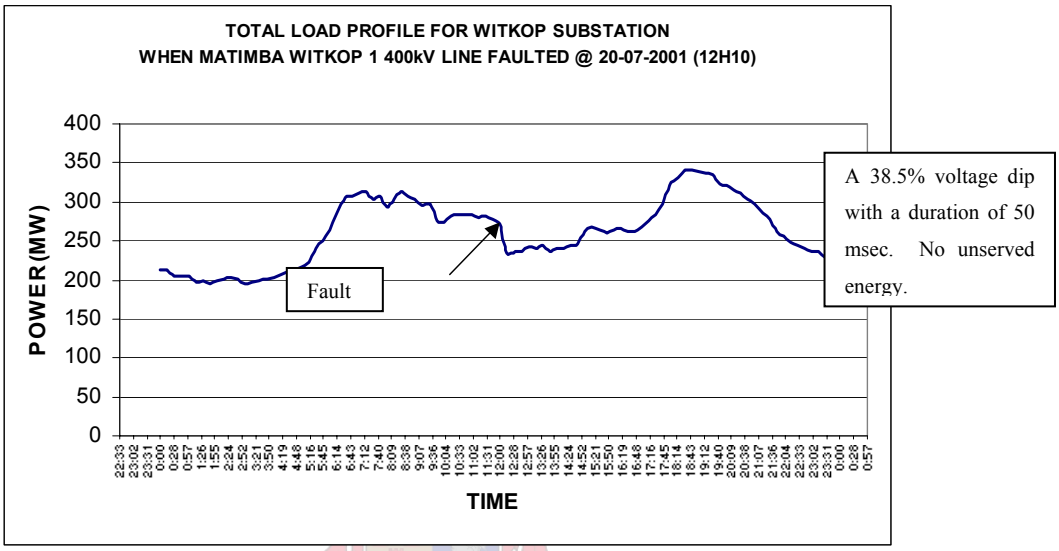
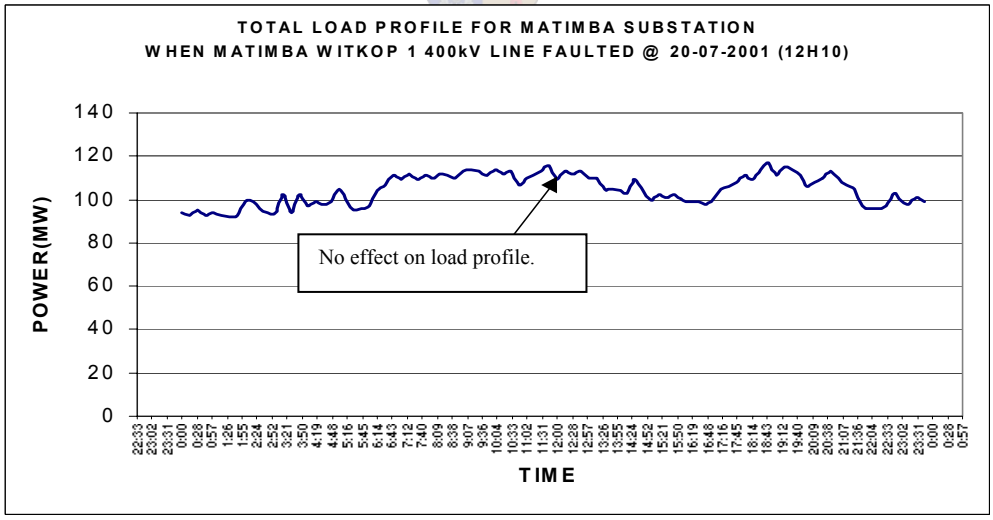
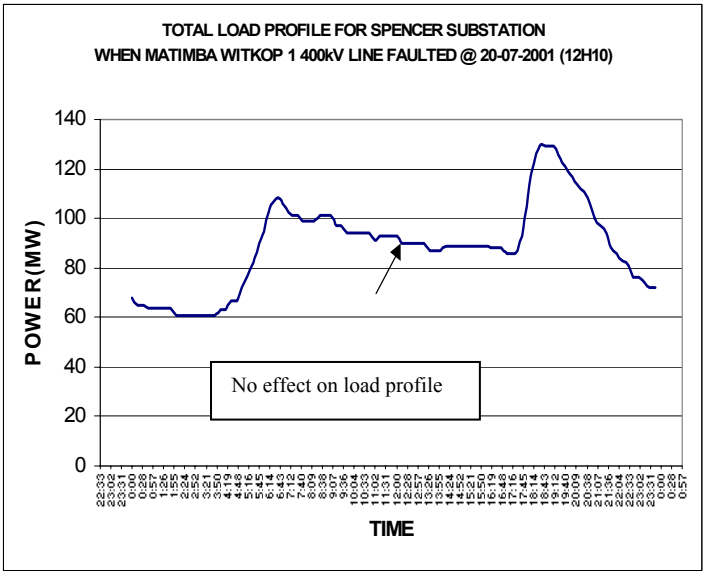


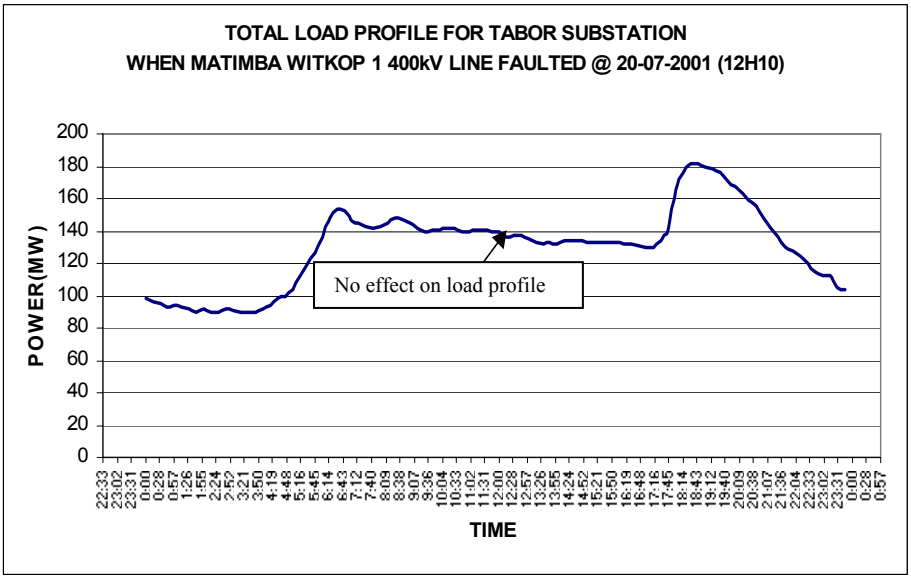
Figure A-1-3 Fault on Matimba-Witkop No.1 400 kV line (on 19 July 2001 at 15:19:00)

The above load profiles indicate that for the fault on Matimba-Witkop No.1 400kV line (on 19 July 2001 at 15:19:00), there was no effect on the load profiles (implying, no unserved energy) at Matimba, Spencer, Tabor and Warmbad Substations. However, the unserved energy at Witkop Substation was calculated as 232 MWH, and the unserved energy at Merensky Substation was calculated as 100 MWH. Thus, there was total of 332 MWH of unserved energy for the fault on Matimba-Witkop No.1 400kV line (on 19 July 2001 at 15:19:00). The unserved energy for each load profile was calculated using the method outlined in section 1.4 of this report.









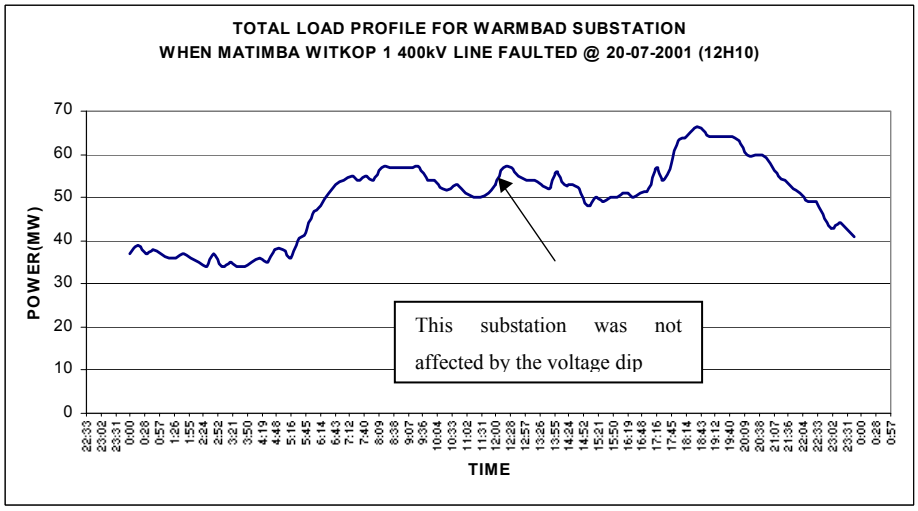


Figure A-1-4 Fault on Matimba-Witkop No. 1 400 kV line (on 20 July 2001 at 12:10:00)

The above load profiles indicate that for the fault on Matimba-Witkop No.1 400kV line (on 20 July 2001 at 12:10:00), there was no effect on the load profiles (implying, no unserved energy) at Witkop, Matimba, Spencer, Tabor and Warmbad Substations. However, the unserved energy at Merensky Substation was calculated as 312 MWH. Thus, there was a total of 312 MWH of unserved energy for the fault on Matimba-Witkop No.1 400kV line (on 20 July 2001 at 12:10:00). The unserved energy for each load profile was calculated using the method outlined in section 1.4 of this report.

The load profiles for the other highlighted faults (in Tables 4 & 5) on the Matimba-Witkop 400 kV line were also studied and the results were similar to that above (that is, there were no effect on the load profiles and hence, no unserved energy in these cases).

A.2.4 Estimation of the cost of unserved energy

19 Faults on Matimba-Witkop 400 kV line		
Customer Costs		
Cost of Unserved Energy		Amount:
Substation	MWH lost	
Witkop	232	R2 320 000.00
Merensky	412	R4 120 000.00
Tabor	0	0
Spencer	0	0
Warmbad	0	0
Matimba	0	0
= >Total MWH lost	644	0
1Total Customer Costs (@ R10000/MWH)		R6 440 000

Table A-7 Faults on Matimba-Witkop 400 kV line

The rate of R10000/MWH (average COUE) was assumed for now. Further analysis of the customer surveys would reveal a more accurate calculation rate. (No customer interviews were conducted for this network).

A.2.5 Eskom costs

Effect of Through-Faults on Transmission Transformers

Refer to page 27 for a description of method used to obtain Eskom's cost.

19 Faults on Matimba-Witkop 400 kV line	
Eskom Costs	
Helicopter Patrol	R34 020
Ground Patrol	R10 711.93
Travel and Subsistence	R16 200
2 Breaker Maintenance Costs	R0
2 CT Maintenance Costs	R0
Transformer Damage Costs	R950 000
Total Eskom Costs	R1 010 931.93
Total Cost of 19 Faults (i.e. Customer & Eskom costs	R7 450 931.93

Table A-8 Faults on Matimba-Witkop 400 kV line

A.3 Case study 3:

Stone on Water Surface Study for a fault on Bighorn-middelkraal 88kv line.

No Transmission performance data was available for Bighorn-Middelkraal 88 kV line.

A.3.1 Quality Of Supply (QOS) Information for affected Substations

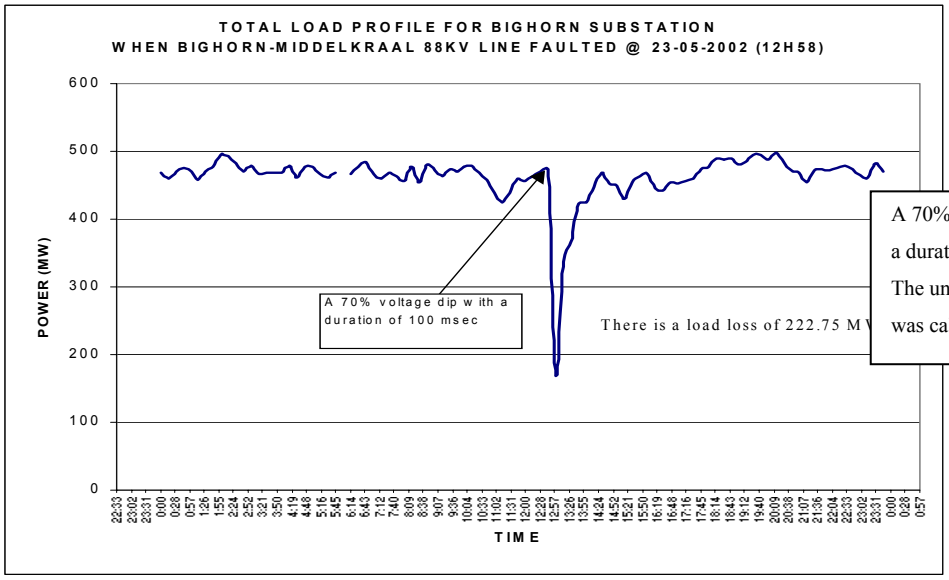
The information that follows includes the QOS data and load profiles for each substation. Note: The highlighted QOS information in the table below indicates which faults were studied.

1	2	3	4	5	6	7	8
Name	Dip Date	Dip Time	Max Depth (%)	Max Duration (ms)	Class	Cause	Effect on Load Profile
QOS Information for Bighorn Substation At this substation, 117 dips were experienced thus far in 2002 ranging from a depth of 10.3% to 70%, and duration of 30msec to 1.27 seconds. The list below only includes data for the line fault of interest.							
Bighorn 400/88kV	23-May	12:58	70	100	T	Human Related	222.75 MWH
Bighorn 400/88kV	22-Aug	17:53	54.1	100	X	Human Interference	Checked - no effect
Bighorn 400/88kV	22-Aug	17:53	53.1	190	S	Human Interference	Assumed no effect
QOS information for Trident Substation. At this substation, 110 dips were experienced thus far in 2002 ranging from a depth of 10.2% to 58.7%, and duration of 30msec to 1.21 seconds. The list below only includes data for the line fault of interest.							
Table Continued…							
Trident 275/88kV	23-May-02	12:58	40.1	70	X	Human Related	19.5 MWH lost
Trident 275/88kV	22-Aug-02	17:53	22.1	90	X	Human Interference	Checked - no effect
Trident 275/88kV	22-Aug-02	17:53	21.3	180	S	Human Interference	Assumed no effect
Trident 275/88kV	23-Oct-02	18:07	25.1	740	Z	Storm Related	Assumed no effect
QOS information for Pluto Substation At this substation, 79 dips were experienced thus far in 2002 ranging from a depth of 11.4 to 59.9%, and duration of 30 msec to 1.19 seconds. For the faults on Bighorn-Middelkraal 88 kV line, there were no QOS data recorded for these faults at Pluto Substation. However, the load profiles (at the time of the faults) were obtained from Encor.							
QOS information for Spitskop Substation At this substation, 90 dips were experienced thus far in 2002 ranging from a depth of 10.5% to 64.6%, and duration of 30msec to 940msec. The list below only includes data for the line fault of interest.							
Spitskop 400/132kV	23-May-02	12:58	15.4	70	Y	Human Related	Checked - no effect

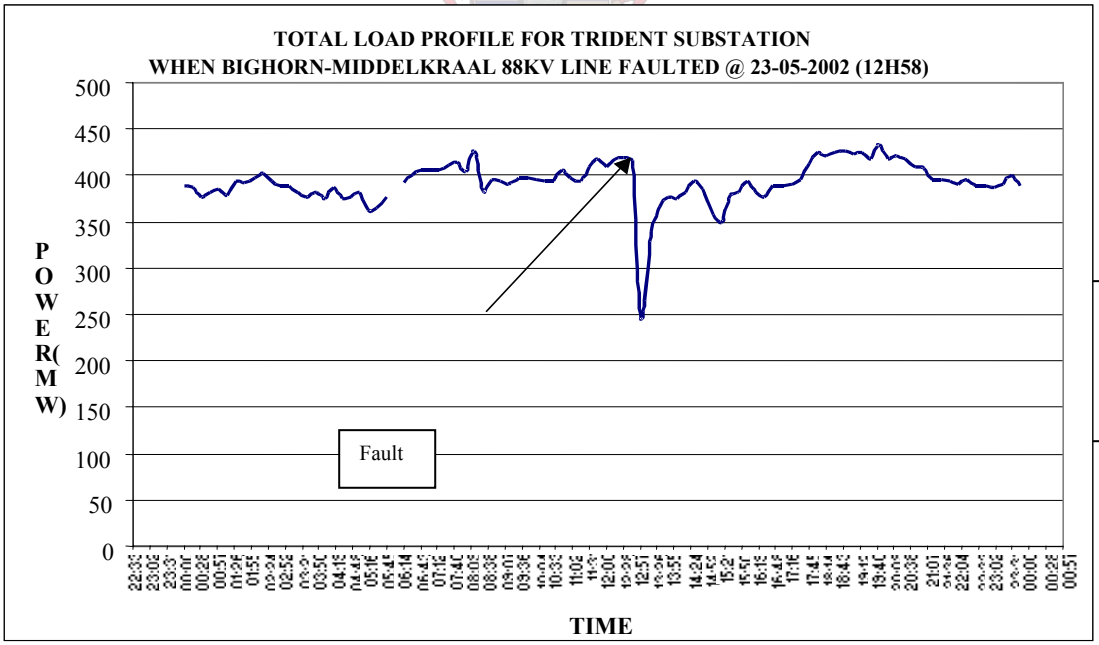
Table A-9 Quality of Supply Information for affected Substations

A.3.2 Load profiles for the affected substations

The ENCOR database keeps records of the instantaneous snapshots (taken every 15 minutes) of the real time network. The results stored in this database are used to generate load profiles of the network at specific locations

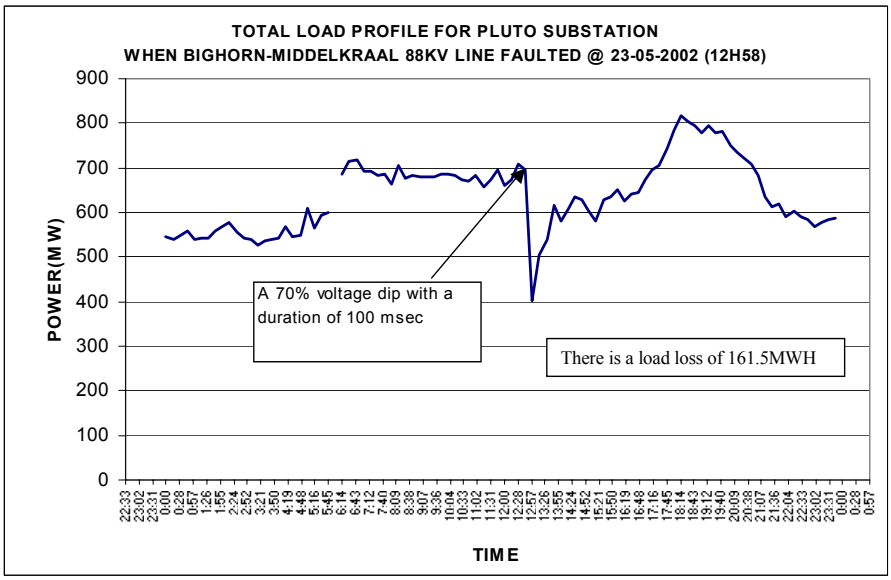


A 70% voltage dip with a duration of 100 msec. The unserved energy was calculated as



A 40.1% voltage dip with a duration of 70 msec. The unserved energy was calculated

P.T.O.



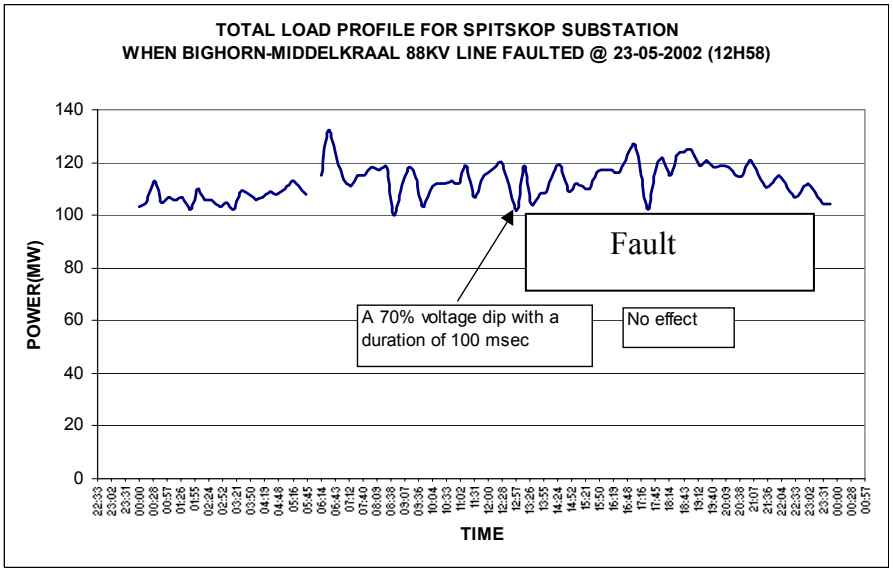
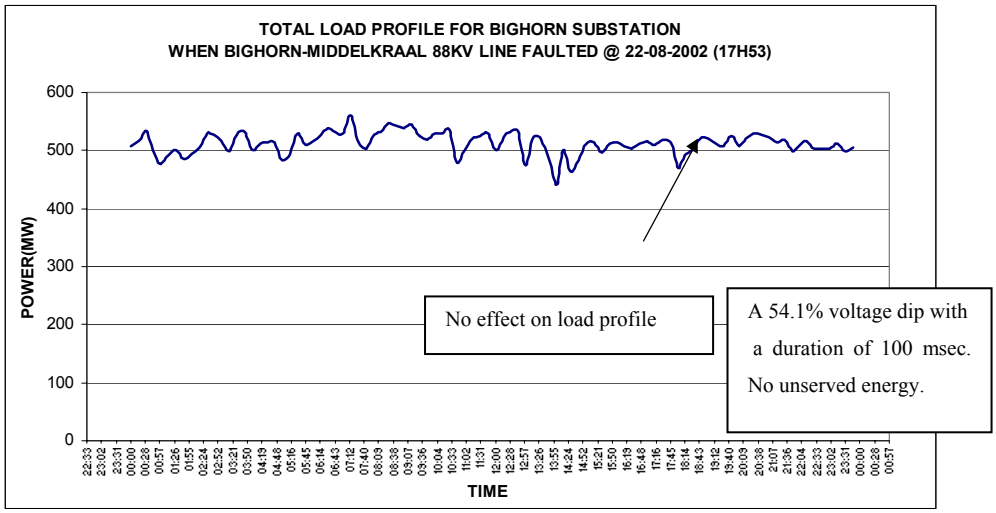
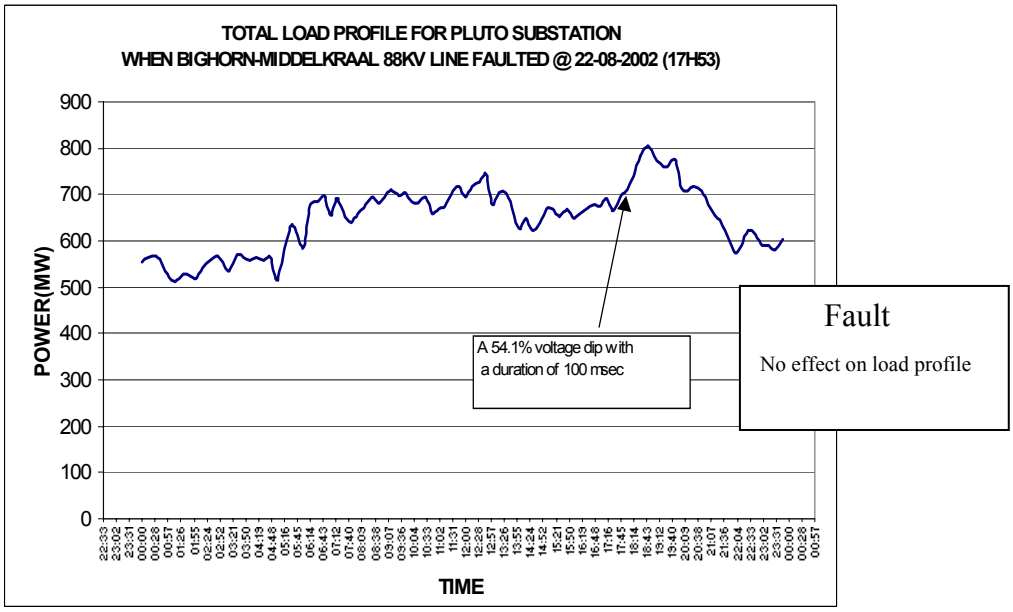
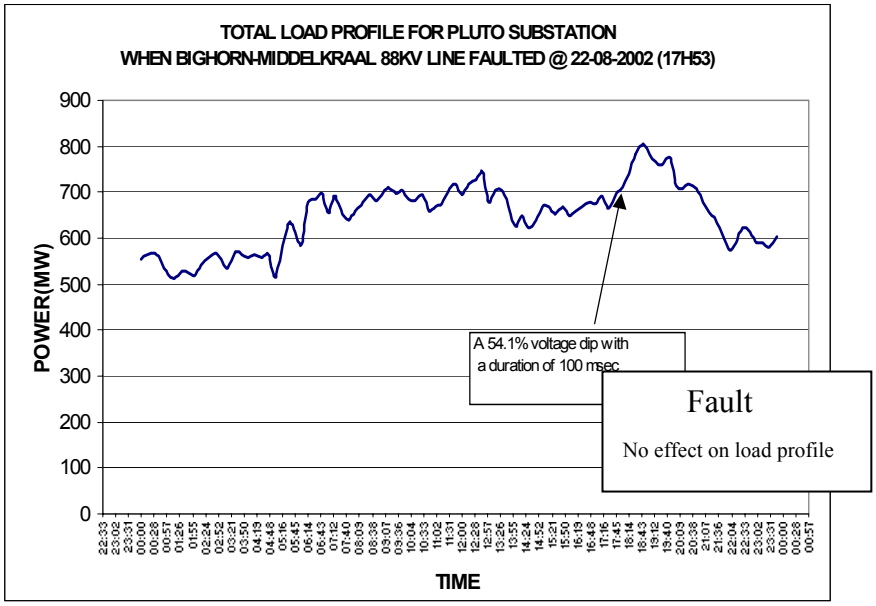


Figure A-1-5 Fault on Bighorn-Middelkraal 88kV line (on 23 May 2002 at 12:58:00)

The above load profiles indicate that for the fault on Bighorn-Middelkraal 88KV line (on 23 May 2002 at 12h58), there was no effect on the load profile at Spitskop Substation; however there was a total of 403.75 MWH unserved energy which consisted of the 222.75 MWH unserved energy at Bighorn Substation, 19.5 MWH unserved energy at Trident Substation, and 161.75 MWH unserved energy at Pluto Substation. The unserved energy for each load profile was calculated using the method explained in section 1.4 of this report.


TOTAL LOAD PROFILE FOR BIGHORN SUBSTATION
WHEN BIGHORN-MIDDELKRAAL 88KV LINE FAULTED @ 22-08-2002 (17H53)
POWER(MW)
TIME
No effect on load profile
A 54.1% voltage dip with a duration of 100 msec. No unserved energy.


TOTAL LOAD PROFILE FOR PLUTO SUBSTATION
WHEN BIGHORN-MIDDELKRAAL 88KV LINE FAULTED @ 22-08-2002 (17H53)
POWER(MW)
TIME
A 54.1% voltage dip with a duration of 100 msec
Fault
No effect on load profile


TOTAL LOAD PROFILE FOR PLUTO SUBSTATION
WHEN BIGHORN-MIDDELKRAAL 88KV LINE FAULTED @ 22-08-2002 (17H53)
POWER(MW)
TIME
A 54.1% voltage dip with a duration of 100 msec
Fault
No effect on load profile

P.T.O.

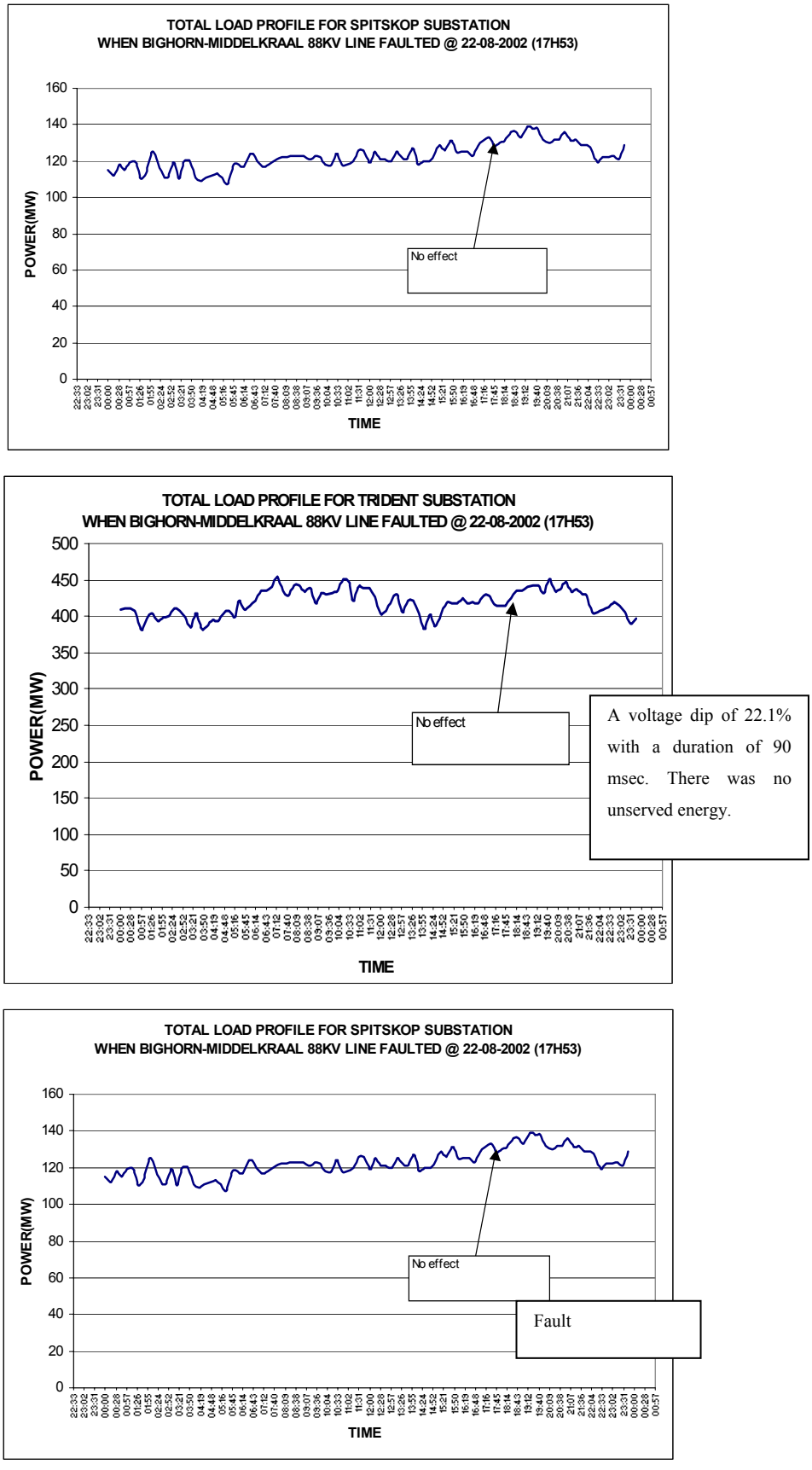


Figure A-1-6 Fault on Bighorn-Middelkraal 88kV line (ON 22 August 2002 AT 17H53)

For the fault on Bighorn-Middelkraal 88KV line (on 22 August 2002 at 17h53), the load profiles for Bighorn, Trident, Spitskop and Pluto Substations indicated that there was no effect on the load profiles and thus there was no unserved energy. Thus, it can be seen that not all faults lead to an unserved energy situation. The severity of the fault, as well as the type of load, will determine whether or not an unserved energy situation will result.

A.3.3 Estimation of the cost of unserved energy

Selected major customers who are supplied from the Bighorn, Trident, Ararat and Spitskop network were interviewed to ascertain the extent and severity of power quality problems experienced and to determine the cost of voltage dips and power interruptions on their operations.

It was established that the costs range between R2.46/kWh for instantaneous dips and R20.13/kWh for long duration interruptions in Ferrochrome mining operations. The results for Platinum mining operations ranged between R21/kWH for instantaneous dips and R214/kWh for long duration power outages. These results indicate that Ferrochrome and Platinum producers are more severely affected by the duration of the dip as compared to the frequency of interruption.

For the purpose of this report, the Cost of Unserved energy figure of R21/kWh is used based.

4 Faults on Bighorn-Middelkraal 88 kV line		
Customer Costs		
Cost of Unserved Energy		Amount:
Substation	MWH lost	
Bighorn	222.75	R4 677 750.00
Trident	19.5	R409 500.00
Pluto	161.5	R3 391 500.00
Spitskop	0	0
= >Total MWH lost	403.75	R8 478 750
Total Customer Costs (@ R21000/MWH)		R8 478 750

Table A-10 Faults on Bighorn-Middelkraal 88 kV line

A.3.4 Eskom costs

Effect of Through-Faults on Transmission Transformers (Table A-11)

4 Faults on Bighorn-Middelkraal 88 kV line	
Eskom Costs	
Helicopter Patrol	R7 560
Ground Patrol	R1 736.36
Travel and Subsistence	R3 600
1 Breaker Maintenance Costs	R0
Table Continued…	
1 CT Maintenance Costs	R0
Transformer Damage Costs	R200 000
Total Eskom Costs	R212 896.36
Total Cost of 4 Faults (i.e. Customer & Eskom costs)	R8 691 646.36

Table A-11 Faults on Bighorn-Middelkraal 88 kV line

These costs are assumed low pending further research.

A.4 Case study 4:

Stone on Water Surface Study for a fault on Avon-Impala 275 kv line.

A.4.1 Lsit of faults for 2001

There was 1 fault for 2000 and 4 faults reported in 2001.

1	2	3	4	5	6	7
START_DT	EQUIP_DESCRIPTION	REASON	REGION	kV	Actual Month	Year
10/10/00 12:51	Avon - Impala No1 275kV Line	Fire - Cane	Eastern	275	2000.10	2000
5/22/01 7:03	Avon - Impala No1 275kV Line	Fire - Cane	Eastern	275	2001.05	2001
5/24/01 1:23	Avon - Impala No1 275kV Line	Under Investigation	Eastern	275	2001.05	2001
9/14/01 3:10	Avon - Impala No1 275kV Line	Under Investigation	Eastern	275	2001.09	2001
9/24/01 6:18	Avon - Impala No1 275kV Line	Fire - Cane	Eastern	275	2001.09	2001

Table A-12 ransmission Line Performance information for Avon-Impala No.1 275kV

A.4.2 Quality of supply (QOS) information for the affected substations

The information which follows includes the QOS data for each substation. Note: The highlighted QOS information in the table below indicates which faults were studied.

1	2	3	4	5	6	7	8
Name	Dip Date	Dip Time	Max Depth	Max Duration	Class	Cause	Effect on Load Profile
QOS information for Impala Substation							
Impala 275/132kV	22-May-01	7:02	16.3	240	Y	Cane Fire	Checked -No effect
Impala 275/132kV	24-May-01	1:22	47.3	70	X	Unknown	Checked -No effect
Impala 275/132kV	24-Sep-01	6:17	57.1	70	X	Cane Fire	Checked -No effect
Impala 275/132kV	11-Jun-02	7:25	36.5	60	X	Cane Fire	Assumed no effect
Impala 275/132kV	26-Jun-02	19:31	23.7	80	X	Cane Fire	Assumed no effect
Impala 275/132kV	09-Jul-02	9:13	19.7	90	Y	Cane Fire	Assumed no effect
QOS information for Avon Substation							
Avon 275/132kV	22-May-01	7:02	29.2	250	S	Cane Fire	Checked -No effect
Avon 275/132kV	24-May-01	1:22	28.3	60	X	Unknown	Checked -No effect
Avon 275/132kV	24-Sep-01	6:17	30.3	80	X	Cane Fire	Checked -No effect
Avon 275/132kV	11-Jun-02	7:25	38.3	70	X	Cane Fire	Assumed no effect
Avon 275/132kV	26-Jun-02	19:31	31	80	X	Cane Fire	Assumed no effect
Avon 275/132kV	09-Jul-02	9:13	34.6	80	X	Cane Fire	Assumed no effect
QOS information for Mersey Substation							
Mersey 400/132kV	22-May-01	7:02	20.1	230	S	Cane Fire	Checked -No effect
Table Continued…							
Mersey 400/132kV	24-May-01	1:22	18.6	60	Y	Unknown	Checked -No effect
Mersey 400/132kV	24-Sep-01	6:17	22.3	70	X	Cane Fire	Checked -No effect
Mersey 400/132kV	11-Jun-02	7:23	25.9	60	X	Cane Fire	Assumed no effect
Mersey 400/132kV	11-Jun-02	7:23	26.5	70	X	Cane Fire	Assumed no effect
Mersey 400/132kV	9-Jul-02	9:13	19.3	50	Y	Cane Fire	Assumed no effect

Table A-13 Quality of Supply Information for affected Substations

A.4.3 Load profiles for affected substations

The ENCOR database keeps records of the instantaneous snapshots (taken every 15 minutes) of the real time network. The results stored in this database are used to generate load profiles of the network at specific locations.

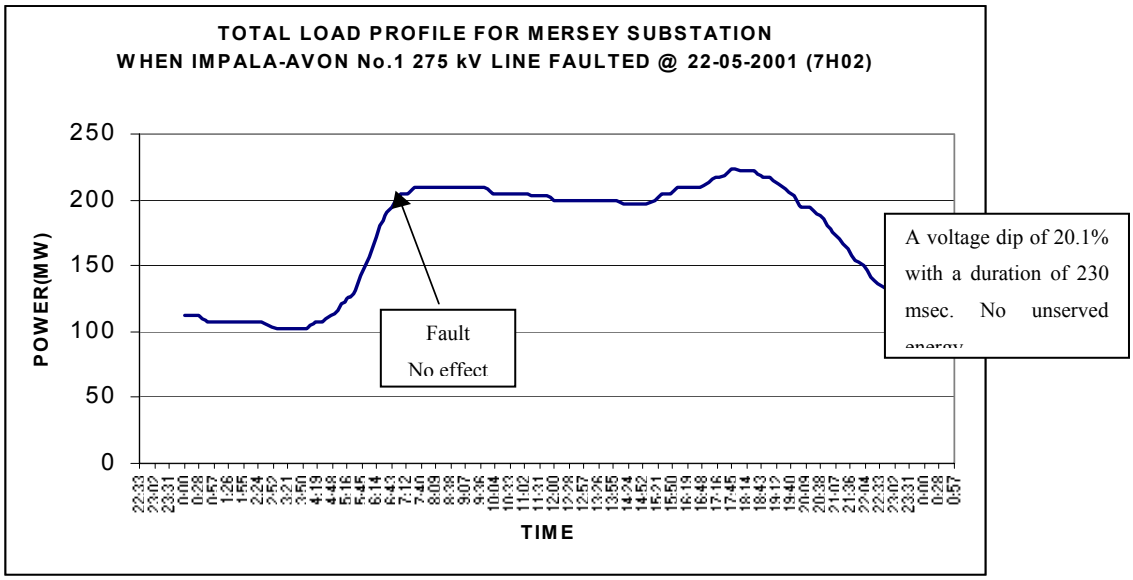


Figure A-1-7 Fault on Avon-Impala No.1 275 kV line (on 22 May 2001 at 07:02)

For the fault on Impala-Avon 275KV line (on 22 May 2001 at 07h02), the load profiles for Impala, Avon and Mersey Substations indicated that there was no effect on the load profiles and thus there was no unserved energy. Thus, it can be seen that not all faults lead to an unserved energy situation. The severity of the fault, as well as the type of load, will determine whether or not an unserved energy situation will result. The load profiles for the other highlighted faults on the Avon-Impala 275 kV line were also studied and the results were similar to that above (that is, there were no effect on the load profiles, and hence no unserved energy in these cases).

A.4.4 Estimation of the cost of unserved energy

3 Faults on Avon-Impala No.1 275 kV line		
Customer Costs		
Cost of Unserved Energy		Amount:
Substation	MWH lost	
Impala	0	0
Avon	0	0
Mersey	0	0
= >Total MWH lost	0	0
1Total Customer Costs (@ R10000/MWH)		R0

Table A-14 Faults on Avon-Impala No.1 275 kV line

The rate of R10000/MWH was assumed for now. Further analysis of the customer surveys would reveal a more accurate calculation rate (I.e. No customer interviews were conducted for this network).

A.4.5 Eskom costs

Effect of Through-Faults on Transmission Transformers

3 Faults on Avon-Impala No.1 275 kV line	
Eskom Costs	
Helicopter Patrol	R5 670
Ground Patrol	R919.03
Travel and Subsistence	R2 700
2 Breaker Maintenance Costs	R0
2 CT Maintenance Costs	R0
Transformer Damage Costs	R150 000
Total Eskom Costs	R159 289.03
Total Cost of 3 Faults (i.e. Customer & Eskom costs)	R159 289.03

Table A-15 Faults on Avon-Impala No.1 275 kV line

APPENDIX B Appendix B - Source Code

B.1 MATLAB source code

B.1.1 Matlab Program to find total harmonic distortion

```
% Matlab Program to find the total harmonic distortion (THD)
% for differnt multilevel levels and dip depths
% Martin Becker
% 8 May 2003
% ooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooo

for dip = 10:1:60                               %Dip depth from 10% to 60%
    for level = 10:1:80                             %Capacitor Voltage 20 - 60V
        x = 0:100e-6:1-100e-6;                      %Take 10000 samples in 1 second
        Vin = (325-325*(dip/100)).*sin(2*pi*50*x);  %Input Voltage minus dip
        n = round(325*(dip/100)/level);             %Determine how many inverter levels
                                                    %should be switched
        y = n*sin(2*pi*50*x);
        z = level*round(y);                         %Series total inverter voltage
        Vout = Vin+z;                               %Output voltage
        b = fft(Vout);                              %Work out THD of output voltage
                                                    %by using an fast fourier transform (fft)
        c = b;
        c(51) = 0;                                  %Remove the main 50Hz component
        c(9951) = 0;
        p_harm = sqrt(sum(abs(c).^2));              %Sum up all distortion harmonics
        p_des = abs(b(51)) + abs(b(9951));
        THD(dip,level) = p_harm/p_des*100;          %Save THD in matrix
        OUT(dip,level) = (220-220*(dip))+n*level;   %Resulting Output Voltage Waveform
    end
end

[x,y] = meshgrid(10:1:60, 20:1:60);                 %Plot the graph with meshgrid
mesh(THD);

ylabel('Dip Depth %');                          %Label the graph
xlabel('Per Step Capacitor Voltage (V)');
zlabel('THD in %');
```

B.1.2 Matlab program to calculte balancing currents

```
% Program that plots the resulting balancing currents between two
% modules for different values of R (Resistance) and C (Capacitance)
% Martin Becker
% 8 May 2003
% ooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooo

clear;
t = 10e-3;                                      %Discharge time of 10ms
Il = 75;                                        %RMS discharge current

for C = 1:1:500                                 %1mF to 500mF
    for R = 1:1:100                             %1mOhm to 100mOhm
        I(R,C) = Il*sqrt(2)*t/(C/1000*R/1000);  %Equation 4.9 in Chapter 4
        if I(R,C) > 2000                        %Don't plot if resulting current
            I(R,C) = Inf;                       %more than 2000A
        end
    end
end

[x,y] = meshgrid(3:1:100, 10:1:500);            %Plot the graph
mesh(I);
```

B.1.3 Matlab code to calculate the voltage drop due to insufficient balancing

```
% Program to find the voltage drop experienced between two modules
% during balancing with only resticted balancing time after each discharge
% Martin Becker
% 8 May 2003
```

```
% oooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooo

clear;
t = 10e-3;                                          %Discharge time 10ms
Il = 75;                                            %Discharge currents 75A (RMS)

for C = 1:1:500                                     %1mF to 500mF
    for R = 1:1:100                                 %1mOhm to 100mOhm
        Einit = Il*sqrt(2)*t/(C/1000);              %Initial voltage drop after
                                                    %discharge
        for It = 1:10                               %Calculate voltage drop after 10
                                                    %cycles
            Vc(It) = Einit *(1-exp(-t/(R/1000*C/1000)));    %Voltage gained during balanceing
            Einit = (Il*sqrt(2)*t/(C/1000) - Vc(It)) + Einit;
            %Cap voltage before next discharge
        end
        Vd(R,C) = Einit - Il*sqrt(2)*t/(C/1000);    %Voltage drop after 10 cycles for certain
                                                    %R and C values.
    end
end

[x,y] = meshgrid(3:1:100, 10:1:500);                 %Plot the graph
mesh(Vd);
```

B.2 C source code

B.2.1 Weighted Least Squares Estimation Algorithm

```
/*****************************************************************************/
/* Weighted Least sqaures algortihm used to find amplitude, phase and frequency
/* of the input signal. For this function a string of variables needs to be
/* stored in a structure 'Line_Data' pointed to by 'Data'. The input arguement
/* is the latest sample of the signal to be analyzed. The resuslts obtained
/* are stored in the stuctures named 'Structure'.Phase , 'Structure'.Amplitude or
/* 'Structure'.Frequency. These are global structures and may be accesssed anywhere
/* in the program.
/*****************************************************************************/


void WLSE(Line_Data *Data, float Line_Volt){

  float P00N, P01N, P10N, P11N;      /* Non global variables needed in func*/
  float x0_new, x1_new, k0, k1;
  float error, r, e_new;

  /* H is a global variable which stores the reference vector. H[0] is the
  real component while H[1] is the imaginary component of the rotating vector*/

    error = abs(Line_Volt - (H[0]*Data->x0 + H[1]*Data->x1));

    /* The error gives the difference between the estimated value
    and the actual sample*/

    if (error > 0.20 * Ref_Volt){       /* If the error is greater than 20%
                                        the covariance variables are reset*/
      Data->P00  = p1;
      Data->P01  = 0;
      Data->P10  = 0;
    Data->P11  = p1;
    Data->q  = Nw;                  /* Here Nw is a large number between 30 and 300
                    This is the amout of samples waited before
                    frequency of reference siganl is altered  */
  }
  else{
    Data->q--;                          /* If the signal is still within tolerable range
                    subtract q-1*/
  }

/*****************************************************************************/
  /* This section is the actual WLSE algorithm. It is out into matrix format */

  r = 1 + H[0]*H[0]*Data->P00 + H[1]*H[0]*Data->P10
        + H[0]*H[1]*Data->P01 + H[1]*H[1]*Data->P11;

  k0 = (Data->P00*H[0]+Data->P01*H[1])*1/r;
  k1 = (Data->P10*H[0]+Data->P11*H[1])*1/r;

  P00N = 1/Y*Data->P00 - 1/Y*(k0*H[0]*Data->P00 + k0*H[1]*Data->P10);
  P01N = 1/Y*Data->P01 - 1/Y*(k0*H[0]*Data->P01 + k0*H[1]*Data->P11);
  P10N = 1/Y*Data->P10 - 1/Y*(k1*H[0]*Data->P00 + k1*H[1]*Data->P10);
  P11N = 1/Y*Data->P11 - 1/Y*(k1*H[0]*Data->P01 + k1*H[1]*Data->P11);

  /* x0_new and x1_new are the new vector components (real, imaginary) of the
  stationary estimated vector of the sampled signal*/

  x0_new = Data->x0 + k0*(Line_Volt - (H[0]*Data->x0 + H[1]*Data->x1));
  x1_new = Data->x1 + k1*(Line_Volt - (H[0]*Data->x0 + H[1]*Data->x1));

/*****************************************************************************/
```

```
  /* Here the phase and amplitude are extracted from the statioary vector*/

  Data->Phase = atan2(x1_new, x0_new);
  Data->Amplitude = x0_new/(cos(Data->Phase));

/*****************************************************************************/
  /* This is the frequency detection algorithm. Here the difference between the
  previous and the current estimated phase suggests that the refernece frequency
  could be wrong. This however is only analyszed when the value q is zero; only after
  the estameted error is less than 20% for Nw cycles the frequency is adjusted*/

  if (Data->q <= 0){
    e_new = Data->Phase - atan2(Data->x1, Data->x0);
    Data->q = 0;
  }
  else {
    e_new = 0;
  }

  /* This is the feedback loop to detect frequency. The change in phase is used
  to estaimate the frequecy. When the estmated signal phase is non-zero the
  frequency is increased slightly till its phase is zero */

  Data->Frequency = Data->Frequency + Kp*e_new + Ki*Data->e_old + Kw*Data->Phase;

  /* The expected signal frequency in this application has either 50 or 60 Hz
  frequency. If it deviates too much it is reset*/

  if ((Data->Frequency > 70*2*pi) | (Data->Frequency < 40*2*pi))
    Data->Frequency = 50*2*pi;

/*****************************************************************************/
/* These values are stored until the next sample of the input signal is available*/

  Data->P00    = P00N;
  Data->P01    = P01N;
  Data->P10      = P10N;
  Data->P11    = P11N;
  Data->x0       = x0_new;
  Data->x1       = x1_new;
  Data->e_old    = e_new;
}
/*****************************************************************************/
```

B.3 VHDL source code

B.3.1 Optical Serial Transmission – Sender

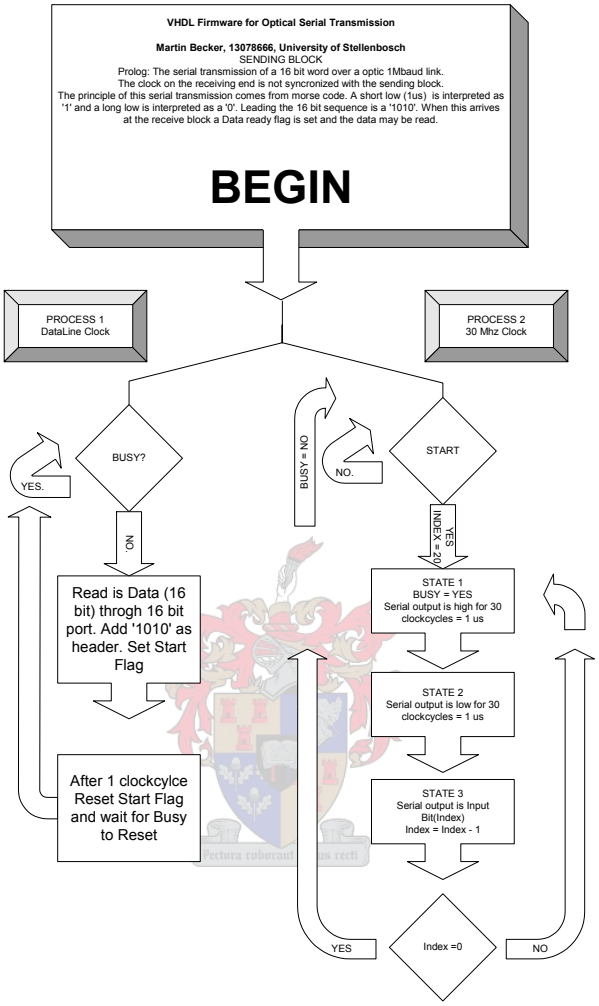


Figure A-1-8 Program flow diagram for VHDL Optical Sender

```
-- ********************************************************************************************
-- VHDL created by Martin Becker, PEG, University of Stellenbscoh
-- This module sends serial data from 16 bit strings
-- Date: June 2003
-- clk30(frequency) = 30 MHz
-- clk75(frequency) = 75 Mhz
--
--
-- All bits need to be led by a high followed by a low. The period between this transition
-- and the next high transition determines weather a '0' or a '1' is transmitted.
-- The maximum transfer speed is limited by the optic fiber transmission to 1Mbs.
--     1 / 1Mbs = 1us
-- The priciple is simple when thinking of morse code. A 0 lasting for more than 1us
-- is interpreted as a '0'. A 0 lasting 0 to 1us is a '1'.
--
--    ___    _____       ____     ____
--      |    |    |      |   |
--      |____| => '1'     |_______| => '0'
--     1us             2us
--
-- To start a bit transmission a '1010' has to be sent before the 16 bit string is sent.
-- Each bit is rotated out of a 20 bit buffer.
--
-- ********************************************************************************************
```

```
library ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

entity optic_send is
  PORT(
    clk75          : IN  STD_LOGIC;           -- Input clock (75 Mhz)
    clk30          : IN  STD_LOGIC;           -- Input clock (30 Mhz)
    Data_Ready       : IN  STD_LOGIC;           -- Data ready flag
    DataIn           : IN  STD_LOGIC_VECTOR(15 downto 0); -- 16 bit data input
    nReset           : IN    STD_LOGIC;           -- (not) reset
    DataVOut         : OUT   STD_LOGIC);            -- serial data out

end entity optic_send;


ARCHITECTURE net OF optic_send is

  TYPE STATE_TYPE IS (Initialize, Init_Write, Zero_One);
  SIGNAL state           : STATE_TYPE;

  SIGNAL Start_Stream, Busy_Stream  : STD_LOGIC;
  SIGNAL Data_Buff         : STD_LOGIC_VECTOR(19 downto 0);-- temporary data buffer


BEGIN


-- To optimize performance on the PEC33 controller board the data can be read with DSP
-- speed of 75Mhz. The actual sending is operating at fpga clock which is 30Mhz.

d_sync: PROCESS (Data_Ready, clk75)

  BEGIN
    IF rising_edge(clk75) THEN
      IF Busy_Stream = '0' THEN         -- All previous data has been sent
        IF Data_Ready = '1' THEN        -- Read data to databuff when ready
          Data_Buff(15 downto 0) <= DataIn;
          Data_Buff(19 downto 16) <= "1010";  -- Four control bits for serial transmission
          Start_Stream <= '1';        -- Start serial transmission
        END IF;
      ELSE
        Start_Stream <= '0';
      END IF;
    END IF;

  END PROCESS d_sync;


-- This is the actual serial transmission operating on a 30 Mhz clock.
-- The transmission speed on a 1Mbaud
-- optical fiber is 16bits per 60us

d_async: PROCESS (clk30, nReset)

  VARIABLE Counter : INTEGER RANGE 0 TO 60;      -- These are clock cycle couters to
                             -- create a signal that can be sent over
                             -- a 1MBaud optical link.
  VARIABLE Index   : INTEGER RANGE 0 TO 19;      -- This is an idex of the 20 bit temporary
                             -- databuff

  BEGIN
    IF nReset = '0' THEN
      state <= Initialize;
    ELSIF rising_edge(clk30) THEN

      CASE state IS

        WHEN Initialize =>          -- Here all variables are reset. The sysyem is ready.
          DataVOut <= '1';        -- Reset output data
          Busy_Stream <= '0';       -- Accnoledge new input data
          Index := 19;
          Counter := 0;
          IF Start_Stream = '1' THEN    -- When new input data is received go to next state
            state <= Init_Write;
          END IF;

        WHEN Init_Write =>
          Busy_Stream <= '1';       -- System is busy transmitting string
          Counter := Counter +1;
          IF Counter = 30 THEN        -- Changed from 60 to 30 3 june 04
            Counter := 0;
            DataVOut <= '0';      -- Send a zero pulse for 30 clock cycles
            state <= Zero_One;      -- go to next state
          END IF;

        WHEN Zero_One =>
          Counter := Counter +1;

          IF Counter = 30 THEN
            DataVOut <= Data_Buff(Index);  -- Here the actual current bit is sent
                        -- for 30 clock cycles
          END IF;

          IF Counter = 60 THEN      -- After 60 clock cycles the transmission is
                         -- complete so a 1 is sent till the next databit
                         -- can be sent
```

```
            IF Index = 0 THEN      -- The next databit is taken until index =0 then
                                   -- all databits have been sent
              State <= Initialize;
            ELSE
              State <= Init_Write;
              Counter := 0;
              DataVOut <= '1';
              Index:= Index -1;
            END IF;
          END IF;

      END CASE;
    END IF;
  END PROCESS d_async;
END ARCHITECTURE net;
```

B.3.2 Optical Serial Transmission – Receiver

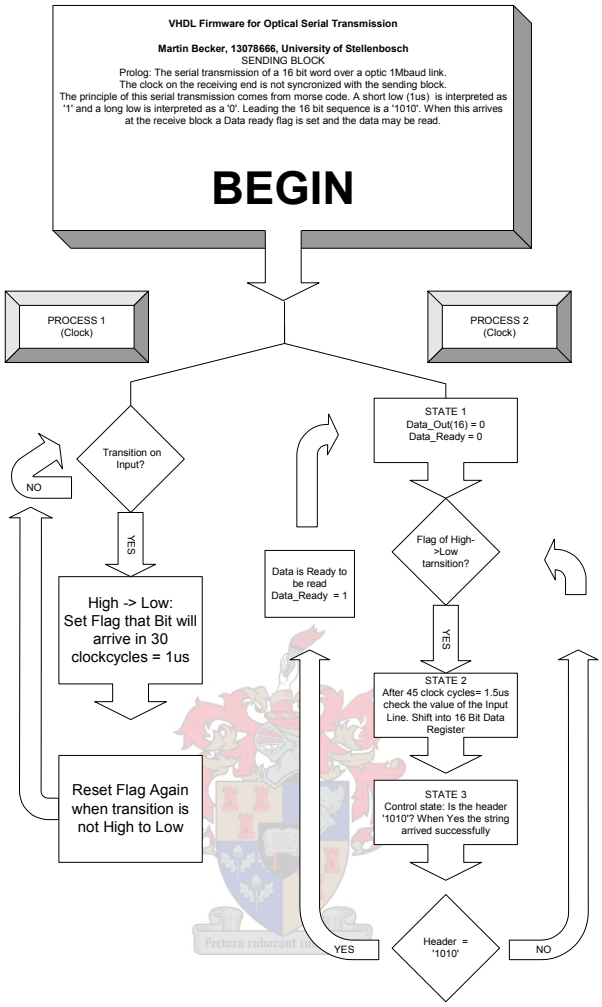


Figure A-1-9 Program flow diagram for VHDL Optical Receiver

```
-- ************************************************************************************************
-- VHDL created by Martin Becker, PEG, University of Stellenbscoh
-- This module receives asyncronous data and interprets it into 16 bit strings
-- Date: June 2003
-- clk30(frequency) = 30 MHz
--
--
-- All bits need to be led by a high followed by a low. The period between this transition
-- and the next high transition determines weather a '0' or a '1' has been transmitted.
-- The maximum transfer speed is limited by the optic fiber transmission to 1Mbs.
--     1 / 1Mbs = 1us
-- The priciple is simple when thinking of morse code. A 0 lasting for more than 1us
-- is interpreted as a '0'. A 0 lasting 0 to 1us is a '1'.
--
--   ___     _____     ____          ____
--      |___|     => '1'     |_______|     => '0'
--     1us             2us
--
-- To start a bit transmission a '1010' has to be sent before the 16 bit string is sent.
-- Each bit is rotated into a 20 bit buffer. When the top four bits are read as '1010' a
-- data_ready flag is set high for 1 clock cycle. During this time the data on the data line
-- is valid.
--
-- ************************************************************************************************

library ieee;
USE ieee.std_logic_1164.all;
```

```
USE ieee.std_logic_arith.all;

entity receive2 is
  PORT(
    clk           : IN  STD_LOGIC;     -- Input clock (30 Mhz)
    DataIn          : IN  STD_LOGIC;     -- Serial Asyncronous Data Input
    DataVOut        : OUT   STD_LOGIC_VECTOR(15 downto 0); -- Syncronous 16 bit Data
    Data_Ready        : OUT   STD_LOGIC;     -- Data valid flag
    Error_Out       : Buffer   STD_LOGIC);     -- Error Flag

  end entity receive2 ;


ARCHITECTURE net OF receive2 is

  TYPE STATE_TYPE IS (Initialize, Wait_state, Write_state, Control_state, Dummy);
  SIGNAL state          : STATE_TYPE;
  SIGNAL EndTimer, SetTimer   : STD_LOGIC;

BEGIN

-- ***********************************************************************************************
-- This process has events that occur on a input bit transition. When a high followed by a low
-- is detected the timer will run to establish weather the siganl transmitted is a '1' or a '0'

read: PROCESS (clk, Endtimer, Error_Out)

  VARIABLE DataInOld       : STD_LOGIC;

  BEGIN
    IF Endtimer = '1' OR Error_Out = '1' THEN
      SetTimer <= '0';
    ELSIF rising_edge(clk) THEN
      IF DataIn /= DataInOld THEN
        IF DataIn = '0' THEN
          SetTimer <= '1';
        END IF;
        DataInOld := DataIn;
      END IF;
    END IF;
  END PROCESS read;

-- ***********************************************************************************************
-- This process runs a timer and determines wheather optical plug is in or not. In the later event
-- An pulse will be sent every 1000 clockcycles to Error_Out.

err_det: PROCESS (clk)

  VARIABLE Err_Counter : integer RANGE 0 TO 1000;

  BEGIN
    IF rising_edge(clk) THEN
      IF DataIn = '0' THEN
        Err_Counter := Err_Counter +1;
      ELSE
        Err_Counter := 0;
      END IF;
      IF Err_Counter = 1000 THEN
        Error_Out <= '1';
      ELSE
        Error_Out <= '0';
      END IF;
    END IF;
  END PROCESS err_det;

-- ***********************************************************************************************
-- This process runs a timer and determines wheather 16 bits have been received or not.

sync: PROCESS (clk, Error_Out)

  VARIABLE Data    : STD_LOGIC_VECTOR(19 downto 0);
  VARIABLE Counter : INTEGER RANGE 0 TO 90;

  BEGIN
    IF Error_Out = '1' THEN
      state <= Initialize;
      DataVOut <= (others => '0');

    ELSIF rising_edge(clk) THEN

      CASE state IS

        WHEN Initialize =>
          Data_Ready <= '0';       -- Reset data ready flag
          Data := (others => '0'); -- All data bits are made '0'
          state <= Wait_state;

        WHEN Wait_state =>
          EndTimer <= '0';       -- This flag is set when the timer runs out
          Counter := 0;          -- The counter monitors time elapsed from high to low
          IF SetTimer = '1' THEN    -- When a high - low transition occured start timer
            state <= Write_state;
          END IF;

        WHEN Write_state =>
          Counter := Counter +1;    -- Each clock cycle the counter is incremented
          IF Counter = 45 THEN    -- After 45 clockcycles (1.5us) the transmited
                          -- value may be read
            Data := Data(18 DOWNTO 0) & DataIn;  -- The bit is shifted into memory
```

```
            state <= Control_state;
            EndTimer <= '1';    -- The timer has run out
          END IF;

        WHEN Control_state =>
          IF Data(19 downto 16) = "1010" THEN  -- Test weather the whole bitstream has
                                               -- been sent
            state <= Dummy;          -- Leave valid data for 1 cycle on data line
            DataVOut <= Data(15 downto 0);
          ELSE
            state <= Wait_state;
          END IF;

        WHEN Dummy =>
          Data_Ready <= '1';
          state <= Initialize;

      END CASE;
    END IF;
  END PROCESS sync;
END ARCHITECTURE net;
```

B.3.3 Index Creation Block for Safe Switching Matrix

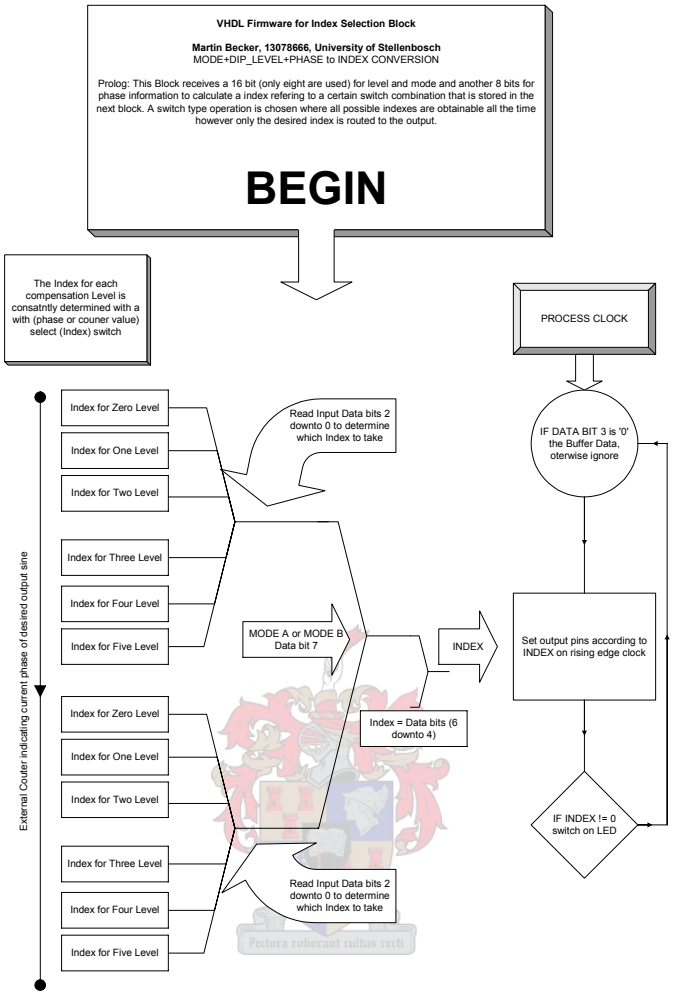


Figure A-1-10 Program flow diagram for VHDL Index Selector

```
-- ************************************************************************************************
-- VHDL created by Martin Becker, PEG, University of Stellenbscoh
-- This module receives a 16 string of which only the lowest 8 are used.
-- The 16 bit string from the DSP contains Data on how many levels should
-- be switched on and in which MODE (A or B) (least significant 8 bits) and
-- at what instant of the one cycle (0' to 360') should it start now (most 8
-- significant bits).
-- Date: March 2004
-- clk30(frequency) = 30 MHz
--
-- Input to this block:
--     16 bits of which only the lowest 8 are used to determine how many
--     levels or if the circuit should be idle, recharge, discharge or off.
--   8 bits giving the current instant in time as to where the DSP reference
--     desires it to be.
--   30 Mhz clock and nReset pin
-- Output of this block:
--     6 bit string containing a number between 1 to 53. This is the index.
--     A matrix stored in the next block contains all possible allowable switch
--   combinations. The index is a pointer that selects a current switch combination
--
-- Usage:
--
-- 16 bit input sting:
-- "XXXX XXXX MRRR OLLL"
-- X = Current position in cycle. Not used on this input.
-- M = Mode ('1' Would be MODE A which means both TOP and BOTTOM switch are closed
--     during recharge,
--      '0' Would be MODE B which only uses the BOT (in positive module) and BOTTOM
```

```
--      (in negative module) for recharging caps. This MODE is useful only
--      with resistive Loads. Inductive loads might cause problems.
-- RRR = Charge, Idle and Off modes.
--     000 - Off.
--     001 -   Bypass.
--     010 -   Off but recharge Caps in Mode A.
--     011 -   Off but recharge Caps in Mode B.
--     100 -   Bypass and recharge Caps in Mode A.
--     101 - Bypass and recharge Caps in Mode B.
--     110 - Dump all voltage inside caps and SCap when connected.
--     111 - Allows Stages 0 - 3 to switch on. (Normal Operation)
-- 0 Must always be '0' when Data is intended for this block. Is 1 when
--     frequency is set in different block for example.
-- LLL = Amount of levels to switch on maximally.
--     000 =   Zero levels so output voltage is zero always. Same as Bypass with
--         Recharge Caps.
--     001 to 100 = Binary count of Maximum Levels to insert serially into line.
--     The actual output volatge in Levels also depends on the instant in cycle.
--
-- 8 Bit input string:
--   Instant in Time of Cycle.
-- 00 (Hex) is zero degrees where FF (Hex) would be 358.6 degerees
-- ************************************************************************************************


LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;


ENTITY MLI_select IS
  PORT (  clk             : in std_logic;
      nReset            : in std_logic;
      Data            : in std_logic_vector(15 downto 0);  -- 16 bit string from DSP
      Data_Ready          : in std_logic;
      ExtCounter          : in std_logic_vector(7 downto 0);  -- 8 bit string giving instant in time
      Run_Led           : out std_logic;          -- Is On when switches are not all zero
      TapIndex          : out std_logic_vector(5 downto 0) -- Index to allowable switch table
  );

END ENTITY MLI_select;

ARCHITECTURE net OF MLI_select IS

  SIGNAL TapIndexNew, Tap_Index, TapIndex0, TapIndex1, TapIndex2, TapIndex3, TapIndex4, TapIndex5,
   TapIndex0A, TapIndex0B, TapIndex1A, TapIndex1B, TapIndex2A, TapIndex2B,
   TapIndex3A, TapIndex3B, TapIndex4A, TapIndex4B, TapIndex5A, TapIndex5B          : integer RANGE 1 TO
53;
  SIGNAL Counter                                  : integer RANGE 0 TO 255;
  SIGNAL Data_Buff                                : std_logic_vector(7 downto 0);

  -- The Const_Table contains all value (number of clockcycles) after which a transition
  -- takes place from one stage to the next.
  TYPE Const_Table IS ARRAY(1 TO 60) OF integer RANGE 0 TO 256;
  CONSTANT Alpha : Const_Table := (   22, 107, 150, 235,          -- Stage1 1-4
                    11, 35, 94, 118,
                    139, 163, 222, 246,         -- Stage2 5-12
                    7, 22, 41, 88,
                    107, 122, 135, 150,
                    169, 216, 235, 250,         -- Stage3 13-24
                    6, 16, 28, 44,
                    85, 101, 113, 123,
                    134, 144, 156, 172,
                    213, 229, 241, 251,         -- Stage4 25-40
                    5, 13, 22, 32,
                    46, 83, 97, 107,
                    116, 124, 133, 141,
                    150, 160, 174, 211,
                    225, 235, 244, 252);        -- Stage5 41-60


BEGIN

  p0: PROCESS (clk, nReset)

  BEGIN
    IF nReset = '0' THEN
      Data_Buff <= (others => '0');
    ELSIF rising_edge(clk) THEN
      TapIndex <= conv_std_logic_vector(TapIndexNew,6);        -- Convert Integer to binary
      Counter <= conv_integer(unsigned(ExtCounter));          -- The current phase is given by an
external counter
      IF TapIndexNew > 1 THEN                     -- When the system is not OFF the LED should be on
        Run_Led <= '0';
      ELSE
        Run_Led <= '1';
      END IF;
      -- Data_Buff(3) is reserved for other peripherals.
      -- Only when Data_Buff(3) is zero a passage is gained to this block.
      IF Data_Ready = '1' THEN
        IF Data(3) = '0' THEN
          Data_Buff <= Data(7 downto 0);
        END IF;
      END IF;
    END IF;
  END PROCESS p0;
```

```
  WITH Data_Buff(6 downto 4) SELECT          -- The index for the first 7 values may be directly read
from Data
    TapIndexNew <=   (CONV_INTEGER(UNSIGNED(Data_Buff(6 downto 4)))+1) WHEN "110" DOWNTO "000",
            Tap_Index WHEN others;

  WITH Data_Buff(2 downto 0) SELECT
    Tap_Index <=   TapIndex0 WHEN "000",      -- Zero Levels are switched
            TapIndex1 WHEN "001",       -- One Level
            TapIndex2 WHEN "010",       -- Two Level
            TapIndex3 WHEN "011",       -- Three Level
            TapIndex4 WHEN "100",       -- Four Level
            TapIndex5 WHEN "101",       -- Five Level
            1 WHEN others;

  WITH Data_Buff(7) SELECT              -- Zero Levels
    TapIndex0   <=   TapIndex0A WHEN '1',       -- Mode A
            TapIndex0B WHEN '0';       -- Mode B

  WITH Data_Buff(7) SELECT              -- One Level
    TapIndex1   <=   TapIndex1A WHEN '1',       -- Mode A
            TapIndex1B WHen '0';       -- Mode B

  WITH Data_Buff(7) SELECT              -- Two Levels
    TapIndex2   <=   TapIndex2A WHEN '1',       -- Mode A
            TapIndex2B WHen '0';       -- Mode B

  WITH Data_Buff(7) SELECT              -- Three Levels
    TapIndex3   <=   TapIndex3A WHEN '1',       -- Mode A
            TapIndex3B WHen '0';       -- Mode B

  WITH Data_Buff(7) SELECT              -- Four Levels
    TapIndex4   <=   TapIndex4A WHEN '1',       -- Mode A
            TapIndex4B WHen '0';       -- Mode B

  WITH Data_Buff(7) SELECT              -- Five Levels
    TapIndex5   <=   TapIndex5A WHEN '1',       -- Mode A
            TapIndex5B WHen '0';       -- Mode B



  TapIndex0A <= 8;                 -- On zero levels the phase is not considerd
  TapIndex0B <= 9;

  WITH Counter SELECT                   -- One Level Mode A
    TapIndex1A  <=   10 WHEN Alpha(1)+1 TO Alpha(2),
            12 WHEN Alpha(3)+1 TO Alpha(4),
            8   WHEN others;

  WITH Counter SELECT                   -- One Level Mode B
    TapIndex1B  <=   11 WHEN Alpha(1)+1 TO Alpha(2),
            13 WHEN Alpha(3)+1 TO Alpha(4),
            9   WHEN others;

  WITH Counter SELECT
    TapIndex2A  <=   10 WHEN Alpha(5)+1 TO Alpha(6),-- Two Level Mode A
            15 WHEN Alpha(6)+1 TO Alpha(7),
            10 WHEN Alpha(7)+1 TO Alpha(8),
            12   WHEN Alpha(9)+1 TO Alpha(10),
            19 WHEN Alpha(10)+1 TO Alpha(11),
            12 WHEN Alpha(11)+1 TO Alpha(12),
            8   WHEN others;

  WITH Counter SELECT
    TapIndex2B  <=   11 WHEN Alpha(5)+1 TO Alpha(6),-- Two Level Mode B
            17 WHEN Alpha(6)+1 TO Alpha(7),
            11 WHEN Alpha(7)+1 TO Alpha(8),
            13   WHEN Alpha(9)+1 TO Alpha(10),
            21 WHEN Alpha(10)+1 TO Alpha(11),
            13 WHEN Alpha(11)+1 TO Alpha(12),
            9   WHEN others;

  WITH Counter SELECT
    TapIndex3A  <= 10 WHEN Alpha(13)+1 TO Alpha(14),-- Three Level Mode A
            14 WHEN Alpha(14)+1 TO Alpha(15),
            22 WHEN Alpha(15)+1 TO Alpha(16),
            15 WHEN Alpha(16)+1 TO Alpha(17),
            10 WHEN Alpha(17)+1 TO Alpha(18),
            12 WHEN Alpha(19)+1 TO Alpha(20),
            18 WHEN Alpha(20)+1 TO Alpha(21),
            30 WHEN Alpha(21)+1 TO Alpha(22),
            19 WHEN Alpha(22)+1 TO Alpha(23),
            12 WHEN Alpha(23)+1 TO Alpha(24),
            8  WHEN others;

  WITH Counter SELECT
    TapIndex3B  <= 11 WHEN Alpha(13)+1 TO Alpha(14),-- Three Level Mode B
            16 WHEN Alpha(14)+1 TO Alpha(15),
            26 WHEN Alpha(15)+1 TO Alpha(16),
            17 WHEN Alpha(16)+1 TO Alpha(17),
            11 WHEN Alpha(17)+1 TO Alpha(18),
            13 WHEN Alpha(19)+1 TO Alpha(20),
            20 WHEN Alpha(20)+1 TO Alpha(21),
            34 WHEN Alpha(21)+1 TO Alpha(22),
            21 WHEN Alpha(22)+1 TO Alpha(23),
            13 WHEN Alpha(23)+1 TO Alpha(24),
            9  WHEN others;

  WITH Counter SELECT
```

```
    TapIndex4A  <= 10 WHEN Alpha(25)+1 TO Alpha(26),-- Four Level Mode A
            14 WHEN Alpha(26)+1 TO Alpha(27),
            23 WHEN Alpha(27)+1 TO Alpha(28),
            38 WHEN Alpha(28)+1 TO Alpha(29),
            24 WHEN Alpha(29)+1 TO Alpha(30),
            15 WHEN Alpha(30)+1 TO Alpha(31),
            10 WHEN Alpha(31)+1 TO Alpha(32),

            12 WHEN Alpha(33)+1 TO Alpha(34),
            18 WHEN Alpha(34)+1 TO Alpha(35),
            31 WHEN Alpha(35)+1 TO Alpha(36),
            44 WHEN Alpha(36)+1 TO Alpha(37),
            32 WHEN Alpha(37)+1 TO Alpha(38),
            19 WHEN Alpha(38)+1 TO Alpha(39),
            12 WHEN Alpha(39)+1 TO Alpha(40),
            8  WHEN others;

  WITH Counter SELECT
    TapIndex4B  <= 11 WHEN Alpha(25)+1 TO Alpha(26),-- Four Level Mode B
            16 WHEN Alpha(26)+1 TO Alpha(27),
            27 WHEN Alpha(27)+1 TO Alpha(28),
            41 WHEN Alpha(28)+1 TO Alpha(29),
            28 WHEN Alpha(29)+1 TO Alpha(30),
            17 WHEN Alpha(30)+1 TO Alpha(31),
            11 WHEN Alpha(31)+1 TO Alpha(32),

            13 WHEN Alpha(33)+1 TO Alpha(34),
            20 WHEN Alpha(34)+1 TO Alpha(35),
            35 WHEN Alpha(35)+1 TO Alpha(36),
            47 WHEN Alpha(36)+1 TO Alpha(37),
            36 WHEN Alpha(37)+1 TO Alpha(38),
            21 WHEN Alpha(38)+1 TO Alpha(39),
            13 WHEN Alpha(39)+1 TO Alpha(40),
            9  WHEN others;

  WITH Counter SELECT
    TapIndex5A  <= 10 WHEN Alpha(41)+1 TO Alpha(42),-- Five Level Mode A
            14 WHEN Alpha(42)+1 TO Alpha(43),
            23 WHEN Alpha(43)+1 TO Alpha(44),
            39 WHEN Alpha(44)+1 TO Alpha(45),
            50 WHEN Alpha(45)+1 TO Alpha(46),
            40 WHEN Alpha(46)+1 TO Alpha(47),
            25 WHEN Alpha(47)+1 TO Alpha(48),
            15 WHEN Alpha(48)+1 TO Alpha(49),
            10 WHEN Alpha(49)+1 TO Alpha(50),

            12 WHEN Alpha(51)+1 TO Alpha(52),
            18 WHEN Alpha(52)+1 TO Alpha(53),
            31 WHEN Alpha(53)+1 TO Alpha(54),
            45 WHEN Alpha(54)+1 TO Alpha(55),
            52 WHEN Alpha(55)+1 TO Alpha(56),
            46 WHEN Alpha(56)+1 TO Alpha(57),
            33 WHEN Alpha(57)+1 TO Alpha(58),
            19 WHEN Alpha(58)+1 TO Alpha(59),
            12 WHEN Alpha(59)+1 TO Alpha(60),
            8  WHEN others;

  WITH Counter SELECT
    TapIndex5B  <= 11 WHEN Alpha(41)+1 TO Alpha(42),-- Five Level Mode B
            16 WHEN Alpha(42)+1 TO Alpha(43),
            27 WHEN Alpha(43)+1 TO Alpha(44),
            42 WHEN Alpha(44)+1 TO Alpha(45),
            51 WHEN Alpha(45)+1 TO Alpha(46),
            43 WHEN Alpha(46)+1 TO Alpha(47),
            29 WHEN Alpha(47)+1 TO Alpha(48),
            17 WHEN Alpha(48)+1 TO Alpha(49),
            11 WHEN Alpha(49)+1 TO Alpha(50),

            13 WHEN Alpha(51)+1 TO Alpha(52),
            20 WHEN Alpha(52)+1 TO Alpha(53),
            35 WHEN Alpha(53)+1 TO Alpha(54),
            48 WHEN Alpha(54)+1 TO Alpha(55),
            53 WHEN Alpha(55)+1 TO Alpha(56),
            49 WHEN Alpha(56)+1 TO Alpha(57),
            37 WHEN Alpha(57)+1 TO Alpha(58),
            21 WHEN Alpha(58)+1 TO Alpha(59),
            13 WHEN Alpha(59)+1 TO Alpha(60),
            9  WHEN others;

END ARCHITECTURE net;
```

B.3.4 Index interpretation for Safe Switching Matrix

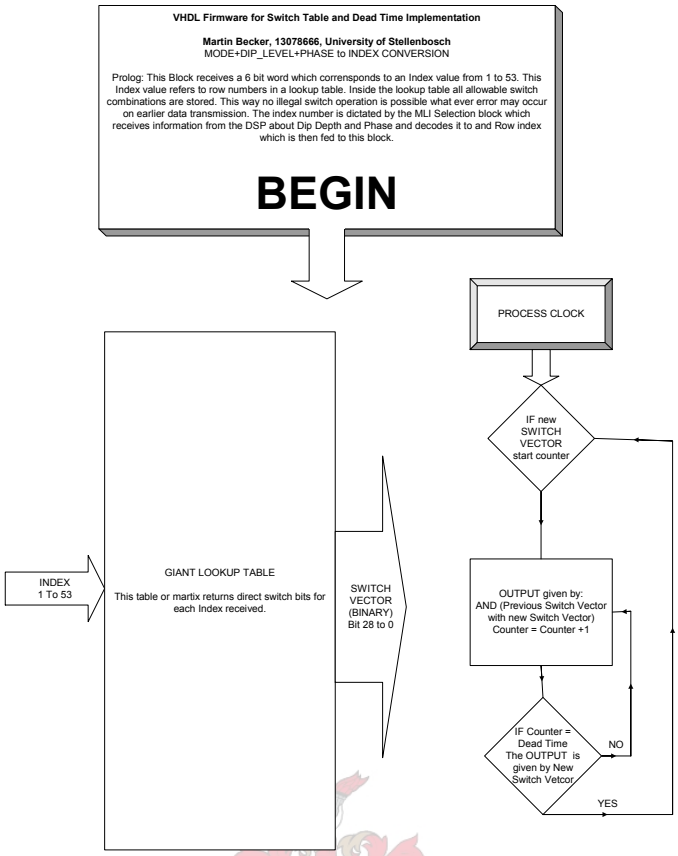


Figure A-1-11 Program flow diagram for VHDL Index Selector

```
-- ************************************************************************************************
-- VHDL created by Martin Becker, PEG, University of Stellenbosch
--
-- This module receives a 6 string of which is an binary index to a switch matrix.
-- Also contained is a variable delay algorithm. Due to the slow response of the
-- MOSFET driving circuit it is desirable to implement quite a lot of dead time between
-- dangerous switch operations. Only a change in switch state will result in dead time
-- impelmented. Other switches will remain unchanged during this dead time implementation.
--
-- Date: March 2004
-- clk30(frequency) = 30 MHz
--
-- Input to this block:
--     6 bits -> index
--   12 bits ->  to set the dead time. The smallest amount of dead time is 0
--         clockcycles -> '000'.
--         The largest ammount is 4096 clock cycles -> 'FFF'.
--   30 Mhz clock and nReset pin
-- Output of this block:
--     29 bit ->   There are 28 swuitches in a five level single phase inverter
--         1 bit to set the realy on and off.
--
-- Usage:
--
-- Refer to Table: "Safe Switching method for Multilevel Inverters using Matrix Table"
-- Table also stored in this FPGA in less undestandable manner. See Code Below:
--
-- ************************************************************************************************


LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;


ENTITY MLI_delay IS
  PORT (  clk             : in std_logic;            -- 30 Mhz Clock
      nReset            : in std_logic;            -- Not Reset
      Dead_Time         : in std_logic_vector(11 downto 0); -- Ammount of Dead Time between swiching
      TapIndexNew         : in std_logic_vector(5 downto 0); -- Index
      switch_vector       : out std_logic_vector(28 downto 0) -- Vector containing siganls for each
switch
  );

END ENTITY MLI_delay;
```

```
ARCHITECTURE net OF MLI_delay IS

  TYPE STATE_TYPE2 IS (Idle, DeadTime);
  SIGNAL State2            : STATE_TYPE2;

  SIGNAL TapIndex          : integer RANGE 1 TO 53;      -- This is the Index Range


  -- The Tap_Table contains all the possible switch variations possible for all 28 switches.
  -- The Most significant bit is the Dump Relay.
  -- Each bit represents one switch. The order is as in "Matrix Table for Multilevel Inverters".
  TYPE Tap_Table IS ARRAY(1 TO 53) OF STD_LOGIC_VECTOR(28 downto 0);
  CONSTANT Taps : Tap_Table := (  "0000000000000000000000000000",  -- 1 - OFF
                  "0011000000000000000000000000",  -- 2 - Bypass
                  "0000010110110110110110110101",  -- 3 - OFF/Charge Mode A
                  "0000000110000110000110000100",  -- 4 - OFF/Charge Mode B
                  "0011010110110110110110110101",  -- 5 - BYPASS/ Charge Mode A
                  "0011000110000110000110000100",  -- 6 - BYPASS/ Charge Mode B
                  "1000001001001001001001001010",    -- 7 - Dump

                  "0011010110110110110110110101",  -- 8 - ZERO(0)A
                  "0011000110000110000110000100",  -- 9 - ZERO(0)B

                  "0110010110110110110110110101",  --10 - POS(1)A
                  "0110000110000110000110000100",  --11 - POS(1)B

                  "0001110110110110110110110101",  --12 - NEG(1)A
                  "0001100110000110000110000100",    --13 - NEG(1)B

                  "0110001010110110110110110101",    --14 - POS(2)A1
                  "0110010110110110110110101101",    --15 - POS(2)A2
                  "0110001010000110000110000100",    --16 - POS(2)B1
                  "0110000110000110000110010100",    --17 - POS(2)B2

                  "0001110101010110110110110101",    --18 - NEG(2)A1
                  "0001110110110110110110101010",    --19 - NEG(2)A2
                  "0001100101000110000110000100",    --20 - NEG(2)B1
                  "0001100110000110000110000010",    --21 - NEG(2)B2

                  "0110001010110110110110101101",  --22 - POS(3)A1
                  "0110001010101010110110110101",  --23 - POS(3)A2
                  "0110010110101010110110101101",  --24 - POS(3)A3
                  "0110010110110110101010101101",  --25 - POS(3)A4

                  "0110001010000110000110010100",  --26 - POS(3)B1
                  "0110001010001010000110000100",  --27 - POS(3)B2
                  "0110000110001010000110010100",  --28 - POS(3)B3
                  "0110000110000110001010010100",  --29 - POS(3)B4

                  "0001110101010110110110110101",  --30 - NEG(3)A1
                  "0001110101010101010110110101",  --31 - NEG(3)A2
                  "0001110110110101010110110101",  --32 - NEG(3)A3
                  "0001110110110110110110101010",  --33 - NEG(3)A4

                  "0001100101000110000110000010",    --34 - NEG(3)B1
                  "0001100101000101000110000100",    --35 - NEG(3)B2
                  "0001100110000101000110000010",    --36 - NEG(3)B3
                  "0001100110000110000101000010",    --37 - NEG(3)B4

                  "0110001010101010110110101101",  --38 - POS(4)A1
                  "0110001010101010101010110101",  --39 - POS(4)A2
                  "0110010110101010101010101101",  --40 - POS(4)A3
                  "0110001010001010000110010100",  --41 - POS(4)B1
                  "0110001010001010001010000100",  --42 - POS(4)B2
                  "0110000110001010010100010100",  --43 - POS(4)B3

                  "0001110101010101010110110101",  --44 - NEG(4)A1
                  "0001110101010101010101010101",  --45 - NEG(4)A2
                  "0001110110110101010101010101",  --46 - NEG(4)A3
                  "0001100101000101000110000010",    --47 - NEG(4)B1
                  "0001100101000101000101000100",    --48 - NEG(4)B2
                  "0001100110000101000101000010",    --49 - NEG(4)B3

                  "0110001010101010101010101101",  --50 - POS(5)A
                  "0110001010001010001010000100",  --51 - POS(5)B
                  "0001110101010101010101010010",  --52 - NEG(5)A
                  "0001100101000101000101000010");   --53 - NEG(5)B


BEGIN

-- ***********************************************************************************************
-- This process (P2) inserts DeadTime between all switching changes

P2:  PROCESS (clk, nReset)

  VARIABLE Delay : integer RANGE 0 TO 4095;          -- How many clockcycles the
                                -- deadtime should be.
  BEGIN
    IF nReset = '0' THEN                    -- When the stop command is
      TapIndex <= 1;                    -- read on data_ln the MLI
      switch_vector <= Taps(1);             -- is switched off immediately
      State2 <= Idle;
    ELSIF rising_edge(clk) THEN
      CASE State2 IS
      -- Normally this process is in Idle. When a transition in switch_vector pattern
      -- is expected the Process goes into DeadTime state to implement deadtime.
        WHEN Idle =>
```

```
          IF TapIndex = conv_integer(unsigned(TapIndexNew)) THEN
            State2 <= Idle;
          ELSE
            Delay := 0;
            State2 <= DeadTime;
          END IF;
        WHEN DeadTime =>
          Delay := Delay +1;
          IF Delay >= conv_integer(unsigned(Dead_Time)) THEN
            State2 <= Idle;
            TapIndex <= conv_integer(unsigned(TapIndexNew));
          END IF;
      END CASE;

      -- A bitwise AND temporarily switches all changig switches off, and leaves others
      -- unchanged.
      switch_vector <= Taps(conv_integer(unsigned(TapIndexNew))) AND Taps(TapIndex);
      -- ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
    END IF;

  END PROCESS;

END ARCHITECTURE net;
```

B.3.5 Index interpretation for Safe Switching Matrix

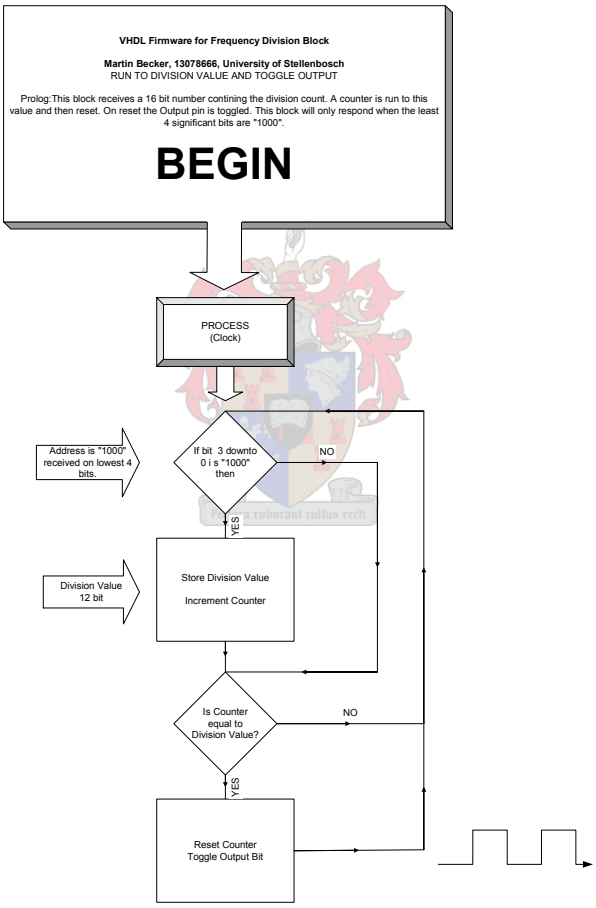


Figure A-1-12 Program flow diagram for VHDL Internal Frequency Setting

---

```
-- ************************************************************************************************
-- VHDL created by Martin Becker, PEG, University of Stellenbscoh
-- This module receives 16 bit Data form the DSP and generates a squarewave with
-- frequency determined by DSP 16 bit Data.
--
-- clk30(frequency) = 30 MHz
--
--
-- A counter is run up to the value determined by the 12 most significat
-- bits in the 16 bit input steam. Then the output is toggled.
-- The 4 least significant bits have to be "1000" for this block to respond
```

```
-- accordingliy. This block is used together with a counter with an 8 bit resolution.
-- The speed of that couter is determined by this block.
--
-- ************************************************************************************************


library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity freq_div is
  port (  clk           : in std_logic;            -- Input clock
      Load_Data       : in std_logic;           -- Data Enable Pin
      nReset          : in std_logic;           -- Not Reset
      Data          : in std_logic_vector(15 downto 0);  -- 16 bit input data (clock division constant)
      clk_out         : buffer std_logic          -- Devided clock output
  );
end entity freq_div;

architecture a of freq_div is


BEGIN

p0: process(clk, nReset) is

    variable counter   : integer range 0 to 4095;        -- The resolution of the counter is 12 bit
    variable Data_Buff   : std_logic_vector(11 downto 0);    -- When the data is intended for this block
                                -- it is Buffered in this vector
  BEGIN
      IF nReset = '0' THEN
        Data_Buff := (others => '0');
        counter := 0;
      ELSIF rising_edge(clk) THEN
          counter := counter +1;                  -- Increment Counter
        IF Load_Data = '1' AND Data(3 downto 0) = "1000" THEN -- When Data is intended for this operation
                                -- the least significant bits will be "1000".
          Data_Buff := Data(15 downto 4);
        END IF;

        IF counter > conv_integer(unsigned(Data_Buff)) THEN   -- When the counter is equal to the input
division consatnt
            clk_out <= NOT(clk_out);            -- Toggle Output to generate divided clock
            counter := 0;
        END IF;
      END IF;
  END PROCESS p0;
END a;
```

APPENDIX C Circuit Diagrams and Components

C.1 List of components

The main components used in the prototype are listed in the table below.

Component	Manufacturer	Ratings	Internal Properties of interest	Total amount used per phase
Mosfet	International Rectifier	80A Continuous	4 mΩ	48
IRFP2907		209A Rated		
		75V Max		
IGBT	Semikron	200A Continuous	9.6mΩ	1
SKIIP202GD		600V Max		
Module				
Capacitors	Hitano	50V	0.1 Ω	200
ECR Series		10000µF		
PEC 33 Controller Board	University of Stellenbosch	75 Mhz Clock		1
		32 A/D, 8 D/A		
		18 Optical Send/Receive		
Cyclone FPGA	Altera	2910 Logic Elements	100Mhz clock	2
EP1C3T100C8				
Current Probe	LEM	200A	Ratio	1
LA205-S			1:2000	

Table Continued…				
UltraCapacitor B48710	EPCOS	67F 42V	20mΩ	1
Snubber Capacitor MKS4	WIMA	0.47µF 630V		10
Optic Senders and Receivers HFBR0501	Agilent Technologies	1 MBD (Mega Baud)		11 Pairs
Component	*Manufacturer*	*Ratings*	*Internal Properties of interest*	*Total amount used per phase*
Thyristors SKKT 250 Module	Semikron	800V 450A	8500A for 10ms	1
Instrumentation Amplifier AD623	Analog Devices	5V single or double supply. Gain 1 to 1000. 800 kHz Bandwidth	Low Noise Low Cost	8
MOSFET Driver TPS 2813	Texas Instruments	Up to 14V Supply 40ns Delay 25ns Rise/Fall	2A Peak Current	24
Optocouplers 4N25	Fairchild	Current Transfer Ratio = 20%	5300V Isolation	24

Table A-16List of Components

C.2 Positive MOSFET Module

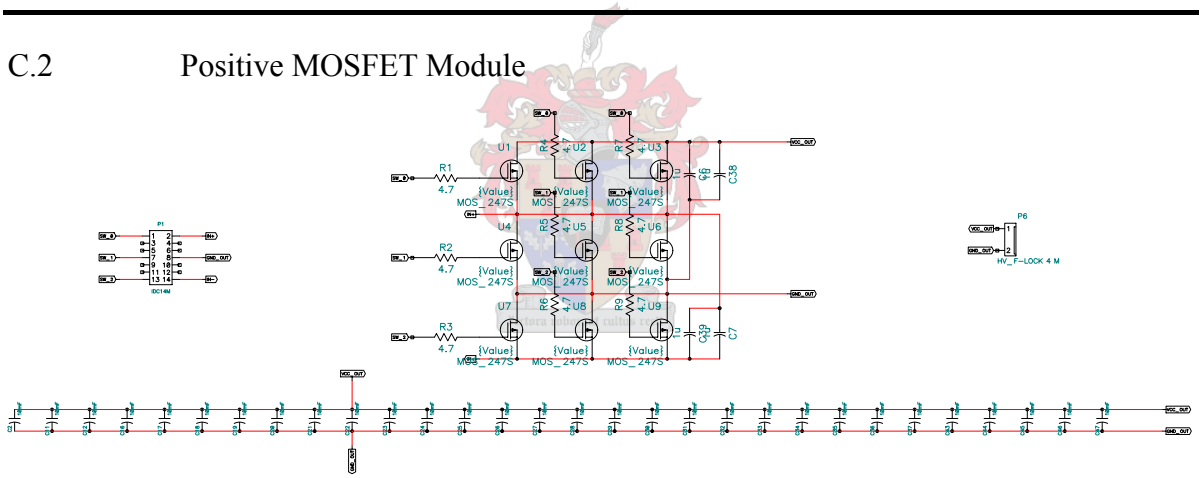


Figure A-1-13 Schematic Diagram of Positive Cycle Marxian Module

C.3 Negative MOSFET Module

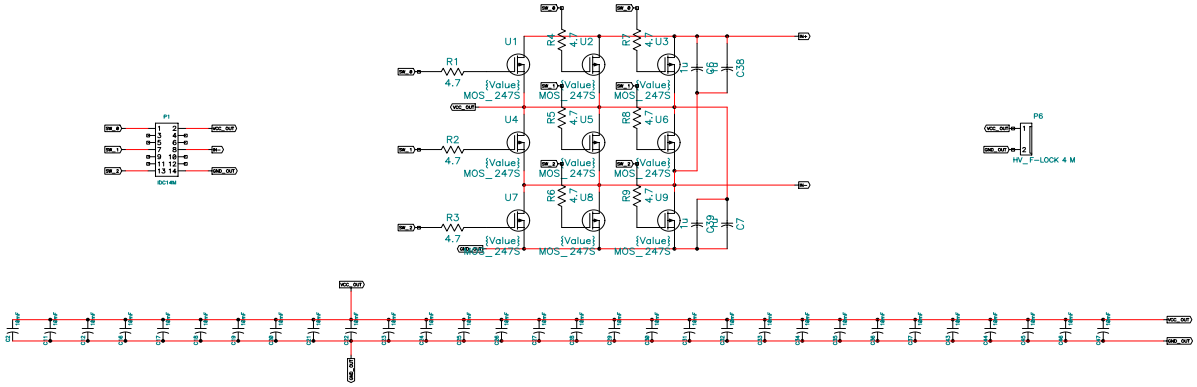


Figure A-1-14 Schematic Diagram of Negative Cycle Marxian Module

C.4 MOSFET DRIVER

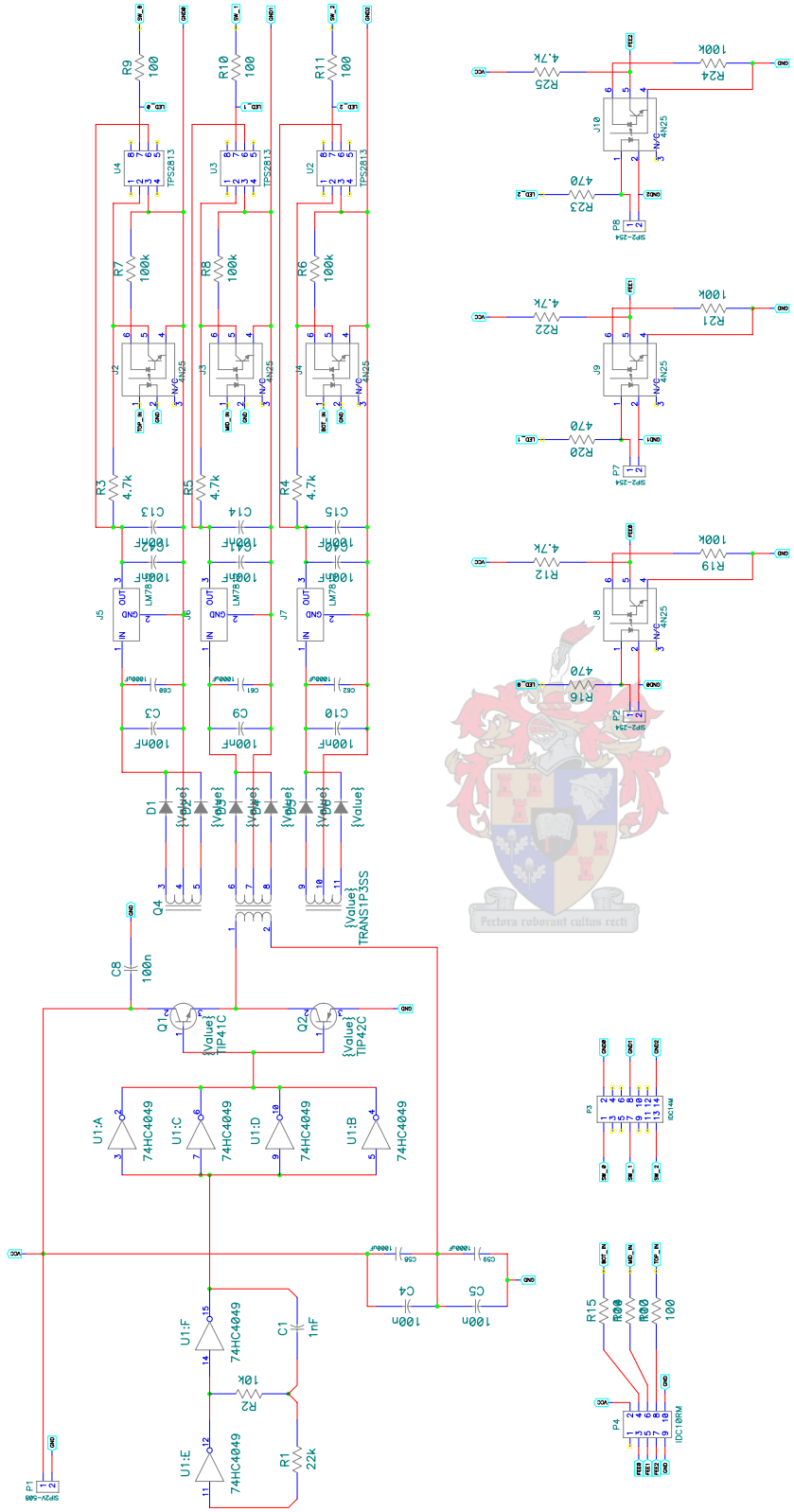


Figure A-1-15 Schematic Diagram of Mosfet Driver with Feedback

C.5 FPGA Module

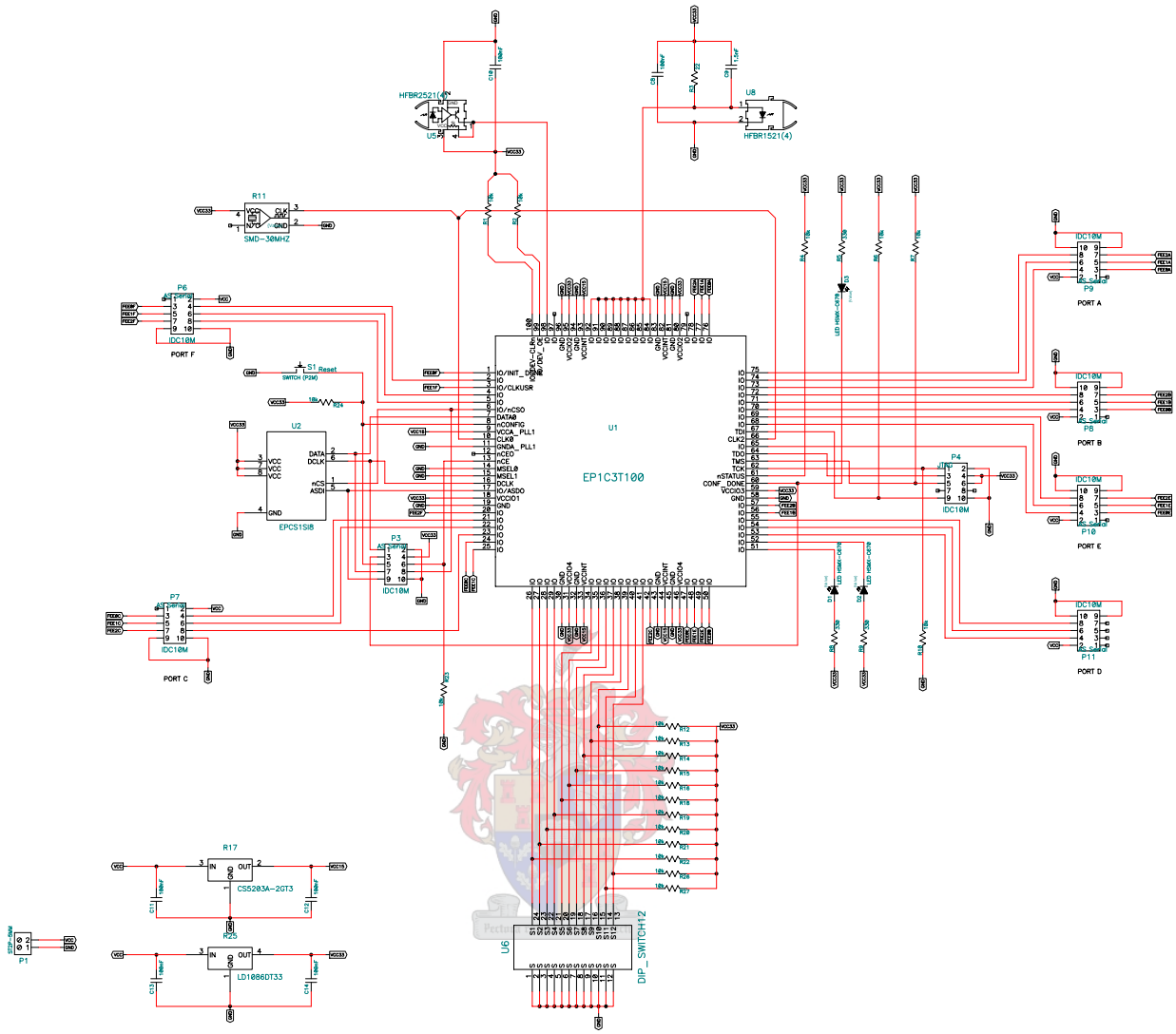


Figure A-1-16 Schematic Diagram of Switch Controller for Marxian MLI

C.6 Voltage Measuring Adapter for PEC33

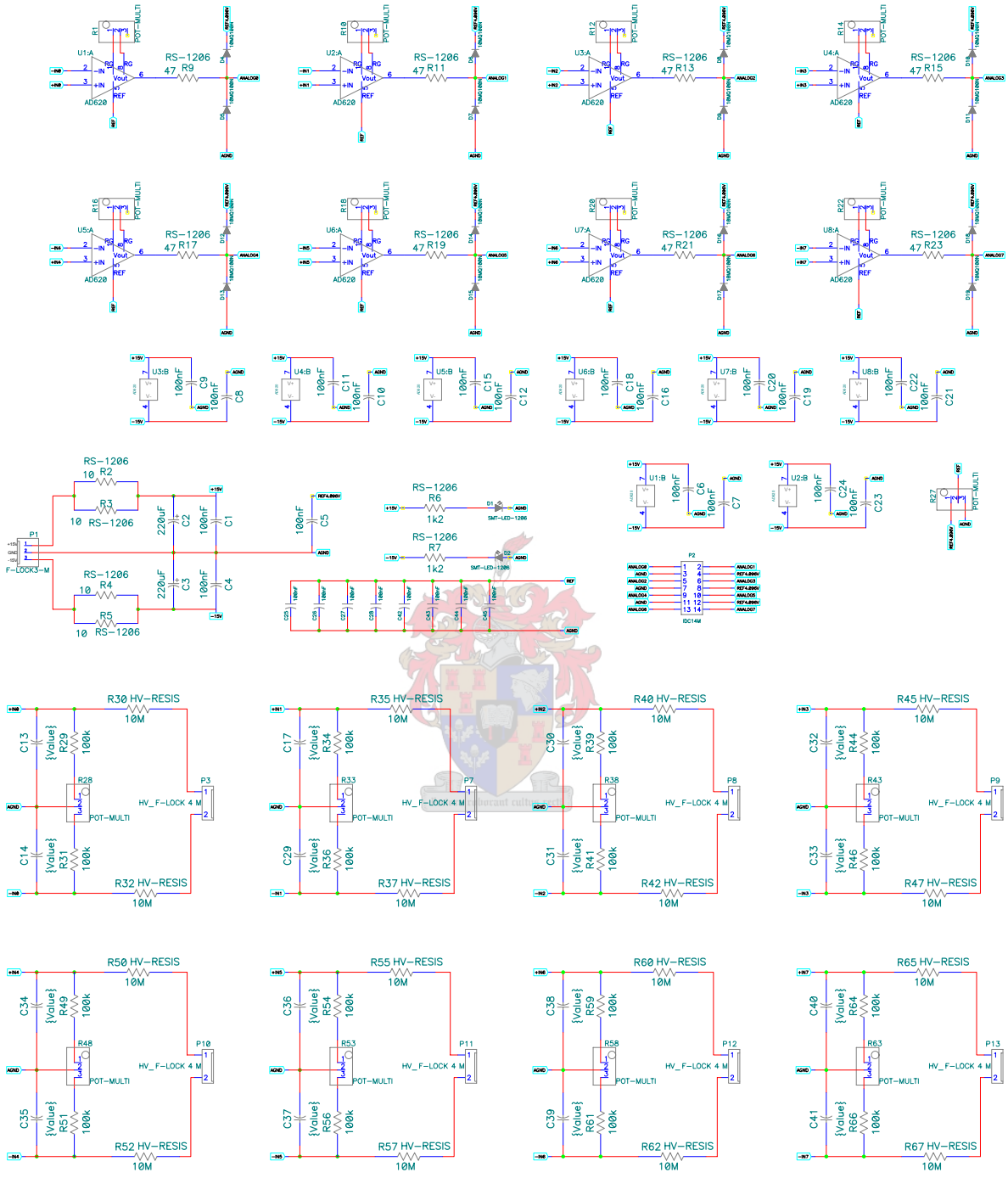


Figure A-1-17 Schematic Diagram of Voltage and Current measurement board

APPENDIX D Further Practical Measurements

D.1 Practical Verification on Capacitance and Efficiency of Ultracapacitor

A number of tests were done on an EPCOS 67F, 42V ultracapacitor. The tests conducted included tests for efficiency, overall capacitance and charge/discharge times. Figure 3.1 shows the setup used to conduct a few lower current tests up to 20A on the ultracapacitor. These tests were done to confirm the rated capacitance.

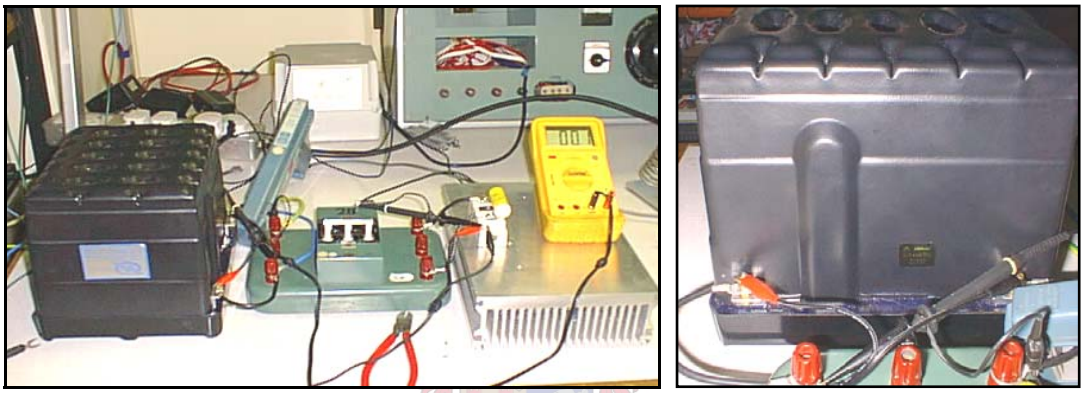


Figure A-1-18 Measurement setup

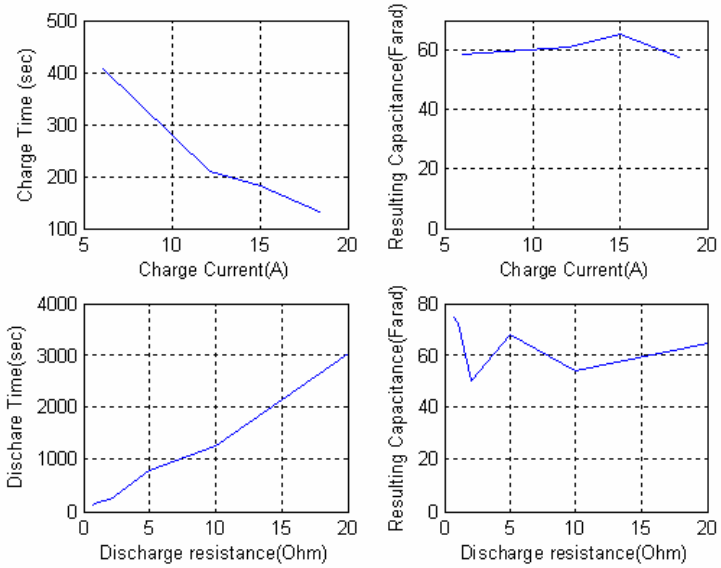


Figure A-1-19 Charge and discharge characteristic curves shown left. The resulting capacitance in Farad calculated shown on right.

A specification not released on the datasheet of the EPCOS 42V, 67F ultracapacitor was efficiency. With the circuit shown in Figure 3.3 the round trip efficiency was tested. The test was conducted by measuring how much energy is taken up in 5 minutes and then comparing this to the energy released in 5 minutes using the same serial resistor.

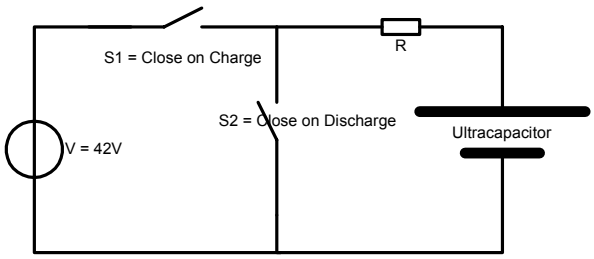


Figure A-1-20 Test schematic for round trip efficiency tests

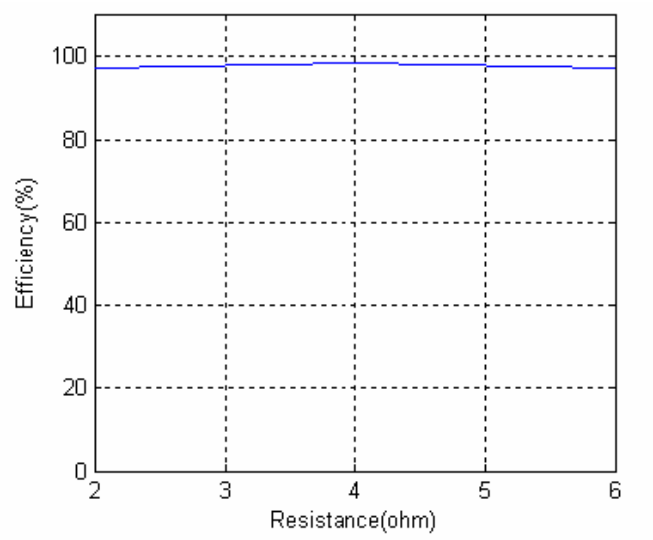


Figure A-1-21 Roundtrip Efficiency of EPCOS Ultracapacitor is set at 97% for load range (2 – 6 ohm)

The self discharge times of the EPCOS ultracapacitor depend on whether it has active or passive balancing. Active balancing of internal cells includes some electronics that maintain individual cell voltages. Passive balancing is done by resistors coupled in parallel to each cell. The ultracapacitor tested at the University of Stellenbosch has passive cell balancing. The disadvantage of this is that the self discharge time is only 4 days (according to datasheet) or 3 days (practical measurement). EPCOS promises a 20 day self discharge time for active balanced modules.