Evaluation and Implementation of Anti-Islanding Methods for Converter-Fed Distributed Generation

by

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DECLARATION

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ABSTRACT

As the number of distributed generation units connected to a distribution network increase, the possibility of island formation increases. An island is formed when distributed generation units continue to energize local loads within a section of the grid, which has been disconnected from the main distribution network. These islands pose significant danger to maintenance personnel as well as to members of the public.

In this study, an investigation is done into various anti-islanding methods. The modes of operation of these methods are discussed, as well as their strengths and weaknesses. The slip-mode frequency shift method and the Sandia voltage shift method, in combination with over/under voltage and frequency protection, are simulated and tested to confirm their functionality. The results obtained show that it is possible to prevent distributed generation units from energizing local loads when the grid is disconnected.

OPSOMMING

Die moontlike toekomstige toename in die aantal verspreide generasie eenhede gekoppel aan die verspreidings netwerk, verhoog die moontlikheid van eiland vorming. ‘n Eiland word gevorm wanneer verspreide generasie eenhede energie aan lokale laste voorsien nadat die netwerk ontkoppel is. Dit hou groot gevaar in vir onderhouds personeel asook vir die publiek.

In die tesis word ‘n studie gedoen oor die verskillende metodes om die vorming van ongewensde eilande te voorkom. Die glipmode-frekwensieskuif metode en die Sandia spanningskuif metode word gekombineer met die oor/onder spanning en frekwensie beskerming metodes. Die kombinasie van metodes word dan gesimuleer en eksperimenteel getoets. Die verkrygde resultate toon dat dit moontlik is om die vorming van ongewensde eilande effektief te voorkom.

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ABBREVIATIONS

- AC - Alternating Current
- ADC - Analog-to-Digital Converter
- AFD - Active Frequency Drift
- DEPWM - Double Edged Pulse Width Modulation
- DC - Direct Current
- DG - Distributed Generation
- DSP - Digital Signal Processor
- GPIO - General Purpose Input and Output
- IGBT - Insulated Gate Bi-polar Transistor
- LCD - Liquid Crystal Display
- LED - Light Emitting Diode
- NDZ - Non-Detection Zone
- OFP - Over Frequency Protection
- OVP - Over Voltage Protection
- PCB - Printed Circuit Board
- PCC - Point of Common Coupling
- PEC - Power Electronic Converter
- PI - Proportional and Integral
- PLCC - Power-Line Carrier Communication
- PLL - Phase-Locked Loop
- PWM - Pulse Width Modulation
- RLC - Resistor, Inductor and Capacitor
- RMS - Root Mean Square
- SCADA - Supervisory Control and Data Acquisition
- SFS - Sandia Frequency Shift
- SMS - Slip-mode Frequency Shift
- SOC - Start of Conversion
- SPD - Signal Produced by Disconnect
- SPI - Serial Peripheral Interface
- SVPWM - Space Vector Pulse Width Modulation

- SVS - Sandia Voltage Shift
- THD - Total Harmonic Distortion
- UFP - Under Frequency Protection
- UVP - Under Voltage Protection

LIST OF SYMBOLS

- MW - Mega Watt
- kW - Kilo Watt
- W - Watt
- Q_f - Quality Factor
- ω_0 - Resonant Frequency in Radians per Second
- f_0 - Resonant Frequency in Hertz
- f_g - Grid Frequency in Hertz
- P - Active Power
- Q - Reactive Power
- L - Inductance
- C - Capacitance
- R - Resistance
- θ - Phase Angle of Current Relative to the Voltage
- Hz - Hertz
- f - Frequency
- V - Volts or Voltage Amplitude
- Z - Impedance
- I - Current Amplitude
- $i(t)$ - Instantaneous Current
- $v(t)$ - Instantaneous Voltage
- f_m - Maximum Frequency Deviation of SMS Method
- θ_m - Maximum Phase Deviation of SMS Method

CHAPTER 1. INTRODUCTION

It is an undeniable fact that there is an increasing demand for electrical power and a growing shortage of fossil fuels needed to deliver this electrical power. Various solutions have been proposed, but there are still wide-ranging debates around the most effective and efficient solutions to this problem.

It is being predicted that by 2050 the global population will be about 9 billion people [1]. This will drastically increase the demand for certain basic needs to survive. Most of these needs are in one way or another connected to processes that produce some or other form of pollution or waste.

As the global population increases, the levels of CO_2 emissions will rise too. It is thus also important to utilize cleaner resources to satisfy the demand for more electrical power. Currently some of the more promising alternative energy sources are wind, hydro, tidal and solar. These resources are sustainable and will be able to deliver power long after the fossil fuel resources have been depleted.

In a developing country like South Africa, it is essential that electrical power is available at all times. Since 2006, ESKOM, has been struggling to satisfy the demand for power in South Africa, and this has led to millions of people quite literally being left in the dark, right across the country. Apart from the inconveniences caused by these power outages, they also pose a great threat to the business sector and thus to the development of South Africa.

In an attempt to reduce the carbon footprint of mankind, more pressure is being placed on companies to switch to cleaner power sources. This leads to a greater focus on technology to improve current methods and to make the utilization of these sources more economical and efficient.

Distributed generation (DG) can be described as the use of small-scale power generation units to provide power to nearby load sites [2]. These units can be connected either

directly to the distribution network or on the customer side of the meter [3]. This makes it possible to reduce distribution costs drastically.

DG units operating in standalone mode also make it possible to provide power to rural areas. It is usually difficult to expand the national grid to these areas, since it is either uneconomical or involves geographically challenging terrain. In such cases, however, it is possible to connect multiple DG units together and thus create a smaller independent power distribution system.

DG also makes it possible for buildings or companies to generate their own electricity and to deliver the surplus electrical power back into the grid. DG generally refers to units that produce less than 10 MW of power [2].

DG has several advantages for both utilities and the customer. Some of these advantages are standby generation, peak shaving capability, peak sharing and base load generation [2]. The main advantage is the possibility of generating electricity close to the source of alternative energy.

DG technologies can consist of the following [2]:

- Micro turbines
- Internal combustion engines and generators
- Photo voltaic panels
- Fuel cells
- Hydroelectric plants
- Wind generators

Studies indicate that by 2010 about 25% of all new generation will be distributed, and in fact the value might even be higher [3].

Figure 1.1 shows the basic layout of a modern DG power system. Great advancements have been made in recent years in terms of switching technology. This allows designers and manufacturers to develop products that enable power systems to function more efficiently and reliably.

Power electronic converters (PECs) make it possible to utilize more and more of these alternative energy sources. These sources usually deliver power in varying quantities, but, by using PECs, these quantities can be regulated and converted into a more stable form of power.

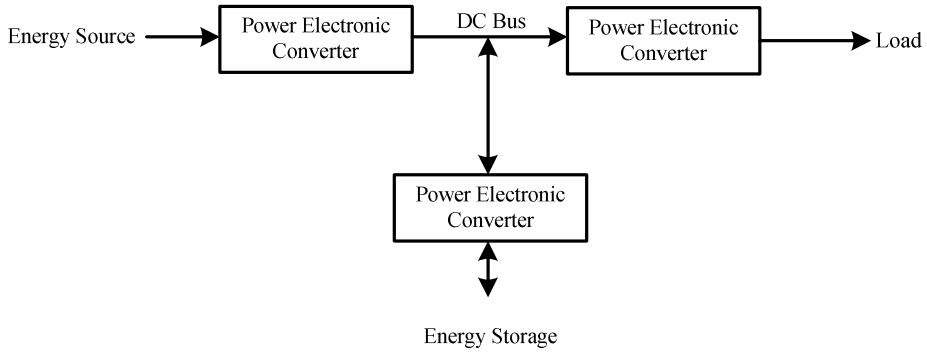

Figure 1.1 Modern DG Power System

Wind power is one of these alternative energy sources. However, both the amplitude and the frequency of the voltage delivered by the generator can vary, depending on the wind speed [4]. A PEC makes it possible to convert it to a fixed DC voltage, which is then either stored or inverted into the desired voltage amplitude and frequency. Similar techniques can be applied to most of the other power sources.

As the number of DG units increases, the transmission and distribution networks start to deviate from conventional layouts. Transmission networks usually have a meshed design [3] and distribution networks a radial or loop design [3]. The power flow in these distribution networks is usually one-directional, but when DG units are added, this has to change [3].

An island is formed when the grid disconnects either intentionally or accidentally from a section of the network and a DG unit(s) continues to energize local loads [5] [6] [7] [8] [9] [10] within that section. An island poses a significant danger to maintenance personnel and the public.

Figure 1.2 shows the network functioning normally with multiple DG units connected at various locations. Power is provided to the load from both the conventional sources as well as from the DG units.

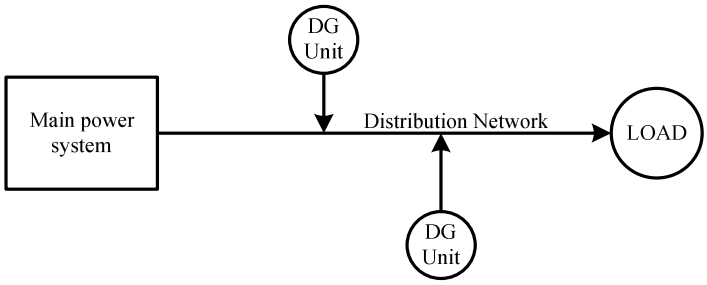

Figure 1.2 Network before islanding has occurred.

Figure 1.3 shows the network after islanding has occurred. The main power source has been disconnected, either accidentally or intentionally. The DG units are still delivering sufficient power to the local loads. The continued energizing of the load can lead to damage of equipment or injury to maintenance personnel working within the islanded section without knowing the system is still alive.

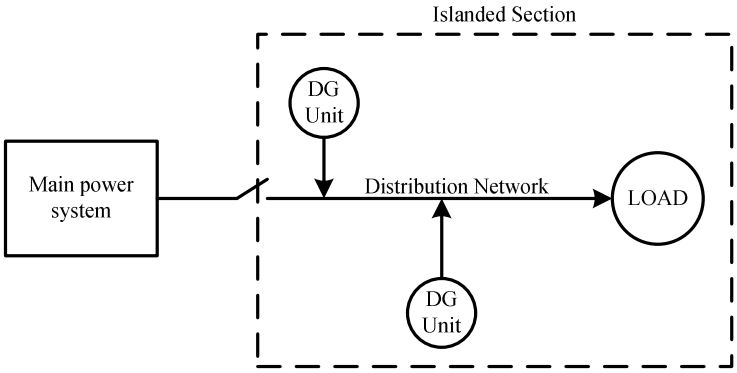

Figure 1.3 Network after islanding has occurred

Most DG units are designed in such a way that they will disconnect from the grid when over/under voltage or frequency occurs on the network. In most cases when the grid disconnects, this will be the case. In the rare case when the load and the source are matched, however, it will appear to the DG units as though the network is still connected to the conventional power sources. The DG units will thus continue to power the line, thereby leading to the formation of an island.

Anti-islanding methods assist the DG units to detect islanding or force the islanded section out of the normal operational specifications of the grid. This is achieved by attempting to perturb either the voltage or the frequency of the network. In the presence of the grid, these perturbations will have no effect on the voltage or frequency. If the grid is disconnected, though, variations in voltage or frequency can occur. These variations

are then detected by the over/under voltage or frequency protection system, and the DG is disconnected or shut down.

The potential future increase in the number of DG units connected to the South African grid has created room for a study of the phenomenon of islanding and its prevention.

Consequently, the focus of this thesis is to investigate several techniques proposed in the literature to avoid islanding, to simulate these and thereafter to propose a technique or combination of techniques to be implemented and tested. The implementation will generally be focussed on wind generator applications, although a large amount of the theory investigated and applied throughout this thesis is also applicable to most of the other DG technologies.

Chapter 2 presents an overview and discussion of various anti-islanding methods. Their respective modes of operation, as well as their strengths, weaknesses and possible non-detection zones are explained.

Chapter 3 investigates the non-detection zones of the relevant inverter based anti-islanding methods. These zones are represented graphically in the *power mismatch* plane and the Q_f *vs.* ω_0 plane. A design guideline is derived for the Sandia voltage shift method and the method selection is discussed.

In Chapter 4, the algorithms needed to simulate and test the selected anti-islanding methods are presented. The system topology is selected and the general system configuration is discussed. Control algorithms for the DC bus regulation and the current loop are designed. The effects of dead time in the switching signals of the insulated gate bipolar transistors (IGBTs) are investigated, and a compensation method is derived to provide improved compensation. Implementation considerations of the selected anti-islanding methods are discussed. These methods are simulated along with the DC bus regulation algorithm and the active rectifier.

Chapter 5 presents the hardware and software used to test the anti-islanding methods practically. The existing hardware is discussed, as is the additional hardware designed in

this thesis. The development of the software used to control the converter is described. An overview of the operational modes of the converter is given along with the configuration of the analog-to-digital converter (ADC) and pulse width modulation (PWM) modules of the digital signal processor (DSP). This is followed by flow diagrams of the interrupts where the control loops of the converter are executed.

In Chapter 6, the results obtained from tests performed on different loads are discussed. A test is done to confirm the regulation of the DC bus and the power reference tracking of the active rectifier. The tests confirm that the energizing of an island can be prevented successfully when the grid is disconnected from a local load.

Chapter 7 gives some conclusions of this thesis and the results obtained.

CHAPTER 2. ANTI-ISLANDING METHODS

This chapter gives an overview of various methods used to prevent islanding. A discussion of their modes of operation, and of their strengths, weaknesses and possible non-detection zones is also provided. A brief overview of the non-detection zone concept is given. This concept will be discussed in more detail in the next chapter.

2.1 INTRODUCTION

Anti-islanding methods are generally divided into two categories, namely passive and active methods. Passive methods monitor selected parameters, such as voltage, frequency or their characteristics, and they switch off the inverter if one of these parameters deviates outside specified boundaries or conditions [10]. Active methods perturb the connected circuit and then monitor the response to determine if islanding has occurred [10]. Figure 2.1 shows the flow of power when the grid is connected. The local load is represented by a resistor, inductor and capacitor (RLC) circuit.

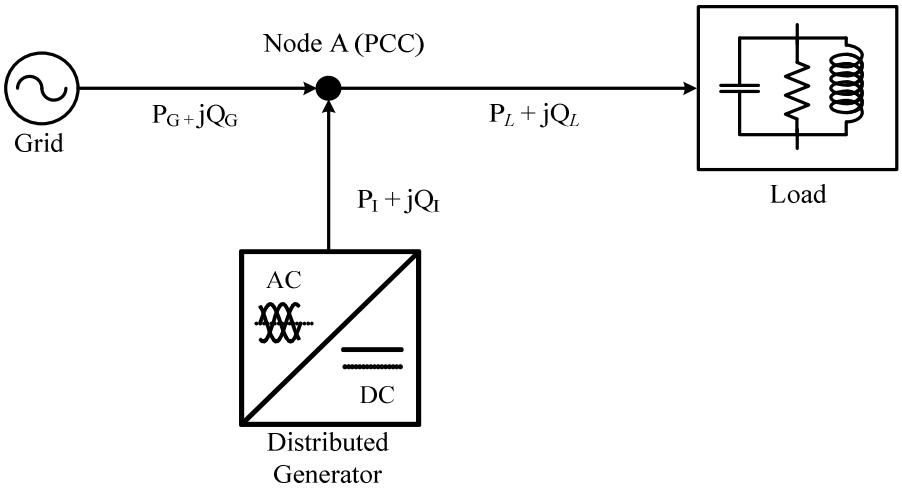

Figure 2.1 Power flow with the grid connected

This load is fed from both the DG and the grid, and the following equations are used to calculate the amount of power drawn from the grid.

$$P_G = P_{Load} - P_I \tag{2.1}$$

$$Q_G = Q_{Load} - Q_I \tag{2.2}$$

Figure 2.2 shows the power flow when the grid is disconnected. In this situation the DG is the only power source, which means that the power that was delivered by the grid must now be supplied by the DG, if available.

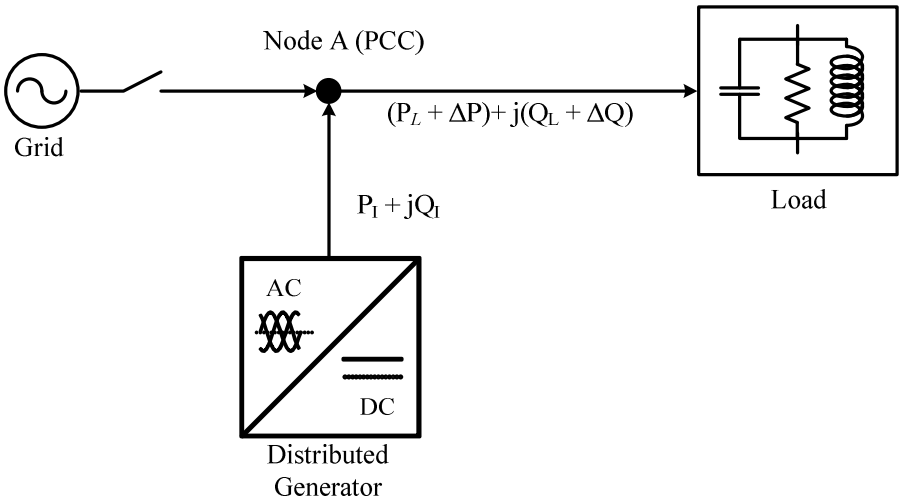

Figure 2.2 Power flow with the grid disconnected

The power mismatch between the DG and the grid is calculated by means of the following equations:

$$\Delta P = P_I - P_{Load} \tag{2.3}$$

$$\Delta Q = Q_I - Q_{Load} \tag{2.4}$$

A non-detection zone (NDZ) represents the changes in active and reactive power that cannot be detected by the anti-islanding algorithm. All passive methods will fail in the case where the DG and the load are 100% matched [5]. The size of the NDZ varies according to the method used and the parameters selected. Passive methods tend to false trip due to disturbances on the grid. This can weaken grid stability and security. Although passive methods are still widely used, they limit the applications of DG units in the long term.

Active methods attempt to create a power mismatch between the load and the DG when they are closely matched. It is possible that some of the active methods can cancel out the mismatch in an attempt to create one. It should also be noted that the positive feedback in some active methods could lead to power-quality degradation [5]. The injection signals can also induce some voltage waveform distortion. Non-detection zones will be discussed in more detail in the next chapter.

2.2 PASSIVE ANTI-ISLANDING METHODS

In this section, several passive anti-islanding methods are described, as are the principles on which they work and the NDZs they may create.

2.2.1 UNDER/OVER VOLTAGE AND UNDER/OVER FREQUENCY [6][10][11]

It is expected that all grid connected inverters will have some form of over/under voltage protection (OVP/UVP) and over/under frequency protection (OFP/UFP). These methods are designed to stop the inverter supplying power if the grid strays outside predefined parameters. Measurements are taken at the point of common coupling (PCC) between the consumer and the grid.

The response of the system upon disconnection will depend on ΔP and ΔQ at the instant before the switch opens.

If $\Delta P \neq 0$ and $\Delta Q \neq 0$ upon disconnection, then the voltage and frequency at node A (see Figure 2.2) will change, depending upon the size of this difference. The frequency of the voltage will drift to the resonant frequency of the load (when $\Delta Q = 0$) if the inverter operates at unity power factor or very close to it.

Since the inverter synchronizes with the system frequency, the islanded frequency is calculated as follows [10]:

$$\omega_i = \frac{1}{\sqrt{LC}} \tag{2.5}$$

The islanded voltage is calculated as follows [6]:

$$V_i = \sqrt{k} V_n \tag{2.6}$$

where

$$k = \frac{P_I}{P_{Load}} \tag{2.7}$$

with

V_i Islanded Voltage

V_n Nominal System Voltage

Usually ω_i and V_i are outside the normal working parameters of the grid and in such a case the inverter is shut down when the grid disconnects.

The NDZs of these methods are very large though. An island will form when $\Delta P = \Delta Q = 0$ upon disconnection of the grid. This occurs because the changes in voltage and frequency are too small to be detected by the UVP/OVP and UFP/OFP algorithm, which is implemented within the software of the inverter itself. The size of the NDZ is increased due to the deviations allowed within the normal functioning of the grid. This implies that, if ΔP and ΔQ are not equal to zero, islanding can still occur. Because of the allowed deviation of the grid, the thresholds of the parameters for this algorithm cannot be set too small.

This method is usually combined with some of the active methods to form a very effective island prevention system.

2.2.2 VOLTAGE PHASE ANGLE JUMP DETECTION [10]

This method monitors both the terminal voltage and the output current of the inverter. It then determines the phase between the two and monitors it for a sudden jump in phase angle. Under normal operation, the current of a current-source inverter will be synchronized with the grid by detecting the rising and falling zero-crossing of the voltage at node A (see Figure 2.2). This synchronization is usually accomplished by using an analog or digital phase-locked loop (PLL).

The current-source inverter uses the grid voltage as a fixed reference. Since the inverter and the grid voltage only synchronize at zero-crossings, the inverter operates in open-loop mode between them. When the grid disconnects, the output current becomes the fixed phase reference. The current is still following the PLL template provided in the inverter. Figure 2.3 shows the result that can be expected when the grid disconnects.

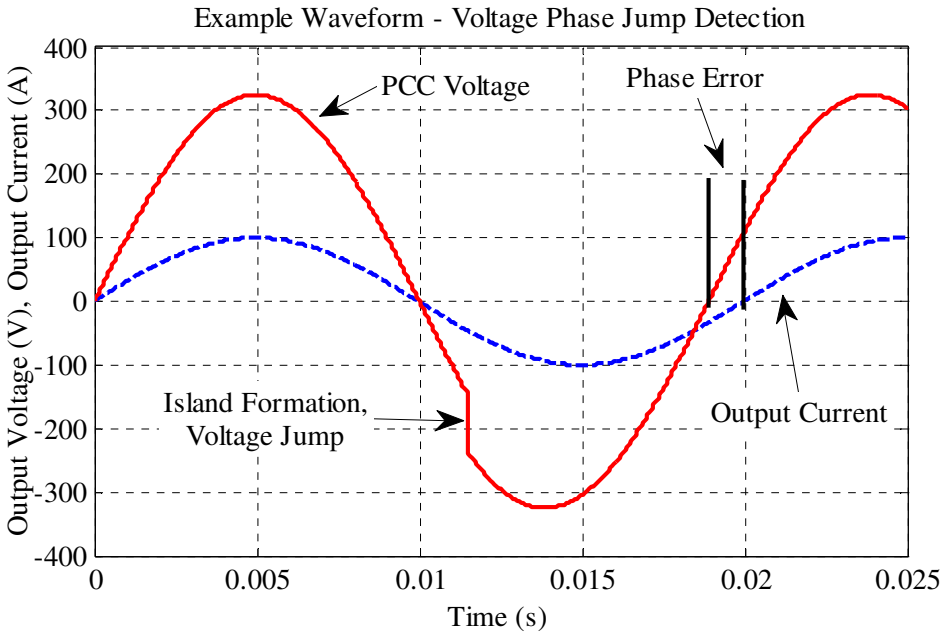

Figure 2.3 Voltage phase jump detection example

The phase angle of the load must be the same as before the grid disconnected, and this will cause the voltage at node A to jump to this new phase. This will result in a phase error between the inverter current and the 'new' voltage. If this value is larger than the threshold, the inverter will be shut down or de-energized. The size of the phase jump will be affected by the power factor of the load.

The advantage of this method is its ease of implementation. The PLL is required by the inverter to synchronize with the grid. To implement phase jump detection the inverter must be able to detect the phase error between the voltage and the current. This method is weakened, however, by the size of the threshold for shutting down, which can cause nuisance tripping when it is too small.

A NDZ exists when the load has a zero phase angle at the grid frequency. Depending on the threshold, this NDZ can be smaller than the NDZ of over/under protection methods.

2.2.3 Detection of Voltage Harmonics and Detection of Harmonics [10]

This method monitors the total harmonic distortion (THD) of the voltage at node A (see Figure 2.2). If the THD goes outside a predefined threshold, the inverter shuts down.

When the grid is connected, the THD is low across the load terminals, and the grid is represented as a 'stiff' voltage source. This causes the load to draw an undistorted sinusoidal current. The current harmonics produced by the inverter flow into the low-impedance grid. These harmonics, in combination with the generally low impedance of the grid, will produce a small voltage distortion at node A. When the grid is connected, the THD at node A is below the threshold value.

Two mechanisms can cause the harmonics to increase at node A when the grid disconnects. The first mechanism is that either the inverter itself will produce current harmonics in its AC output current, or the switching of the IGBTs will place harmonics on the current. When the grid disconnects, the harmonics produced by the inverter will flow into the load with much higher impedance than the grid.

The second mechanism that can cause an increase in the harmonic distortion is the presence of a transformer between the grid and node A. However, this mechanism has not been tested using the current standards [10]. If the breaker is located between the transformer and the grid, the secondary side will be excited by the output of the inverter. The voltage response of the transformer is highly distorted due to magnetic hysteresis and other nonlinearities. This will increase the THD at node A. Nonlinearities in the local loads can also increase the distortion at node A.

It is usually the third harmonic that is monitored when this method is implemented in practice. Previous methods also attempted to detect the pulse width modulation frequency on the output voltage of the inverter.

This method should work well in theory and has the potential to detect islanding under various conditions, but has similar setbacks to the voltage phase jump method. It is not always easy to select a correct threshold to avoid nuisance trips. The threshold should be higher than the level of harmonics that can be expected under normal operating conditions, but lower than potential levels that can be expected when islanding occurs.

Typically, inverters are allowed a THD of 5% at full rated current. Some RLC loads can cause the THD to be lower than 5% when islanding occurs due to low-pass

characteristics that attenuate the higher frequencies. This implies that the threshold will have to be set lower than the allowed maximum THD for normal operating conditions. The presence of power electronic converters can also increase the THD due to current harmonics at system resonance frequencies. Transient voltage disturbances caused by the switching of equipment such as large capacitor banks can also increase the THD and cause a nuisance trip of the inverter.

NDZs exist in cases where the load has strong low-pass characteristics in the absence of a transformer inside the islanded section. Loads with a high quality factor also lead to a NDZ. The method can also fail when loads at the generator are able to shunt reactive currents as well as when the inverter has a high quality, low distortion output.

2.3 ACTIVE ANTI-ISLANDING METHODS

In this section, several active anti-islanding methods are discussed, together with possible NDZs associated with them.

2.3.1 IMPEDANCE MEASUREMENT METHOD [10]

The output of an inverter that operates as a current source has a current that appears to the grid as follows:

$$i_{inv} = I_{inv} \sin(\omega t + \phi) \tag{2.8}$$

where

I_{inv} is the amplitude of the inverter output current

ω is the inverter frequency in radians/second

ø is the inverter phase angle.

Although all three parameters may be varied, it is normally the amplitude of the current, which is perturbed. This perturbation leads to a variation in voltage and power. The size of this variation will depend on the nominal values of the grid resistance and power. The change in voltage can be calculated as follows:

$$\Delta V = \frac{\Delta P}{2}\sqrt{\frac{R}{P}} \tag{2.9}$$

If the grid is connected, the voltage remains constant, but when the grid disconnects, the variations will be measurable at node A (see Figure 2.2). This variation can be used to prevent islanding. This method is named impedance measurement because the inverter is measuring dV_a / di_{inv}. The current shift should be of such magnitude that it would cause the voltage to deviate outside the UVP/OVP window when the grid is disconnected. Depending upon the size of the window, this will have to be quite a large perturbation of the current.

This method has a very small NDZ if the local load has larger impedance than the grid. If the load and the inverter power output are balanced upon disconnection, the variation in the inverter output will disturb this balance and the inverter will trip due to the OVP/UVP mechanism.
High levels of penetration weaken this method. The resultant current variations of multiple units might cancel each other out and not produce the required deviation to prevent islanding. This problem can be solved if the units are synchronized in some way. This is a viable solution if the inverters are located close to each other, but this might pose a problem on more large-scale networks.

A synchronized system can also result in some problems, like flickering, grid instability or false tripping. This can also happen if the grid has high impedance. These problems can increase as the density of the inverters increases in a local area. The above implies that this method is only suitable in small, preferably single-inverter networks.

The weakness of the multi-inverter setup is a greater drawback for this method than the size of the NDZ, which is quite small. The size of the NDZ depends on the threshold that has been set. If this value is set too low, nuisance trips can occur, whereas if the value is set too high, islanding can occur.

To summarise, the impedance measurement method has no practical use in multiple inverter setups, but it can be used in a single-inverter small network setup.

2.3.2 DETECTION OF IMPEDANCE AT A SPECIFIC FREQUENCY [10]

By injecting a current harmonic at a specific frequency rather than measuring existing current harmonics, the passive harmonic detection method is converted into an active method. These harmonics will be absorbed into the network if the impedance of the grid is much lower than that of the local load and, in that case, the harmonics will not affect the voltage much.

When the grid disconnects, however, the injected harmonics will flow into the load. If it is assumed that the local load is a parallel RLC circuit, the load will produce a harmonic voltage that will be detected by the inverter and cause it to shut down. The amplitude of this harmonic voltage depends on the impedance of the load at the frequency of the harmonic current.

When implemented as described above, this method has the same NDZ as the harmonic detection method. The NDZ can be eliminated if a sub-harmonic is used, but this can cause problems on the grid. Multiple inverters injecting the same current harmonic can also lead to false trips.

2.3.3 SLIP-MODE FREQUENCY SHIFT [10]

Slip-mode Frequency Shift (SMS) uses positive feedback to destabilize the inverter output when the grid disconnects. From (2.8) it is noted that it is possible to change the phase of the current relative to the voltage at node A (see Figure 2.2). This will prevent the voltage frequency at node A from stabilizing once the grid has disconnected.

An inverter usually operates at unity power factor, having a zero degree phase difference between the grid voltage and the output current. SMS alters this phase to be a function of the frequency of the voltage at node A, as shown in Figure 2.4. The frequency of the grid is not affected by this phase difference when it is connected.

The response curve in Figure 2.4 is designed in such a way that the phase of the inverter increases/decreases more rapidly than that of the RLC load around the grid frequency, ω_0. By doing this, the inverter is operating at an unstable working point around the grid

frequency. This point is stabilized by the grid when connected. When it is disconnected, however, a fixed phase and a fixed frequency reference are not available, and the phase and frequency will deviate along the response curve.

When an island is formed, the inverter must be operating at an intersection of the load line and the inverter response curve. This implies that the inverter can be at A, B or C as shown in Figure 2.4.

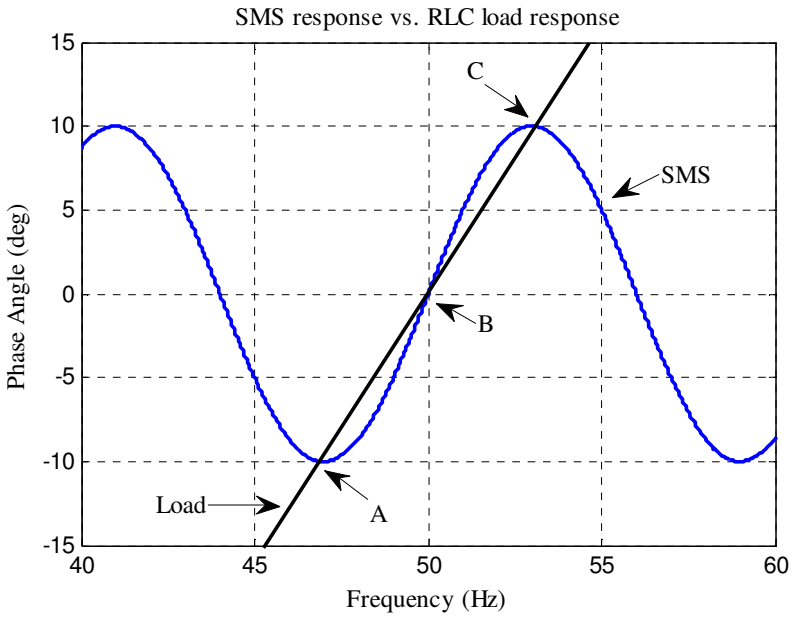

Figure 2.4 Plot of the current-voltage phase angle vs. frequency characteristic of an inverter utilizing the SMS islanding prevention method

Since positive feedback is used, a small perturbation of the frequency will cause the error to increase, not decrease. This causes instability of the inverter around ω_0, which will drive the inverter to a new operating point at either A or C, depending on the direction of the initial disturbance.

If the response curve was designed correctly for this load, points A and C should be outside the window of operation of the inverter and the inverter will be shut down by the UFP/OFP method.

This method is relatively easy to implement, since it is done within the software, and it uses components that are already required. It has a small NDZ compared to other active methods. This method also works in multi-unit systems, while still enabling the inverter

to have a small compromise in power quality. If the gains are set too high within the positive feedback loop, however, problems can be experienced in terms of power quality, especially at very high levels of penetration.

A NDZ exists in the case where the phase response of the load is faster than that of the inverter. In such a case the nominal line frequency will be a stable operating point and islanding will occur. These loads are typically loads with a high quality factor and a resonant frequency close to the line frequency.

2.3.4 FREQUENCY BIAS [10]

This method is also known as the active frequency drift method (AFD). This method is implemented in an inverter with a microprocessor-based controller. It places a slight distortion onto the current injected into node A (see Figure 2.2). When the grid is connected, this has no effect on the frequency.

When the grid disconnects, however, the frequency is forced to drift up or down depending on the sign of the so-called 'chopping fraction'. Figure 2.5 show an example of how the current waveform can be expected to look in the frequency bias method.

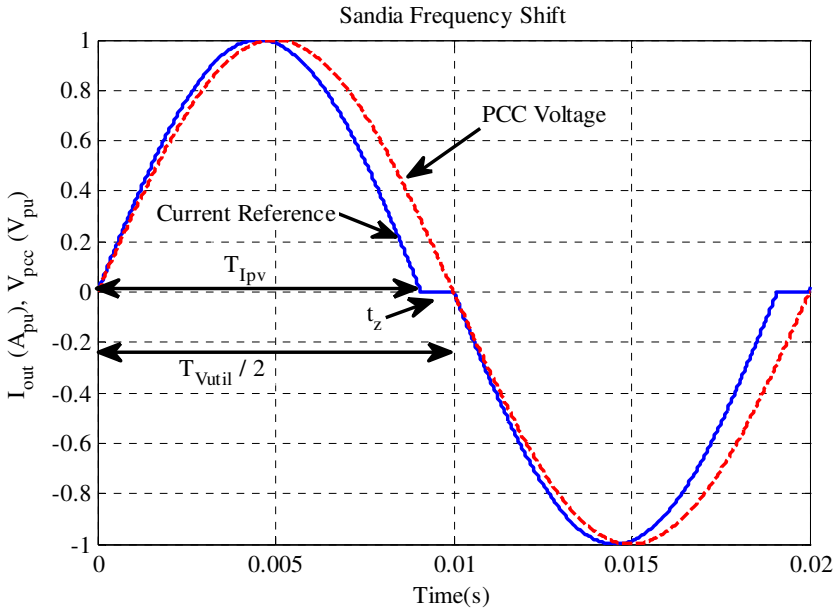

Figure 2.5 Example waveform used in the frequency bias method

In this case, the frequency of the current output is slightly higher than that of the voltage. T_{Ipv} is the period of the current output. T_{Vutil} is the period of the grid voltage and t_z is the zero or dead time of the current output. The 'chopping fraction' is calculated as follows:

$$cf = \frac{2t_z}{T_{V_{Util}}} \tag{2.10}$$

During a half-cycle, the frequency of the current is higher than that of the voltage. When the current reaches zero, it remains there until the voltage reaches zero too. At this instance, the frequency of the voltage is calculated and the frequency of the current is adjusted according to the 'chopping fraction'. The frequency can be forced to go either higher or lower.

If an island has been created, however, the voltage response will follow the distorted current waveform. The voltage will thus decease to zero in a shorter time than under normal operation. The inverter then increases the frequency of the current output, causing the frequency of the voltage to rise again. This process continues until the frequency is outside the window of the OFP/UFP and the inverter shuts down.

This method causes a small degradation of the output power quality of the inverter. It can fail in a multi-inverter setup, if the inverters do not all have the same frequency bias direction. The discontinuous waveform may also cause radio frequency interference.

The size of the NDZ will depend on the 'chopping fraction' value. A 'chopping fraction' that is smaller than 1% will result in a NDZ similar to that of SMS. The NDZs for high quality factor loads are quite large for any value of the 'chopping fraction'. The NDZ is also quite large compared to that in other active methods. This renders this method of little practical use and it is therefore not highly recommended.

2.3.5 SANDIA FREQUENCY SHIFT (SFS) [10]

This method is an extension of the frequency bias method. It also utilizes positive feedback to prevent the formation of an island. The positive feedback is applied to the frequency of the voltage at node A (see Figure 2.2). A 'chopping fraction' is once again

used, leading to the same result as seen in Figure 2.5. This fraction is a function of the error in the line frequency and is calculated as follows:

$$cf = cf_0 + K(f_a - f_{line}) \tag{2.11}$$

Where

cf_0 is the 'chopping fraction' when there is no frequency error

K is an accelerating gain that does not change the direction

f_a is the line frequency measured at node A

f_{line} is the nominal line frequency.

The small frequency changes that are detected when the grid is connected will cause the method to attempt to increase the frequency, but the stability of the grid will prevent this from happening. Upon disconnection, though, the stability of the grid falls away, thus making it possible for the method to change the frequency of the PCC voltage.
As the frequency deviates from the operational frequency of the line, the 'chopping fraction' is accelerated. This will continue to happen until the frequency falls outside the window of the OFP/UFP method. This method works for either increasing or decreasing frequencies, depending of the sign of the 'chopping fraction'.

This method is attractive due to its simplicity of implementation. It also has one of the smallest NDZs. This method has been extensively studied in literature and has been shown to be very effective. It provides a good compromise between island detection, output power quality and transient response. In combination with the Sandia Voltage Shift method, it has been proven to be a very effective method of preventing island formation.

As mentioned before, this method causes degradation in the output power quality of the inverter. As the 'chopping fraction' increases, the degradation can worsen. When connected to weak grids, this can lead to undesirable transient behaviour. This problem is likely to worsen, as the level of penetration increases. It is possible to reduce these effects by lowering the value of K, but this will increase the size of the NDZ and that is also not desirable.

As with most other methods, it seems that this method also has a NDZ for loads with a high quality factor, thus a larger C, a small L and/or a high R. This method does have a very small NDZ, though, which has been proven experimentally.

2.3.6 SANDIA VOLTAGE SHIFT (SVS) [10]

This method monitors the voltage at node A (see Figure 2.2). It is usually the RMS voltage, which is measured. If there is a decrease in the RMS voltage, the current output is lowered, which lowers the power output of the inverter. Alternatively, if there is an increase in the RMS voltage, the converter attempts to increase the output power. If the grid is connected, it will have no effect since the extra power required/provided is then provided/absorbed by the grid. The preferred response of the inverter is a power reduction to reduce the chance of equipment damage.

It has been proposed that an accelerated method should be used to reduce the trip time. The current change would then happen in exponentially increasing step sizes.

This method is very easy to implement in micro-controller-based inverters. It is also believed that this method is the most effective in terms of the positive feedback methods. In combination with the Sandia Frequency Shift method, a theoretical NDZ is created that is so small that it is difficult to create it experimentally.

This method is not recommended if the grid is weak or has poor power quality. The efficiency of the inverter is reduced because of the reduction in the output power. Inverters that use maximum power point tracking will be operating slightly below their maximum power levels.

If used on a weaker grid, it is recommended that the penetration levels be kept as low as possible to avoid system-level problems.

The method has a NDZ similar to UVP/OVP but much, much smaller. The effect that the quality factor of the load has on this method is negligible.

2.3.7 REACTIVE POWER PERTURBATION METHOD [6]

This method perturbs the reactive power output (Q_I) by a predefined percentage while keeping the real power output constant (P_I). The real and reactive power supplied by the inverter is varied by altering the phase between the grid voltage and the inverter current. The voltage and frequency at node A (see Figure 2.2) are monitored continuously.

The islanded frequency can be calculated as follows:

$$\omega_i = \frac{1}{\sqrt{LC}}\left(\frac{1}{2}\frac{Q_I}{Q_f P_I}+1\right) \tag{2.12}$$

And the deviation as follows:

$$\Delta\omega_i = \omega_{i[k]} - \omega_{i[k-1]} \tag{2.13}$$

Where

Q_f is the quality factor of the load

P_I is the active power output of the inverter

Q_I is the reactive power output of the inverter.

When the grid is connected, the deviation in the reactive power will have no effect and the frequency will remain fixed. When the grid disconnects, a change in $\Delta\omega_i$ is noticed due to the perturbation in Q_I. A change in $\pm 1\% \le \Delta\omega_i \le \pm 2\%$ is considered to result in a higher possibility of islanding. This change is observed for at least four cycles. If there is an increase in frequency, the inverter will be automatically shut down.

If the change remains within the above mentioned range, the real power is automatically lowered to 80% for another 10 cycles. If the voltage drops below 0.9 per unit, islanding is confirmed and the inverter is shut down. If the voltage remains normal, the inverter continues to operate normally.

This method may fail if several small units are connected and if they operate independently of each other. The method has a very small NDZ and is fast acting. Both

simulation and experimental results confirmed that this method is effective and that it is of practical use.

2.3.8 FREQUENCY JUMP [10]

The frequency jump method is a modification of the frequency bias method with similarities to the impedance measurement method. This method inserts dead zones into the output current according to pre-assigned patterns. Some of these patterns can be quite complicated.

As long as the grid is connected, the voltage waveform is dominated by the grid. After disconnection, islanding is prevented by deviation in frequency or by monitoring the voltage at node A (see Figure 2.2) for variations.
This method is only relatively effective in the single-inverter case and less effective in the multi-inverter instance. If the pattern is sophisticated enough, then this method should prevent islanding for almost all cases in a single-inverter system. Effectiveness can be improved in the multiple inverter case if the patterns can be synchronized.

2.3.9 MAINS MONITORING UNITS WITH ALLOCATED ALL-POLE SWITCHING DEVICES CONNECTED IN SERIES (MSD) - ALSO CALLED ENS [10]

This system consists of two independent automatic isolating facilities, diverse parallel mains monitoring devices with allocated switching devices connected in series in the external and neutral conductor. The two units are independently controlled and use multiple methods to prevent and/or detect islanding.

Figure 2.6 is a general block diagram showing a design of an automatic disconnection device according to DIN-VDE-0126[10]. The methods used in this setup are impedance detection, OVP/UVP and OFP/UFP. Both units monitor the quality of the grid by continuously measuring the voltage, frequency and impedance.

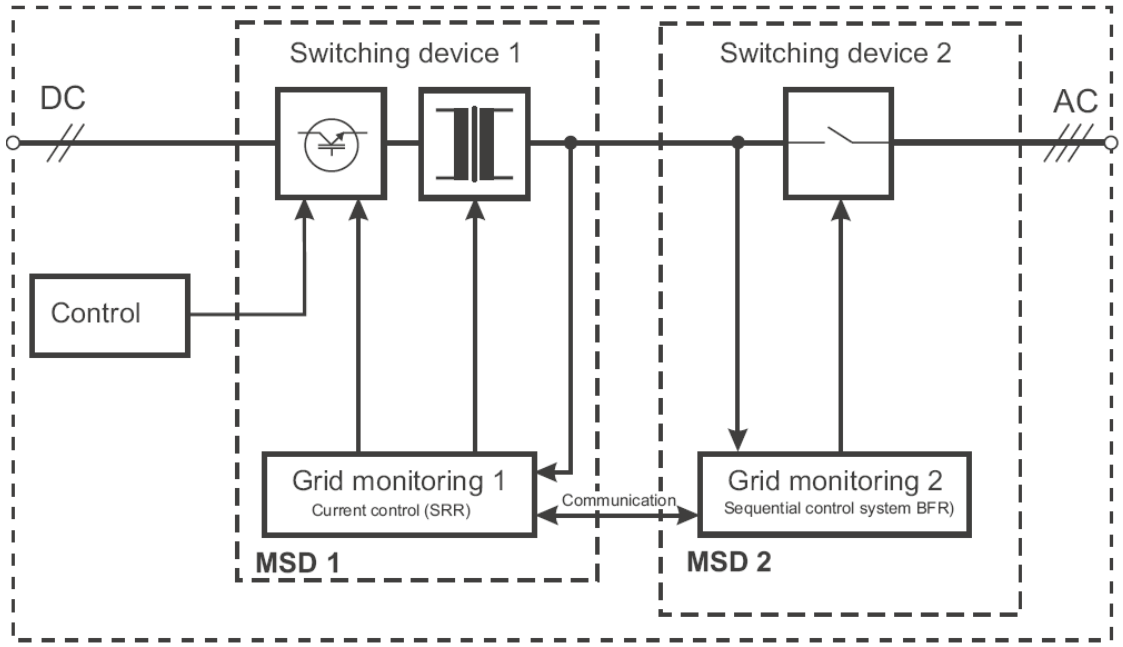

Figure 2.6 Design of an automatic disconnection device

The units also perform an automatic self-test before connecting to the grid. This improves the reliability of this method. The basic design has changed over time as various manufacturers made improvements. Checking the impedance has been one of the major improvements and changes that have been made.

The impedance of the grid is monitored by injecting a small current into the grid. The circuit then checks for significant changes in the impedance of the grid over a short period. These kinds of changes usually happen when the grid disconnects. The size of the allowed change varies by country and sometimes by utility.

All switches used in this method are required to have a load break rating in accordance with the nominal power output of the inverter. The circuit also checks functionality on a regular prescribed basis. An isolation transformer is usually used in this instance. All inverters that implement this method must be 100% factory tested before they are delivered.

Self-testing at start-up in combination with the impedance measurement method makes this a very practical and reliable method. This method should work very well in a large multiple inverter system, though it has not yet been proven.

The possibility of nuisance trips rises as the number of units increases on a system, but most modern units check for other installations and then adjust the timing of their current injections to reduce interference. Variation in line impedance might also cause some problems.

A NDZ will consist of values in impedance, frequency and voltage inside the detection limits of the trip windows. The de-synchronization of the injection time can also contribute to the size of the NDZ.

2.4 METHODS AT UTILITY LEVEL

2.4.1 IMPEDANCE INSERTION [10]

This method inserts a low-value impedance, which is usually a capacitor bank on the grid side of the system inside the potential island, as shown in Figure 2.7. The switch connecting the capacitor to node B is normally open.

When the switch that connects the grid at node B opens, the switch that connects the capacitor closes after a time delay. If the local load is balanced, islanding will occur before the capacitor is connected. Upon connection of the capacitor, the balance will be disrupted and the inverter will shut down. The capacitor will cause a change in current phase and frequency.

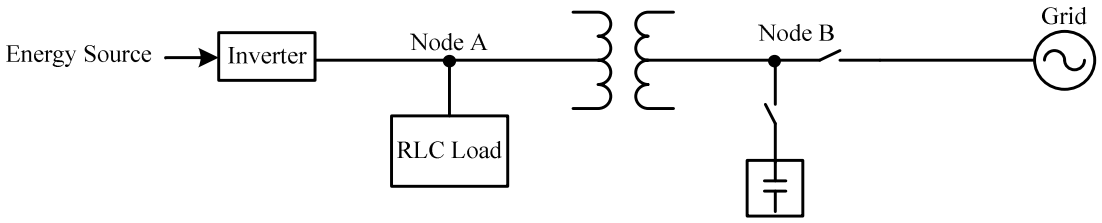

Figure 2.7 Impedance insertion method with capacitor bank

The purpose of the time delay between the disconnection of the grid and the connection of the capacitor is to eliminate the possibility that the addition of the capacitor will balance the load. If an island is formed before the capacitor is connected, the inverter will shut down prior to the connection of the capacitor.

It is possible to use another type of impedance, but capacitors are preferred because the same designs can be used that are implemented in network compensation.

This method has been shown to be very effective if the delay is small enough. As mentioned before, these capacitors are already in use in most utilities. If the capacitor is already connected, it can simply be disconnected to prevent islanding.

Nonetheless, there are some major drawbacks to this method as well. It can be expensive, since additional capacitor banks will be needed in most cases. If multiple units are installed at different times, it can furthermore lead to uncertainty as to who should carry the costs of the additional capacitors. The addition of more switches can result in additional islanding branches. The operation time of this method is also much longer than that of most of the other methods. This can lead to equipment damage and the failure to meet certain network compliances. The method also requires equipment to be installed on the grid side of the PCC, which can require additional permits and costs.

The advantage of this method is that no NDZs exist when it is properly implemented.

2.5 UTILITY/INVERTER COMMUNICATION METHODS

2.5.1 POWER LINE CARRIER COMMUNICATIONS (PLCC) [10]

This method is implemented by sending a low-energy communications signal along the power line itself. This signal is then used to perform a continuity test for the line. Figure 2.8 shows the basic configuration of such a system. The transmitter (*T*) sends a signal along the line to the receiver (*R*). The receiver is located on the customer side of the PCC. The implementation of the receiver will depend on the design specification of the inverter.

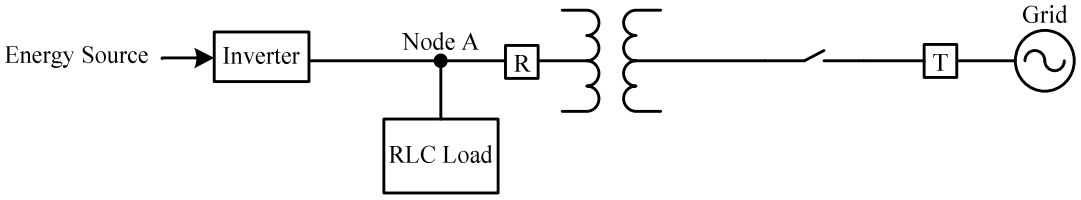

Figure 2.8 System configuration including PLCC

This method also makes it possible to use the DG unit as a backup power supply. The customer can be disconnected from the grid without shutting down the inverter itself. PLCC methods are already being used during load shedding, thus making it possible to shut down non-critical loads during high demand periods.

To use this method fully, the PLCC signal should have certain characteristics. The signal must be sent from the utility to the customer. A continuous carrier signal should be used, thus ensuring that the system is fail-safe. The signal must be able to propagate well and easily through the distribution network. The series inductance of the transformers will block the high frequency signals. This means that the signal should have a low frequency. The use of sub-harmonic signals would be preferred. These signals would propagate more easily through the system, and would only be produced inside an island under highly abnormal conditions.

This method has several strengths, especially within multiple unit systems. If all loads are within normal functioning ranges, it has no NDZ. It causes no degradation of power output quality and has no impact on system transient response. The overall performance is not affected by the amount of units connected to the grid. This holds for any type of distributed generation. Existing PLCC signals can be used without affecting their normal operation and using an inexpensive receiver. Only one transmitter is needed to cover a large area.

Unfortunately, there are some weaknesses as well. There must be a PLCC unit on the system capable of sending signals to all inverters connected to the grid. This is not very common on most networks, and the transmitters tend to be a bit expensive in widespread networks. In small networks, where there is a high density of DG units, it could be viable though. Unless a larger inverter is being installed for commercial use, it would be uneconomical to install a transmitter.

As mentioned before, the only time a NDZ can occur, will be if a load inside the island replicates the PLCC signal, but this will only happen if some loads are operating under abnormal conditions.

2.5.2 SIGNAL PRODUCED BY DISCONNECT (SPD) [10]

This method is similar to the PLCC method except that it does not use the power lines to communicate. The recloser is equipped with a small transmitting unit, which send a signal to the DG unit via a microwave link, a telephone line, or other means, when the recloser opens. A continuous signal is also used to prevent failure. This will ensure that the method functions at all times.

This method has similar advantages as the PLCC method. It also makes it possible to allow additional control to be exercised over the DG. This will enhance coordination between various units and the grid.

The weakness of this method is that all switches will have to be equipped with this technology. This will firstly make it expensive, and secondly licensing can be an issue in cases where microwave transmitters are used.

2.5.3 SUPERVISORY CONTROL AND DATA ACQUISITION (SCADA) [10]

This method uses systems that are already implemented throughout the grid. This implies that it will use the sensors and communication networks already in place for normal grid operations. These SCADA networks cover most of the grid.
If sensors detect voltages when the grid is disconnected, a warning system can be triggered and the necessary precautions taken. If the inverter itself is connected to the SCADA network, it is possible to exercise some control over the inverter.

The method has similar strengths and weaknesses as the SPD method. It requires major utility involvement, which can make the installation of smaller units impractical and expensive. Furthermore, the SCADA network seldom reaches beyond substation level, where most of the smaller units are implemented. If implemented properly, though, it should have no NDZ.

2.6 SUMMARY

All the methods discussed in this chapter will deliver a reasonable form of protection against islanding. It would not be possible to implement all of them at the same time, though, due to conflicting modes of operation. It is thus necessary to identify a method or a combination of methods that would work well together and complement each other in order to create the smallest possible NDZ or even to eliminate it.

OVP/UVP and OFP/UFP will be implemented by default, since these are already in use in most inverters and furthermore form the basis of most of the other active methods. These methods are also very simple to implement within micro-controllers.

Although MSD, impedance insertion, PLCC, SPD and SCADA all have basically no NDZ and appear to be extremely effective, it would be too expensive both financially and administratively to implement most of these approaches. These methods also rely on certain equipment either being in place already or installed additionally onto the network. It would be preferable if the selected method were entirely independent of the utility. This would make it easy to install and to avoid the unnecessary time and administration that are required by the above methods.

In the next chapter, the NDZs of anti-islanding methods are discussed in more detail.

CHAPTER 3. NON-DETECTION ZONES

This chapter investigates the NDZs (mentioned in the previous chapter) of the relevant inverter based anti-islanding methods. The utility level methods are excluded as they do not fall within the scope of this thesis.

3.1 INTRODUCTION

A NDZ can be defined as a load or a range of loads under which an anti-islanding method would fail. To gain a better understanding of the effectiveness of the available passive and active anti-islanding methods, the NDZs are represented graphically. This makes it possible to gain a better understanding of how the methods will perform under various load conditions. The passive methods are represented in a *power mismatch plane* [12]. However, it is not possible to describe the theoretical non-detection zones of the active methods in the power mismatch plane for general RLC loads, as more than one combination of L and C is possible for a fixed reactive power mismatch [13]. The method proposed in [14] represents the non-detection zones in a normalized capacitance versus inductance plane. This is a time-consuming and laborious method, as a new curve needs to be calculated for each load condition. A simplified method is proposed in [12] and in [13]. In terms of this simplified method, it is not necessary to calculate a new curve for different load conditions, as the quality factor and resonant frequency are used to illustrate the non-detection zones. This plane is referred to as the $Q_f \ vs. \omega_0$ plane.

In the case of the SVS method, a design equation is derived to serve as a guide when designing this method.

3.2 THE POWER MISMATCH PLANE

This plane is used to determine the non-detection zones of the passive anti-islanding methods. A simplified representation of the circuit used to determine the NDZ is shown in Figure 3.1. If the DG and the load are matched ($\Delta P = \Delta Q = 0$), the highest probability of island formation exists when S1 opens. If island formation is detected, then S2 will open. If the DG and the load are not exactly matched, the voltage and frequency at the PCC will jump to a new value after S1 has opened. If the power mismatch ($\Delta P, \Delta Q$) is

large enough, the voltage and the frequency may fall outside the nominal values of the voltage and frequency protection methods. In that case, island formation is prevented and the converter is shut down.

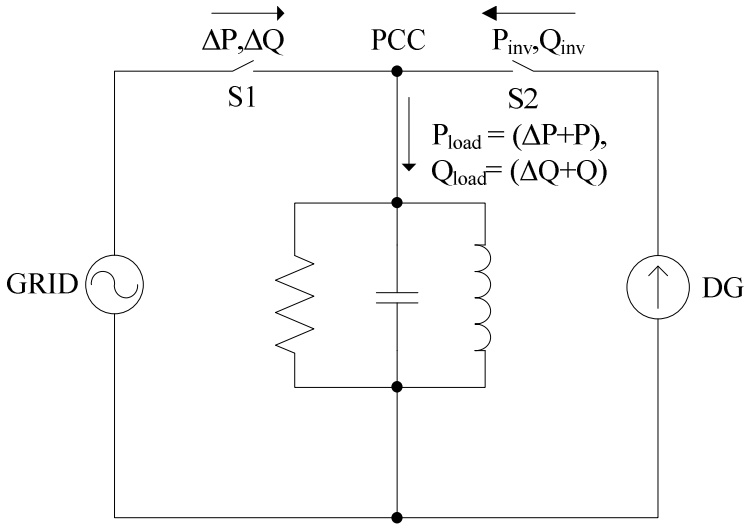

Figure 3.1 Circuit of a generic system used to test anti-islanding methods

The axes of the plane are represented by the percentage power mismatch between a load that is 100% balanced with the DG power output and the actual load, where the x-axis is *ΔP/P* and the y-axis *ΔQ/P*.

To comply with the IEEE 1547:2003 standards, the definition for the RLC load as a testing condition is as follows:

1. The RLC load must resonate at the nominal frequency of the grid.
2. The quality factor Q_f of the RLC load is set to 2.5.
3. The power generated by the DG should match that of the RLC load.

Under ideal conditions, such a load will result in the DG and RLC load resonating at the nominal voltage and frequency of the grid. If there is a mismatch between the load and the DG, though, the resonating voltage and frequency will be different. The power mismatch plane is used to illustrate the mismatch graphically, which can result in the resonating values still falling within the operational specification of the network.

It is possible to derive a relationship between the power mismatch and the voltage/frequency thresholds for the voltage and frequency protection methods [11]. This derivation is simplified by omitting the quadratic terms, but is still deemed accurate enough [11]. The derived relationship is expressed as follows [11]:

$$\left(\frac{V_{nom}}{V_{\max}}\right)^2 - 1 \le \frac{\Delta P}{P} \le \left(\frac{V_{nom}}{V_{\min}}\right)^2 - 1 \tag{3.1}$$

$$Q_f \cdot \left(1 - (\frac{f_{nom}}{f_{\min}})^2\right) \le \frac{\Delta Q}{P} \le Q_f \cdot \left(1 - (\frac{f_{nom}}{f_{\max}})^2\right) \tag{3.2}$$

The maximum and minimum values of the voltage and frequency protection are selected in accordance with the levels specified in the NRS 048-2:2004 standard. By using the values listed in Table 3.1 the non-detection zone for over/under voltage and frequency protection is calculated.

Table 3.1 NDZ Parameters

Parameter	Value
Q_f	2.5
V_{nom}	400 V
f_{nom}	50 Hz
V_{max}	440 V
V_{min}	360 V
f_{max}	51 Hz
f_{min}	49 Hz

The results from solving (3.1) and (3.2) with the values as in Table 3.1 are as follows:

$$-17.36\% \le \frac{\Delta P}{P} \le 23.13\% \tag{3.3}$$

$$-10.31\% \le \frac{\Delta Q}{P} \le 9.71\% \tag{3.4}$$

It is possible to decrease the size of the NDZ by changing the tripping limits of the DG, but this can lead to nuisance trips when the grid is connected, as the level will then fall within the compatibility levels of the NRS 048-2:2003 standard. The graphical

representation of the NDZ is shown in Figure 3.2. The limits of the over/under protection methods are indicated.

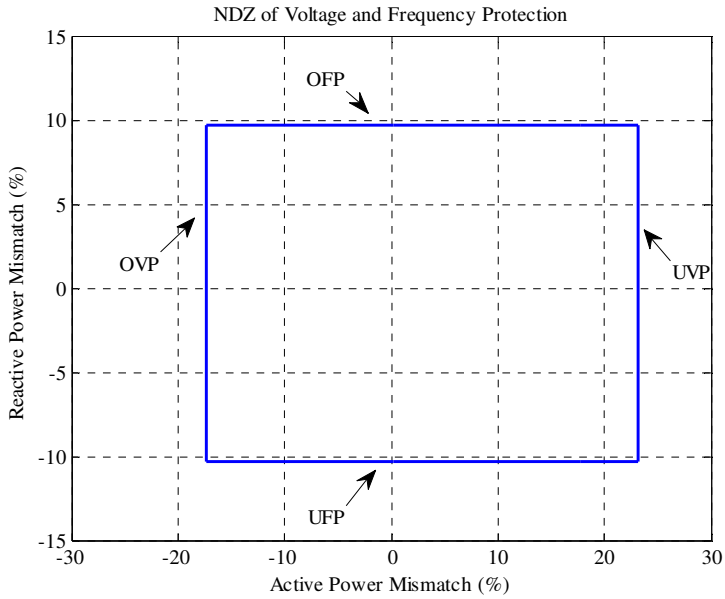

Figure 3.2 NDZ of over/under voltage and frequency protection

Four cases are identified in which OVP/UVP or OFP/UFP will prevent the formation of an island [15]:

1) $\Delta P > 0$: The active power output of the inverter is less than that required by the load. After disconnection, when $\Delta P = 0$, the voltage at the PCC will decrease. If the voltage drop is significant enough, the UVP method will cause the inverter to shut down.
2) $\Delta P < 0$: The inverter is producing more active power than the load requires. After disconnection, when $\Delta P = 0$, the voltage at the PCC will increase. If the increase is significant enough, the OVP method will cause the inverter to shut down.
3) $\Delta Q > 0$: The load has an inductive reactive component, which results in a lagging power factor. After disconnection, when $\Delta Q = 0$, and if assumed $Q_{inv} = 0$, then frequency at the PCC must increase to lower the inductive part and to increase the capacitive part. The change in frequency will continue until $Q_{load} = 0$. If the change is large enough, the OFP method will cause the inverter to shut down.
4) $\Delta Q < 0$: The load has a leading power factor that corresponds to a capacitive reactive component. After disconnection, when $\Delta Q = 0$, the frequency must decrease until $Q_{load} = 0$. If the decrease in frequency is large enough, the UFP method will cause the inverter to shut down.

The size of the NDZ may vary when different control strategies are implemented [11]. All grid connected inverters must have UVP/OVP and UFP/OVP protection to comply with the IEEE 1547:2003 standard.

In addition to the voltage and frequency protection method, the voltage phase jump method is a very commonly used passive island prevention method. The NDZ of the voltage phase jump method in the power mismatch plane is derived as follows [11]:

$$\left|\arctan\left(\frac{\Delta Q / P}{1+\Delta P / P}\right)\right| \leq \theta_{thres} \tag{3.5}$$

where θ_{thres} is the threshold of the phase jump detection. If the threshold is set too low, it can lead to nuisance trips, but if it is set too high, it can lead to poor performance of the protection method. By adjusting (3.5) as follows, it is possible to map the NDZ of the phase jump detection method in the power mismatch plane:

$$\frac{\Delta Q}{P} \leq \tan\left(\theta_{thres}\right) \cdot \frac{\Delta P}{P} + \tan\left(\theta_{thres}\right) \tag{3.6}$$

The power mismatch plane representation of the voltage phase jump method is shown in Figure 3.3. The NDZs for various threshold settings are indicated, and the limits of the voltage and frequency protection methods are shown.

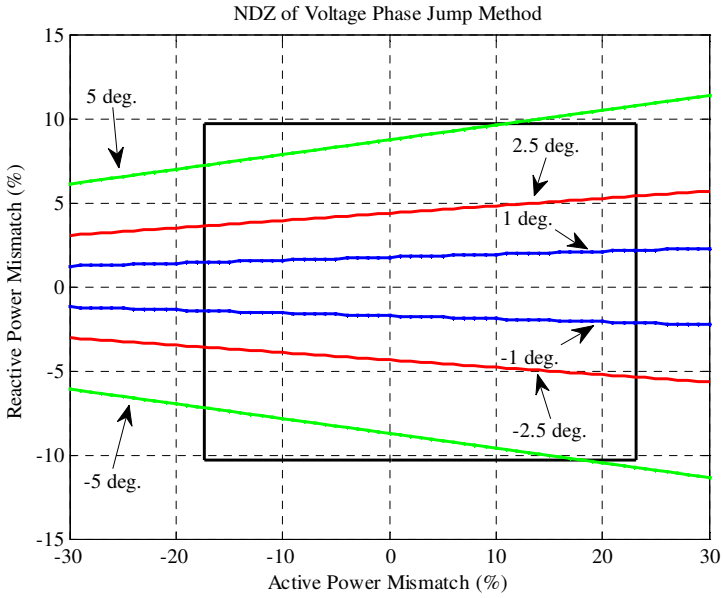

Figure 3.3 NDZs of various voltage phase jump thresholds

It should be noted that the NDZ is independent of the quality factor of the load. Like the frequency protection method, the phase jump method is less sensitive to active power mismatches. By increasing the threshold, the size of the NDZ also increases, leading to poor performance of the method. If the threshold is set too low, a false trip can be generated during switching events of the power systems.

The voltage phase jump method will thus not be implemented in this thesis as the active methods provide better island prevention options.

3.3 THE Q_f VS. ω_0 PLANE

The power mismatch plane is inadequate to determine the non-detection zones of frequency drift active island prevention methods. This is because, for a fixed reactive power mismatch, more than one combination of L and C is possible [13]. By using the quality factor of the load as a parameter, the various combinations of RLC loads are accounted for. The work in this section is a summary of the work presented in [12] and in [13], but is adapted to a grid with a nominal frequency of 50 Hz.

The quality factor is defined as the ratio of the stored energy to the dissipated energy per cycle at a given frequency, with the quality factor for a parallel RLC load calculated as follows:

$$Q_f = \frac{2\pi\left(\frac{1}{2}CR^2I^2\right)}{\frac{\pi RI^2}{\omega_0}} = \omega_0 RC = \frac{R}{\omega_0 L} = R\sqrt{\frac{C}{L}} \tag{3.7}$$

where $\omega_0 = (1/\sqrt{LC})$ is the resonant frequency of the load. The magnitude and phase of a parallel RLC load in terms of the resonant frequency f_0, the quality factor and an arbitrary frequency are as follows:

$$\left|Z_{load}\right| = \frac{1}{\sqrt{\frac{1}{R}+\left(\frac{1}{\omega L}-\omega C\right)^2}} = \frac{R}{\sqrt{1+Q_f^2\left(\frac{f_0}{f}-\frac{f}{f_0}\right)^2}} \tag{3.8}$$

$$\phi_{load} = \tan^{-1}\left(R\frac{1-\omega^2 LC}{\omega L}\right) = \tan^{-1}\left[Q_f\left(\frac{f_0}{f}-\frac{f}{f_0}\right)\right] \tag{3.9}$$

The change in magnitude of the load impedance is very small for loads with a $Q_f < 2.5$ in the region close to the compatibility levels of the grid, as specified in the NRS 048-2:2003 standards. Figure 3.4 is an example of how the magnitude of the load impedance changes with frequency for various quality factors and $R = 14.4\ \Omega$.

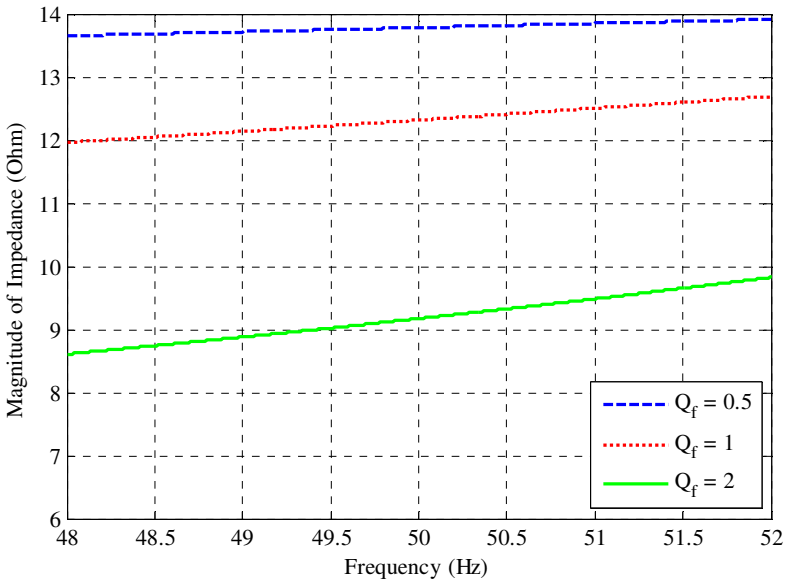

Figure 3.4 Magnitude of load impedance vs. frequency of grid

It can be assumed from this that the voltage magnitude does not vary within the system frequency limits. In Figure 3.5 it is shown how the load phase angle θ_{load} ($\theta_{load} = -\phi_{load}$) changes with frequency for loads with different resonant frequencies.

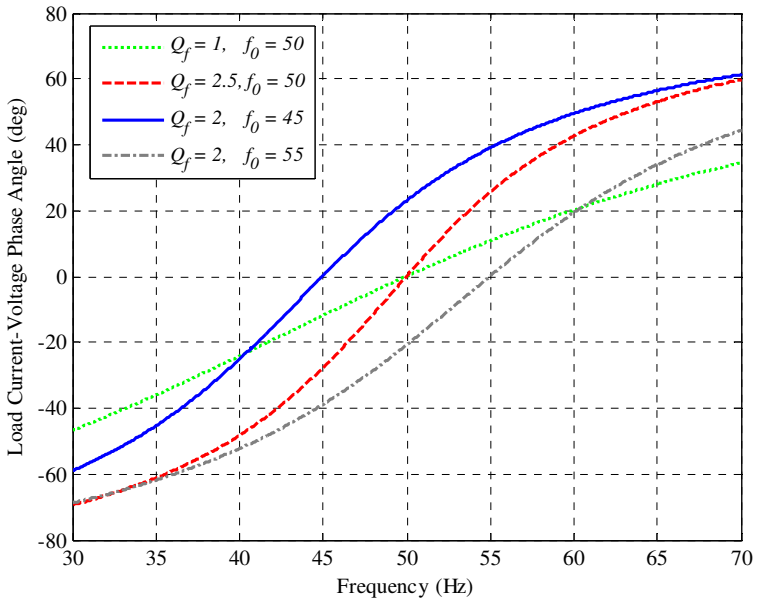

Figure 3.5 Load angle variations of a RLC load for different values of Q_f and f_0

In addition, it is also noted that loads with a resonant frequency lower than the grid frequency are net capacitive at the grid frequency (the current leads the voltage) and net inductive at the grid frequency (the current lags the voltage) when the resonant frequency is higher.

By using power balance equations, the steady state island voltage magnitude and frequency for a parallel RLC circuit can be calculated as follows:

$$P_{load,island} = \frac{V_{island}^{\ 2}}{R} = P_{inverter} \tag{3.10}$$

$$Q_{load,island} = \frac{V_{island}^{\ 2}}{X_{C,grid}} \left[\left(\frac{f_0}{f_{island}} \right)^2 - 1 \right] = Q_{inverter} \tag{3.11}$$

It can be concluded from (3.10) that the islanded voltage is dependent on the active power output of the converter and the value of *R*. The large change in active power required to change the islanded voltage makes it impractical to implement only a voltage drifting island prevention method. The frequency is drifted by varying the reactive power output of the converter. Such a method will be more practical if it is assumed that the island voltage magnitude only depends on $P_{inverter}$ and *R*. A change that is smaller in reactive power than in active power is required to drift the voltage frequency outside the specified limits.

To determine the NDZs for the active frequency drift methods, the phase angle of the current relative to the voltage needs to be approximated. Sandia frequency shift, active frequency drift and the frequency jump method all insert dead time into the current reference. As these methods are very similar to each other, only the NDZ of the Sandia frequency shift method will be determined. NDZs for the other two methods can be derived in a similar way. The NDZ of the slip mode frequency shift method will also be determined, as it also drifts the frequency, but without the insertion of dead time.

3.3.1 NON-DETECTION ZONE OF THE SLIP MODE FREQUENCY SHIFT METHOD

The reactive power output of the converter is changed by shifting the phase of the current relative to the voltage. The current phase angle is set to be a function of the deviation of the cycle-by-cycle frequency of the island from the grid frequency. The current reference can be expressed as follows:

$$i_k = I_{peak} \sin(2\pi f_{vk-1} t + \theta_{SMS}) \tag{3.12}$$

The phase angle can be expressed in terms is the maximum frequency f_m and the maximum phase shift θ_m as follows:

$$\theta_{SMS} = \theta_m \sin\left(\frac{\pi}{2}\frac{f_{vk-1} - f_g}{f_m - f_g}\right) \tag{3.13}$$

In order for the frequency of the islanded system to drift after disconnecting from the grid, the following equation must be satisfied at the grid frequency:

$$\frac{d\theta_{load}}{df} < \frac{d\theta_{SMS}}{df} \tag{3.14}$$

By using (3.14), a design equation for the slip mode frequency shift method is derived as follows:

$$\frac{\theta_m}{f_m - f_g} \geq \frac{12 Q_f}{\pi^2} \tag{3.15}$$

where Q_f is the maximum quality factor at which the formation of an island can be prevented. By using the phase criteria, the NDZ of the slip mode frequency shift method can be derived by setting (3.9) equal to (3.13). That is:

$$\tan^{-1}\left[Q_f\left(\frac{f_0}{f_{is}} - \frac{f_{is}}{f_0}\right)\right] = \theta_m \sin\left(\frac{\pi}{2}\frac{f_{vk-1} - f_g}{f_m - f_g}\right) \tag{3.16}$$

where f_{is} is the islanded frequency. The above equation can then be transformed into the following equation to plot the NDZ:

$$f_0^2 - \frac{f_{is} \tan\left[\theta_{SMS}(f_{is})\right]}{Q_f} f_0 - f_{is}^2 = 0 \tag{3.17}$$

It is shown in [12] how (3.17) can be simplified to the following:

$$f_0 = \frac{2Q_f f}{2Q_f + \theta_{SMS}(f)} \tag{3.18}$$

Loads with a resonant frequency lower than the grid frequency will have a stable operational point lower than the grid frequency and vice versa for loads with a resonant frequency higher than the grid frequency. The boundaries of the NDZ are plotted by using the following equations:

$$\begin{aligned} f_{0,\max} &= \frac{2Q_f f_{\max}}{2Q_f + \theta_{sms}(f_{\max})} \quad \text{when } f_0 > f_g \\ f_{0,\min} &= \frac{2Q_f f_{\min}}{2Q_f + \theta_{sms}(f_{\min})} \quad \text{when } f_0 < f_g \end{aligned} \tag{3.19}$$

where f_{max} and f_{min} are the trip limits of the frequency protection method. In Figure 3.6, the non-detection zones are shown for different values of θ_m. The maximum frequency, f_m, is selected as 53 Hz. The NDZ is the region between the curves. If the load has a resonant frequency and a quality factor that falls within this region, it will not be detected by the island prevention method.

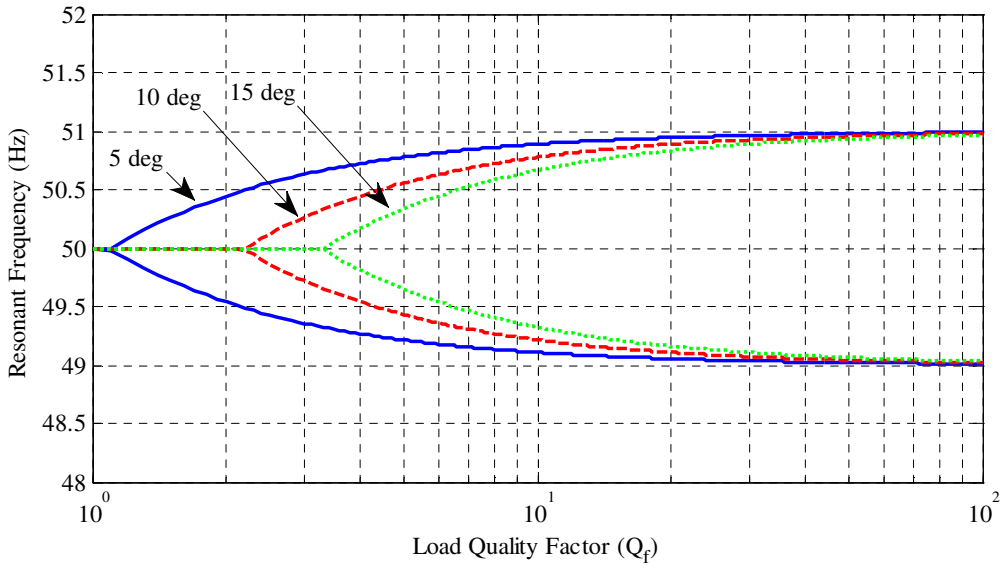

Figure 3.6 NDZs for different values of the maximum phase deviation of the slip mode frequency shift method

It can be seen that by changing the value of θ_m the size of the NDZ changes. For an angle of 15˚ no NDZ exists for loads with a $Q_f < 3.3$. Thus, designing the island protection method correctly would make it possible to avoid island formation entirely.

3.3.2 NON-DETECTION ZONE OF THE SANDIA FREQUENCY SHIFT METHOD

The dead time inserted into the current reference by the Sandia frequency shift method also results in a phase shift between the voltage and the current. The dead time results in a distorted reference signal. It is shown in [16] that the distorted reference can be represented by a Fourier series, which has a sinusoidal fundamental that is time shifted by $t_z/2$ (refer to Figure 2.5). The load voltage will be in phase with the fundamental component of the reference. Therefore, the frequency of the load voltage will always be lower than that of the reference by $t_z/2$. The output phase angle of the inverter can be expressed as follows:

$$\theta_{SFS}(f) = \frac{\omega t_z}{2} = \frac{\pi c f(f)}{2} \tag{3.20}$$

where the 'chopping fraction' is calculated by using (2.11). The NDZ of the Sandia frequency shift method can be derived by using the phase criteria as follows:

$$\tan^{-1}\left[Q_f\left(\frac{f_0}{f} - \frac{f}{f_0}\right)\right] = \frac{\pi}{2}\left[cf_0 + k\left(f_{is} - f_g\right)\right] \tag{3.21}$$

As in the SMS method, the above equation can be transformed into the following to plot the NDZ of the Sandia frequency shift method. That is:

$$f_0^2 - \frac{f_{is}\tan\left[\theta_{SFS}\left(f_{is}\right)\right]}{Q_f} f_0 - f_{is}^2 = 0 \tag{3.22}$$

In Figure 3.7 the non-detection zones of the Sandia frequency shift method are shown for different gain values. The zero error chopping fraction is $cf_0 = 0.05$.

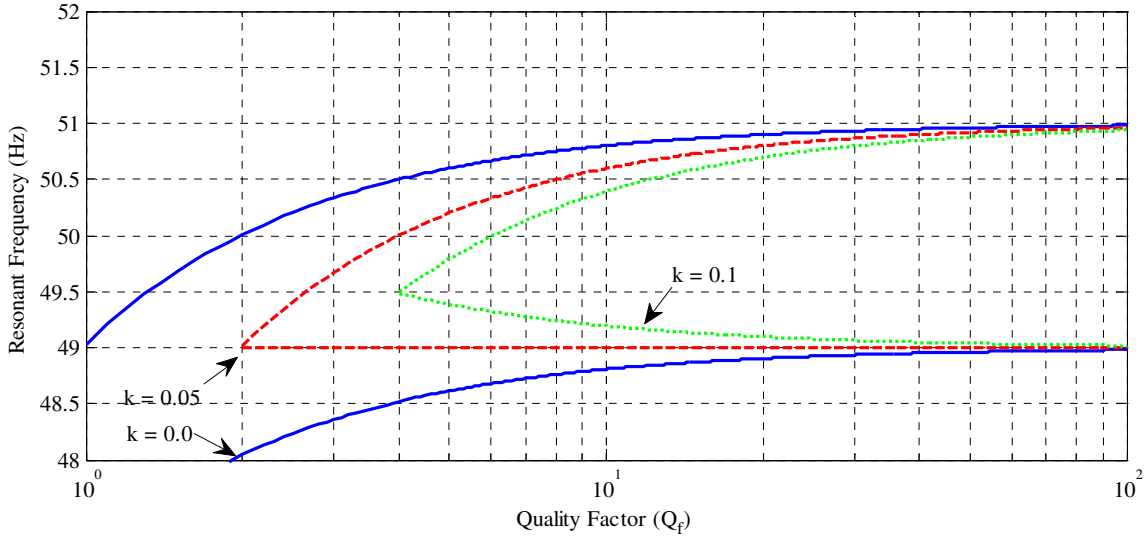

Figure 3.7 NDZ of the Sandia frequency shift method for different gain values

By increasing the gain of the feed forward loop, the quality factor for which islanding can be prevented also increases. In the case where the gain is set to zero, the non-detection zone is the same as for the active frequency drift method. As with the slip mode frequency shift method, this method will prevent the formation of an island if designed correctly.

3.4 NON-DETECTION ZONE OF THE SANDIA VOLTAGE SHIFT METHOD

Changes in the voltage at the PCC will activate the feed forward response of the Sandia voltage shift method. The amplitude of the per unit reference current is changed in the direction of the deviation. The maximum change is limited to prevent run-away of the reference, which could damage the inverter. This limit is set outside the UVP/OVP limits. When connected to the grid, the inverter cannot change the voltage at the PCC. After disconnection, the absence of the grid enables the inverter to change the output voltage. If there is more than one inverter connected to the PCC, the performance of the island prevention method is improved, since the voltage at the PCC is common to all the inverters. The RMS voltage is measured over a half-cycle and the reference is then updated for the next cycle.

The equation that is used to update the amplitude of the reference is

$$I_{pu} = 1 + K_{SVS}(V_{RMS,k} - V_{RMS,k-1}) \tag{3.23}$$

where

K_{SVS} is an accelerating gain, not changing the sign,

V_{RMS} is the filtered RMS value of the current half-cycle

$V_{RMS,\,filt}$ is the filtered RMS value of the previous half-cycle.

The control block diagram of the Sandia voltage shift method is shown in Figure 3.8. A low-pass filter is used to control the response time of the method as well as to filter out unwanted noise caused by the switching of the converter on the measurements.

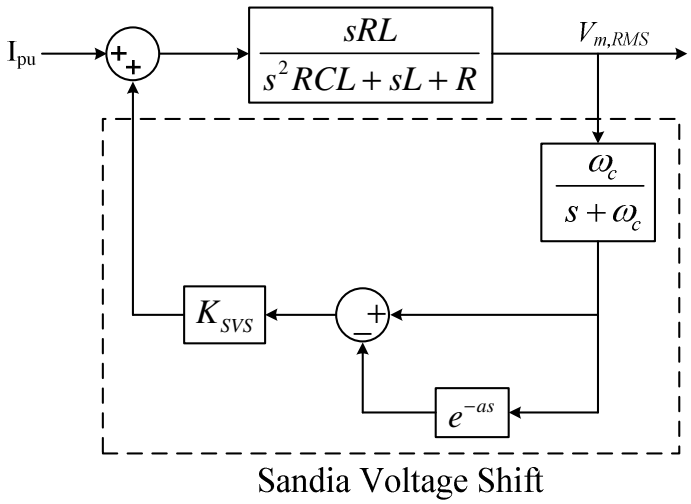

Figure 3.8 Control block diagram of the Sandia voltage shift method

To determine the transfer function the control block diagram needs to be simplified. The Sandia voltage shift method is therefore reduced as shown in Figure 3.9.

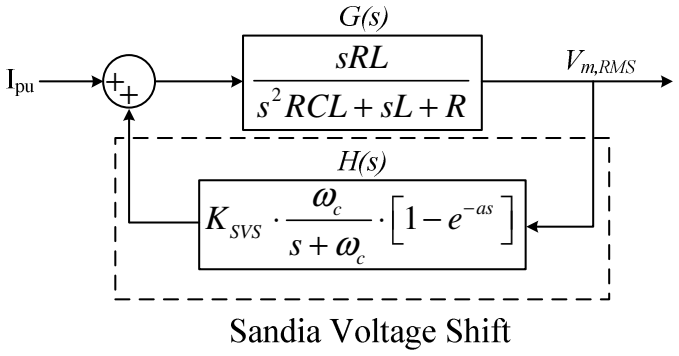

Figure 3.9 Simplified control block diagram of the Sandia voltage shift method

The exponential term of the time delay is simplified by using a Taylor series expansion as in [17]. The Taylor series is

$$e^{x} = \sum_{n=0}^{\infty} \frac{x^{n}}{n!} = 1 + \frac{x}{1!} + \frac{x^{2}}{2!} + \frac{x^{3}}{3!} + ... \approx 1 + x \tag{3.24}$$

which simplifies the time delay as

$$e^{-as} \approx 1 - as \tag{3.25}$$

The basic block diagram of a feedback loop can be expressed as follows [18]:

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1 + G(s) \cdot H(s)} \tag{3.26}$$

It is now possible to determine the transfer function of the Sandia voltage shift method and the load.

$$\frac{V_{m}(s)}{I_{pu}(s)} = \frac{s^{2} RL + s\omega_{c} RL}{s^{3} RLC + s^{2}\left(L + \omega_{c} RLC - aRLK_{svs}\omega_{c}\right) + s\left(R + \omega_{c}\right) + \omega_{c} R} \tag{3.27}$$

After disconnection, the system must be unstable to force the voltage outside the limits. A pole in the right hand side of the imaginary plane will destabilize the system after disconnection. This can be achieved by selecting the correct combination of gain and cut-off frequency of the filter. To place a pole in the right hand side of the imaginary plane, the following inequality must be met:

$$L + \omega_{c} RLC - aRLK_{SVS}\omega_{c} < 0 \tag{3.28}$$

thus,

$$K_{SVS} > \frac{1}{aR\omega_{c}} + \frac{C}{a} \tag{3.29}$$

The value of K_{svs} must be selected to be large enough to prevent the formation of an island, but also small enough to avoid performance issues or nuisance trips of the system. In Table 3.2 the parameters of 3.3 kW load are listed. The load resonates at 50 Hz and the low-pass filter has a cut-off frequency of 25 rad/s. The interval at which the Sandia voltage shift calculations are done is 0.01 ms.

Table 3.2 Sandia voltage shift parameters

Parameter	Value
P	3.3 kW
R	16.03 Ω
C	100 uF
L	101.32 mH
ω_c	25 rad/s
a	10 ms

By using (3.29) the stability threshold gain is calculated as K_{svs} = 0.2595. The transfer function of the system is calculated by using (3.27) with K_{svs} = 0.2.

In Figure 3.10, the magnitude and phase Bode plot of this system is shown.

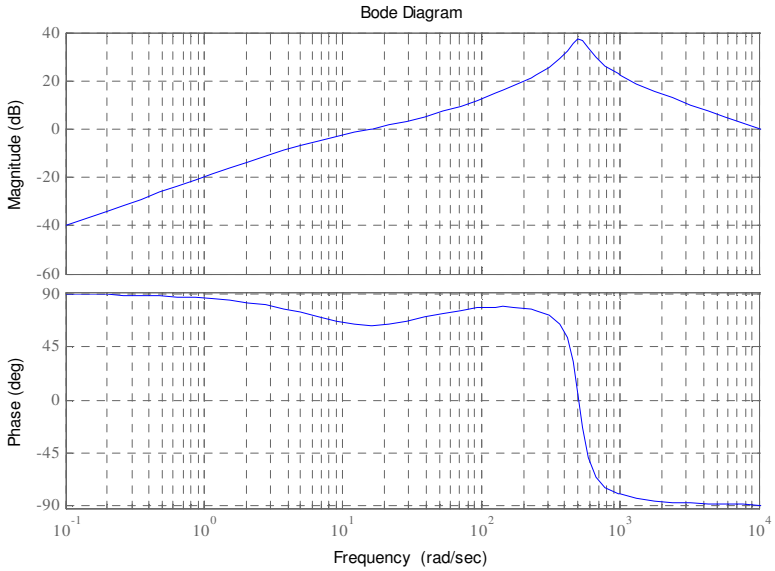

Figure 3.10 Bode plot of SVS system with K_{svs} = 2

For the system to be stable, the following must hold for the system after disconnection [19]:

$$\begin{aligned} &\angle\left(H(j\omega)G(j\omega)\right) > -180° \quad \text{if} \quad \left|H(j\omega)G(j\omega)\right| = 1 \\ &\left|H(j\omega)G(j\omega)\right| < 1 \quad \text{if} \quad \angle\left(H(j\omega)G(j\omega)\right) = -180° \end{aligned} \tag{3.30}$$

The system in Figure 3.10 complies with this and is thus stable. The gain is now set to K_{svs} = 3.

The Bode plot is shown in Figure 3.11.

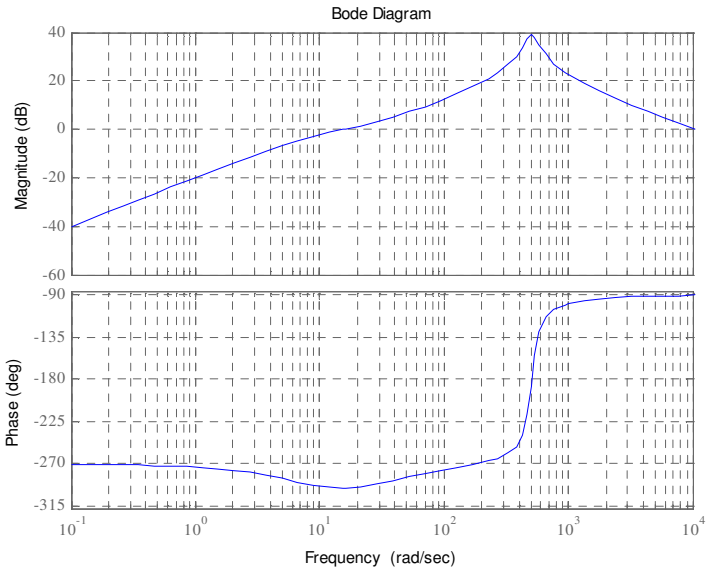

Figure 3.11 Bode plot of SVS system with K_{svs} = 3

In this case, the system is unstable after disconnection. The unstable behaviour of the system will be used to prevent the formation of an island. By increasing the gain the level of instability is increased.

It is also possible to plot the Sandia voltage shift method in the Q_f *vs.* ω_0 plane by using (3.7) and (3.29). The resulting equation is as follows:

$$\omega_0 > \frac{\omega_c Q_f}{aRK_{svs}\omega_c - 1} \tag{3.31}$$

The curve shown in Figure 3.12 is for a fixed load with different gains. For different inductor and capacitor combinations, the quality factor and resonant frequency of the load can be varied. By selecting the correct gain value, the Sandia voltage shift method can be designed for instability for any load with a quality factor less than 2.5, which falls within the limits of the over/under frequency protection method. In Figure 3.13, the gain is fixed at 3 and the load resistance is varied. This shows that, if the Sandia voltage shift method is designed to prevent island formation at the rated values of the converter, it will prevent island formation for all other operational loads of the converter too.

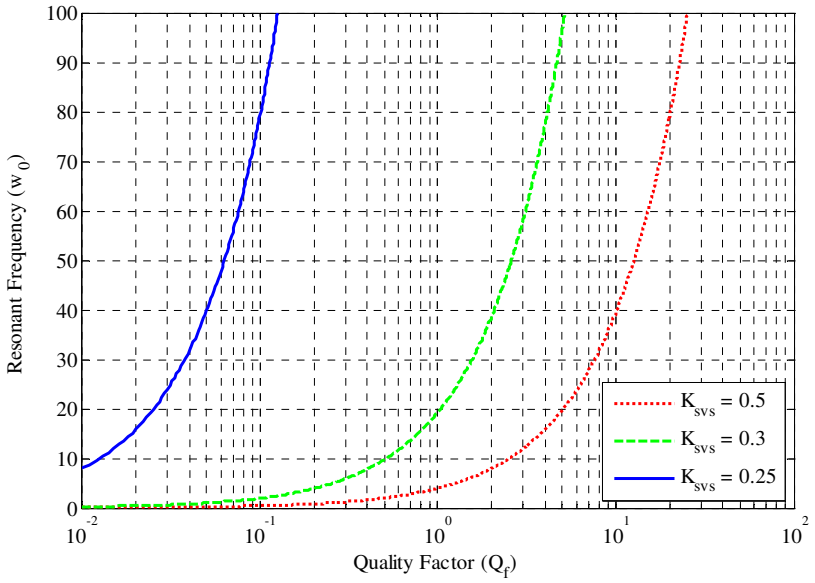

Figure 3.12 Quality factor vs. resonant frequency for different gains with a fixed load resistance

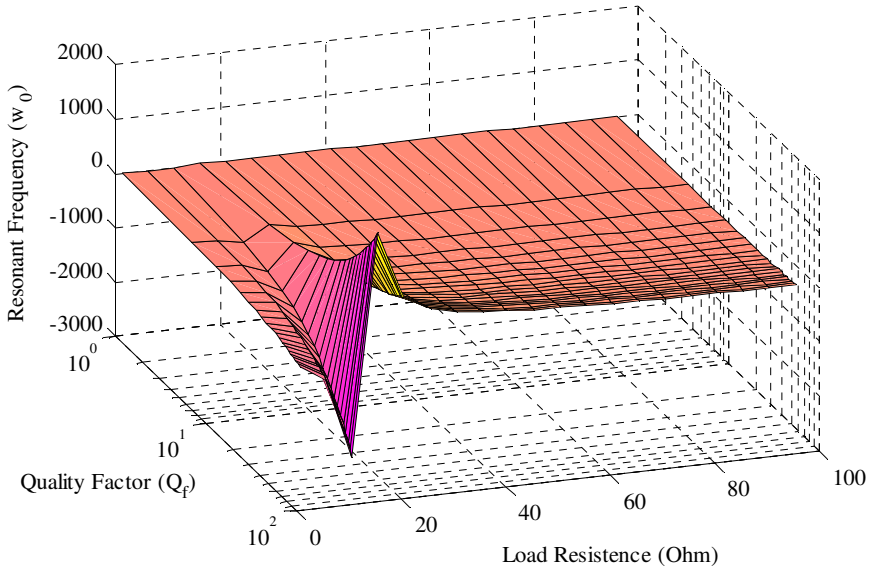

Figure 3.13 Quality factor vs. resonant frequency for a fixed gain with different load resistances

Although some of the load parameters are required to determine the gain value, this method will still aid in preventing island formation. The instability of the voltage after disconnection will also act as a trigger to activate the frequency protection methods.

3.5 ANTI-ISLANDING METHOD SELECTION

The over/under voltage and frequency methods must be implemented to shut down the converter when the voltage of the PCC is outside the limits listed in Table 3.1.

The use of methods at utility level (refer to Section 2.4) and utility/inverter communication methods (refer to Section 2.5) fall outside the scope of this thesis, however, and will not be considered. Literature has shown that the frequency drift methods are very effective in the prevention of island formation. The most common methods used in this category are active frequency drift, slip mode frequency shift and Sandia frequency shift. It can be shown that the active frequency drift method still has a NDZ [16], effectively eliminating this method.

Both the slip mode frequency shift method and the Sandia frequency shift method can be designed to have no non-detection zone. Selecting a method depends on the control strategies used and the available computational time. In this thesis, a three-phase coupled system is used. A coupled system implies that the centre tap of the DC bus is not connected to the neutral wire of the grid. Space vector pulse width modulation is used. The control calculations are done in the $\alpha\beta$-plane. Although the Sandia frequency shift method has a faster response time than the slip mode frequency shift method, it is more complicated to implement in the $\alpha\beta$-plane than the slip mode frequency shift method. To generate the Sandia frequency shift reference waveforms directly in the $\alpha\beta$-plane, the waveforms as shown in Figure 3.14 are required.

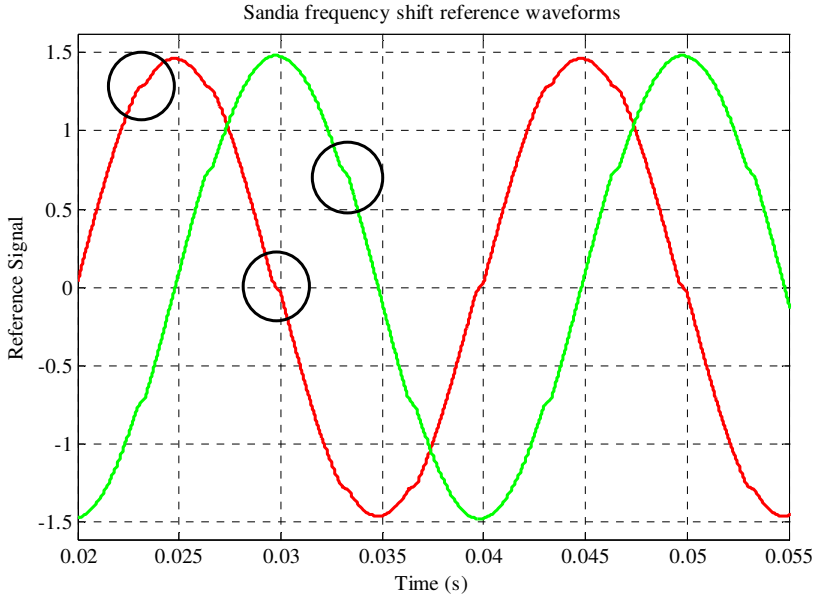

Figure 3.14 Sandia frequency shift reference waveforms in the $\alpha\beta$-plane

The distortions in the waveform required are indicated. Although it is possible to generate the reference in the *abc*-plane first, and then convert it to the $\alpha\beta$-plane, it would

require a substantial amount of additional computational time, which is not desired. The implementation of the slip mode frequency shift method is much simpler, as it only requires a phase shift in the reference vector, which is calculated directly in the $\alpha\beta$-plane. In view of the above mentioned reasons, it was decided that the slip mode frequency shift method would be implemented.

The Sandia voltage shift method will be implemented in conjunction with the slip mode frequency shift method. It is possible to implement this method independently of the frequency shift method. This method is selected because of its ability to cause a voltage trip, but also because the instability in the output voltage after disconnection will help to activate and possibly accelerate the slip mode frequency shift method.

The combination of these methods forms a very effective mechanism preventing the formation of islands.

3.6 SUMMARY

The non-detection zone concept was introduced in this chapter as a method to represent graphically the range of loads that will cause a particular anti-islanding method to fail. In the power mismatch plane, the non-detection zones of the passive methods were represented by a mismatch between the power required by the load to maintain the grid voltage amplitude and frequency on the one hand, and the power delivered by the inverter on the other. A worst case test load that complies with the IEEE 1547:2003 standard was defined and described. The compatibility levels of the grid as specified in the NRS 048-2:2004 standards were used to plot the non-detection zone of the passive over/under voltage and frequency protection methods. These methods are compulsory to all grid connected converters.

The non-detection zones of the active anti-islanding methods were graphically represented in the Q_f *vs.* ω_0 plane due to inadequacies in the *power mismatch* plane. It was shown that designing the active methods correctly could prevent the formation of an island. An equation is derived to act as a guide in designing the Sandia voltage shift method. The equation also makes it possible to represent graphically the non-detection zone of this method.

Lastly, the slip mode frequency shift method was selected as the active method to drift the frequency of the voltage beyond the compatibility levels of the grid, and the Sandia voltage shift method was selected to increase the amplitude of the voltage beyond the compatibility levels of the grid.

CHAPTER 4. ALGORITHM DEVELOPMENT AND SIMULATIONS

4.1 INTRODUCTION

The system shown in Figure 4.1 consists of two converters connected back-to-back via a DC link. One converter is connected to the grid, whereas the other is connected to a generator. An LC-filter is used to filter out the switching harmonics. The converter connected to the grid acts as a bi-directional converter. The DC bus is initially charged from the grid. During this period, the converter functions as an active rectifier. Once charged, the DC bus is regulated by exchanging power between the grid and the DC bus. During windy periods, the grid-side converter primarily functions as an inverter by delivering power to the grid.

The converter connected to the generator only functions as an active rectifier. The output voltage of the generator varies according to the speed at which the rotor of the generator turns. As the speed increases, the voltage increases in magnitude and frequency; alternatively, as the speed decreases, the voltage will decrease in magnitude and frequency. The amount of power available depends on the instantaneous wind speed. By using power electronics and the correct control algorithms, the power flow from the generator to the DC bus at various wind speeds can be controlled.

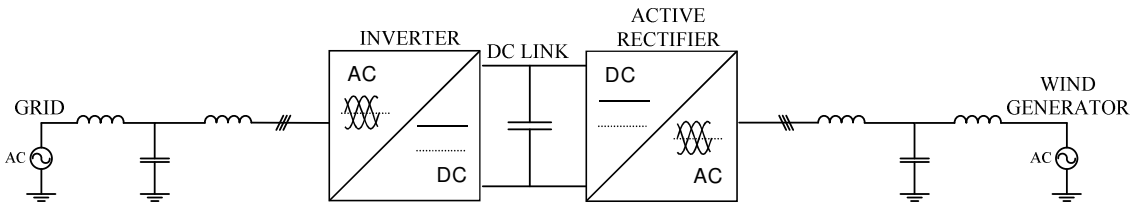

Figure 4.1 Overview of the Back-to-back system layout

In the following sections the system layout, the design of the control algorithms and dead time compensation will be discussed. The implementation of the selected anti-islanding methods will also be discussed. Finally, simulations are done to illustrate the different components of the system and the anti-islanding methods.

4.2 SYSTEM LAYOUT

4.2.1 TOPOLOGY SELECTION

The system can be connected as either a three-wire system with an insulated neutral or a four-wire system with the neutral connected to the centre tap of the DC bus. The switching is done with an insulated gate bi-polar transistor (IGBT). Each IGBT has an anti-parallel diode to serve as a free flow path for the inductor current. In Figure 4.2, the three-wire system is shown. At the output stage there is a LC low-pass filter, which is connected to the voltage source. The absence of the neutral wire implies that each phase is coupled to each other. Consequently, the output voltage of the converter depends on the switching state transitions during each switching period.

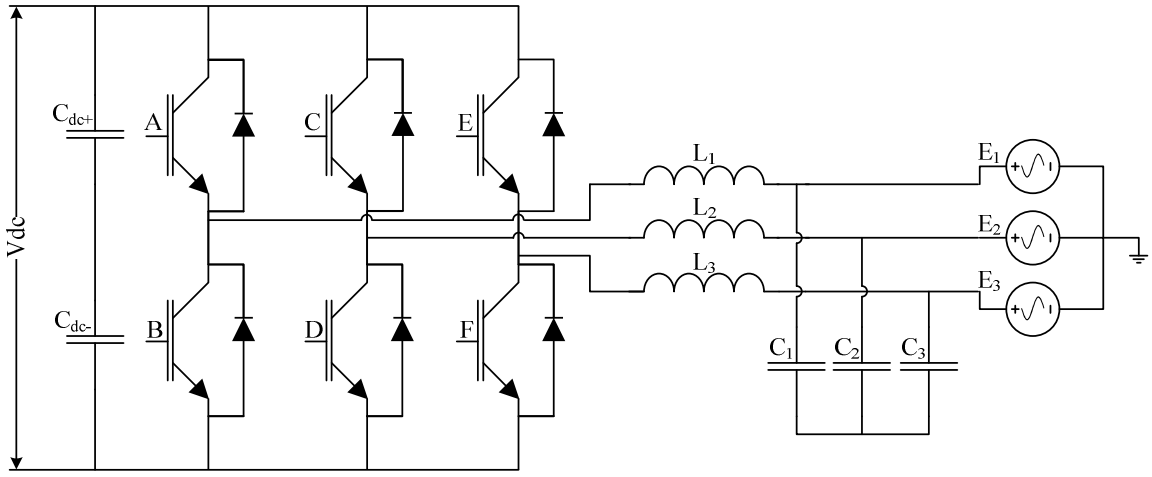

Figure 4.2 A 3-wire converter with insulated neutral wire

The interconnected nature of this topology requires a different pulse width modulation (PWM) strategy than in the case of a topology where each phase arm switches independently. This PWM strategy is referred to as space vector pulse width modulation (SVPWM). By using SVPWM, the control organization of a coupled 3-phase system can be simplified to a decoupled 2-phase system.

If the neutral wire is available, it can either be connected to the centre tap of the DC bus or be switched by an additional phase arm. In the configuration shown in Figure 4.3, the neutral wire is connected to the centre tap of the DC bus. In this case, each phase arm is decoupled from the others. Each phase arm operates independently and can be viewed and controlled as a single-phase converter. An output low-pass filter is also shown with

the system connected to the voltage source. In this case, the use of SVPWM is not required.

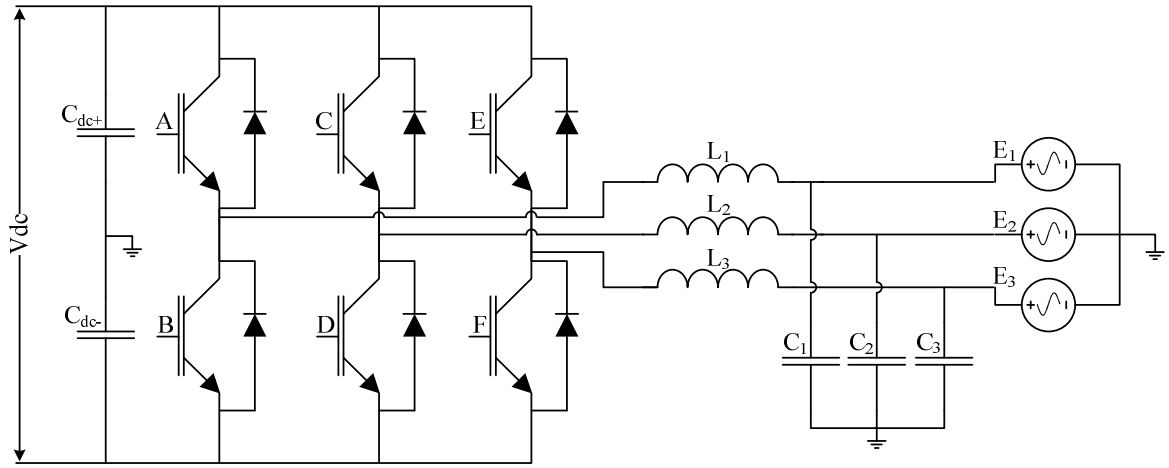

Figure 4.3 A 4-wire converter with neutral connected to DC bus centre tap

In each of the above mentioned cases, there are limitations to the DC bus voltage value. When the system is coupled, the minimum DC bus voltage can be calculated as follows:

$$V_{dc,\min} = \sqrt{2} \cdot V_{LL} \tag{4.1}$$

where V_{LL} is the line-to-line voltage. In the case of a decoupled system, in contrast, the minimum DC bus voltage can be calculated as follows:

$$V_{dc,\min} = 2 \cdot \sqrt{2} \cdot V_{LN} \tag{4.2}$$

where V_{LN} is the line-to-neutral voltage. These voltages are the values that will be forced onto the DC bus when the converter is connected to the grid and the DC bus is charged through the diodes with all the IGBTs off. If V_{LN} = 230 V_{RMS} then for the 3-wire configuration the minimum bus voltage will be $V_{dc,min}$ = 565 V, whereas for the 4-wire configuration $V_{dc,min}$ = 650 V.

It would be possible to use either of the configurations on the grid side, but only the 3-wire topology on the generator side. The 3-wire topology is selected for both sides of the converter since balanced 3-phase currents will always be drawn on both sides. This enables the use of SVPWM on both sides of the converter.

4.2.2 THE INVERTER

The inverter is used to convert the DC voltage to an AC voltage. The inverter is synchronized with the grid by using the grid voltages as a reference. The inverter serves as a current source to the grid, with no voltage control loop implemented on the AC side. By changing the phase angle between the output current of the inverter and the grid voltage, reactive power can also be delivered to the grid. Typically, the inverter will only deliver active power to the grid.

4.2.3 THE ACTIVE RECTIFIER

The active rectifier converts an AC voltage to a DC voltage. The output voltage of the generator varies in amplitude and frequency as the wind speed changes. The active rectifier should be able to track these changes and remain synchronized with the generator. In some cases, the generator is more efficient under non-unity power factor operation. It is possible to change the phase angle between the voltage and current to operate the generator under different power factors. By using an active rectifier, it is also possible to draw more power efficiently from the generator as in the case of using a diode rectifier.

4.2.4 THE DC LINK

The DC link consists of capacitors connected in series and parallel. The amount of energy that can be stored in the link depends on the capacitance value. The DC bus voltage is regulated to a fixed value by the controller. The value must be higher than the voltage calculated using (4.1). The energy from the generator is transferred to the grid via the link. The DC link de-couples the inverter from the active rectifier, enabling independent control of both converters.

4.2.5 THE LC-FILTER

The LC-filter is used to filter out the switching harmonics in the output current. The filter will typically have a cut-off frequency that is one-tenth of the switching frequency. In Figure 4.4, the LC low-pass filter configuration is shown.

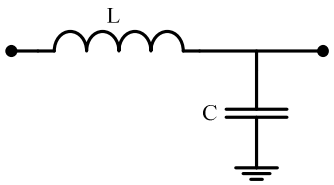

Figure 4.4 LC low-pass filter

The cut-off frequency of the low-pass filter can be calculated as follows:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.3}$$

It must be noted that the value of the inductor affects the efficiency of the system and the size of the ripple on the inductor current.

4.3 SYSTEM CONTROL

4.3.1 THE CLARKE TRANSFORMATION

The Clarke transformation can be used to reduce a three-phase system model to an equivalent two-phase system model. This reduced system can be represented in the *αβ*-plane. It is assumed that the three-phase system under discussion is balanced, with each phase separated by 120º. The graphical representation between the *abc*-plane and *αβ*-plane is depicted in Figure 4.5,

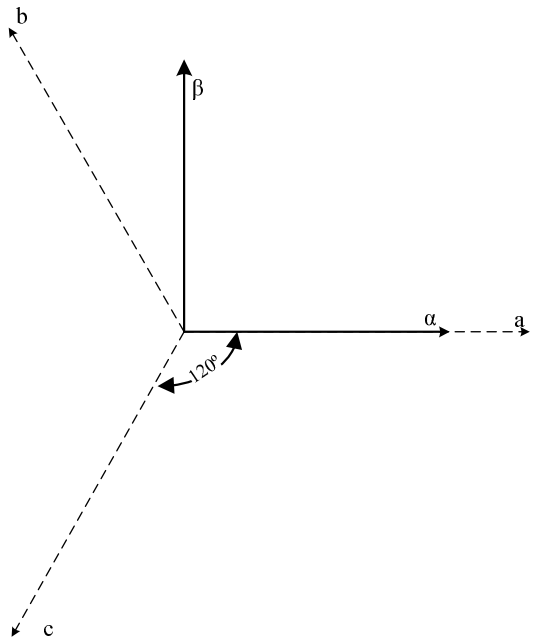

Figure 4.5 Graphical representation of the *abc*-plane and the *αβ*-plane

The following transformation matrix can be used to represent the *abc*-plane electrical variables of the system (voltage or current) in the $\alpha\beta\gamma$-plane. :

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_\gamma \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{4.4}$$

This matrix is derived by using simple trigonometric properties. Furthermore, because it is assumed that the system is balanced, the following property arises:

$$x_a + x_b + x_c = 0 \quad \rightarrow \quad x_\gamma = 0 \tag{4.5}$$

As long as this property holds, the tri-dimensional transformation matrix can be reduced to a bi-dimensional transformation matrix. The $\alpha\beta$ transformation matrix is defined as follows:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{4.6}$$

This matrix is referred to as the Clarke transformation matrix. The inverse of (4.6) is as follows:

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/\sqrt{2} & \sqrt{3}/2 \\ -1/\sqrt{2} & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{4.7}$$

If this matrix is applied to the instantaneous voltages of a three-phase system ($v_a(t)$, $v_b(t)$ and $v_c(t)$), it translates into an instantaneous space vector with components $v_\alpha(t)$ and $v_\beta(t)$. If the *abc*-voltages of the three-phase system are balanced, then sinusoidal signals are created as follows:

$$\begin{aligned} v_a(t) &= V_{peak} \sin(\omega t), \\ v_b(t) &= V_{peak} \sin(\omega t - 120°), \\ v_c(t) &= V_{peak} \sin(\omega t + 120°). \end{aligned} \tag{4.8}$$

The corresponding $\alpha\beta$-voltages are:

$$\begin{aligned} v_\alpha(t) &= 1.5 V_{peak} \sin(\omega t), \\ v_\beta(t) &= -1.5 V_{peak} \cos(\omega t) \end{aligned} \tag{4.9}$$

An example of the *αβ*-components such a translation is shown in Figure 4.6.

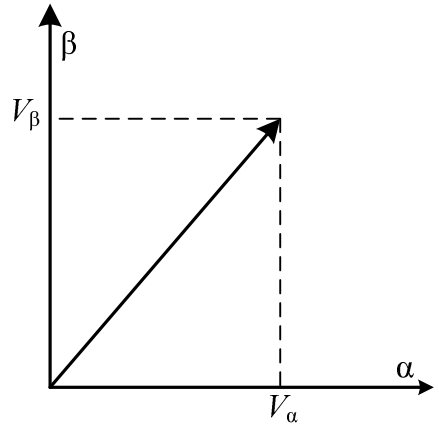

Figure 4.6 Instantaneous translation of *abc*-voltages to *αβ*-voltages

If this matrix is applied to the instantaneous values of a three-phase system for an entire cycle (eg. 20ms, 50 Hz), the resulting space vector will rotate through a full 360º. The graphical depiction of such a full cycle is shown in Figure 4.7.

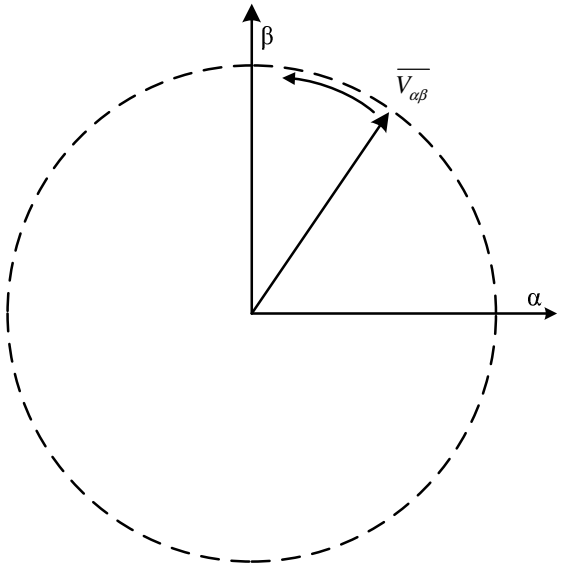

Figure 4.7 Graphical representation of instantaneous *abc* values in the *αβ*-plane

It can now be concluded that a balanced three-phase system can be represented in the *αβ*-plane by a rotating vector $\overline{V_{\alpha\beta}}$ with amplitude $\left|\overline{V_{\alpha\beta}}\right| = 1.5\left|\overline{V_{abc}}\right|$,where $\overline{V_{abc}}$ is a vector in the *abc*-plane. The vector in the *αβ*-plane rotates at an angular speed equal to ω.

4.3.2 SPACE VECTOR PULSE WIDTH MODULATION

Space vector pulse width modulation (SVPWM) makes it possible to simplify the control strategies used in a power electronic converter with an insulated neutral. To implement SVPWM, the instantaneous inverter output needs to be converted to the $\alpha\beta$-plane. This is done by using the Clarke transformation as explained in Section 4.3.1. The converter states are shown in Figure 4.8. Each of the inverter outputs is referred to node g. This implies that on each of the phases the output can either be equal to the bus voltage or zero. In each phase, the IGBTs are switched complimentarily. It can be concluded that the output voltage vector of the converter can only be one of eight possible values at a given instant. The idea behind the implementation of SVPWM is to output the desired voltage presented in the $\alpha\beta$-plane by superimposing different output vectors onto each other over a modulation period. The average voltage over the modulation period is equal to the desired output voltage.

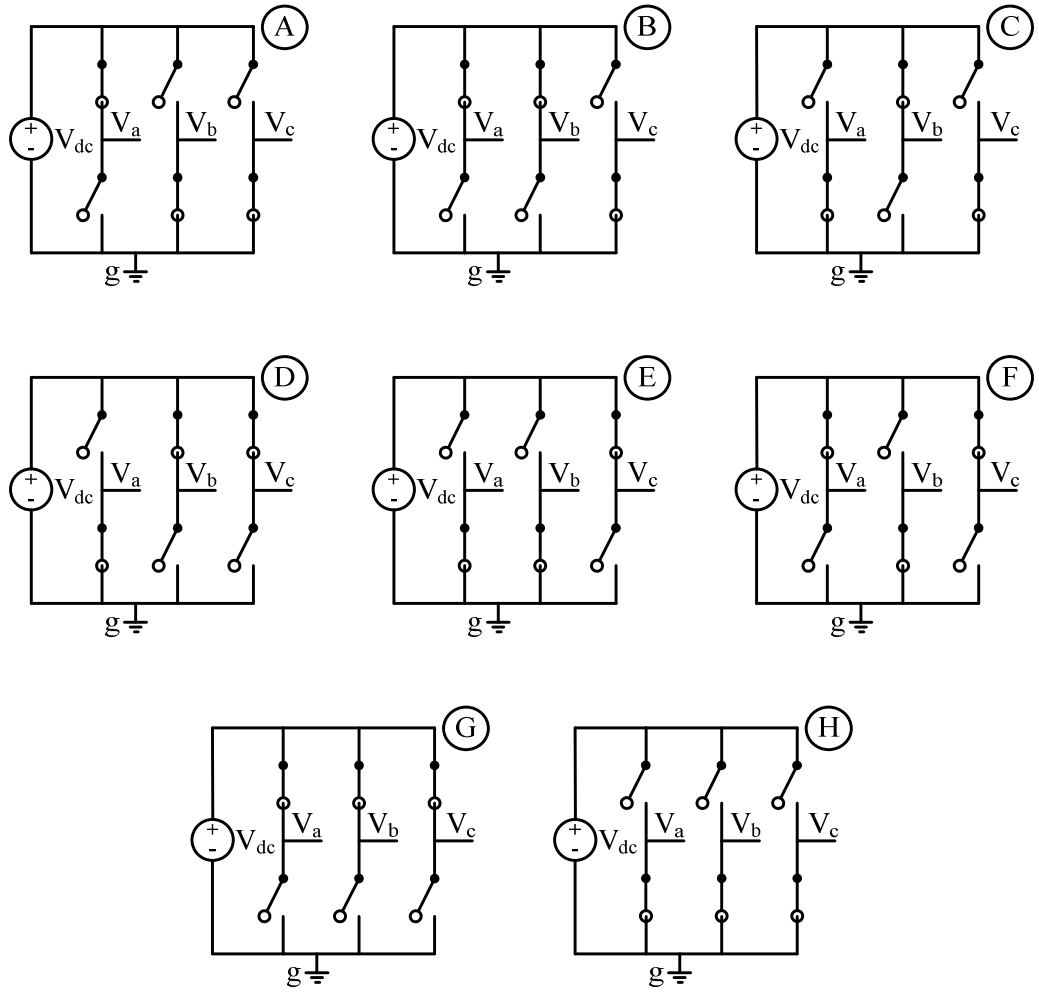

Figure 4.8 SVPWM switching states

In Table 4.1, the output voltage on each phase is shown for the different states.

Table 4.1 SVPWM state voltages

State	V_{ag}	V_{bg}	V_{cg}
A	V_{dc}	0	0
B	V_{dc}	V_{dc}	0
C	0	V_{dc}	0
D	0	V_{dc}	V_{dc}
E	0	0	V_{dc}
F	V_{dc}	0	V_{dc}
G	V_{dc}	V_{dc}	V_{dc}
H	0	0	0

The different vectors corresponding to each switching state are shown in Figure 4.9.

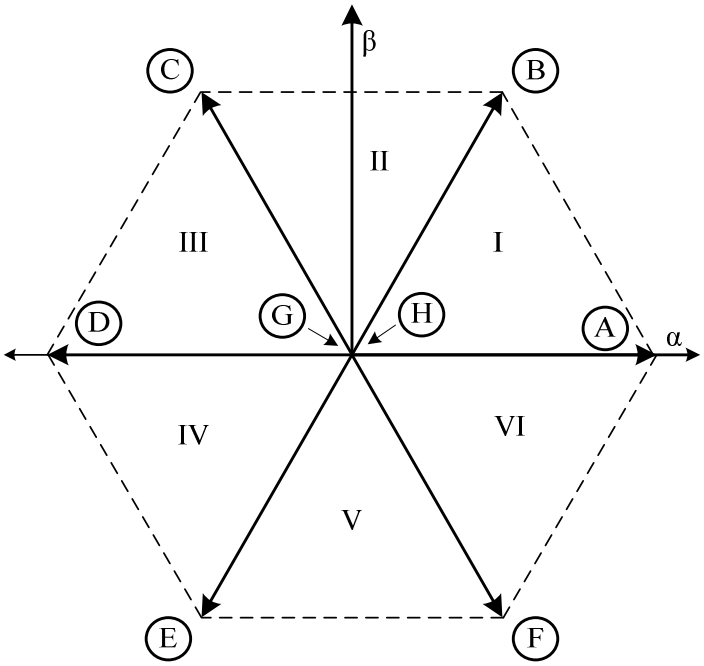

Figure 4.9 Converter output vectors and sectors

There are six vectors of the same length and two of zero length. It can be seen that adjacent vectors only differ by the switching of one phase arm at a time. The lengths of the six finite vectors are:

$$\left|\overline{V_A}\right| = \left|\overline{V_B}\right| = \left|\overline{V_C}\right| = \left|\overline{V_D}\right| = \left|\overline{V_E}\right| = \left|\overline{V_F}\right| = V_{dc} \tag{4.10}$$

Also indicated in Figure 4.9 are the six sectors in which the desired output vector can be located. To determine the optimal switching pattern it is firstly necessary to determine in which sector the output voltage is located. This is done by using a sequence of *if*-statements and some trigonometry. After the sector has been determined, another sequence of trigonometry calculations is done to calculate finally the required duty cycle of each phase that will result in the desired output voltage.

To minimise the amount of switching during a modulation period, an optimal switching period is needed. This can be achieved by noting that in each sector the desired voltage can be obtained by only switching the two adjacent vector to that sector and to two zero vectors. Further optimization can be obtained by switching these vectors in the correct sequence. The detailed discussion of this falls outside the scope of this thesis, but is available in the literature.

4.3.3 PREDICTIVE CURRENT CONTROL ALGORITHM

A feedback loop is implemented to regulate and control the current flow through the inductors. This makes it possible to set a reference signal that the current should follow in terms of amplitude and frequency. In Figure 4.10, the control block diagram of the current controller is shown.

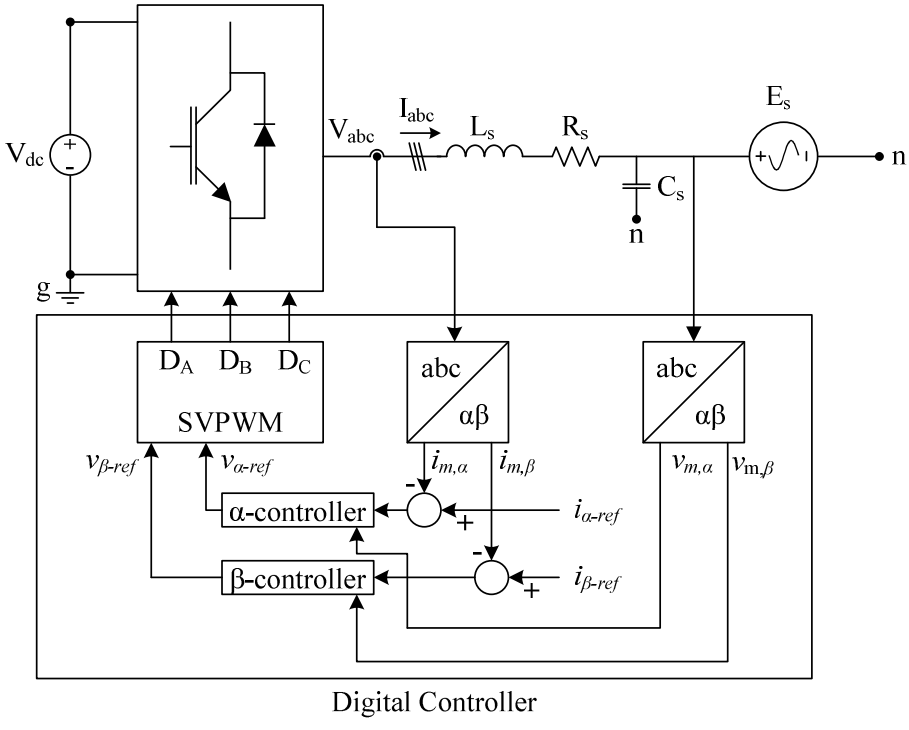

Figure 4.10 Overview of digital SVPWM controller

By assuming that the load is balanced and symmetrical, it is possible to design the α-controller and the β-controller in the same way as designing a single-phase current controller. This can be verified by defining the continuous time state space model of the converter. The phase voltages of the converter with respect to ground and neutral are as follows (also refer to Figure 4.8):

$$\begin{aligned} v_{an} &= v_{ag} - v_{ng} \\ v_{bn} &= v_{bg} - v_{ng} \\ v_{cn} &= v_{cg} - v_{ng} \end{aligned} \tag{4.11}$$

Because the system is balanced, the following holds:

$$v_{an} + v_{bn} + v_{cn} = 0 \tag{4.12}$$

v_{ng} can now be calculated as:

$$v_{ng} = \frac{v_{ag} + v_{bg} + v_{cg}}{3} \tag{4.13}$$

By substituting (4.13) into (4.11), the phase voltage can be represented in matrix form as follows:

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \tag{4.14}$$

The continuous time state space model can now be expressed as:

$$\begin{aligned} \frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} &= -\frac{R_s}{L_s}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{3L_s}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \\ &\quad -\frac{1}{L_s}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} e_{san} \\ e_{sbn} \\ e_{scn} \end{bmatrix} \end{aligned} \tag{4.15}$$

By using the Clarke transformation matrix (4.6), and the inverse of the Clarke transformation matrix (4.7), the converter can be expressed in term of its $\alpha\beta$-components as follows:

$$\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{R_s}{L_s}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$
$$+\frac{1}{3L_s}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_{\alpha g} \\ v_{\beta g} \end{bmatrix} \qquad (4.16)$$
$$-\frac{1}{L_s}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} e_{\alpha n} \\ e_{\beta n} \end{bmatrix}$$

This matrix can now be simplified to the following:

$$\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = -\frac{R_s}{L_s}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} v_{\alpha g} \\ v_{\beta g} \end{bmatrix} - \frac{1}{L_s}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} e_{\alpha n} \\ e_{\beta n} \end{bmatrix} \qquad (4.17)$$

The phase interference caused by the contribution of V_{ng} is cancelled out by the application of the Clarke transformation matrix. The system is now decoupled in the $\alpha\beta$-plane, which means that it can be viewed as two entirely independent systems.

The purpose of predictive current control is to calculate the average converter output voltage that will result in an average inductor current equal to the reference signal by the end of the next modulation period. An average circuit model of the converter is shown in Figure 4.11. The average output voltage of the converter is V_c and the average output inductor current is I_o.

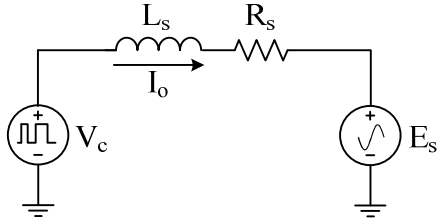

Figure 4.11 Average circuit model of converter

In this thesis, double-edged pulse width modulation (DEPWM) is implemented. This implies that a triangular waveform is used as the carrier signal. The modulation signal is compared to the carrier signal to determine the switching periods of the IGBTs. In this case, the carrier signal is implemented digitally by using a counter, as shown in Figure 4.12. A digital value is set to represent the duty cycle. While the counter is less than the

set value, the gate signal to the top IGBT is kept low, and the gate signal to the bottom IGBT is kept high. When the counter is more than the set value, the gating signals are toggled. By using DEPWM and sampling in the middle of the modulation period, the average value of the inductor current can be sampled more accurately.

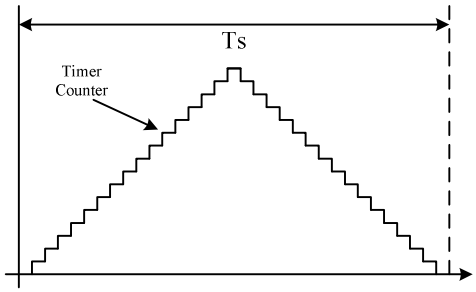

Figure 4.12 DEPWM counter with modulation period shown

In Figure 4.13, an example is shown of the converter output voltage and inductor current over three modulation periods. This example is used to explain the approach to predictive current control. In Figure 4.13 (a), it is assumed that the period at which the counter changes is small enough to represent it as a continuous curve. The reference current, the inductor current and the current error are shown in Figure 4.13. The point at which the inductor current is sampled is also indicated.

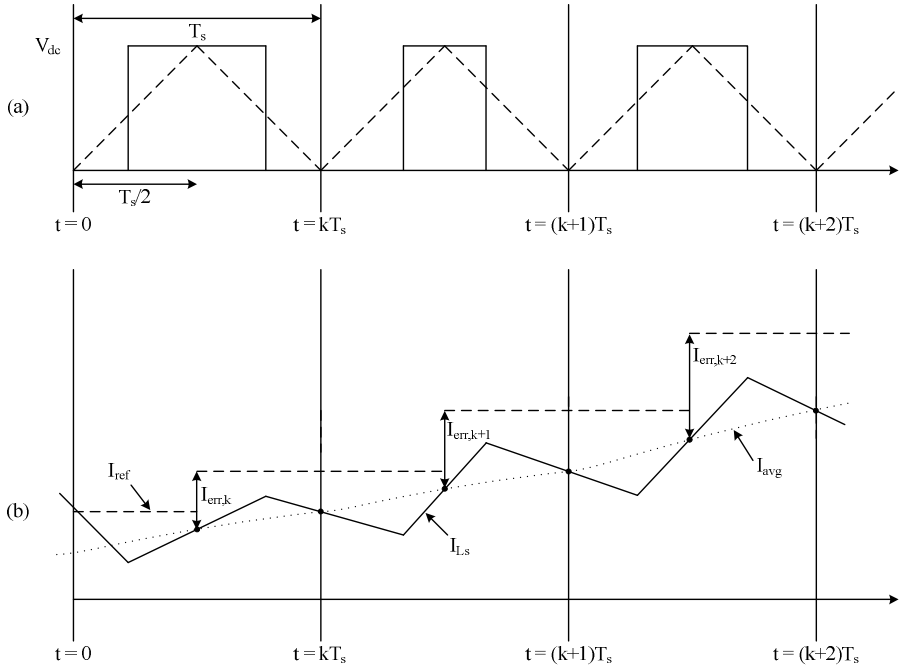

Figure 4.13 (a) Inverter output voltage and triangle reference (b) Inductor current and reference current with current error

During the modulation period from $t=0$ to $t=kT_s$ at $t=T_s/2$, the inductor current is sampled. In the period from $t=T_s/2$ until $t=kT_s$, the computations are done to determine which output voltage during the next modulation period ($t=kT_s$ to $t=(k+1)T_s$) will result in an average output inductor current equal to the reference current. Because the calculations done in the period $t=0$ to $t=kT_s$ are only set for the next modulation period, there is a phase error between the average inductor current and the reference. This can be minimized by advancing the reference space vector in the $\alpha\beta$-plane by the appropriate time. The phase shift will depend on the period of the carrier signal relative to the modulation signal. It is very important to note that the calculations must be completed before the end of the current modulation period. Failing to do so will result in an unwanted increase in the error between the reference and the measured value as well as an increase in the phase difference between the reference and the measured value.

It is now possible to derive the control algorithm based on the previous discussion and using Figure 4.11. The differential equation based on Figure 4.11 is as follows:

$$v_c = L_s \frac{di}{dt} + i_o R_s + e_s \tag{4.18}$$

The equivalent discrete time representation of this dynamic system is:

$$v_c(k+1) = L_s \frac{\Delta i(k)}{T_s} + i_o(k) R_s + e_s(k) \tag{4.19}$$

To further simplify the equation it is assumed that $R_s = 0$. The control algorithm in terms of the error between the reference value and the measured value is:

$$v_c(k+1) = \frac{L_s}{T_s}(i_{ref}(k) - i_m(k)) + e_s(k) \tag{4.20}$$

The controller derived above can now be implemented on both the α-phase and the β-phase to calculate the reference voltage needed by the SVPWM to generate the appropriate duty cycles for each phase. These controllers are implemented as follows:

$$\begin{aligned} v_{ref,\alpha}(k+1) &= \frac{L_s}{T_s}\left[i_{ref,\alpha} - i_{m,\alpha} \right] + v_{m,\alpha} \\ v_{ref,\beta}(k+1) &= \frac{L_s}{T_s}\left[i_{ref,\beta} - i_{m,\beta} \right] + v_{m,\beta} \end{aligned} \tag{4.21}$$

By manipulating the reference signals accordingly, the anti-islanding methods are implemented.

4.3.4 DC BUS REGULATION ALGORITHM

The DC bus is controlled by using two feedback controllers. In Figure 4.14 a block diagram representation of this double feedback loop is shown.

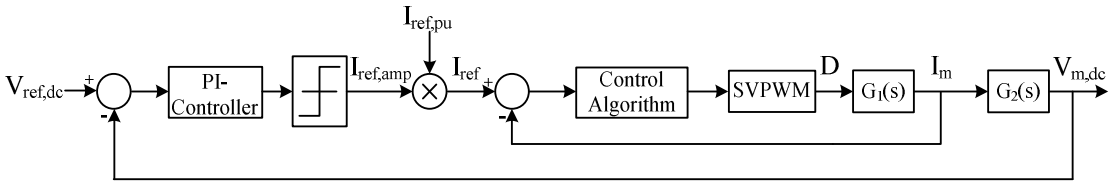

Figure 4.14 Block diagram of DC regulation controller

The inner feedback loop uses the current controller discussed in the previous section. The outer feedback loop controls the amplitude and phase of the reference current. By shifting the phase of the current relative to the grid voltage, power can either be drawn from the grid or delivered to the grid. This is done by setting the reference current phase relative to the voltage to either 0° or 180°. The equation to calculate the power flow direction is:

$$P = VI\cos\theta \tag{4.22}$$

where θ is the phase angle between the current and the voltage. A reference signal with amplitude of 1 is multiplied by the amplitude and sign calculated by the PI controller.

It is assumed that the inner control loop works correctly and that the measured current follows the reference correctly. Based on this assumption, it is possible to simplify the control block diagram as shown in Figure 4.15.

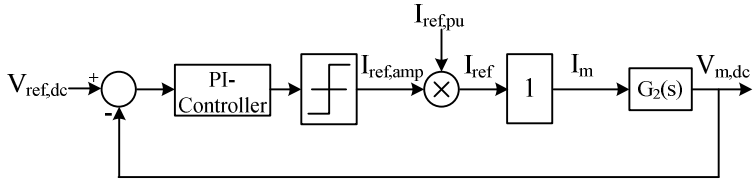

Figure 4.15 Simplified control block diagram of DC regulation controller with current limits

The current controller is now replaced by a gain of 1. To prevent the occurrence of a reference amplitude that is outside the operational capabilities of the converter, the amplitude is limited. This limit is important; if it has been set too low, the converter

would not be able to transfer power effectively from the DC link to the grid. The maximum limits are also very important when the capacitors in the DC link are initially charged. If these are set too low, the initial charge period will be too long, whereas if they are set too high, the DC bus can overcharge which can damage the capacitors or cause the converter protection to trip.

The current limits are removed when designing the PI controller, as these limits are specific to the converter used. This simplifies the control block diagram even further, as shown in Figure 4.16.

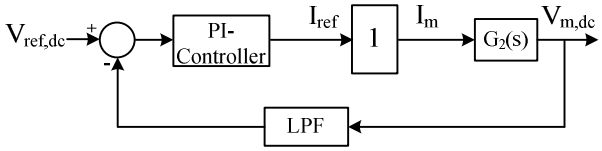

Figure 4.16 Simplified control block diagram of DC regulation controller with low-pass filter on measurement

A low-pass filter is added to the measurement of the DC voltage. This is to filter out noise caused by the switching in the actual system.

The closed loop transfer function of the system is as follows [20]:

$$\frac{V_m(s)}{V_{ref}(s)} = \frac{C(s)G_2(s)}{1+H(s)C(s)G_2(s)} \tag{4.23}$$

where *C(s)* is the PI controller to be designed, *H(s)* the low-pass filter and $G_2(s)$ is the DC link. The transfer function of the DC link is:

$$G_2(s) = \frac{1}{sC} \tag{4.24}$$

and the transfer function of the-low pass filter is:

$$H(s) = \frac{\omega_{filt}}{\omega_{filt}+s} \tag{4.25}$$

The cut-off frequency of the low-pass filter is calculated as follows:

$$\omega_{filt} = \frac{1}{RC} \tag{4.26}$$

A cut-off frequency of 188.5 rad/s is selected for the low-pass filter. The capacitance of the DC link is 4700 μF.

The bandwidth of the PI controller is selected as one-tenth of the fundamental grid frequency, which are ω_c = 31.4 rad/s. The sampling time ω_s, is 0.0001 μs, this makes $\omega_s > 20\omega_c$. This makes it possible to design the controller directly in the continuous time space and then afterwards to convert it into the discrete time space [20]. This process is referred to as *design by emulation*.

The system is designed to be optimally damped, thus $\zeta = 0.707106$. The undamped natural frequency is selected as $\omega_n = 31.4$ rad/s. This places the desired closed loop poles of the systems at:

$$p_{1,2} = 22.1998 \pm j22.1998 \tag{4.27}$$

In Figure 4.17, the open loop root locus of the system with no compensation is shown. To place the closed loop poles at the desired location, the root locus needs to be reshaped in such a way that the open loop root locus passes through the location of the desired closed loop poles. By adding the PI compensator to the system, an extra pole and zero are added to the root locus plot.

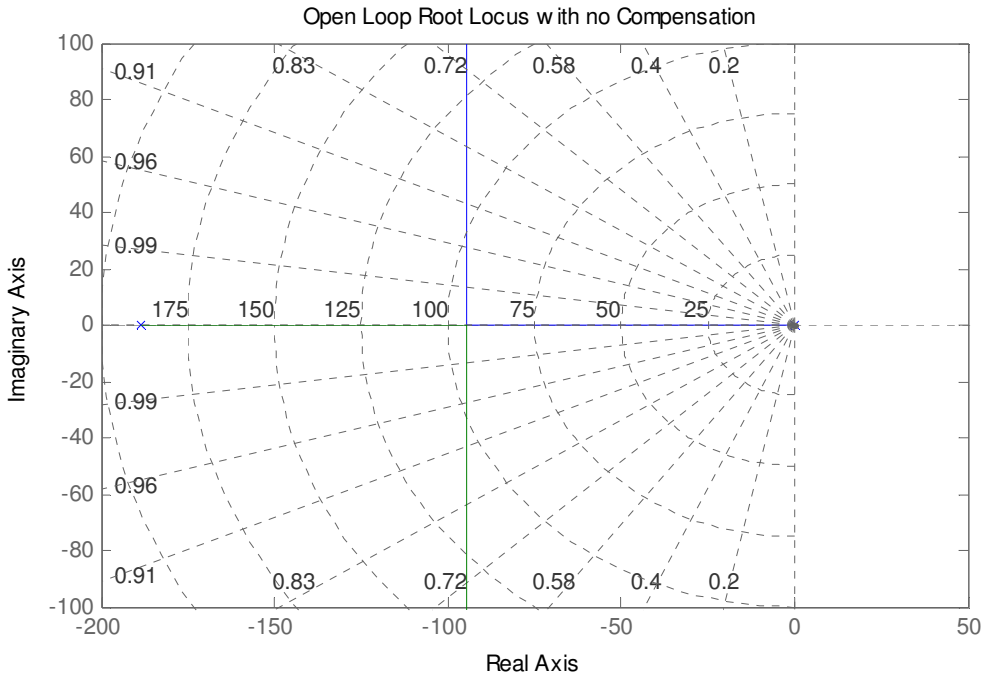

Figure 4.17 Open loop root locus with no compensation

The PI compensator adds a pole at the origin and zero is placed at $z_{comp} = -19.4$. This shapes the open loop root locus as shown in Figure 4.18. The closed loop poles are indicated.

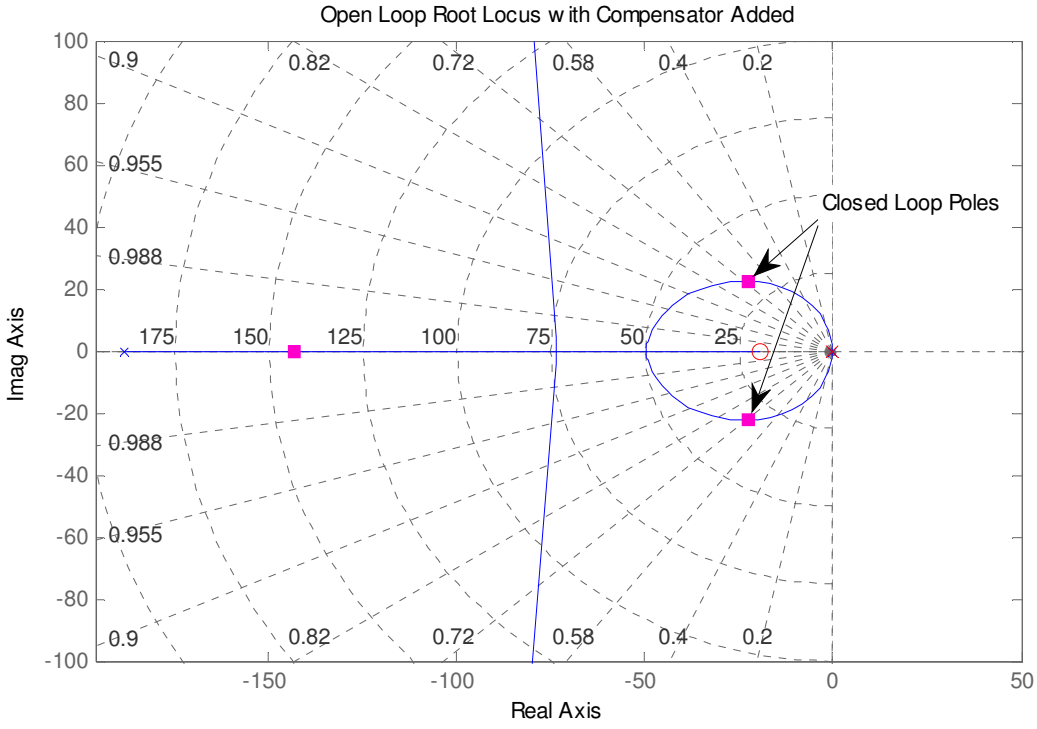

Figure 4.18 Open loop root locus with compensator added

A Bode plot of the open loop compensated system is shown in Figure 4.19. The phase margin is sufficient to ensure adequate stability and good damping of the system.

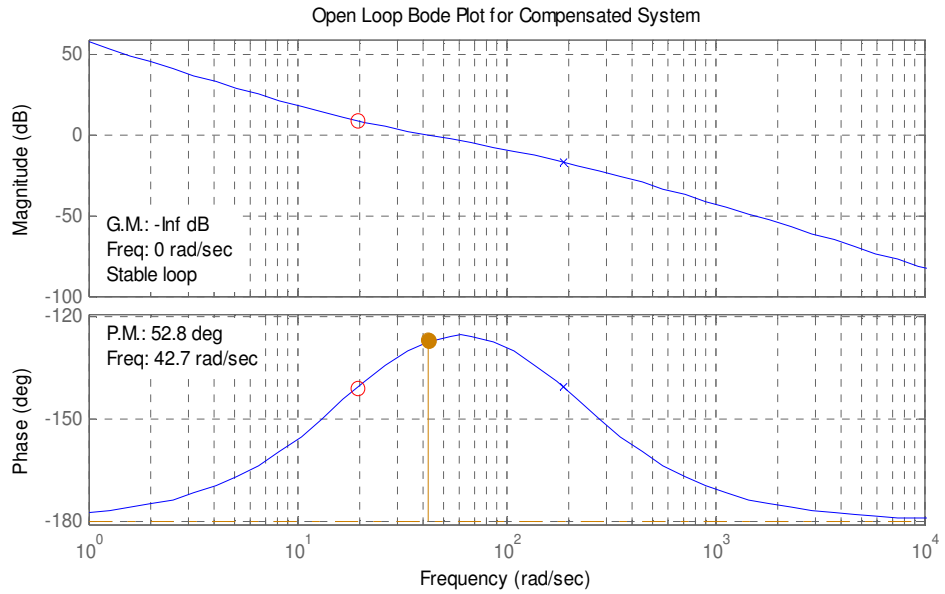

Figure 4.19 Bode plot of open loop system with compensator added

The transfer function of the PI controller is:

$$C(s) = \frac{3.6375}{s} + 0.1855125 \tag{4.28}$$

From this the gains of the controller are K_p = 0.1855125 and K_i = 3.6375. Using (4.23), the closed loop transfer function of the system is calculated. This is:

$$G_{CL}(s) = \frac{39.8443s^2(s+19.42)(s+188.5)}{s^2(s+143.2)(s^2+45.35s+1019)} \tag{4.29}$$

A Bode plot of the closed loop system (see Figure 4.20) confirms that the system is stable.

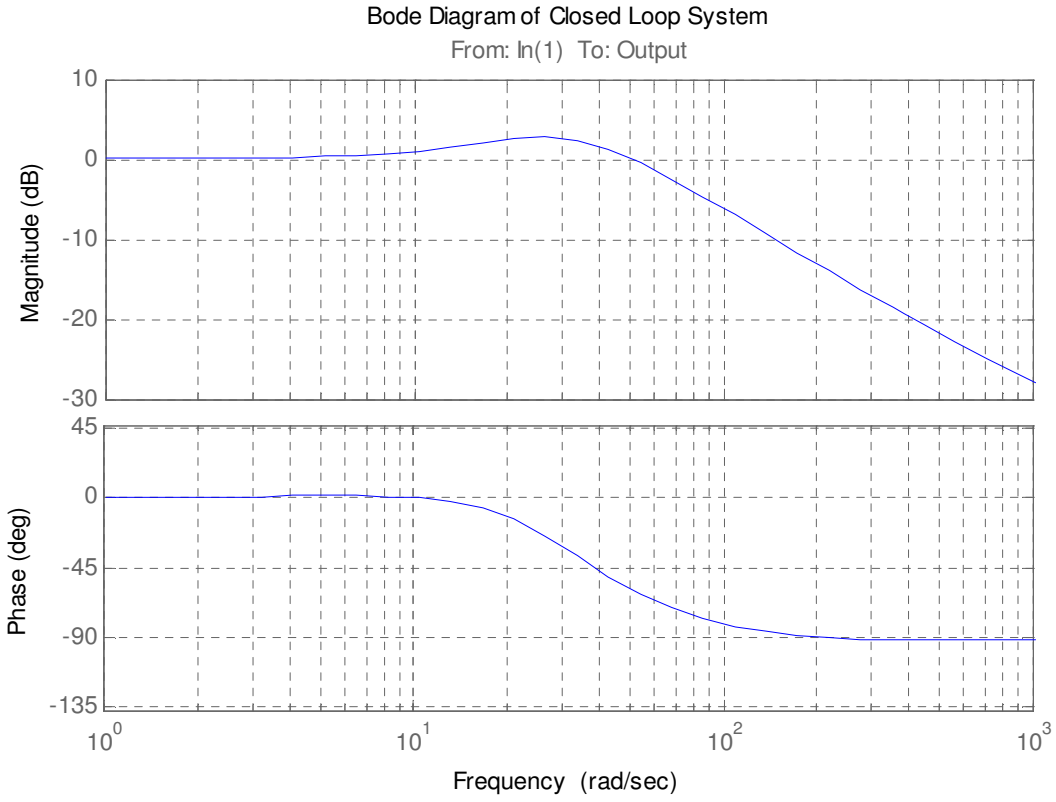

Figure 4.20 Bode diagram of closed loop system of DC regulator

To implement the controller it needs to be transformed into its equivalent discrete-time domain model. This is done by using an integration approximation method. The following forward rectangular relationship is used for the conversion [20]:

$$s \to \frac{z-1}{T_s} \tag{4.30}$$

where T_s is the sampling period, which in this case is 100 μs.

In Figure 4.21, the block diagram model of the PI controller is shown.

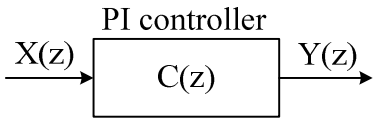

Figure 4.21 Block diagram of the PI controller

The discrete transfer function of the PI controller in terms of its input and output is:

$$C(z)=\frac{Y(z)}{X(z)}=\frac{0.1855(z-0.998)}{z-1} \tag{4.31}$$

To implement the controller digitally it needs to be in difference equation form. This can be done using the following two properties, which converts the discrete equation into a difference equation [20]:

$$\begin{aligned} zX(z)&=x(k+1),\\ X(z)&=x(k) \end{aligned} \tag{4.32}$$

The PI controller in difference form is

$$y(k)=0.1855\left[x(k)-0.998x(k-1)\right]+y(k-1) \tag{4.33}$$

This controller is implemented digitally to regulate the DC bus and to control the power flow from the generator to the grid.

4.4 DEAD TIME COMPENSATION

4.4.1 INTRODUCTION

Dead time is required within power electronic inverters to prevent both switches conducting at the same time. In order to satisfy this condition, the dead time needs to be longer than the non-zero switching transition times of the power devices. Dead time has a detrimental effect on the output voltage, however, which leads to several undesirable effects, such as phase current distortion [21], torque pulsation [21], [22], harmonic distortion [22], [23], [24], and a fundamental output voltage drop [23]. A secondary effect is poor performance of the control algorithms [21]. Even though the period of the dead time is usually small compared to the switching period (typically 1% to 3%), the average error resulting from the current dependency is very non-linear.

Several strategies have been proposed in the literature to compensate for the effects of

dead time. Compensation methods based on an average model of an error (voltage or phase) resulting from the dead time are proposed in [25], [26], [27]. In these methods, a fixed value is added to or subtracted from the command voltage or duty cycle depending on the sign of the current reference. The pulse based compensation method proposed in [28] does a pulse-by-pulse correction of the dead time error. As compensation is done twice per switching period, it yields very good results, but this might not be a viable option in all applications. A self-tuning method is proposed in [24]. In this method, the output current is used as a feedback parameter to adjust the compensation parameters continuously. It primarily assesses the harmonic distortion (5^{th} and 7^{th}) of the current. The information gathered from these components is then used to tune the algorithm. Although the above-mentioned methods all provide some form of compensation, the characterization of the dead time in the zero-crossing region remains vague and relies on self-tuning measurements as proposed in [24].

4.4.2 ANALYSIS OF THE DEAD TIME

This section describes how the addition of dead time alters the output voltage of the inverter. Figure 4.22 shows the topology and circuit parameters used. The inverter is configured in a half-bridge topology with insulated gate bipolar transistors (IGBTs) chosen as switching devices. The anti-parallel diodes serve as freewheeling paths for the inductor current.

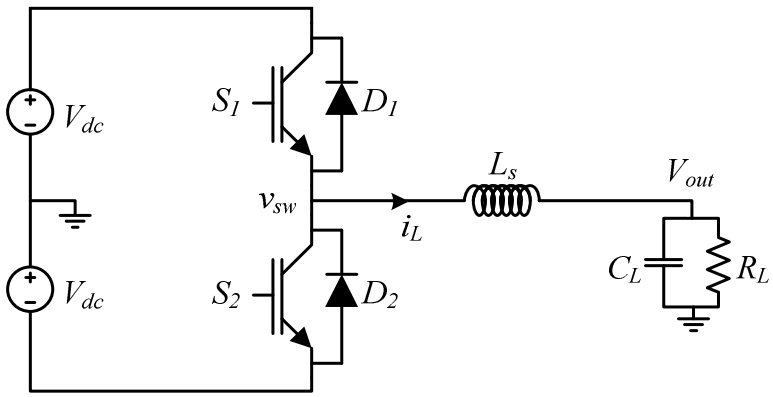

Figure 4.22 Definition of the inverter topology and circuit parameters

An example of a switched current waveform is shown in Figure 4.23 with the envelope of the current as indicated. By using the boundaries of the envelope, the current can be

divided into three distinct regions. In region *A* the upper and lower boundaries are both positive, i.e. the current does not change polarity in this region.

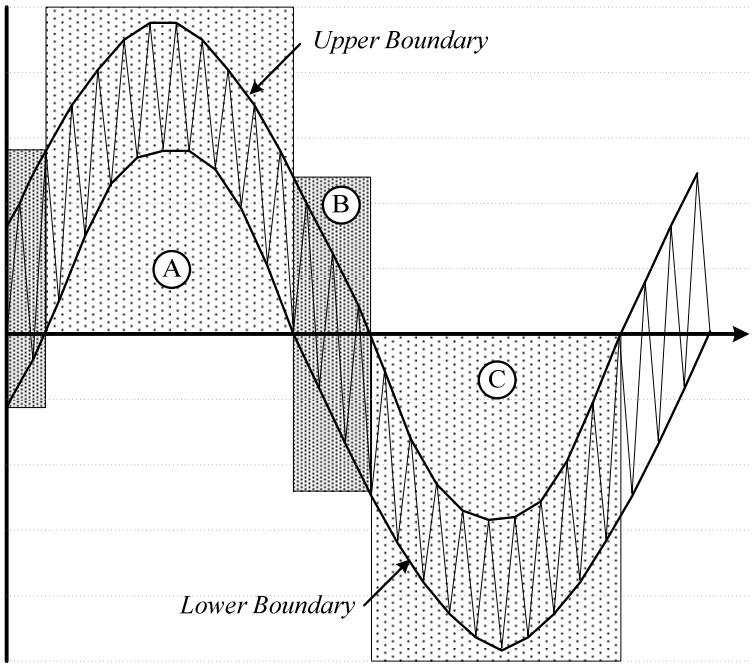

Figure 4.23 Definition of the various inductor current regions

In region *B,* the upper boundary is positive, while the lower boundary is negative, and as a result, the current changes polarity in this region. Similar to region *A* the polarity of the current remains unchanged in region *C* (both boundaries are negative). Since intervals *A* and *C* are similar, only regions *A* and *B* will be considered.

a) Distinctly Positive or Negative Current (A and C)

This section contains a brief overview of the well-known effect of dead time within regions *A* and *C*. The switching waveforms for the inductor current falling within the above-mentioned intervals are shown in Figure 4.24. Waveforms S_1* and S_2* are the ideal gating signals, i.e. no dead time is included, while S_1 and S_2 are the actual gating signals with the addition of a non-zero dead time t_d. Figure 4.24 (e) illustrates the switched output voltage (v_{sw}) of the inverter when the current is in region *A*, while Figure 4.24 (f) shows the switched output voltage when the current is in region *C*. If the current through the inductor falls within region *A* and the gating signal S_1 is high, the voltage at the output of the inverter is equal to V_{dc}. After the gating signal S_1 has been set low, the positive current continues to flow through the freewheeling diode D_2. This forces the

output voltage to $-V_{dc}$. The gating signal S_2 is set high after the dead time has elapsed and the IGBT takes over the current from D_2. This result is the same switched output voltage for an immediate transition of S_2 from low to high, i.e. the ideal case is reproduced.

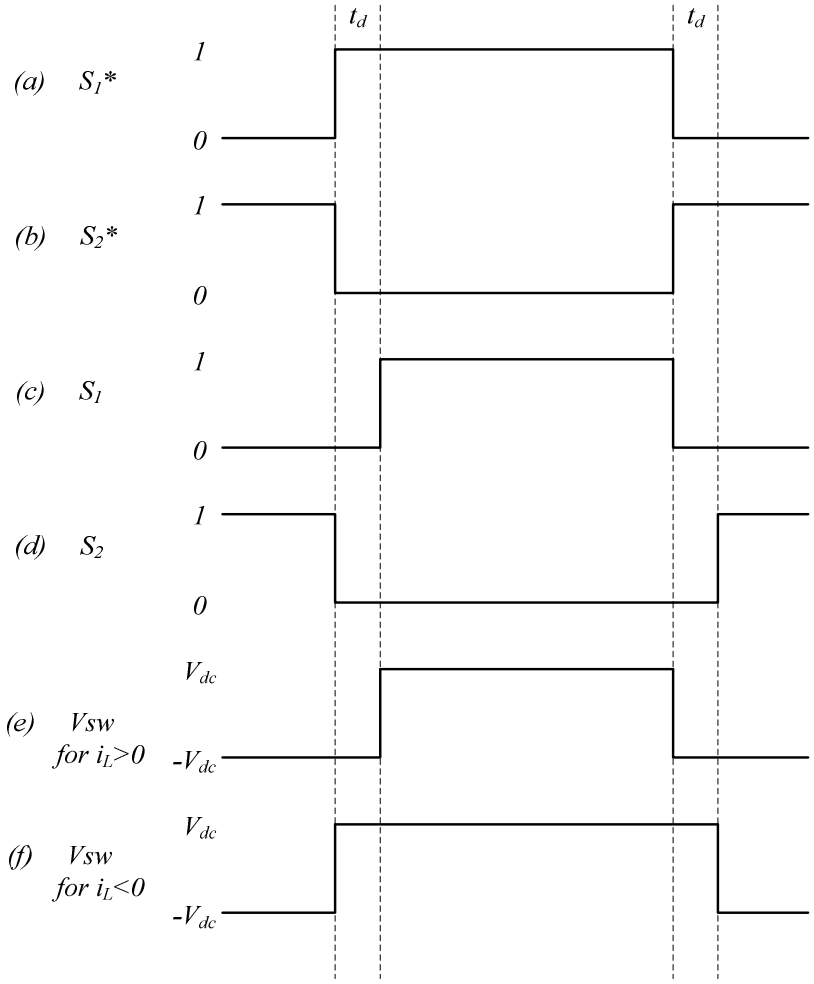

Figure 4.24 Switching waveforms within regions *A* and *C*

Still for an inductor current within region *A*, consider the condition when the gating signal S_1 is low and S_2 is high. The voltage at the output of the inverter thus equals $-V_{dc}$. When the gating signal S_2 is set to low, the freewheeling diode D_2 is switched on and the output voltage remains at $-V_{dc}$ instead of V_{dc}. This condition results in an error (loss of voltage). After the dead time has elapsed and the gate signal S_1 has been set high, the output voltage switches to V_{dc}. Using a similar approach it can be shown that the commutation sequence during the dead time within region *C* results in a voltage gain being introduced.

b) Undefined Current Region (B)

This region (denoted by *B* in Figure 4.23) is located around the zero-crossing of the inductor current. The duration of this interval depends on the switching frequency, filter inductance, DC bus voltage, and modulation index, as well as on the load resistance. In this region the current changes polarity during the dead time interval, which in turn has an impact on the effective voltage error caused by the dead time. Since only the diodes are conducting during this period, they play an important role in the response of the system. Figure 4.25 shows the reverse recovery current waveform of a power diode [29]. When the current changes polarity, the diode conducts in the opposite direction for a short time until the excess carriers are swept out, after which it switches off completely [29]. This period (t_{rr}) is referred to as the reverse recovery period of the diode. $I_{rr,max}$ is the maximum reverse recovery current and Q_{rr} the reverse recovery charge.

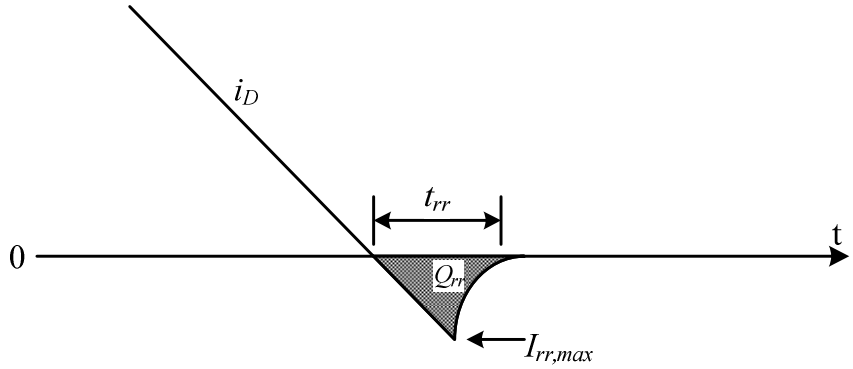

Figure 4.25 Power diode reverse recovery response [29]

Consider a change in current polarity from positive to negative during the dead time interval as shown in Figure 4.26. The conducting diode (D_2) reverse recovers as the current changes polarity, after which it switches off once the excess charge has been removed. Once the reverse recovery of D_2 is complete, D_1 is forced on. The output voltage of the inverter switches between V_{dc} and $-V_{dc}$ as diodes D_1 and D_2 conduct and reverse recover. This leads to the average output voltage of the inverter being different from regions *A* and *C*.

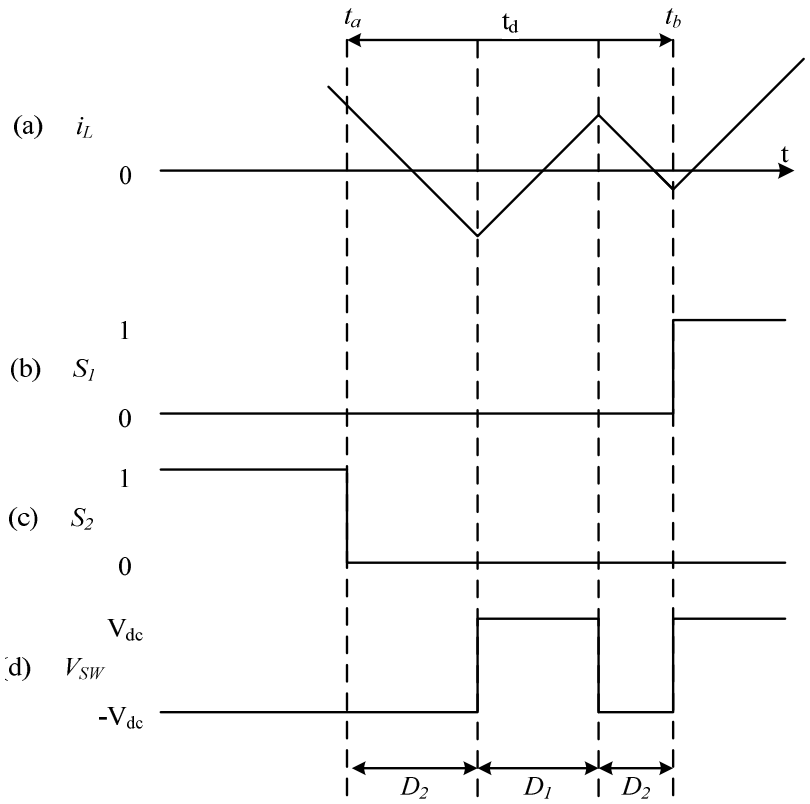

Figure 4.26 Switching waveforms for region *B*

The reverse recovery time of the diode plays a major role in the response during the dead time. Figure 4.27 shows various illustrative waveforms. The switched output voltage of the inverter will remain the same if the reverse recovery time of the diode is longer than the dead time. Such an example is shown in Figure 4.27 (a) and Figure 4.27 (b). Initially, when the current enters region *B*, the change in polarity occurs close to t_b. In this case, only one diode goes into reverse recovery. In Figure 4.27 (c) and Figure 4.27 (d), a polarity change close to t_b is shown. The output voltage changes state only once, but the average voltage over the dead time interval is less than the case where no change in voltage occurs. The initial change in current polarity moves towards t_a as the average current approaches zero. In Figure 4.27 (e) and Figure 4.27 (f), the current changes polarity just after time t_a. This forces the diodes into reverse recovery more than once. As a result the output voltage of the inverter switches between V_{dc} and $-V_{dc}$ numerous times, which results in the average voltage being very close to zero. The latter two examples result in a much smaller error than in regions *A* and *C*.

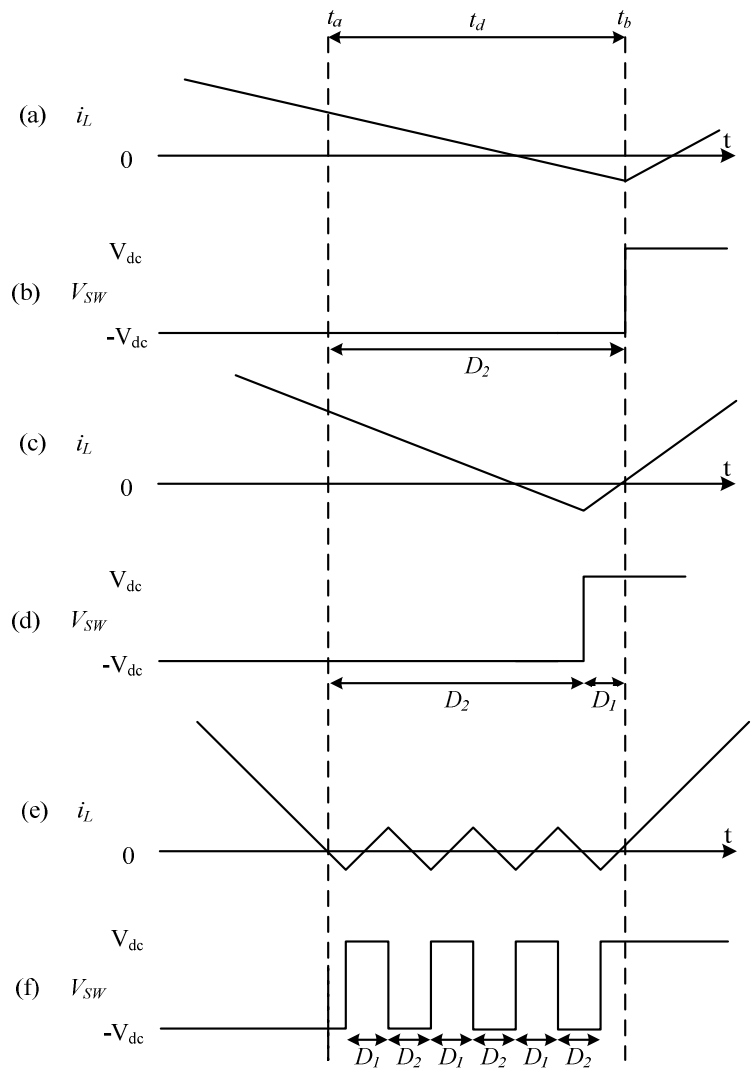

Figure 4.27 Current waveforms in region *B*

4.4.3 SIMULATIONS

In the previous section, all components were assumed ideal with no losses. This section explains the method developed and used to acquire results that are more realistic.

a) Methodology

As mentioned before, the diodes go into reverse recovery when the current changes polarity during the dead time. The following two equations can be used to estimate the reverse recovery time and current [29]:

$$t_{rr} \approx 2.8\times10^{-6} BV_{BD} \sqrt{\frac{I_F}{di_R / dt}} \tag{4.34}$$

$$I_{rr} \approx 2.8\times10^{-6} BV_{BD} \sqrt{I_F \, di_R / dt} \tag{4.35}$$

Where BV_{BD} is the breakdown voltage and I_F the inductor current. (4.34) and (4.35) can now be adapted under the assumption that the duty cycle is 50% around the zero-crossing average current, which in turn results in the maximum current ripple for a purely resistive load. The maximum current ripple for a half-bridge topology is given by [30]:

$$\Delta i_{L\max} = \frac{V_d}{8Lf_s} \tag{4.36}$$

The current waveform during the dead time is calculated using a series of initial and end conditions, established from (4.34) and (4.35). Consider the waveforms shown in Figure 4.28. Variable t_c is the time it takes for the current to change polarity once the dead time has been initiated. The equivalent switched output voltage is shown in Figure 4.28 (b), where W_n is the width of each pulse during t_d.

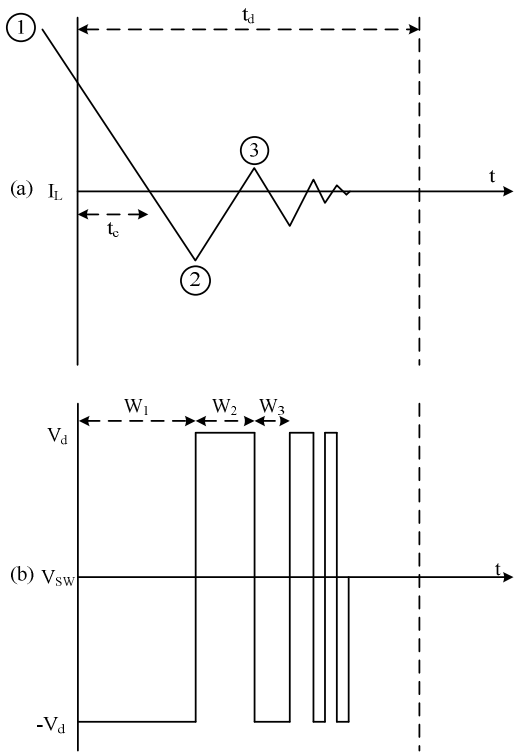

Figure 4.28 Inductor current and switched output voltage

The initial conditions at ① are calculated using (4.36). By substituting the result obtained into (4.34) and (4.35), the reverse recovery time and current at ② can be determined. These values, which are calculated next, serve as initial conditions at ③. This process is repeated until the end of the dead time interval from where the average voltage during this interval can be determined.

b) Results

In this section, the analytical equations of the previous section are implemented. The parameters used are shown in Table 4.2.

Table 4.2 Dead Time Simulation Parameters

Parameter	Value
Switching Frequency (f_s)	5000 Hz
Inductance (L_s)	666.67 μH
Bus Voltage ($2V_{dc}$)	30 V
Bus Capacitance	2200 μF
Load Resistance (R_L)	1 Ω
Load Capacitance (C_L)	633 μF
Diode Voltage (BV_{BD})	1000 V

The dead time in Figure 4.29 Dead time inductor current of t_d = 50 μs is set to 50 μs and t_c is 5 μs. The initial reverse current is large, but decreases as the energy in the inductor is dissipated in the load.

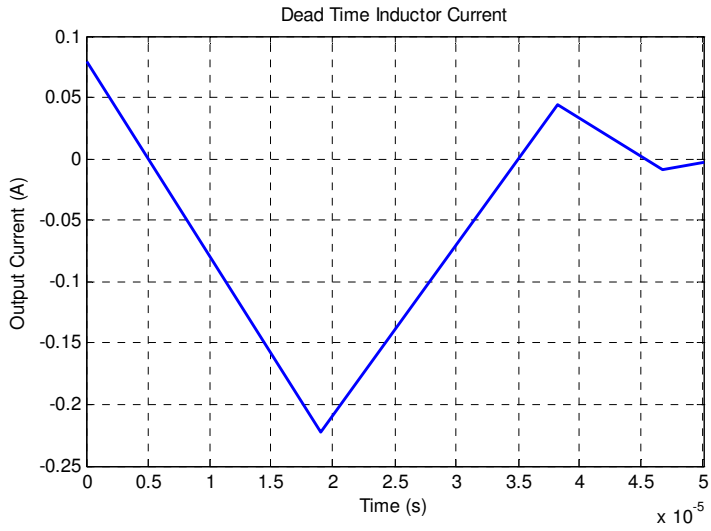

Figure 4.29 Dead time inductor current of t_d = 50 μs

A very elaborate case is shown in Figure 4.30. The dead time is 150 μs and t_c is 15 μs. Although this is an unlikely scenario, it shows how the energy in the inductor decreases. Upon depletion, there is not enough current to turn the diodes on, and the output voltage of the inverter remains at zero.

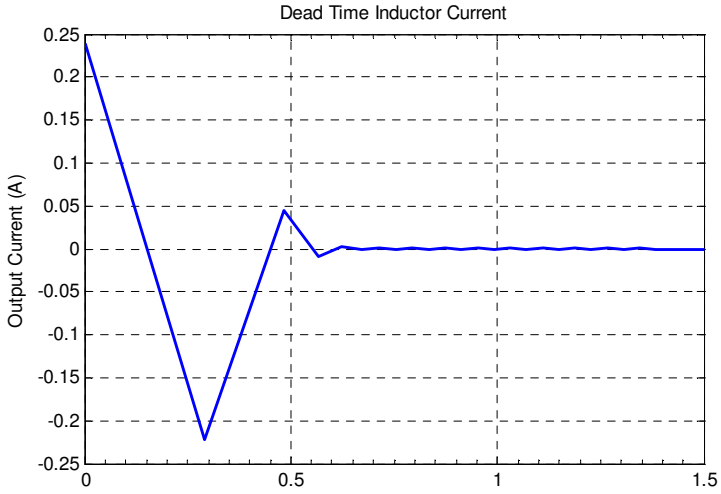

Figure 4.30 Dead time inductor current of t_d = 150 μs

Figure 4.31 illustrates a more realistic scenario where the dead time is 20 μs and t_c is 0.5 μs. In this case, only D_2 goes into reverse recovery and the output voltage would have switched to V_{dc}, altering the average output voltage.

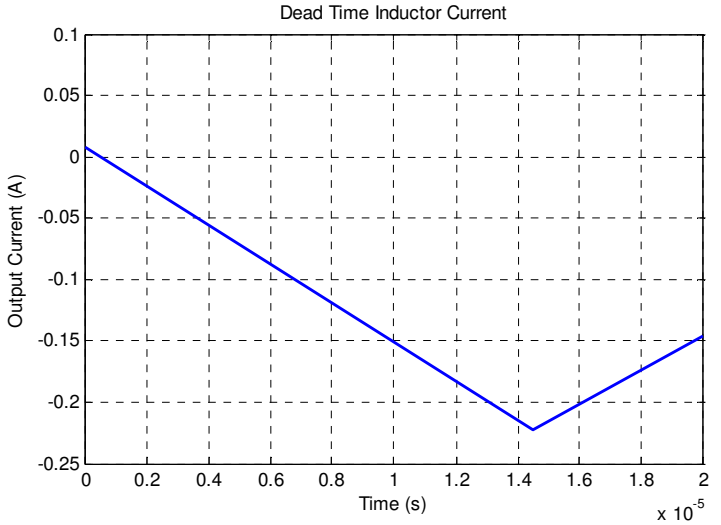

Figure 4.31 Dead time inductor current of t_d = 20 μs

The pulse width of the output voltage can be determined from the turn-on times of the diodes. To calculate the average output voltage for an initial polarity change from positive to negative, the following equation is used:

$$V_{avg} = \frac{V_d \cdot \sum_{n=2,4,6,\ldots} W_n - V_d \cdot \sum_{m=1,3,5,\ldots} W_m}{t_d} \tag{4.37}$$

Note that a similar relation to (4.37) holds for an initial transition from negative to positive. As already mentioned, the average voltage approaches zero as t_c decreases.

Consequently, the effect of the dead time also decreases. In Figure 4.32, the value of t_c is increased from 1 μs to 15 μs in 1 μs steps.

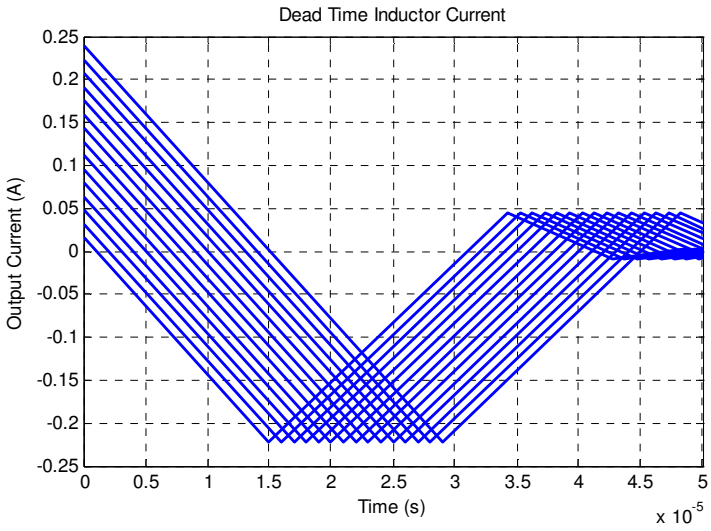

Figure 4.32 Dead time current for different values of t_c

By using (4.37), the average voltage is calculated for each value of t_c. Figure 4.33 shows how the average output voltage increases as the value of t_c increases. When t_c is equal to the dead time period, the current does not change polarity and the output voltage remains the same during the dead time. In the next section, the results are verified experimentally.

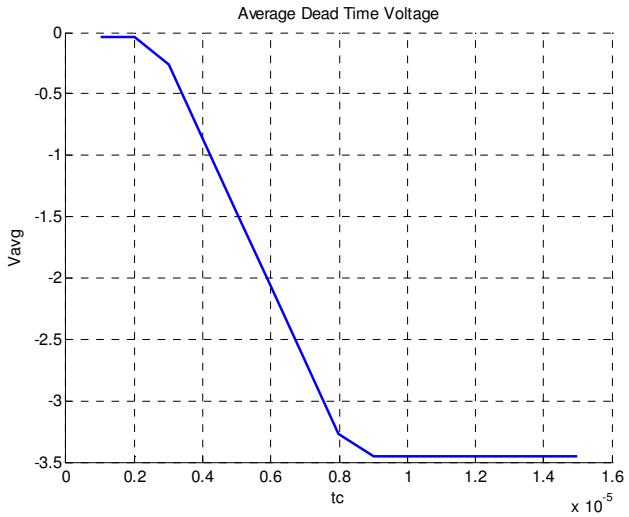

Figure 4.33 Average output voltage of inverter

4.4.4 EXPERIMENTAL RESULTS

The experimental inverter is configured in the same topology as Figure 4.22 with parameters corresponding to Table 4.2. A TMS320F28335 DSP is used to generate the gating signals. A simple open loop, two-level sinusoidal pulse width modulation scheme

is used. The dead time is generated by the DSP and is adjusted via the software. In Figure 4.34 (a), the gating signals are shown and in Figure 4.34 (b) the output voltage and current. Note that the output voltage is scaled by 0.0333 to clarify the relationship between the inductor current polarity and the switched output voltage.

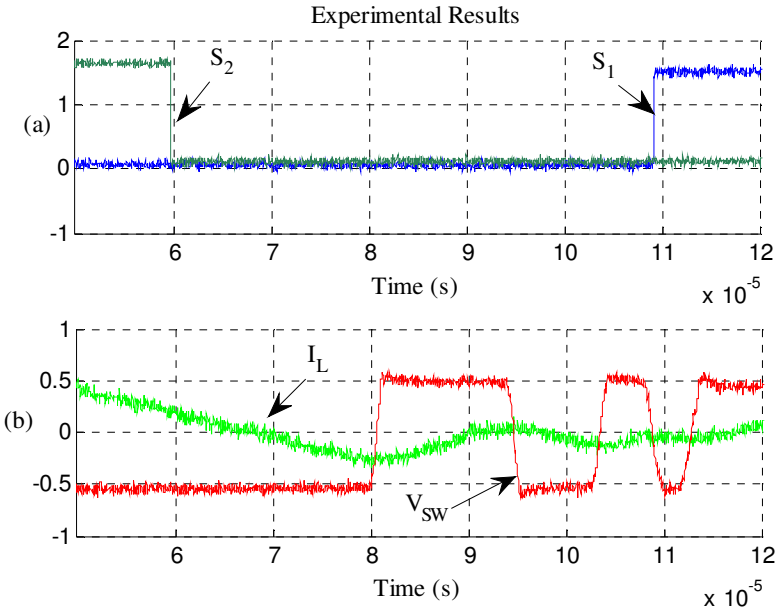

Figure 4.34 Measurements with $t_d = 50\ \mu s$

The current changes polarity at roughly 70 μs. At 80 μs D_2 turns off and D_1 turns on. This changes the output voltage from $-V_{dc}$ to V_{dc}. The process is repeated three more times, after which the gating signal S_1 is set high and the output voltage remains at V_{dc}. The average voltage during the dead time is calculated at roughly –3 V. This compares well with the value calculated by the simulation, which is –2.5261 V. If the current polarity remained the same during the dead time, the average voltage would have been –15 V. It is shown in Figure 4.35 how the current fades as the energy in the inductor is depleted. As mentioned before, this is a very elaborate case and is only included for illustrative purposes. Because of the fading energy, the diodes cannot switch on fast enough or at all. Eventually the output voltage fades to zero.

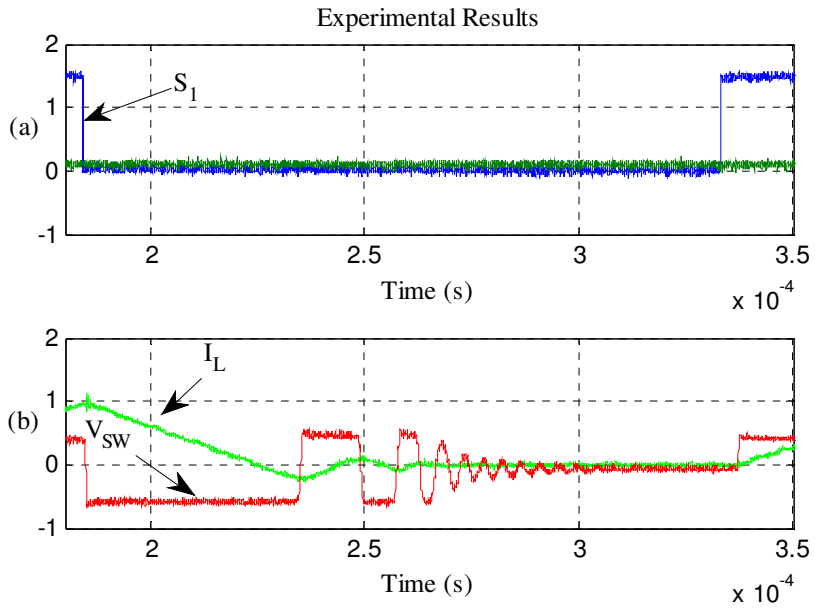

Figure 4.35 Measurements with t_d = 150 μs

The filtered output voltage is shown in Figure 4.36. The effect of the dead time around the zero crossing is also indicated. In Figure 4.36 (a) and Figure 4.36 (b), the dead times are set to 15 μs and 30 μs respectively. By applying an appropriate compensation method this effect can be almost eliminated.

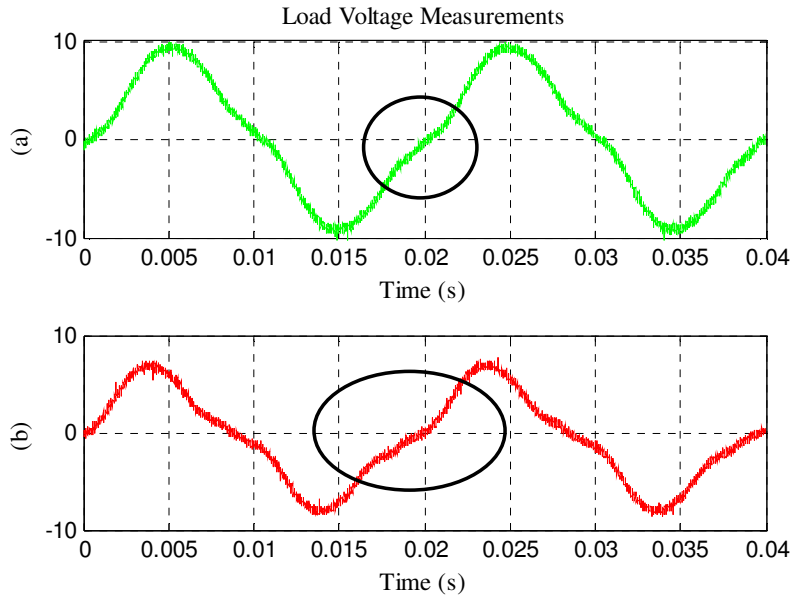

Figure 4.36 Filtered output voltage

In Figure 4.37 the reference, output and error voltages are shown. The three current regions are also indicated. It can be seen how the error voltage changes in region B, but remains the same in regions A and C.

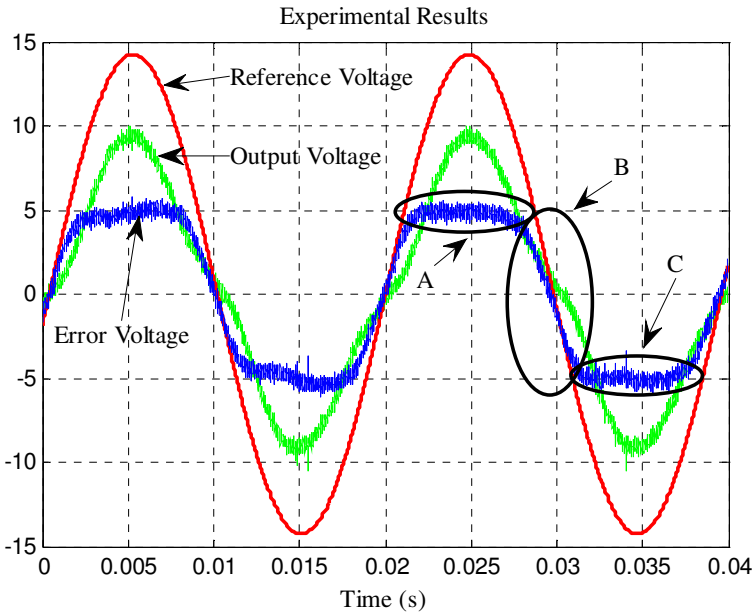

Figure 4.37 Comparison of output voltages

The change in the error voltage is similar to the effect shown in Figure 4.33. In Figure 4.38, the output voltage and the voltage spectrum are shown. The dead time is 10 μs.

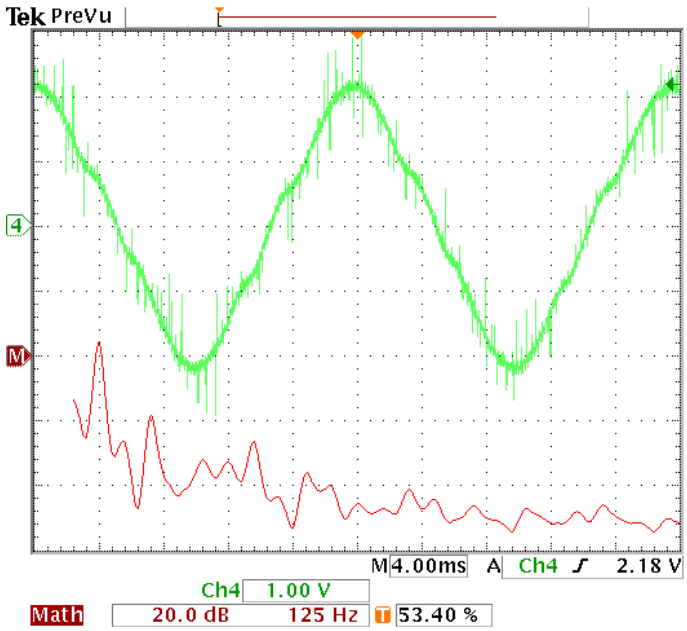

Figure 4.38 Output voltage and spectrum with no compensation

The average model used in Figure 4.39 adds the dead time to the calculated duty cycle when the reference is positive and subtracts it when it is negative. There is still some waveform distortion because of the inaccuracies in the region close to zero. The addition of the square wave to the sinusoidal reference adds odd order harmonics [24].

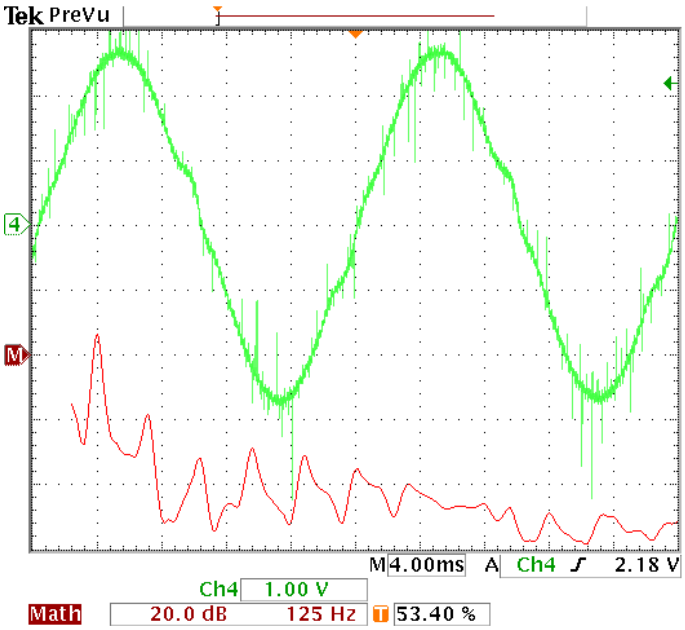

Figure 4.39 Output voltage and spectrum with average model compensation

A linear model is used in Figure 4.40. The amount of dead time added or subtracted is varied linearly in the region close to zero. It eliminates the discontinuity, which is present in the average model. This effectively reduces the odd order harmonics in the output voltage.

The spectrum measurements for the three output voltages are shown in Table 4.3. The amplitude of the fundamental component for both compensation methods is larger. This implies that the voltage amplitude error is improved in both cases.

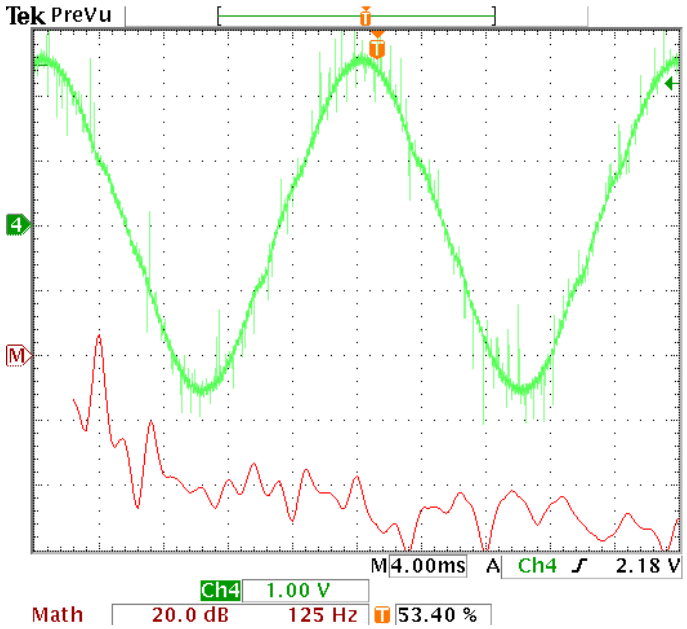

Figure 4.40 Output voltage and spectrum with linear model compensation

There is also an improvement in the harmonic content of the linear model compared to the average model. Further improvement could be possible by using a non-linear model as suggested in [24] or by further tweaking the linear model.

Table 4.3 Dead Time Spectrum Measurements

	Fund.	3rd	5th	7th	9th
No Comp.	4.8 dB	-18dB	-31.6 dB	-26 dB	-36 dB
Avg. Model	6.8 dB	-18.4 dB	-31.6 dB	-28.4dB	-30.8 dB
Lin. Model	6.8 dB	-20 dB	-40.4 dB	-32.8 dB	-34.8 dB

4.4.5 IMPLEMENTATION OF DEAD TIME COMPENSATION

The following equation shows an example of how dead time would be compensated for by adding a fixed value:

$$\begin{aligned} &\text{if}(I_{ref} > 0)\{\ I_{ref} = I_{ref} + I_{dt};\} \\ &\text{if}(I_{ref} < 0)\{\ I_{ref} = I_{ref} - I_{dt};\} \end{aligned} \tag{4.38}$$

where I_{ref} is the reference current and I_{dt} is the dead time current to be added. If a linear model is used to compensate for the dead time, a threshold value is added to determine where the linear compensation should start.

An example of such a compensation method is shown in the following equation:

$$\begin{aligned}
&\text{if}(I_{ref} > I_{thres})\{ I_{ref} = I_{ref} + I_{dt}; \}\\
&\text{if}(I_{ref} < I_{thres} \text{ and } I_{ref} > 0)\{ I_{ref} = I_{ref} + (I_{ref}/I_{thres}) \times I_{dt}; \}\\
&\text{if}(I_{ref} < -I_{thres})\{ I_{ref} = I_{ref} - I_{dt}; \}\\
&\text{if}(I_{ref} > -I_{thres} \text{ and } I_{ref} < 0)\{ I_{ref} = I_{ref} + (I_{ref}/I_{thres}) \times I_{dt}; \}
\end{aligned} \tag{4.39}$$

where I_{thres} is the threshold current for the linear compensation. In Figure 4.41 (a) an example of dead time compensation with a fixed model is shown. The reference current, compensated current and the dead time current added are shown. The spectrum of the compensated current is shown in Figure 4.41 (b). The addition of the square wave to the sinusoidal reference adds additional harmonics to the compensated current. In this example a 10 A_{peak} signal is used as the reference signal and a 1 A signal as the compensation current.

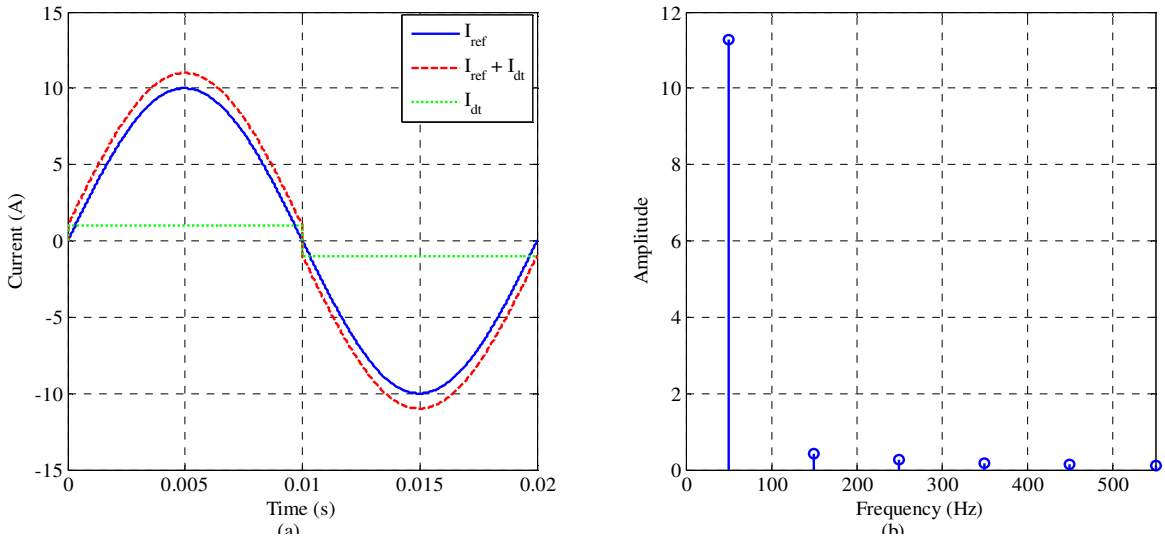

Figure 4.41 Dead time compensation with a fixed model and spectrum

Figure 4.42 (a) is an example of dead time compensation with a linear model. The reference current, compensated current and the dead time current added are shown. The spectrum of the compensated current is shown in Figure 4.42 (b). The same reference signal as in the previous example is used. In this case, the threshold for the linear compensation is 3 A. As the reference signal approaches zero, the amount of compensation is decreased.

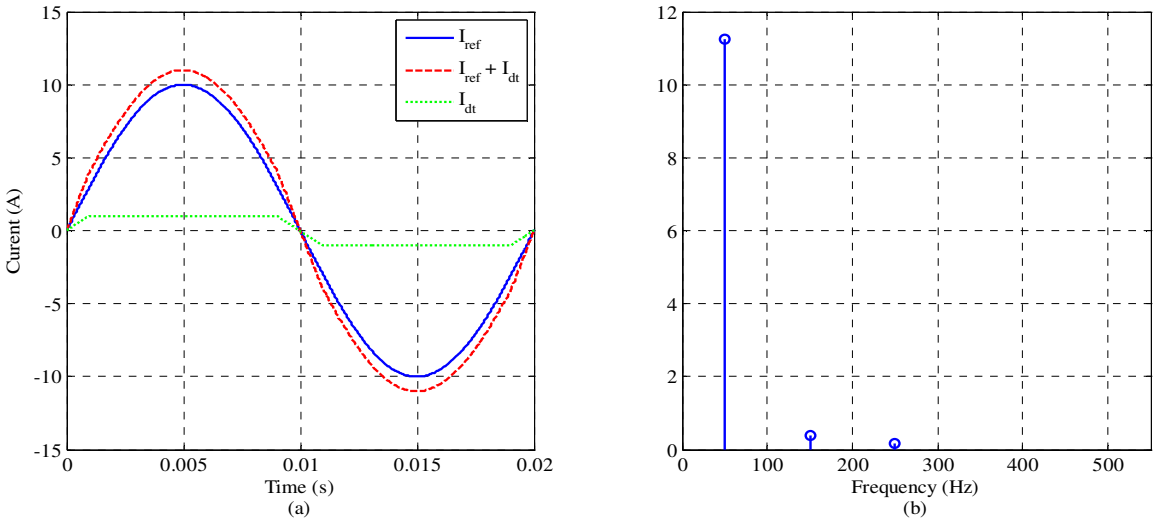

Figure 4.42 Dead time compensation with a linear model and spectrum

The linear model has less harmonic components than the fixed model. This is as a result of the smoother transition between the positive half-cycle and the negative half-cycle. The threshold can either be calculated or determined through an iterative method. In this thesis, the linear model is implemented. It should be noted that, when the duty cycle is less than the dead time, i.e. close to zero, or close to 100%, then alternative compensation is necessary. Refer to Appendix B. for the code used to implement the dead time compensation.

4.5 IMPLEMENTATION OF THE ANTI-ISLANDING METHODS

The anti-islanding methods are implemented by modifying the per unit reference signal. In the case of the SMS method, the phase of the reference is shifted relative to the grid voltage. To implement the SVS method, the amplitude of the per unit reference is adjusted. The working of the anti-islanding methods is firstly verified by simulation. These simulations are done in *Simplorer*™.

The system used has the same configuration as in Figure 4.2. Control calculations and the anti-islanding control are done using VHDL-AMS. This makes it possible to use code in a similar way as it will be implemented in the actual system. In addition to the control calculations themselves the frequency is also calculated, as this is needed for the SMS method. This is done by determining the time elapsed between each zero crossing of the voltage at the point of common coupling.

In Figure 4.43, the rotation of the reference vector is shown. The vector $\overline{I_{pu}}$ is in phase with the supply vector $\overline{V_{\alpha\beta}}$, whereas the vector $\overline{I_{ref}}$ is rotated by the angle (θ) calculated by using the methods explained in Section 3.3.1.

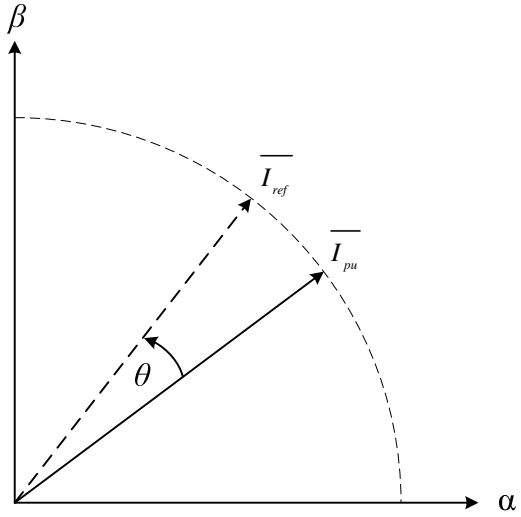

Figure 4.43 SMS reference vector rotation

To rotate the vector a rotation matrix is used to calculate the new α and β components of the reference vector. This matrix is as follows:

$$\begin{bmatrix} i_{\alpha,ref} \\ i_{\beta,ref} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{\alpha,pu} \\ i_{\beta,pu} \end{bmatrix} \tag{4.40}$$

The rotational direction of the vector can be controlled by using the absolute value of the angle calculated by using (3.13).

In the case of the SVS method the fraction calculated, as explained in Section 3.4, is either added to or subtracted from the per unit reference signal. To prevent damage to the converter the maximum value added to the unity reference needs to be limited. This limit will largely depend on the voltage of the DC link, as the amplitude of the diode rectified voltage cannot be higher than the reference voltage set for the DC link. If this limit is set too low, the change in power resulting from the increased reference will be too low to drive to voltage at the PCC outside the protection limits.

4.6 SIMULATION RESULTS

In this section, the functioning of the anti-islanding methods is verified using simulation studies. The active rectifier and DC regulator are also simulated. Figure 4.44 shows the line diagram of the three-phase system. The RLC load that will be used to form a potential island is included. The switch, S_1, is used to disconnect the converter from the grid, to form the islanded section.

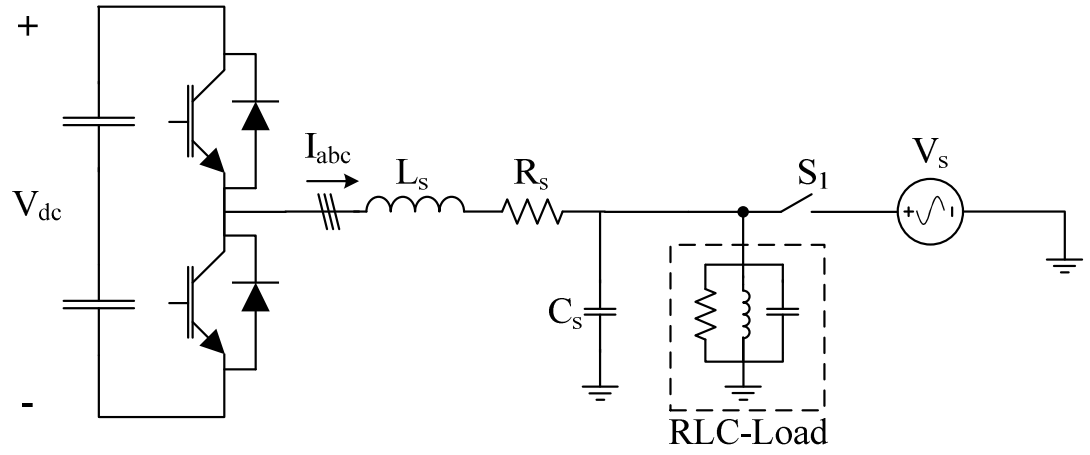

Figure 4.44 Line diagram of three-phase system with RLC load

The fixed parameters of the system are listed in Table 4.4. These parameters remain the same during all the simulations. The RLC load will be adjusted to test the different anti-islanding methods.

Table 4.4 Fixed simulation parameters

Parameter	Value
L_s	800 µH
R_s	0 Ω
C_s	13.2 uF
V_s	230 V, 50 Hz
$V_{dc,ref}$	750 V
C_{dc}	4700 µF

4.6.1 SIMULATION OF THE DC BUS REGULATOR

In this simulation, no RLC load is connected to the converter. All the power required is drawn from the grid or delivered to the grid. Figure 4.45 shows the charging and regulation of the DC bus. The DC bus voltage, whose reference is set to 750 V, and the

inductor current are shown; the inductor current is scaled by a factor 10 for clarity. After connecting to the grid, the PWM signals are left off. The DC bus is initially charged through the diodes. Once the maximum diode rectified voltage is reached, the bus is boost-charged to the reference voltage value.

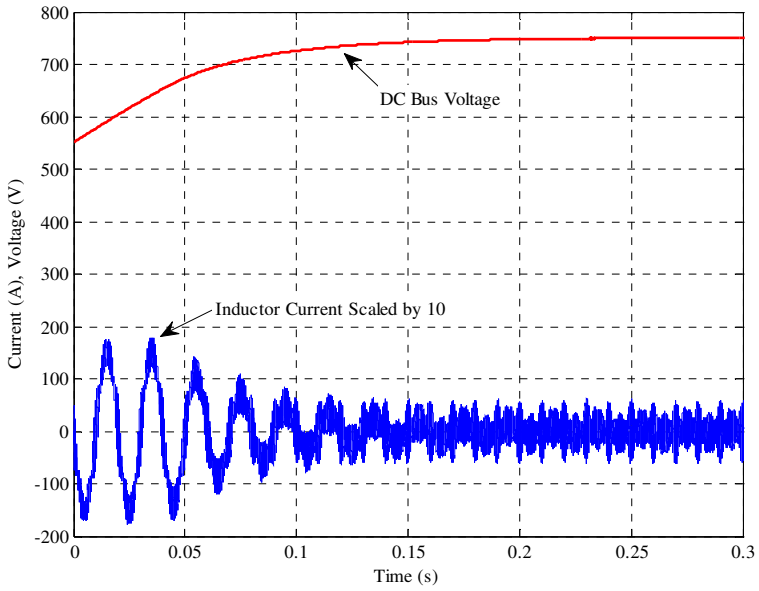

Figure 4.45 Charging of DC bus and regulation

In Figure 4.45, the initial values of the bus capacitor are set to 550 V. This is done to show how the DC voltage is boosted and then regulated. In the simulation the amplitude of the current is limited to 15 A. By changing this limit, the charge time of the DC bus capacitors is varied.

4.6.2 SIMULATION OF THE ACTIVE RECTIFIER

The active rectifier is simulated to verify current reference tracking as well as power reference tracking. When connected to a generator, the active rectifier should be able to track a power reference calculated by an algorithm such as a maximum power point tracker. In Figure 4.46, the measured power and reference power is shown. At 50 ms the power reference, indicated by a dashed line, is stepped from 0 kW to 3.3 kW and at 100 ms the reference is stepped from 3.3 kW to 1.5 kW. The generator voltage and inductor current is shown in Figure 4.47. Throughout the simulation, the generator voltage is kept constant at 230 V, whereas the current amplitude changes to track the power reference.

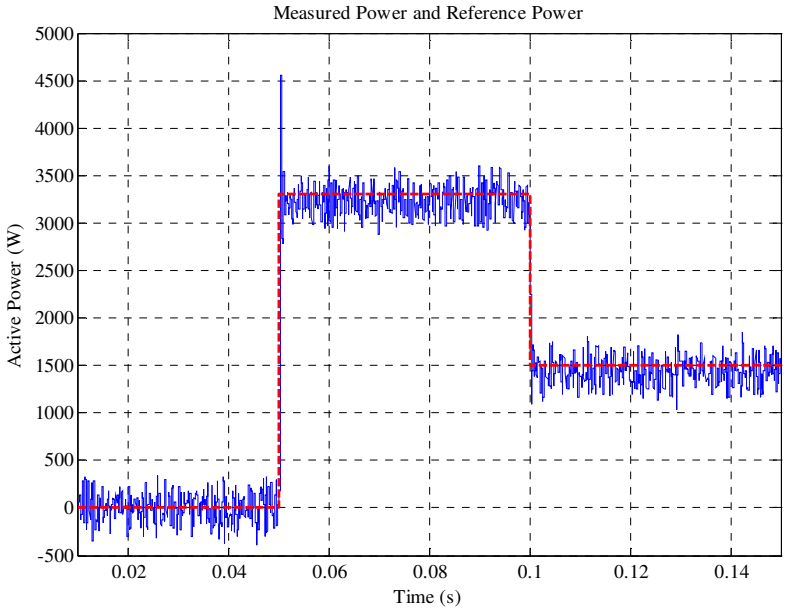

Figure 4.46 Active rectifier measurement with varied power reference

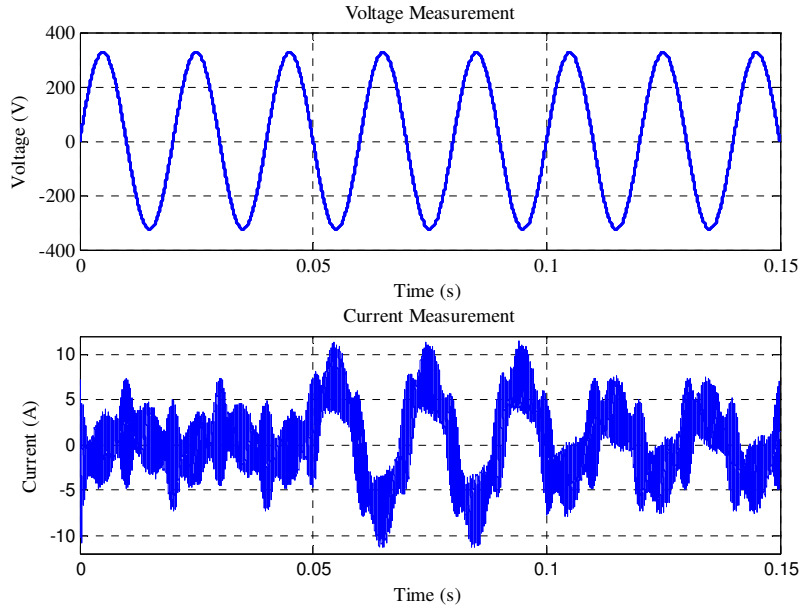

Figure 4.47 Active rectifier voltage measurement and inductor current with constant voltage

The phase of the current and the voltage is 180º out of phase. This is because power is being drawn from the grid and delivered into the DC bus.

In the following simulation, the power reference is kept constant while the generator voltage is varied. In Figure 4.48 the power reference is set to 3.3 kW. The power reference, indicated by a dashed line, and the measured power are shown.

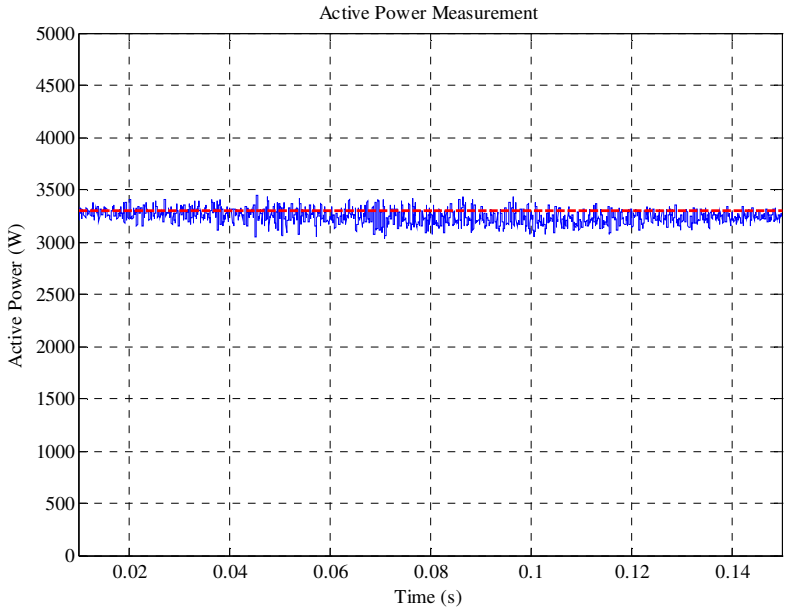

Figure 4.48 Active rectifier measurement with constant power reference

In Figure 4.49, the generator voltage and inductor current are shown. During the period from 0 ms to 50 ms, the generator voltage is gradually varied from 100 V to 230 V. The voltage is then kept constant at 230 V until 100 ms, after which it is gradually varied back to 100 V. To track the power reference the amplitude of the inductor current is decreased, as the voltage amplitude increases and vice versa.

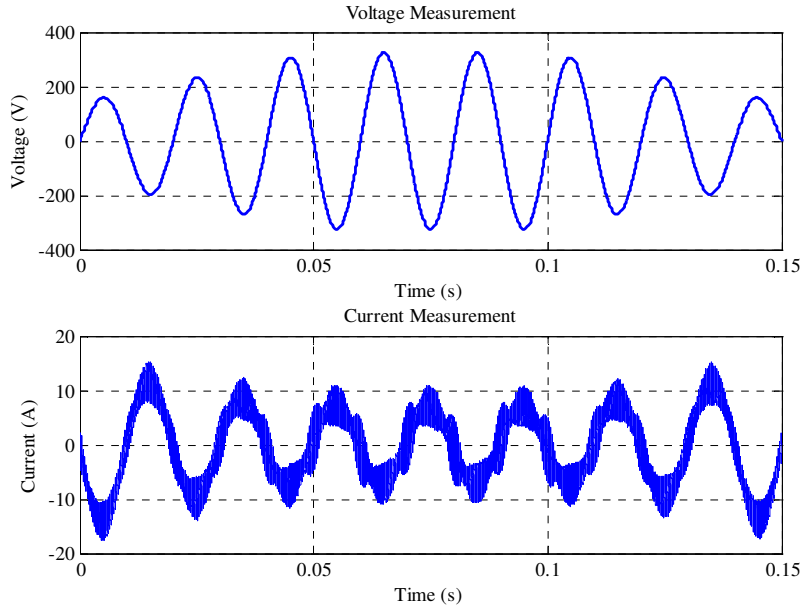

Figure 4.49 Active rectifier voltage measurement and inductor current with varied voltage

In both of the above cases, a near instant tracking of the power reference was achieved. In a practical system, the output voltage of the generator will not change instantaneously due to the inertia of the generator and the blades connected to it. A more gradual change will occur, resulting in a gradual change in the inductor current amplitude over time.

4.6.3 SIMULATION OF ANTI-ISLANDING METHODS

In this section, the selected anti-island methods are simulated. Initially a base case is simulated with no anti-islanding method implemented. The purpose of this is to confirm the formation of an island that falls within the compatibility levels of the grid, once disconnected. Thereafter the island prevention methods are simulated.

4.6.3.1 SIMULATION OF A LOAD WITH $Q_F = 1.52$

The load in this simulation has the parameters as listed in Table 4.5.

Table 4.5 Parameters for load with $Q_f = 1.52$

Parameter	Value
L_{load}	100 mH
R_{load}	48.09 Ω
C_{load}	86.8 µF
C_{filt}	13.2 µF
Q_f	1.52
f_0	50.32 Hz

In Figure 4.50, the voltage at the PCC and the supply current are shown. The dashed lines indicate the trip limits of the voltage protection. At 100 ms, the grid is disconnected and no current flows from the grid; the grid current is scaled by a factor 10. The voltage and current are indicated. After disconnection, the voltage amplitude remains within the trip limits.

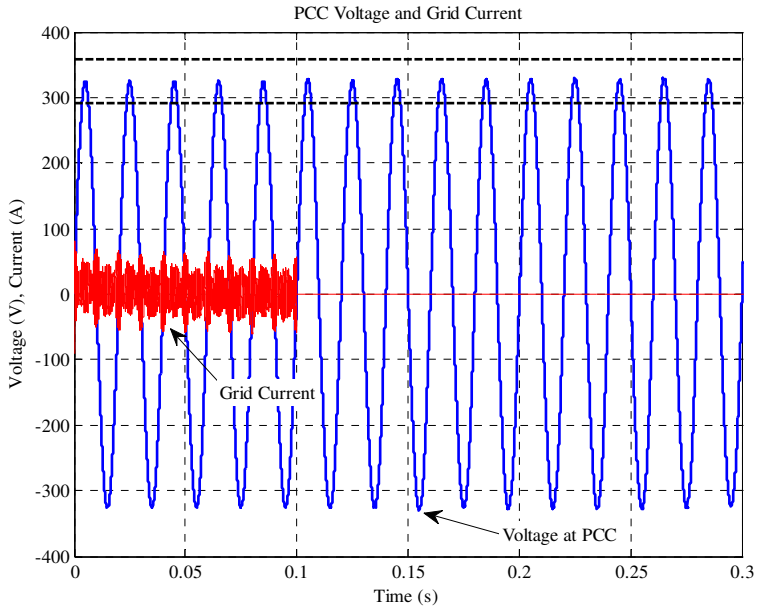

Figure 4.50 PCC voltage and supply current for base case with Q_f = 1.52

The frequency of the voltage at the PCC and the inductor current are shown in Figure 4.51. The trip limits of the frequency are indicated by the dashed line. After disconnecting from the grid, there are slight variations in the frequency, although the variations remain within the limits of the frequency protection. The inductor current remains unchanged after the grid is disconnected.

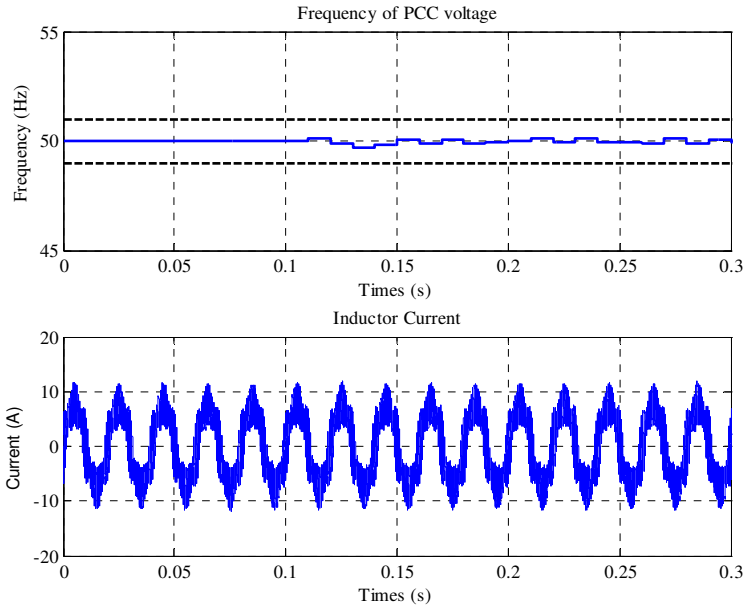

Figure 4.51 PCC voltage frequency and inductor current for base case with Q_f = 1.52

After disconnecting from the grid, both the voltage amplitude and frequency remains within the compatibility levels of the grid. In this case, the converter will continue to energize the local load.

The SMS method is implemented with a load that is identical to the base case. The maximum phase deviation is calculated as explained in Section 3.3.1. The maximum deviation is calculated for a load with a quality factor of 2.7. This is slightly higher than the maximum quality factor for the recommended maximum test load (refer to Section 3.2). The maximum phase deviation is 10º and the maximum frequency deviation is set to 53 Hz. The absolute value of the frequency error is used to calculate the 'new' phase. This makes it possible to force the direction of the frequency drift.

In Figure 4.52, the voltage at the PCC and the grid current, scaled by 10, are shown. After disconnection at 100 ms, the voltage amplitude remains within the trip limits.

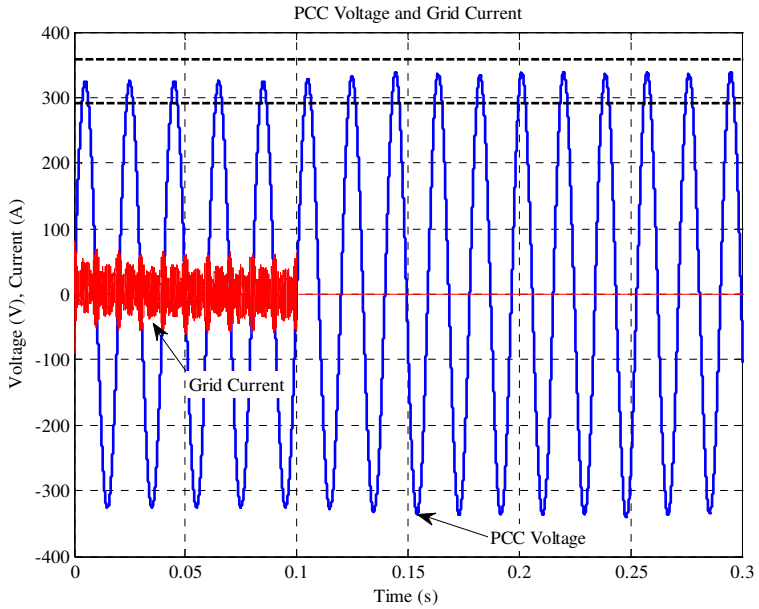

Figure 4.52 PCC voltage and grid current for SMS method with Q_f = 1.52

The frequency trip is disabled in this simulation. This is to show how the frequency drifts outside the limits. After disconnecting from the grid the frequency of the PCC voltage drifts outside the protection limits at 150 ms, as shown in Figure 4.53. At 170 ms, the frequency deviation reaches the limit at 53 Hz.

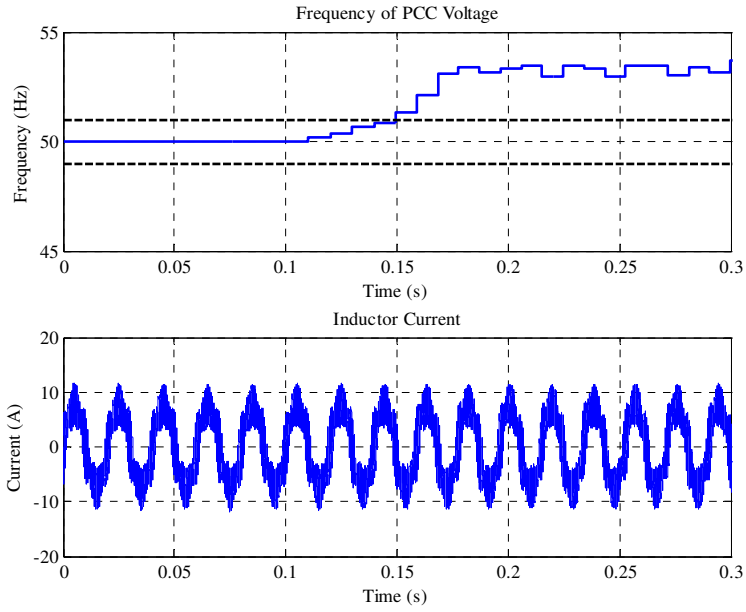

Figure 4.53 PCC voltage frequency and inductor current for SMS method with Q_f = 1.52

After disconnecting from the grid, the voltage amplitude remains within the protection limits, but the frequency drifts outside the limits. If the frequency protection were enabled, the converter would have ceased to energize the local load at 150 ms.

The SVS method is implemented to drive the voltage outside the limits of the voltage protection. The gain is calculated by using (3.29). The cut-off frequency of the low-pass filter is 10 rad/s. In Figure 4.54, the voltage at the PCC, the grid current (scaled by factor 10) and the inductor current are shown. The limits of the voltage protection are indicated with a dashed line. The gain is K_{svs} = 0.22. At 100 ms, the grid is disconnected. A negative voltage error occurred, which drove the voltage amplitude outside the limits at 145 ms. It can be seen how the amplitude of the inductor current decreases, resulting in the voltage drop. The limits to which the current reference could change are 1.6 per unit and 0.6 per unit. The voltage trip was disabled in the simulation to show how the voltage level decreases.

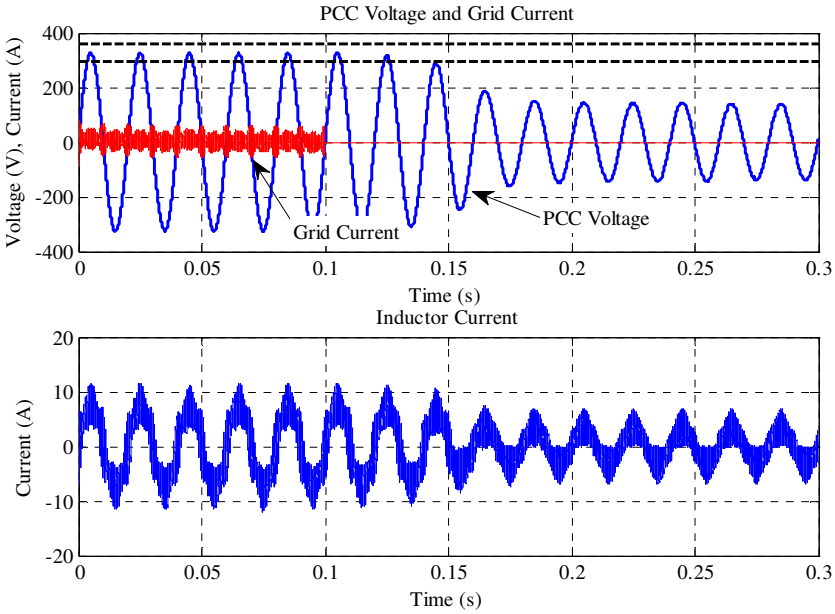

Figure 4.54 PCC voltage, grid current and inductor current for SVS method with $Q_f = 1.52$

For both island prevention methods implemented the energizing of an island with a quality factor 1.52 is successfully prevented.

4.6.3.2 SIMULATION OF A LOAD WITH $Q_F = 2.53$

The load parameters for this simulation are as listed in Table 4.6.

Table 4.6 Parameters for load with Qf = 2.53

Parameter	Value
L_{load}	94 mH
R_{load}	75 Ω
C_{load}	93.8 µF
C_{filt}	13.2 µF
Q_f	2.53
f_0	50.18 Hz

In this simulation, the voltage and frequency protection is enabled. The frequency trip levels are 51 Hz and 49 Hz. The voltage trip levels are 253 V and 207 V. If one of the measurements drifts outside these values, the converter is shut down. A base case is simulated to confirm the formation of an island with protection enabled. The voltage at the PCC and the grid current, scaled by 10, are shown in Figure 4.55. The trip limits are

indicated with dashed lines. After disconnecting from the grid at 100 ms, the island voltage amplitude remains within the limits.

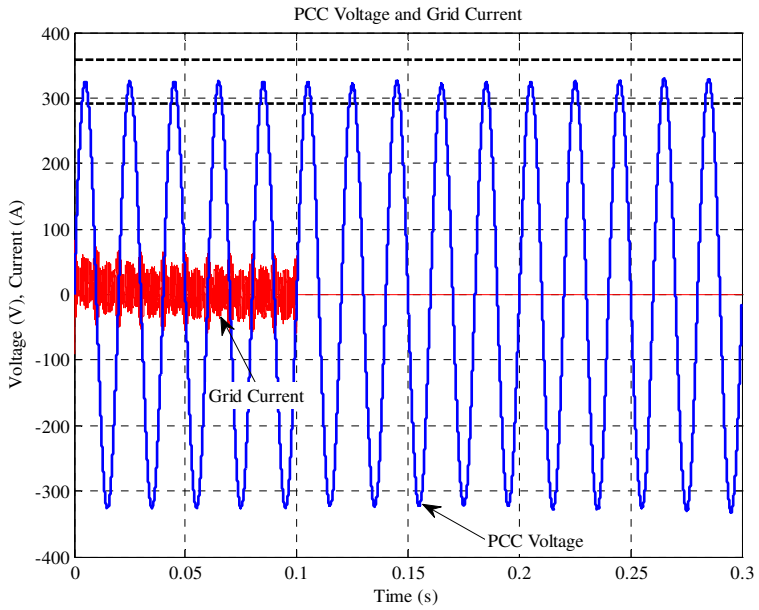

Figure 4.55 PCC voltage and supply current for base case with Q_f = 2.53

Figure 4.56 show the voltage frequency after the grid is disconnected at 100 ms. Although there are slight variations in the frequency, it remains within the protection limits.

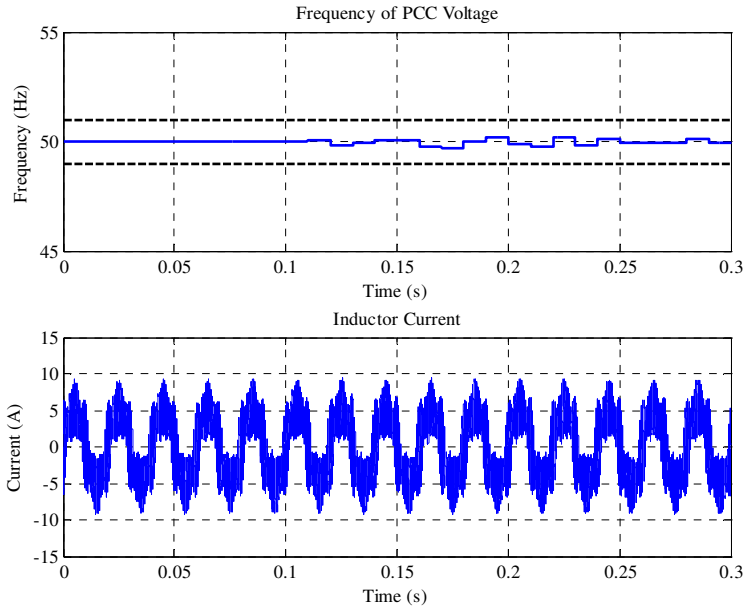

Figure 4.56 PCC voltage frequency and inductor current for base case load with Qf = 2.53

The SMS method is implemented with the same load as in the base case. The maximum phase deviation is designed for a load with a quality factor of 3. The maximum phase angle is calculated as 11°. The maximum frequency deviation is set to 53 Hz. In Figure 4.57, the PCC voltage and grid current are shown. The grid is disconnected at 100 ms. At 220 ms the frequency drifts outside the limits and the converter is shut down. After disconnection, the voltage gradually fades away.

The frequency of the PCC voltage and the inductor current are shown in Figure 4.58. After disconnecting the grid, the frequency of the fading voltage is still calculated; this is irrelevant, however, as the converter has already shut down. The energizing of the island is prevented.

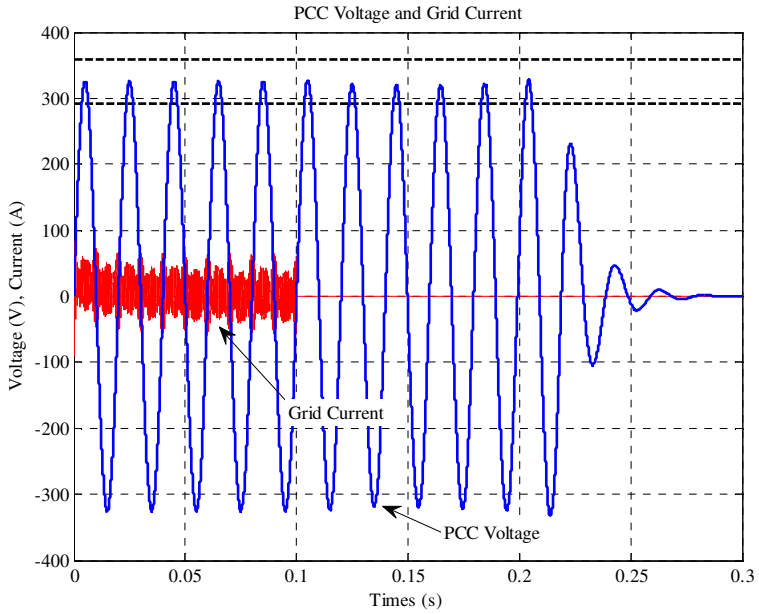

Figure 4.57 PCC voltage and grid current for SMS method with $Q_f = 2.53$

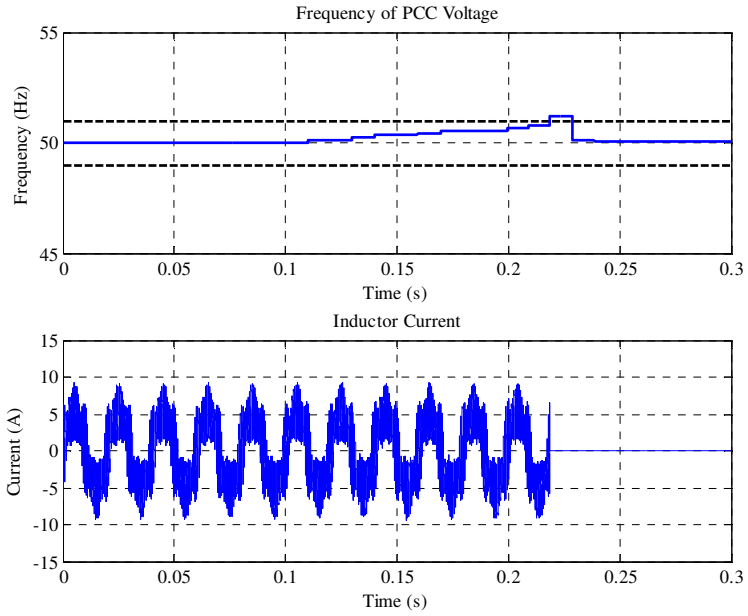

Figure 4.58 PCC voltage frequency and inductor current for SMS method with Q_f = 2.53

The SVS is implemented with a gain of, K_{svs} = 0.17. The cut-off frequency of the low-pass filter is 10 rad/s. After disconnection, a negative voltage error starts to decrease the amplitude of the reference current. At 206 ms, the converter is shut down. Although the voltage drops below the limits at 175 ms, the converter is only shut down when the filtered voltage drops below the trip level. This delay will prevent the converter shutting down unnecessarily during voltage drips when the converter is still connected to the grid. The filter can also be used to adjust the response time of the SVS method.

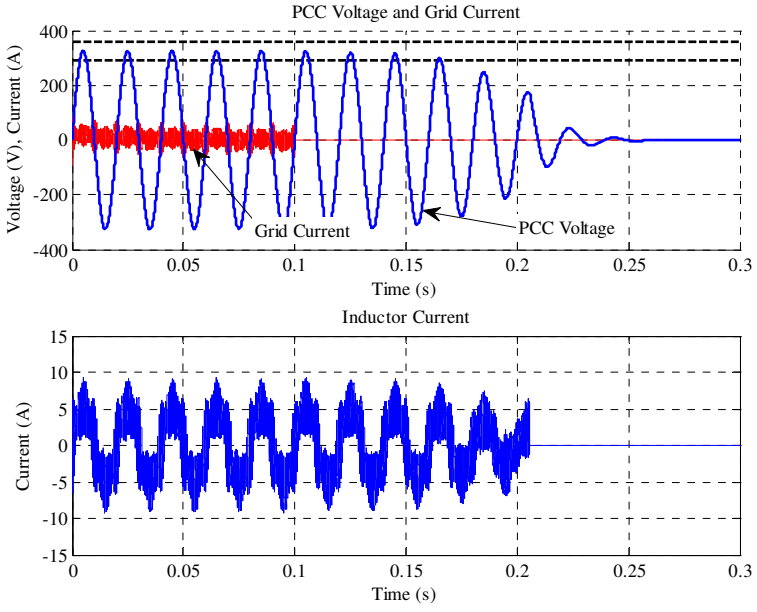

Figure 4.59 PCC voltage, grid current and inductor current for SVS method with Q_f = 2.53

Both the SMS and SVS method prevented the continued energizing of the islanded load with a quality factor of 2.53.

4.6.3.3 SIMULATION OF A LOAD WITH $Q_F = 3.99$

Although a load with a quality factor of 3.99 falls outside the limits of the suggested maximum test load (refer to Section 3.2), it is included to show that the formation of an island can be prevented in the case of higher quality factor loads. The parameters for the simulated load are as listed in Table 4.7.

Table 4.7 Parameters for load with $Q_f = 3.99$

Parameter	Value
L_{load}	48 mH
R_{load}	60 Ω
C_{load}	198.8 µF
C_{filt}	13.2 µF
Q_f	3.99
f_0	49.89 Hz

In Figure 4.60, the base case simulation is shown. The voltage remains within the compatibility levels of the grid after disconnection at 100ms.

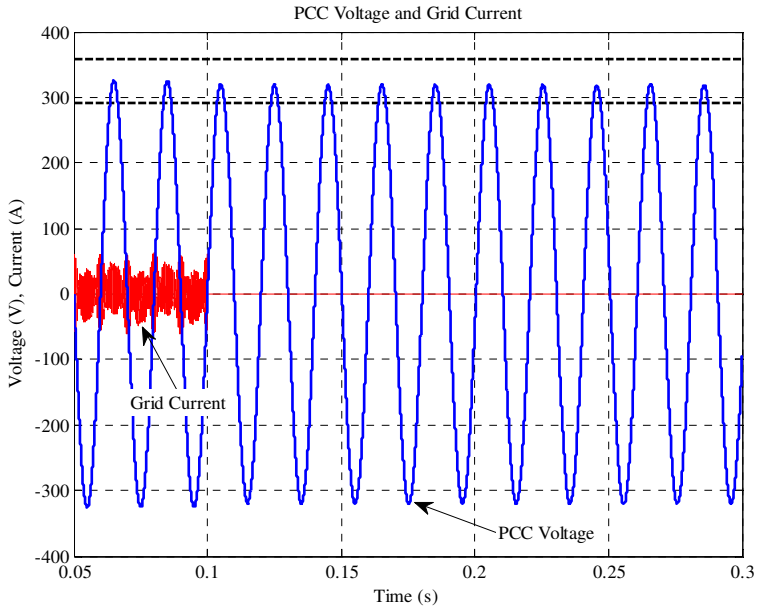

Figure 4.60 PCC voltage and grid current for base case with $Q_f = 3.99$

The frequency of the PCC voltage drop slightly, but remains well within the limits. This is shown in Figure 4.61. With no anti-islanding method implemented the island is continuously energized once the grid is disconnected.

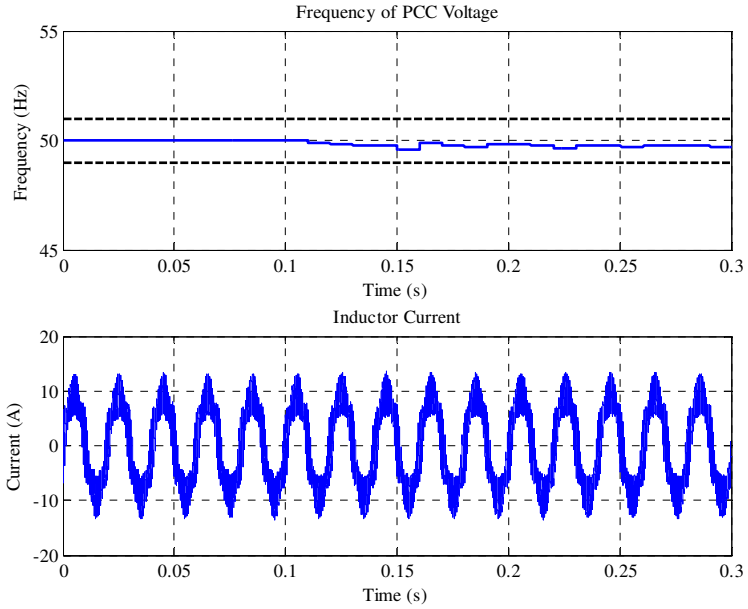

Figure 4.61 PCC voltage frequency and inductor current for base case with $Q_f = 3.99$

The SMS method is implemented with a maximum phase deviation designed for a load with a quality factor of 4.5. The maximum phase deviation is calculated as 16.5º and the maximum frequency deviation is set to 53 Hz. The voltage and frequency protection is enabled. The PCC voltage and grid current are shown in Figure 4.62. The grid is disconnected at 100 ms and the converter is shut down at 190 ms. The voltage amplitude remains with the trip limits, but the frequency deviated. The frequency and the inductor current are shown in Figure 4.63. After disconnecting from the grid, the frequency starts to vary, which activates the SMS methods feed forward response and then drives the frequency outside the limits. The continued energizing of the islanded load is successfully prevented.

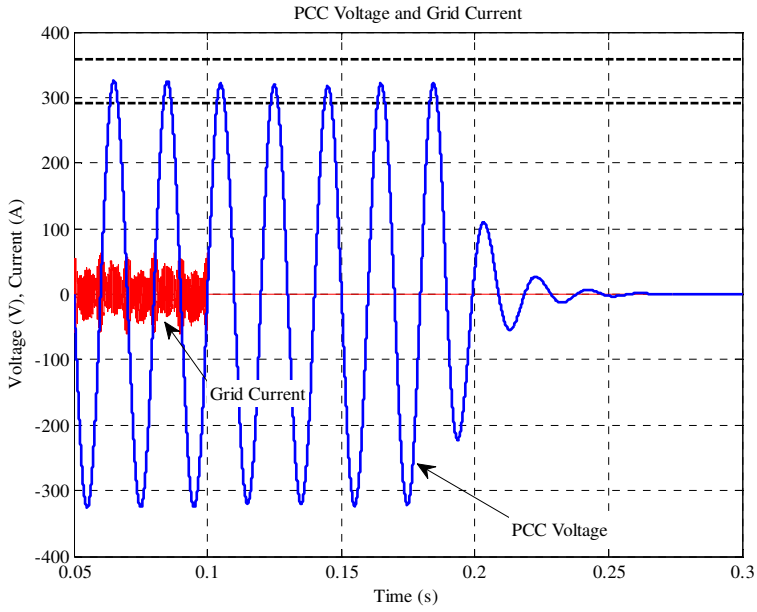

Figure 4.62 PCC voltage and grid current for SMS method with Q_f = 3.99

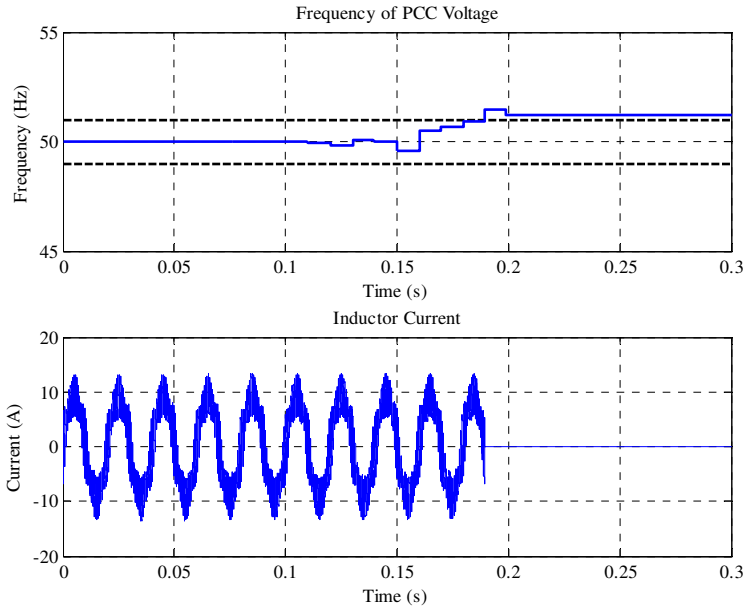

Figure 4.63 PCC voltage frequency and inductor current for SMS method with Q_f = 3.99

The SVS method is implemented with a gain of, K_{svs} = 0.2. The cut-off frequency of the low-pass filter is 10 rad/s. The PCC voltage, grid current and inductor current are shown in Figure 4.64. After disconnecting from the grid at 90 ms, a positive voltage error occurred. The amplitude of the reference current is increased. Consequently, the output voltage increases. The increase is limited to 1.3 per unit. The filter causes a delay in the response of the voltage trip. The converter is shut down at 165 ms.

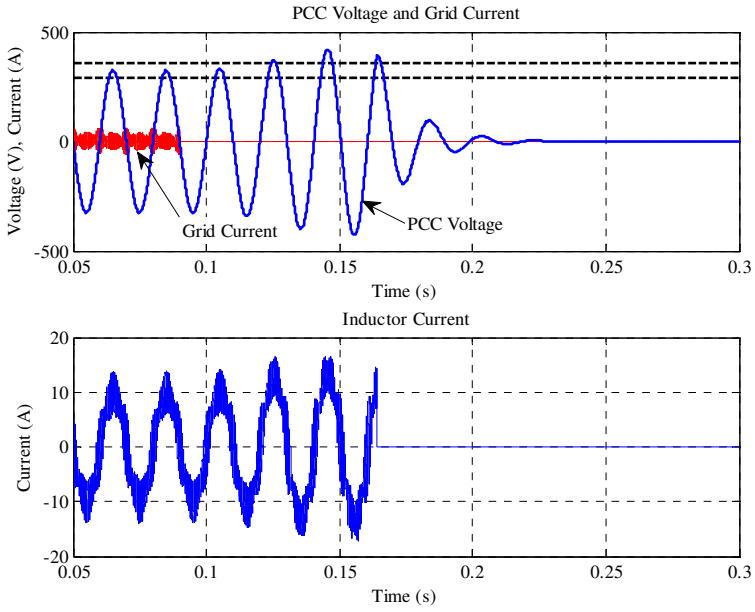

Figure 4.64 PCC voltage, grid current and inductor current for SVS method with $Q_f = 1.52$

The voltage increase is limited by the DC bus voltage. If the limit is set too high the diode rectified voltage will be higher than the active rectified voltage. This will interfere with the control of the inductor current and the regulation of the bus voltage.

This simulation shows that the anti-islanding methods can be implemented successfully for loads with higher quality factors too.

4.7 SUMMARY

In this chapter, the algorithms required to simulate and test the anti-islanding methods were developed and discussed. The system topology was selected and the different components of the converter were discussed. Space vector pulse width modulation and the Clarke transformation were discussed as methods of controlling the selected 3-wire topology of the converter. Predictive current control was explained and the control algorithm for the current loop was derived. To regulate the DC bus of the converter a control algorithm was designed. This algorithm also controls the power exchange between the DC bus of the converter and the grid.

A brief overview was given of the effects that dead time in the gating signals had on the overall performance of a power electronic inverter. Possible compensation methods were also briefly discussed. Three polarity regions for the inductor current were identified,

after which a detailed description was given for each region with a focus on the region close to zero. In the region close to zero, the inductor current was analytically characterised to show how the reverse recovery of the diodes affected the output voltage error made during the dead time. These effects were verified through both simulation and experimental results.

The simulated results obtained confirm the functionality of the DC bus regulation algorithm and the reference tracking of the active rectifier. Simulations of the anti-islanding methods suggest that, if implemented correctly, the energizing of loads within an islanded section can successfully be prevented.

CHAPTER 5. HARDWARE AND SOFTWARE DEVELOPMENT

In this chapter, the hardware and software that are used to verify the simulated results are discussed.

5.1 HARDWARE DESCRIPTION

This section gives an overview of the converter used to verify the simulations. The converter was built as part of a previous project, but the digital signal processor (DSP), the interface, the liquid crystal display (LCD), the soft-start circuit and the voltage measurements were designed as part of this project.

Two converters are connected back-to-back, effectively forming an AC to AC converter. The active rectifier switches the 3-phase AC voltages to DC, whereas the inverter switches the DC voltage to 3-phase AC voltages. Switching is done by using a SEMITOP® 3 SK-35-GD-126-ET 3-phase IGBT module from SEMIKRON. This module is rated at 1200 V and 28 A_{RMS}. The gating signals connected to the IGBTs are from a SEMIDRIVER® Dual IGBT SKHI20op driver. This driver provides the required isolation between the controller and the IGBT modules and translates the signal from the controller to the correct level to switch the IGBT modules. On each phase of the converter, the current is measured by a LEM™ LA 55-P hall-effect current sensor. Figure 5.1 shows a top view of the converter. The IGBT modules are located underneath the drivers.

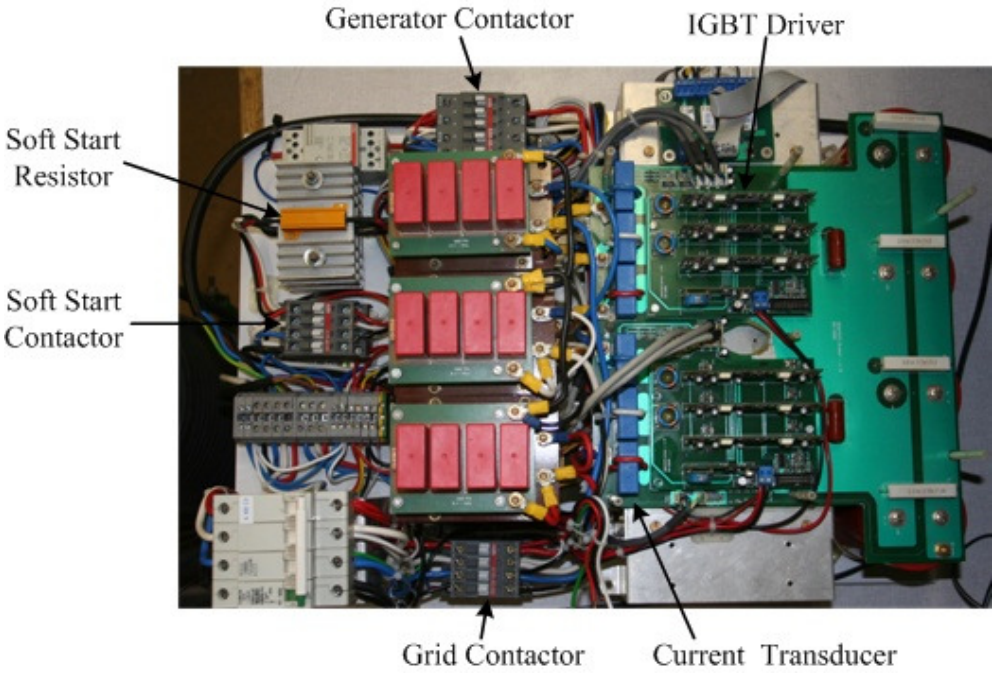

Figure 5.1 Top view of back-to-back converter

On the grid side, an ABB A16-40-00 contactor is used to connect to the grid and an ABB A30-30-10 contactor on the generator side. These contactors are switched by a relay, which is operated by the controller. A soft-start resistor stage is included to protect the anti-parallel diodes of the IGBTs from the inrush currents when initially connecting to the grid.

Figure 5.2 shows the LC filter of the converter. The inductor cores are E65 type ferrite cores made of N27 material, and each inductor has a total inductance of 800 μH. The capacitors are WIMA MKP4 3.3 μF. Four of these capacitors are connected in parallel to give a total capacitance of 13.2 μF on each phase. By using (4.3), the cut-off frequency of the filter is calculated as 1.548 kHz.

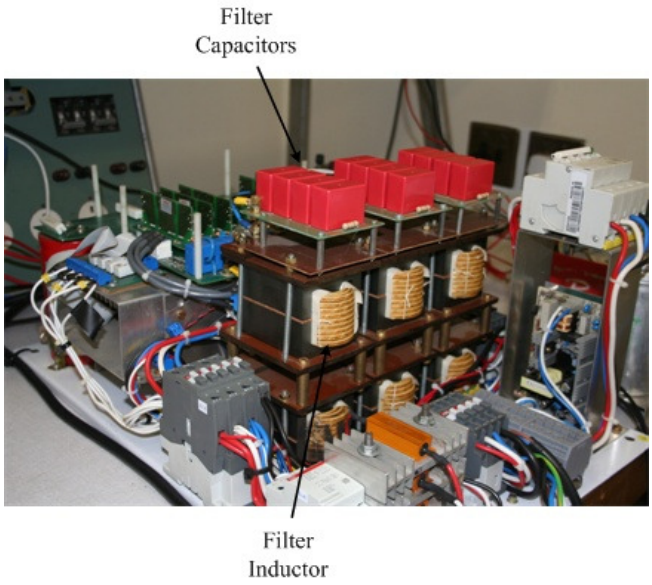

Figure 5.2 Side view of the converter

The DC bus consists of four 450 V, 4700 μF capacitors. In Figure 5.3, the configuration of the DC bus capacitors is shown. Two capacitors are placed in parallel and the two pairs are connected in series. In total the bus capacitance is 4700 μF with a rated voltage of 900 V.

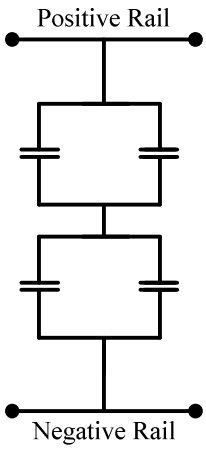

Figure 5.3 Capacitor configuration of DC bus

Figure 5.4 illustrates the inter-connections of the different components of the system. The various control signals, data signals and measurements are shown. The voltage measurements are relayed to the DSP via the interface. Current measurements are scaled on the interface board to be compatible with the ADC channels of the DSP. The LCD and buttons are connected directly to the DSP. A light emitting diode (LED) display is included to give the user a quick visual indication of the system status.

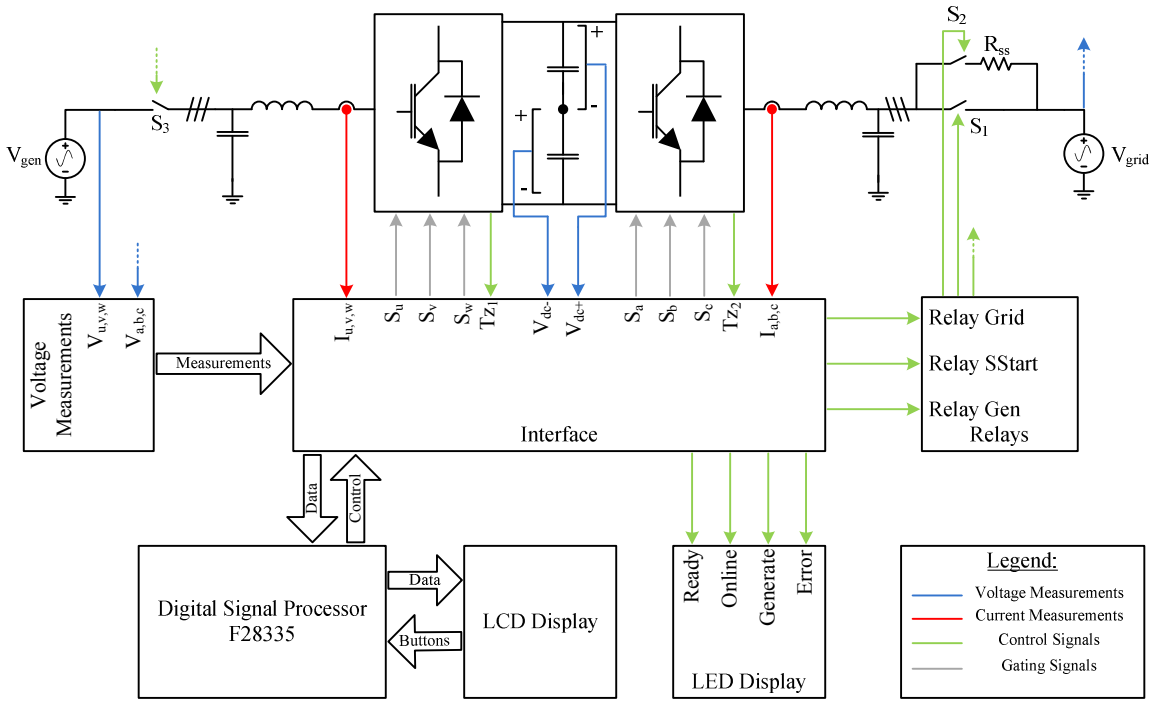

Figure 5.4 System interface diagram

5.1.1 THE DSP CONTROLLER

To do the calculations required and perform the necessary measurements a digital signal processor (DSP) is used. An eZdsp™ F28335 floating point DSP from Texas Instruments is used for this purpose. The DSP has the following features:

- A clock speed of 150 MHz
- 12 PWM channels, which can be configured as 6 complimentary pairs
- Adjustable dead time in the PWM signals
- 16 ADC channels with a 12-bit resolution and an adjustable way of starting the conversion

The DSP is responsible for executing the control loops as well as for overall system control. This controller is mounted on an evaluation board designed by *Spectrum Digital*. The required signals and ADC channels are connected to the interface boards via a ribbon cable and Molex friction locks.

5.1.2 THE VOLTAGE MEASUREMENT BOARD

The voltage measurement board is used to measure and scale the 3-phase voltages on each side of the converter. These voltages are measured differentially. The scaled signals are then connected to the ADC channels of the DSP. The circuit used to scale down the

voltage and remove common mode measurements are shown in Figure 5.5. On each of the input terminals, a voltage division circuit is used. The circuit coinciding with *opamp1* is used to remove common-mode voltages from the measurements.

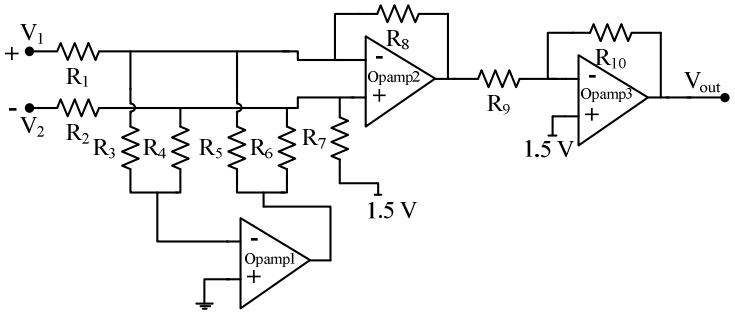

Figure 5.5 Voltage measurement circuit

By assuming that there are no common mode voltages present or that all common mode voltages are removed, the voltage measurement circuit is simplified as in Figure 5.6.

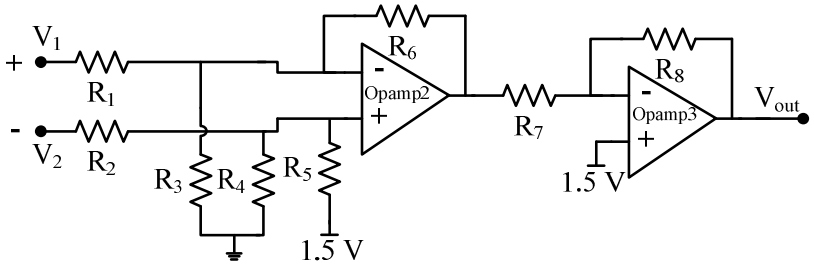

Figure 5.6 Simplified voltage measurement circuit

The assumption is made that $R_1=R_2$, $R_3=R_4$, $R_5=R_6$ and $R_7=R_8$. The output voltage of the measurement circuit can be calculated as follows:

$$V_{out} = 1.5 + \frac{R_5}{R_1}\left[V_1 - V_2\right] \tag{5.1}$$

The circuit coinciding with *opamp2* measures the voltage differentially and scales it down. Additionally an off-set of 1.5 V is added. The phase difference of 180º is removed by the inverting circuit of *opamp3*. A peak voltage of 400 V can be measured and is scaled down to a voltage between 0 V and 3 V that swings around 1.5 V. In Figure 5.7, the PCB of the voltage measurements is shown.

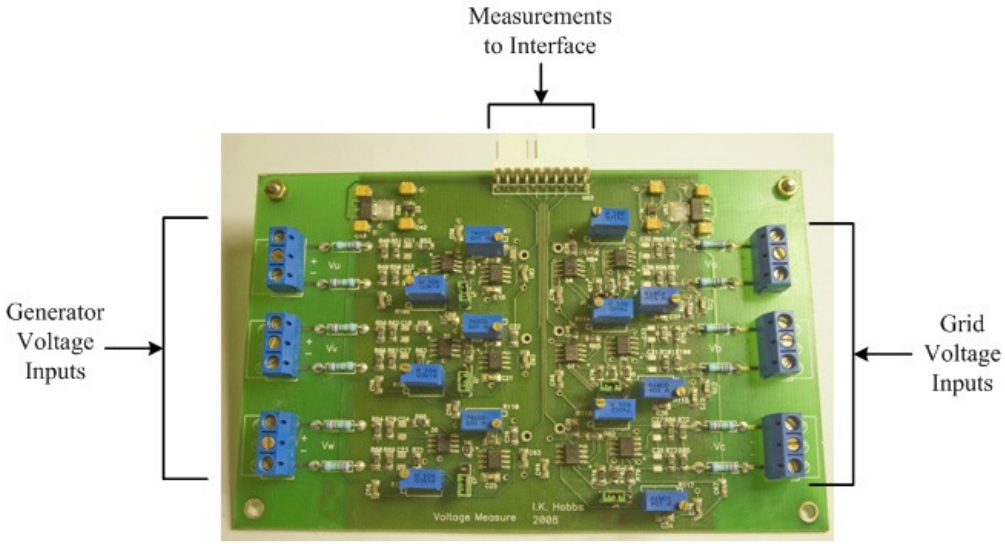

Figure 5.7 6-phase voltage measurement PCB

5.1.3 THE DSP INTERFACE

The interface board serve as the primary link between the DSP and the converter. All measurements and control signals are relayed via the interface board. Additional push-buttons and LEDs are included for debugging purposes. Figure 5.8 shows the interface board. The current measurements and DC bus measurements are scaled on the interface to be compatible with the ADC channels of the DSP.

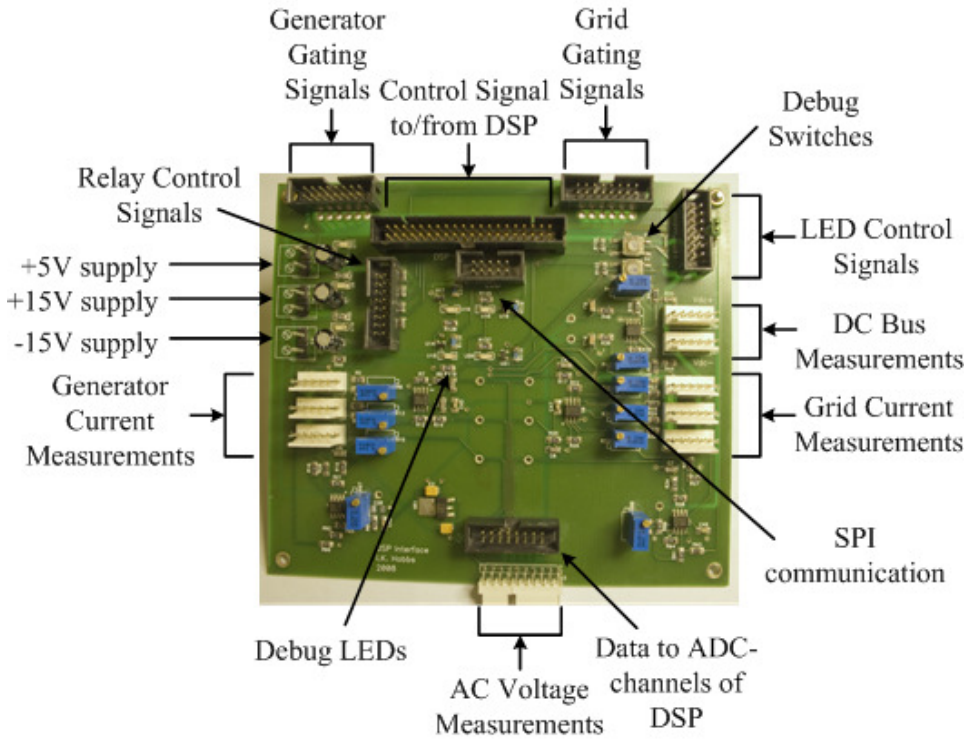

Figure 5.8 DSP-converter interface board

The power supply is connected to the interface from where the power is redistributed to components like the current transducers and LEDs. Additional test points are included to aid in debugging or verifying signals. Serial peripheral interface (SPI) communication is available should communication to external devices be required.

A 2N2222A transistor is used to drive the debugging LEDS and to protect the general purpose input and output (GPIO) pins of the DSP. The absolute maximum current rating for the GPIO pins is 2 mA while the amount of current required by the LEDs is between 10 mA and 20 mA, depending on the desired brightness. By using these transistors less current is drawn from the DSP, reducing the risk of damage to the device. Figure 5.9 shows the driving circuit of the LEDs.

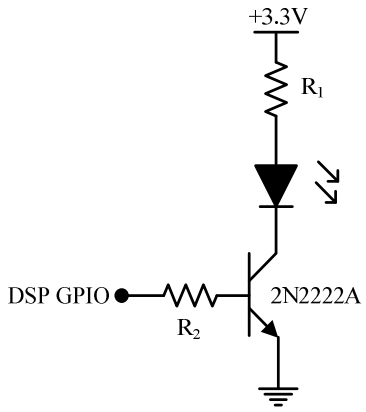

Figure 5.9 LED drive circuit

When R_1 is selected as 125 Ω and R_2 as 30 kΩ the current drawn from the DSP is 86 μA. The brightness of the LED is changed by selecting a different value for R_1.

The current measurements received from the existing system have an offset of 2.5 V and can swing between 0 V and 5 V. This is incompatible with the ADC channels of the DSP. The circuit shown in Figure 5.10 is used to scale the voltage down to an offset of 1.5 V swinging between 0 V and 3 V.

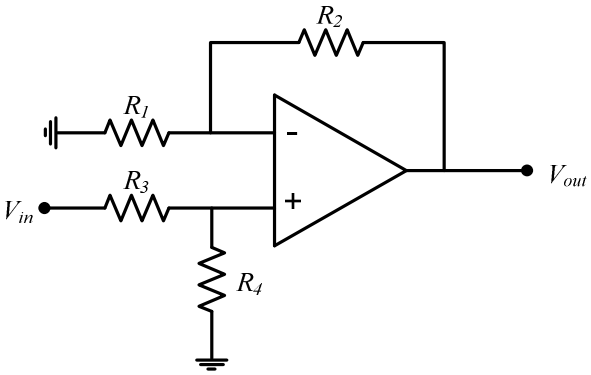

Figure 5.10 Current measurement scaling circuit

The transfer function of the scaling circuit is:

$$\frac{V_{out}}{V_{in}} = \frac{R_4}{R_1}\left[\frac{R_1 + R_2}{R_3 + R_4}\right] \tag{5.2}$$

By selecting $R_1 = R_3$ and $R_2 = R_4$ the transfer function is simplified to:

$$\frac{V_{out}}{V_{in}} = \frac{R_4}{R_1} \tag{5.3}$$

To convert 5 V to 3 V the ration between R_4 and R_1 is 0.6. The resistors selected is $R_1 = R_3 = 20\ k\Omega$ and $R_2 = R_4 = 12\ k\Omega$. The DC bus measurements are scaled using the same circuit.

5.1.4 THE LIQUID CRYSTAL DISPLAY

The LCD is used to display the status of the system and the measurements. In Figure 5.11, the LCD is shown. There are also LEDs to indicate the mode in which the system is. The control buttons are used to start and stop the system. The up and down buttons are used to scroll through the menu.

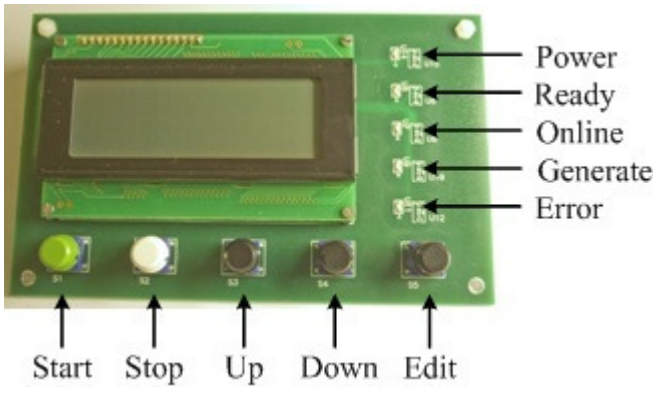

Figure 5.11 PCB of LCD

It is possible to edit some of the parameters in real time with the edit button. The LCD used is a MSC-C204DGLY-31W 4x20 character module from Truly. A SN74LS07 voltage translation chip is used to translate the output signal of the DSP of 0 - 3 V to be compatible with the input signals of the LCD, which is 0 - 5 V.

5.1.5 THE SOFT-START CIRCUIT

A soft-start resistor stage is added to protect the anti-parallel diodes of the IGBT modules and the DC bus capacitors. This limits the inrush currents when the converter is initially connected to the grid. Figure 5.12 shows the layout of the soft-start circuit.

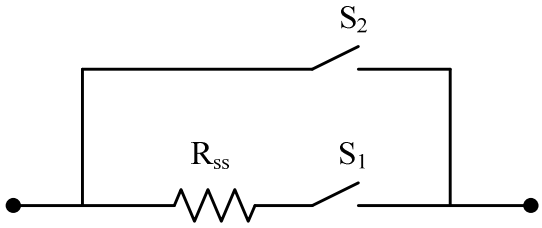

Figure 5.12 Soft-start circuit layout

Initially, when the converter is turned on, the DC bus is discharged. Should the converter be connected directly to the grid, the peak inrush current will be over 600 A for a 4700 µF bus capacitance. Although this peak current occurs for only a short time, it can cause damage to the anti-parallel diodes or other components of the converter. The peak inrush current is therefore reduced by first charging the DC bus through R_{ss}. A 47Ω, 50 W resistor is used to limit the inrush current to less than 15 A.

Two options can be implemented, but the method selected will depend on the rating of the IGBT module and the resistors. In the first method, S_1 is initially closed with the PWM signals disabled. The bus voltage is measured until a preset value is reached. This value will typically be the maximum value that the bus can be charged to through the resistors. Once this value is reached, S_1 is opened and S_2 is closed. If there is a voltage drop over the resistor, a current spike will occur when S_2 is closed, but it will be much less than in the case when directly connecting to the grid. Once S_2 is closed, the PWM signals can be enabled and the DC bus is charged to the reference value.

In the second method, S_1 is also initially closed. Once a preset value for the bus is reached, the PWM signals are enabled. The DC bus is charged through the resistors to

the reference value or a value close to it. Once this value is reached, S_2 is closed, thereafter S_1 is opened.

Although both methods work well, the second method can damage the resistors if there should be a problem during the charge procedure, or if the current limit is set too high. The first method is therefore implemented.

5.1.6 THE GENERATOR SETUP

The generator side of the converter consists of a DC machine driving an alternator. The DC machine used is a *Bruce Peebles & Co* with a rating of 10.8 kW. The alternator is a *Markon* brushless alternator with a rating of 20 kVA.

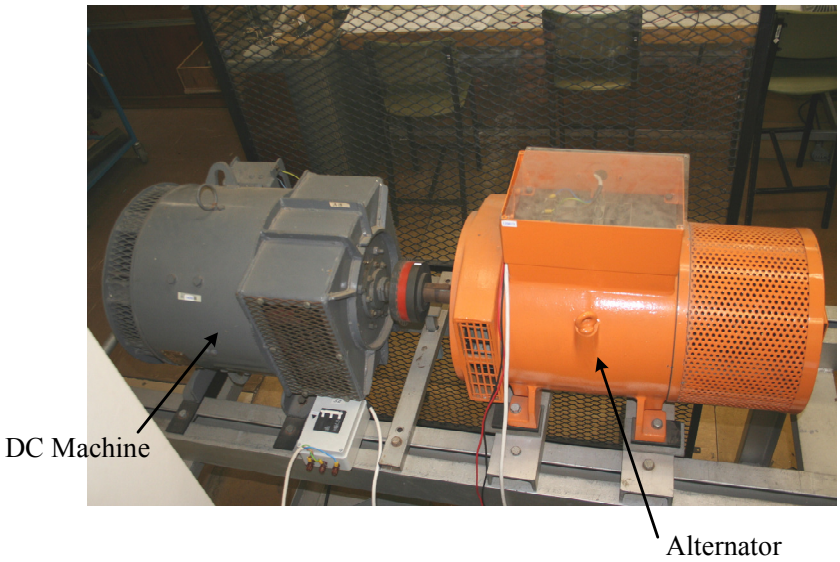

Figure 5.13 DC machine and alternator setup

By adjusting the input power to the DC machine, the maximum amount of power that can be extracted from the generator is varied.

5.2 SOFTWARE DESCRIPTION

In this section, the software development is discussed. The software is included on a CD at the back of the thesis.

5.2.1 OPERATIONAL MODES

The software to operate the DSP is written in *Code Composer Studio* from Texas Instruments. To ensure that the converter functions correctly, 5 modes of operation are

implemented. These modes are subdivided into different states, depending on the complexity of the mode. Figure 5.14 shows the mode transition diagram of the software. A mode transition is initiated either by a system condition or from a user input.

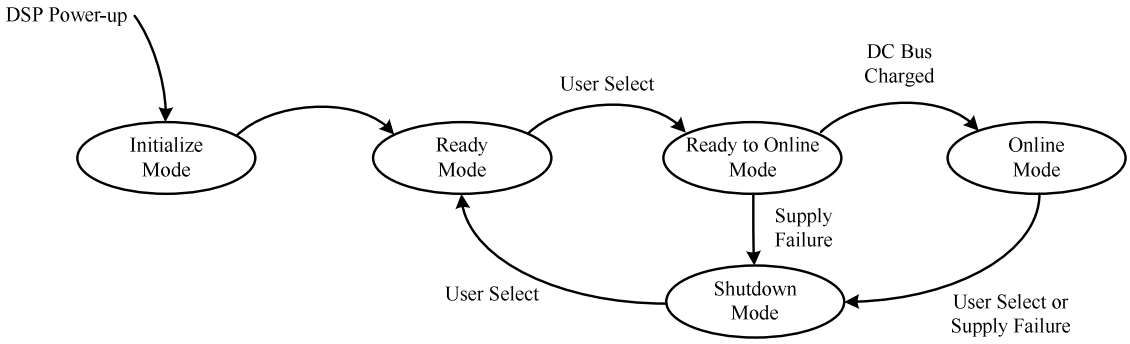

Figure 5.14 Controller modes and transitions

An endless *for-loop* is used in *main.c* to keep the DSP running. In the *for-loop* the function *Mode()* executes the current mode and its state(s).

5.2.1.1 INITIALIZE MODE

The DSP starts up in the initialize mode. The code for this mode is located in *mInit.c*. The GPIO pins are assigned and the ADC configured. A timer is configured for accurate timing purposes. The function *LCD_setupIO()* configures and initializes the LCD. After the state transitions for this mode are complete, an automatic mode transition is done to the ready mode.

5.2.1.2 READY MODE

This is an idle mode for the converter. The DSP is configured and waiting for a user input. By pressing the *start* button on the LCD a mode transition is executed to the ready-to-online mode.

5.2.1.3 READY-TO-ONLINE MODE

The soft-start procedure explained in Section 5.1.5 in executed in this mode. The code for this mode is located in *mReadyOnline.c*. Figure 5.15 shows the flow diagram of the ready to online mode.

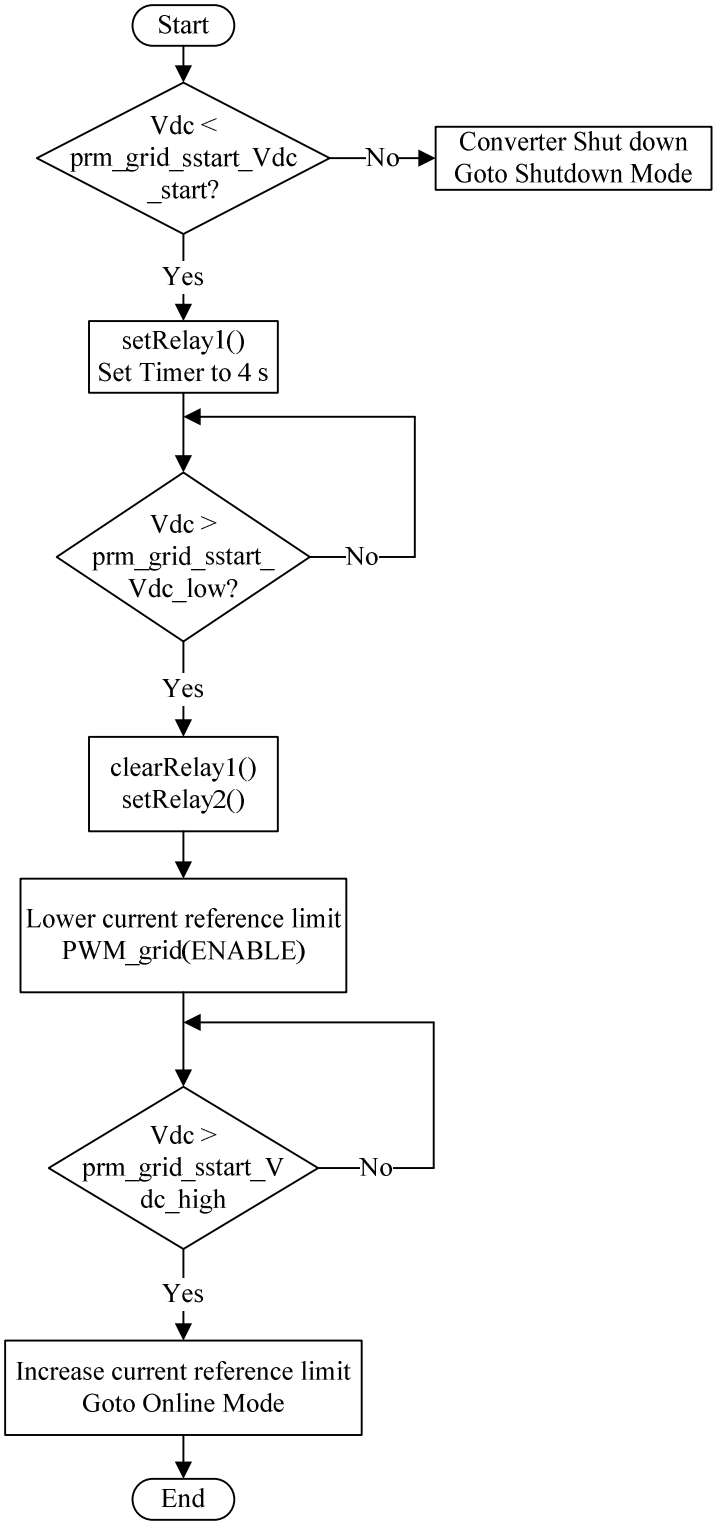

Figure 5.15 Flow diagram of the *ready-to-online* mode

As a safety feature, the converter is shut down if the DC bus voltage is above *prm_grid_sstart_start*, set at 200 V, before the procedure starts. The converter is connected to the grid through the soft-start resistors by calling *setRelay1()*. A timer is set to limit the time allowed for the DC bus to charge through the resistors. A timeout error

event occurs if the DC bus does not charge above *prm_grid_sstart_low*, set at 520 V, within 4 s of connecting to the grid. After the limit is reached, the resistors are disconnected from the grid by calling *clearRelay1()* and the converter is connected directly to the grid by calling *setRelay2()*. The limit of the current reference is lowered to 4 A_{peak} and the PWM signals are enabled. The DC bus is charged to *prm_grid_sstart_high*, set at 750 V, after which the current limit is increased and the transition to online mode is executed.

The supply is monitored during the entire charge procedure by calling *CheckSupply()*. The converter goes into shutdown mode if there is a supply failure during the soft-start procedure.

5.2.1.4 ONLINE MODE

Upon entering this mode the converter is already synchronized with the grid and the DC bus voltage is regulated. The generator is connected and the PWM signals are enabled. Power drawn from the generator is delivered into the grid via the DC link. In this mode the frequency and voltage levels of the supply are monitored. The converter remains in this mode until the *stop* button on the LCD is pressed or an error occurs, in which case the converter goes into shut-down mode.

5.2.1.5 SHUT-DOWN MODE

The shut-down mode is invoked if any error occurs during the operation of the converter. This mode can also be entered manually by pressing the *stop* button on the LCD. In this mode, all PWM signals are disabled and the contactors are opened. An error code is displayed on the LCD screen, refer to Appendix A. for a list of the error codes. Shut-down mode is entered by calling *ErrorCrytical(type_Err ErrCode).*To exit shut-down mode, the user must first acknowledge the error by pressing the *start* button on the LCD, which places the converter in ready mode again.

5.2.2 ADC CONFIGURATION

The ADC module of the DSP is configured when the converter is in initialize mode. The functions to configure the ADC are located in the *setupADC.c* file. *InitAdc()* is called first to power up the ADC module and the reference circuitry. A 5 ms delay is included

to give all the analog circuitry time to power up and settle. Function *configADC()* maps the input pins of the ADC to the result registers and configures the sequencer of the ADC. The sequencer is configured to operate in dual mode with two 8-state sequencers, SEQ1 and SEQ2. Measurements on the grid side are mapped to SEQ1 and the generator measurements are mapped to SEQ2. The start of conversion (SOC) signal is received from the PWM module and an interrupt is generated at the end of the conversion sequence. The acquisition window size is set to 240 ns. This is the time during which the sampling switch remains closed before completing the conversion of the input voltage.

In *serviceADC()* the sampled values are read from the result registers and converted into their corresponding real-time values. These measured values are then stored in the corresponding variables located in *variables.c*.

5.2.3 PWM CONFIGURATION

The 6 PWM modules are configured to generate the 10 kHz switching signals. The configuration functions are called from the *setupEPWM.c* file. The counter mode of the PWM modules is set to up-down (see Figure 4.12). This means that during one modulation period the counter increases to the value set in the TBPRD register and then decreases to zero. The clock of the DSP is sub-divided by two and the TBPRD register is set at 3750 to give a modulation period of 100 µs. Dead time of 2 µs is inserted for the reasons explained in Section 4.4. PWM modules 1-3 are synchronized and PWM 4-6 are synchronized, but shifted 180º relative to modules 1-3. This is done to separate the control calculations of the two sides of the converter.

The SOC signal for SEQ1 of the ADC module is generated by PWM4 and by PWM1 for SEQ2. The signal is generated when the counter is equal to 3750, thus 50 µs into the modulation period.

The short-circuit protection output of the IGBT modules is connected to the trip zone (TZ1 and TZ2) inputs of the DSP. A low input on either of these pins will force all the PWM signals into a low state and generate an interrupt. To recover from this state the DSP must either be reset or manually cleared by writing a 1 to the TZCLR register. The

trip zone inputs must remain low for at least three clock cycles to be valid. The aim of this is to prevent false trips that can be generated by switching noise.

5.2.4 GRID SIDE INTERRUPT PROCEDURE

This interrupt is invoked after the conversion of the sampled data on the grid side is complete; the function name for this interrupt is *GRID_isr(void)*. Figure 5.16 shows the function flow diagram of the grid side interrupt service routine. These functions are included from the source files through header files containing the function declarations.

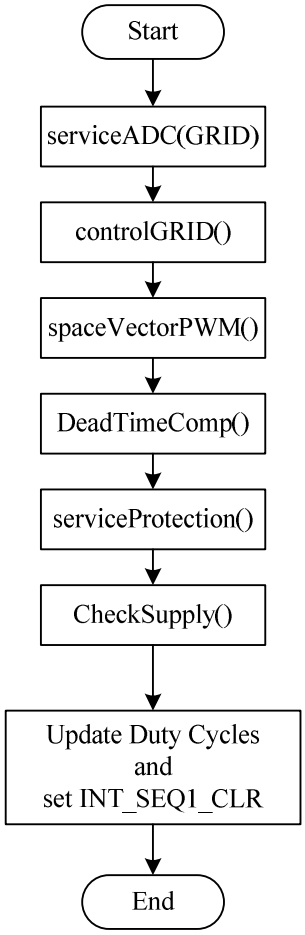

Figure 5.16 Function flow diagram of grid interrupt service routine

The function *serviceADC(GRID)* converts the sampled data on the grid side into real-time data. The function *controlGRID()* located in *controlCalc.c* is called next. Figure 5.17 illustrates a flow diagram of this function. The code of this function is in Appendix B.

The measured phase voltages and currents are converted to the $\alpha\beta$-plane using (4.6). The magnitude of the vectors is calculated as follows:

$$\left|\overline{x_{\alpha\beta}}\right| = \sqrt{x_\alpha^2 + x_\beta^2} \tag{5.4}$$

The alpha phase voltage is monitored for zero crossings. The frequency is calculated by counting the number of interrupts that occur between each zero crossing and using the fixed interval of the interrupt. In the case of a 50 Hz grid, the counter will be at 100 after a half-cycle. For a valid zero crossing to occur the counter must be larger than 50. If a zero crossing occurs when the counter is at less than 50, it is considered invalid and no action is taken.

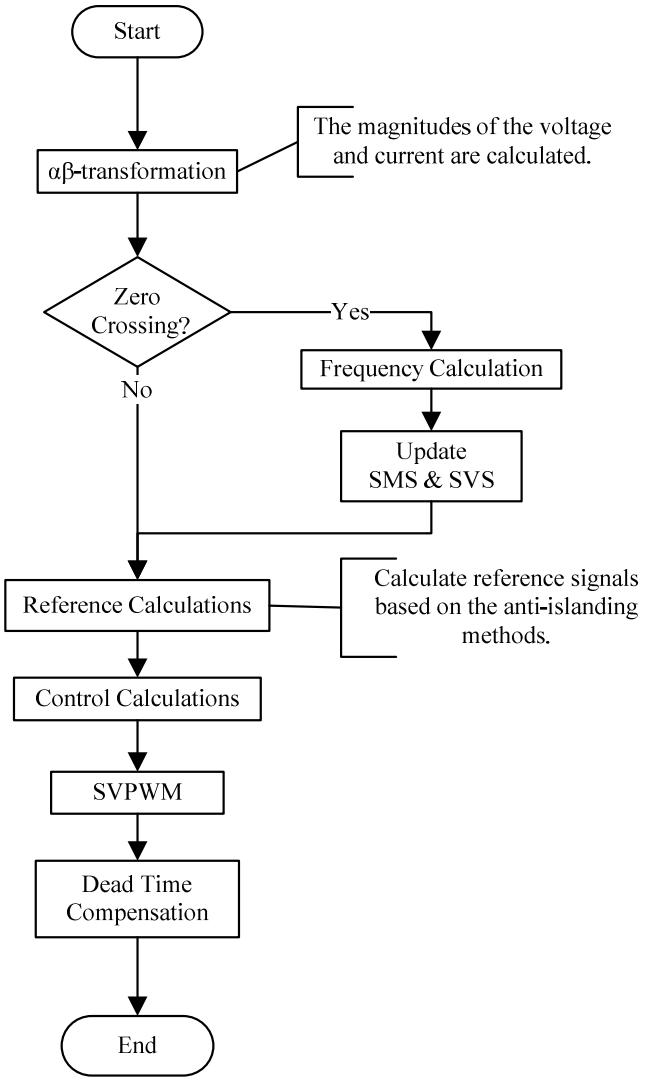

Figure 5.17 Flow diagram of the function *controlGRID()*

The phase angle of the SMS method is updated when a zero crossing from the negative half-cycle to the positive half-cycle occurs. The new phase angle is calculated using (3.13). The absolute value of the error between the measured frequency and nominal grid frequency is used to force the direction of the frequency drift upwards. The amplitude reference of the SVS method is updated at every zero crossing. This reference amplitude is calculated using (3.23).

The converter is synchronized with the grid by using the measured voltages to generate the per unit reference signals. For the base case implementation the alpha and beta components of the measured voltage are divided by the voltage magnitude calculated by using (5.4). This yields per unit reference signals that are in phase with the grid voltage. The SMS method is implemented by using the rotation matrix as explained in Section 4.5 to generate the per unit reference signals. The SVS method is implemented by scaling the reference signals used in the base case implementation.

The instantaneous active and reactive power is calculated by using the instantaneous alpha and beta components of the measured voltage and current. The calculations are as follows:

$$\begin{aligned} P &= 0.6666(V_\alpha I_\alpha + V_\beta I_\beta) \\ Q &= 0.6666(V_\alpha I_\beta - V_\beta I_\alpha) \end{aligned} \tag{5.5}$$

The measurements are scaled by 0.6666, because the alpha and beta components are 1.5 times larger than the actual values (see Section 4.3.1).

The control calculations are done as explained in Sections 4.3.3 and 4.3.4. To calculate the duty cycle for each phase the function *spaceVectorPWM()* is called. Compensation for the dead time is done in *DeadTimeComp()*.

The function *serviceProtection()* uses the sampled values to determine if the converter is within the compatibility levels. *CheckSupply()* monitors the grid voltage magnitude and frequency. If either of these values falls outside the specified limits of the grid, the converter is shut down.

Finally, the duty cycles are updated and the interrupt flag cleared to acknowledge the interrupt and allow further interrupts to occur.

5.2.5 GENERATOR SIDE INTERRUPT PROCEDURE

This interrupt is invoked after the conversion of the sampled data on the generator side is complete; the function name for this interrupt is *GEN_isr(void)*. Figure 5.18 is a flow diagram of the functions called during the interrupt. These functions are included from the source files through header files containing the function declarations.

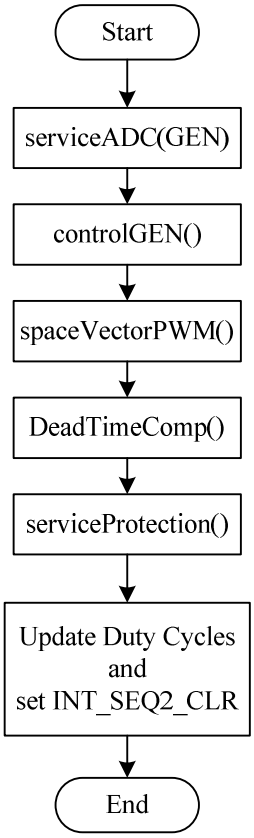

Figure 5.18 Function flow diagram of generator interrupt service routine

In *serviceADC(GEN)* the sampled data is retrieved from the result registers and converted to the real-time data. The flow diagram of the function *controlGEN()* is shown in Figure 5.19. The code for this function is given in Appendix B. The phase voltages and currents are converted to the $\alpha\beta$-plane using (4.6) and the magnitudes calculated using (5.4). The frequency of the voltage is calculated in the same way as explained in Section 5.2.4 and the active and reactive power measurements are calculated using (5.5).

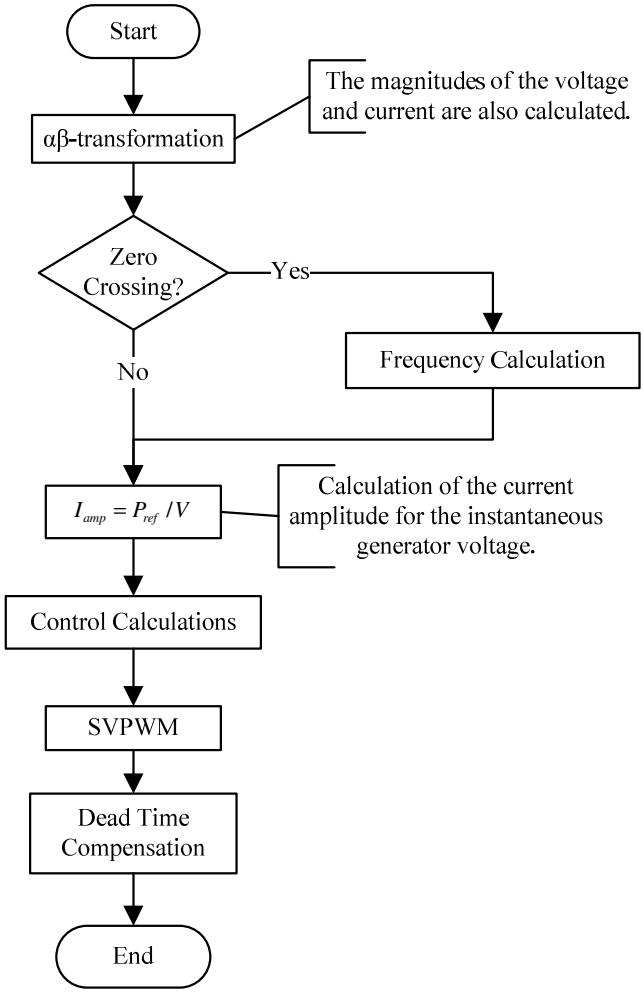

Figure 5.19 Flow diagram of the function *controlGEN()*

The per unit reference signals, with unity power factor, are generated by dividing the measured alpha and beta voltages by their magnitude. The reference current amplitude is calculated by dividing the power reference by the measured output voltage of the generator.

The control calculations are done as explained in Sections 4.3.3 and 4.3.4. To calculate the duty cycle for each phase, the function *spaceVectorPWM()* is called. Compensation for the dead time is done in *DeadTimeComp()*.

In *serviceProtection()* the voltages of the bus capacitors and measured current amplitude are checked. If these values are outside the safe compatibility levels, the converter is shut down.

The duty cycles are updated and the interrupt flag cleared before the interrupt service routine is completed.

5.2.6 DIGITAL LOW-PASS FILTERING

To filter out noise on the measurements a digital low-pass filter is implemented. This filter is only implemented on DC values and not on the AC voltages and currents. The primary use of the filter is for the measurements displayed on the LCD screen and for adjusting the response time of the anti-islanding methods. A digital version of a low-pass RC filter is used, as shown in Figure 5.20.

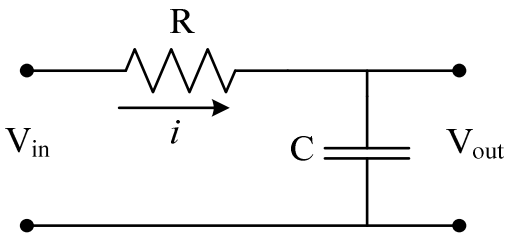

Figure 5.20 Model of digital low-pass filter.

To determine the cut-off frequency of the filter the following equation is used:

$$f_0 = \frac{1}{2\pi RC} \tag{5.6}$$

The instantaneous voltage over the resistor is as follows:

$$V_R = V_{in}(t) - V_{out}(t) = Ri(t) \tag{5.7}$$

The instantaneous current through the capacitor, which is the same as the current through the resistor, is:

$$i_C(t) = C\frac{dv_C(t)}{dt} \tag{5.8}$$

It is now possible to substitute (5.8) into (5.7) as follows:

$$v_{in}(t) - v_{out}(t) = RC\frac{dv_{out}(t)}{dt} \tag{5.9}$$

Because the filtering is done within the interrupts, the samples are taken at a fixed, evenly spaced interval. The discrete version of (5.9) is as follows:

$$v_{in}(k) - v_{out}(k) = RC\frac{v_{out}(k) - v_{out}(k-1)}{\Delta T} \tag{5.10}$$

where ΔT is the sampling period. By rearranging the terms the discrete filter output can be written as:

$$v_{out}(k) = v_{in}(k)\left[\frac{\Delta T}{RC + \Delta T}\right] + v_{out}(k-1)\left[\frac{RC}{RC + \Delta T}\right] \tag{5.11}$$

The discrete implementation of a RC low-pass filter is essentially a weighted moving average, which can finally be expressed as:

$$v_{out}(k) = \alpha v_{in}(k) + (1-\alpha) v_{out}(k-1) \tag{5.12}$$

where

$$\alpha = \frac{\Delta T}{RC + \Delta T} \tag{5.13}$$

The low-pass filter cut-off frequencies vary depending on their requirements, and they are implemented accordingly.

5.2.7 LCD MENU STRUCTURE

The menu structure of the LCD is shown in Figure 5.21. The general layout is stored in an array with only the relevant data updated periodically. By pressing the *up* and *down* buttons on the display, it is possible to scroll through the menu of the LCD. The DC reference voltage and anti-islanding settings can be edited while the converter is running by pressing the *edit* button in the relevant menu item. The parameter, which is currently active for editing, is indicated by a >. To modify the parameters the *up* and *down* buttons are used, and to switch between parameters the *edit* button is used.

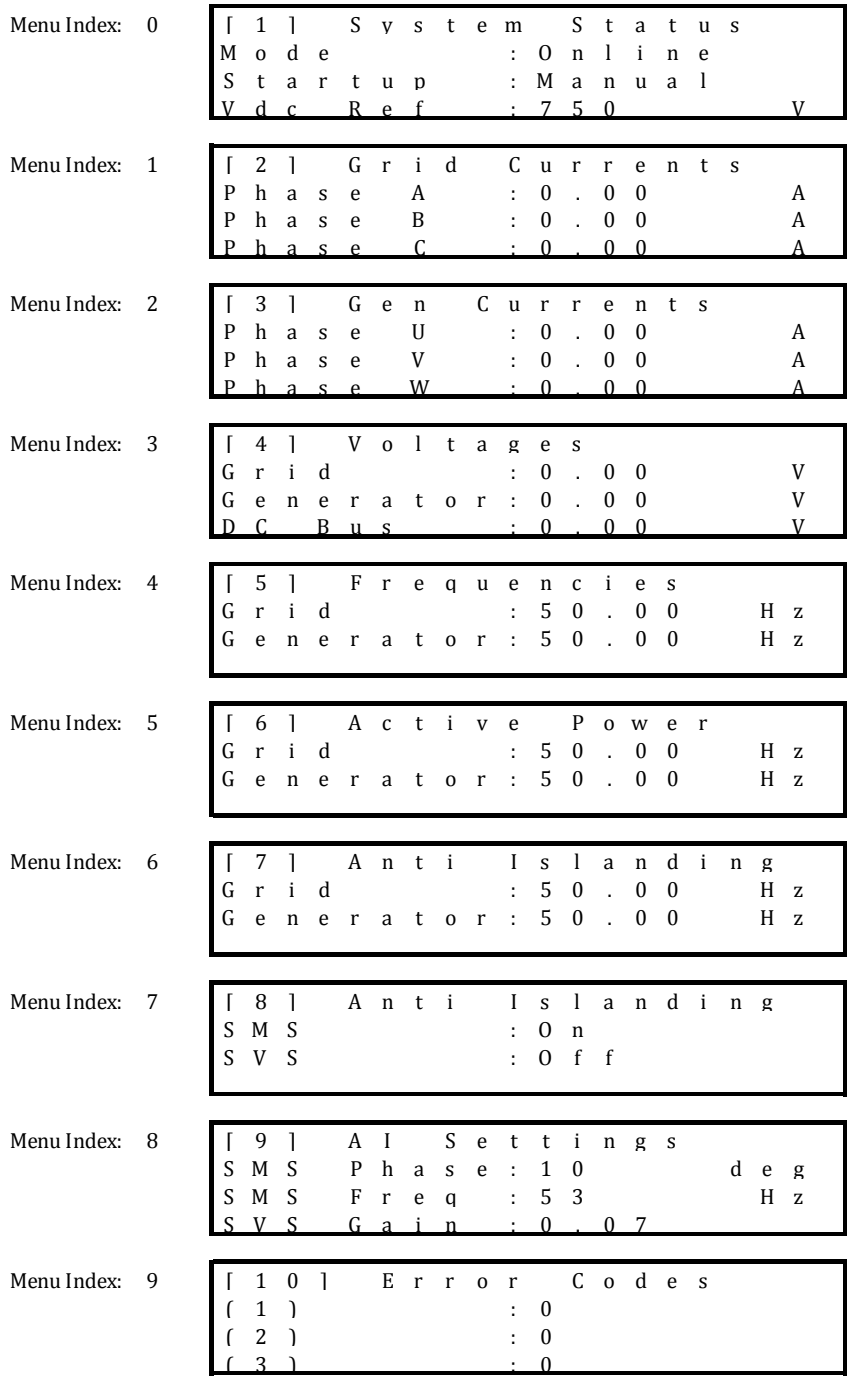

Figure 5.21 LCD menu structure.

5.3 SUMMARY

In this chapter, the hardware and software used to test the anti-islanding methods practically were developed. The existing hardware was discussed as well as the additional hardware designed in this thesis. The development of the software used to control the converter was described. An overview of the operational modes of the

converter was given, along with the configuration of the ADC and PWM modules of the DSP. This was followed by flow diagrams of the interrupts where the control loops of the converter are executed.

The design and implementation of a digital low-pass filter was discussed in detail. This filter was used to filter out switching noise on the measured values and to adjust the response time of the anti-islanding methods.

CHAPTER 6. EXPERIMENTAL RESULTS

In this chapter, the simulated results of Chapter 4 are verified experimentally. The hardware and software described in Chapter 5 are used for the verification purposes. Parameters of the actual system are listed in Table 4.4. Measurements were taken using a Tektronix TDS 3014 oscilloscope. The voltage measurements were taken with a Tektronix P5205 100 MHz high voltage differential probe, whereas a Tektronix TCP202 current probe was used for current measurements.

6.1 TESTING OF THE DC BUS REGULATOR

In Figure 6.1, the soft-start procedure and regulation of the DC bus are illustrated. The inductor current and DC bus voltage are shown. At the start of period A, the DC bus is discharged. After connecting to the grid through the resistors, the current decreases as the DC bus is charged. At the end of period A, the DC bus is charged to 525 V. The soft-start resistor is now disconnected and the converter is connected directly to the grid. Due to the voltage drop over the soft-start resistor, there is still some in-rush current when the converter is connected directly to the grid. By the end of period B, the DC bus is charged to 565 V. The PWM signals are enabled at the start of period C. This boost charges the bus to the reference voltage of 750 V. Once the reference voltage has been reached, the bus is regulated to maintain this voltage.

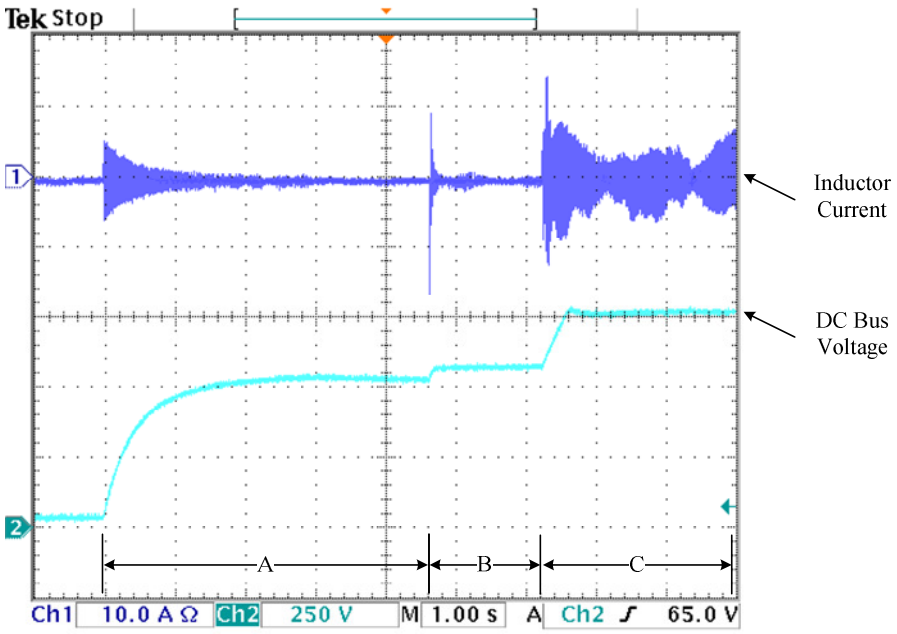

Figure 6.1 Soft-start of converter and DC regulation

6.2 TESTING OF THE ACTIVE RECTIFIER

The active rectifier is tested with the maximum power reference step of 0 kW to 3.3 kW. In Figure 6.2, the results of this test are shown, indicating the inductor current and generator voltage. The point in time where the power reference step occurs is also indicated. The current amplitude changes almost instantaneously to track the power reference. Because of the increased torque on the generator, it slows down and the output voltage decreases. By increasing the current amplitude as the voltage drops, the power reference is tracked.

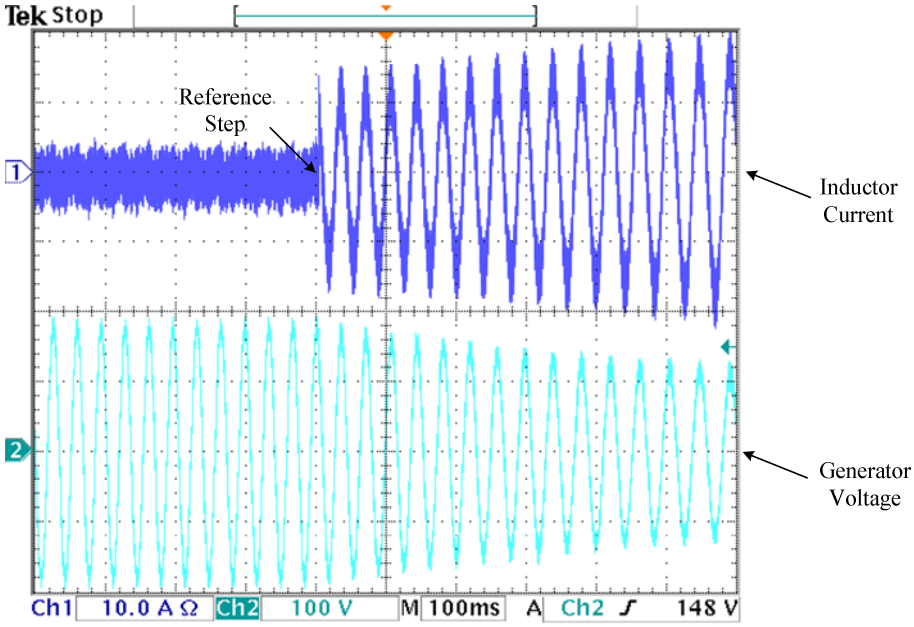

Figure 6.2 Active rectifier test with reference step from 0 kW to 3.3 kW

In Figure 6.3, the power reference is kept fixed at 2 kW, while the output voltage of the generator is varied. The inductor current and generator voltage are indicated. As the output voltage of the generator is increased, the current amplitude decreases to track the power reference.

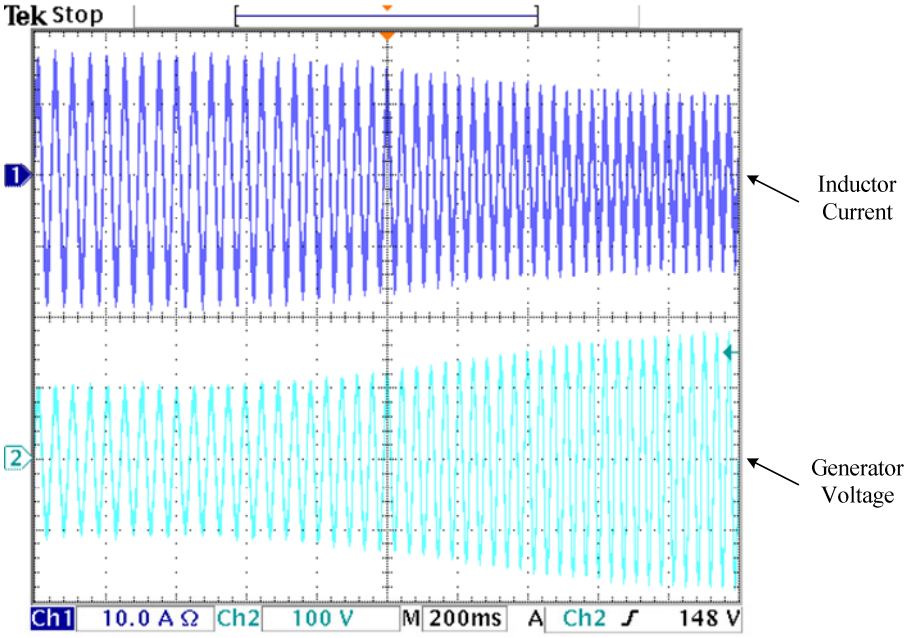

Figure 6.3 Active rectifier test with fixed reference and varying voltage

These above tests show that the active rectifier can track the power reference under either a reference step or varying voltage conditions.

6.3 TESTING OF ANTI-ISLANDING METHODS

In this section, the anti-islanding methods are verified experimentally. A base case is tested to verify that an island is successfully formed and continuously energized once disconnected from the grid with no anti-islanding method implemented. The RLC load used to test the anti-islanding methods depicted in Figure 6.4.

Figure 6.4 RLC test load

By changing the resistance, inductance and capacitance, the quality factor and resonant frequency of the load are varied.

6.3.1 TESTING OF A LOAD WITH $Q_F = 1.39$

The parameters for the load in this test are listed in Table 6.1.

Table 6.1 Parameters of test load with $Q_f = 1.39$

Parameter	Value
L_{load}	100.7 mH
R_{load}	45.15 Ω
C_{load}	81.526 µF
C_{filt}	13.3 µF
Q_f	1.3856
f_0	51.51 Hz

The base case test result is shown in Figure 6.5. After disconnecting from the grid at the indicated time, the amplitude of the PCC voltage remains nearly unchanged. The filtered frequency of the PCC voltage is shown in Figure 6.6. The time at which the grid is disconnected is indicated with a dashed line. The frequency of the voltage is calculated in MATLAB by determining the intervals between the zero crossings of the voltage. After disconnecting from the grid, the voltage and frequency remain within the compatibility levels of the grid.

The calculated resonant frequency of the load is outside the compatibility levels of the grid, although the load resonates within the limits. This can be ascribed to the additional in-circuit capacitance that cannot be measure once the load is connected. Only an additional 5 µF of in-circuit capacitance is required for the load to be within these levels.

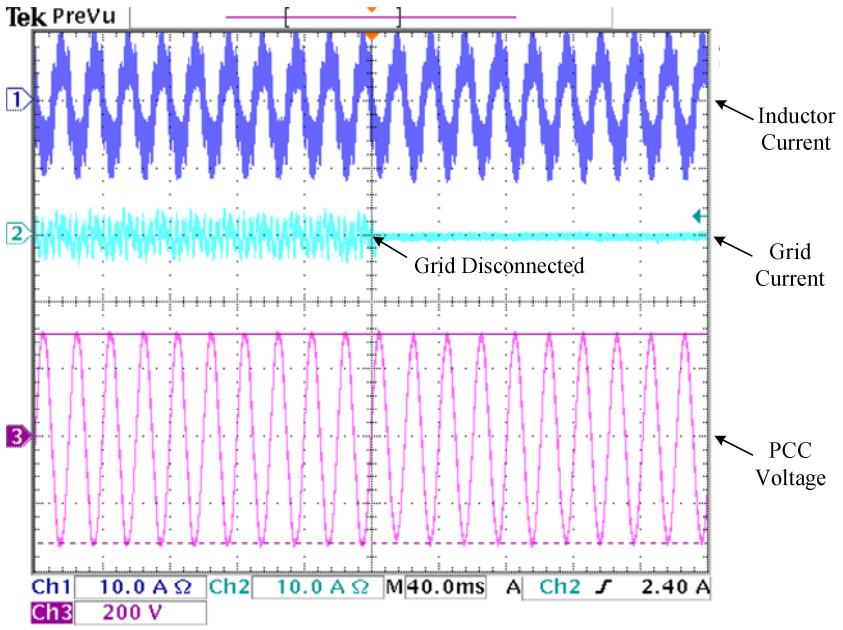

Figure 6.5 Base case test for load with $Q_f = 1.39$

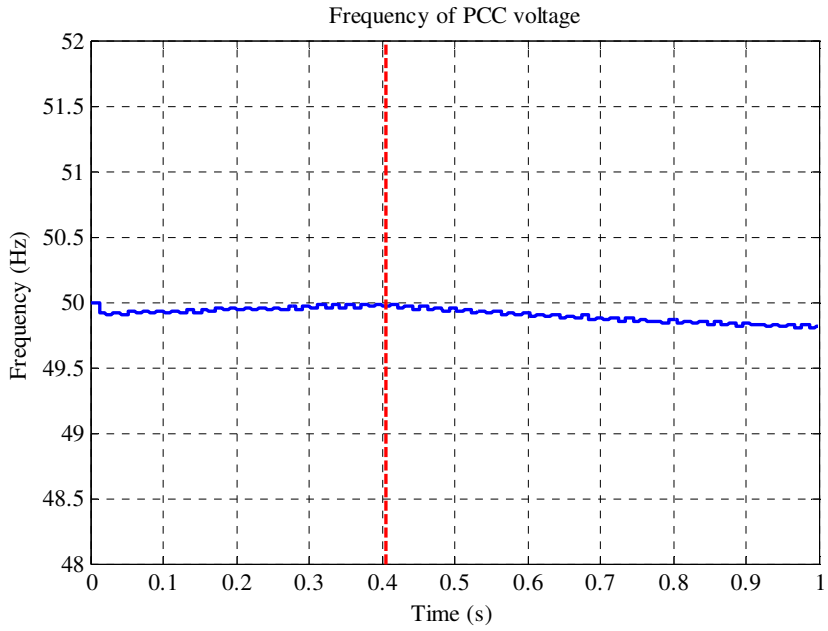

Figure 6.6 Filtered PCC voltage frequency for base case test load with $Q_f = 1.39$

The SMS method is implemented to drive the frequency of the PCC voltage outside the compatibility levels of the grid, once an island is formed. In Figure 6.7 the inductor current, grid current and PCC voltage are shown. The filtered frequency of the PCC voltage is shown in Figure 6.8.

The frequency measurement has a low-pass filter with cut-off frequency of 160 Hz. The maximum phase deviation is set at 11° and the maximum frequency to 53 Hz.

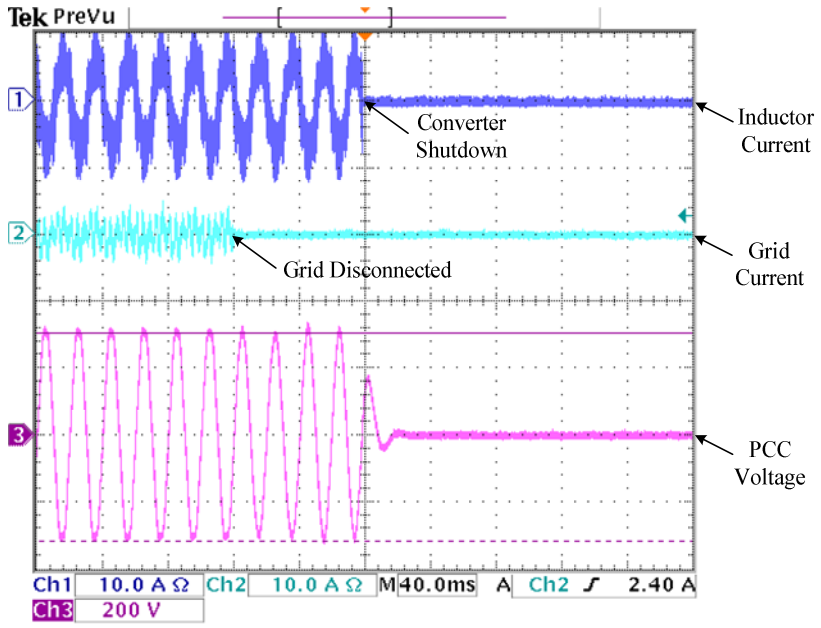

Figure 6.7 SMS test for load with Q_f = 1.39

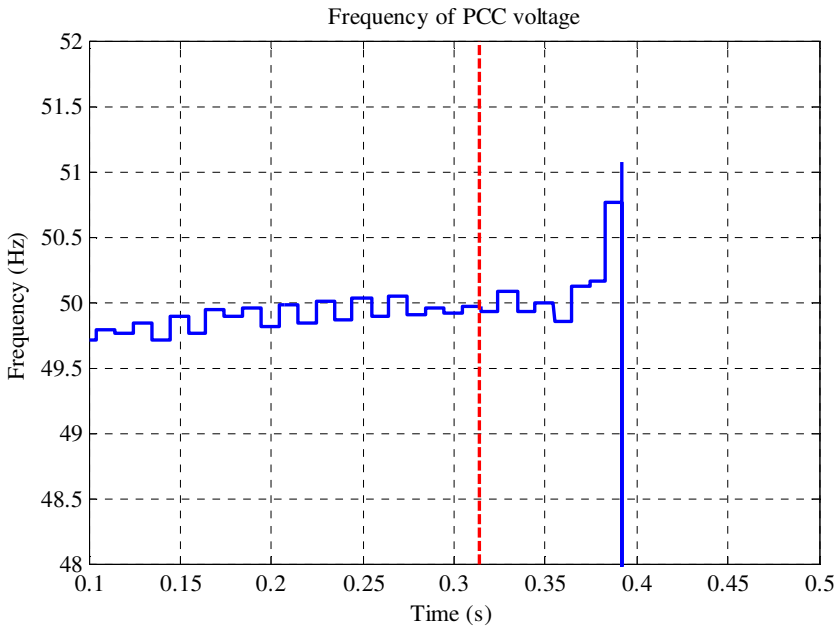

Figure 6.8 Filtered PCC voltage frequency for SMS test load with Q_f = 1.39

The frequency trip levels of the converter are set at 49 Hz and 51 Hz. The points where the grid disconnects and the converter shuts down are indicated. It takes approximately 80 ms for the frequency of the voltage to drift outside the frequency limits after disconnecting from the grid. The cut-off frequency of the low-pass filter is lowered to 16 Hz. Figure 6.9 shows the inductor current, grid current and PCC voltage with the adjusted filter. The filter frequency of the PCC voltage is shown in Figure 6.10, with the disconnection interval indicated by a dashed line.

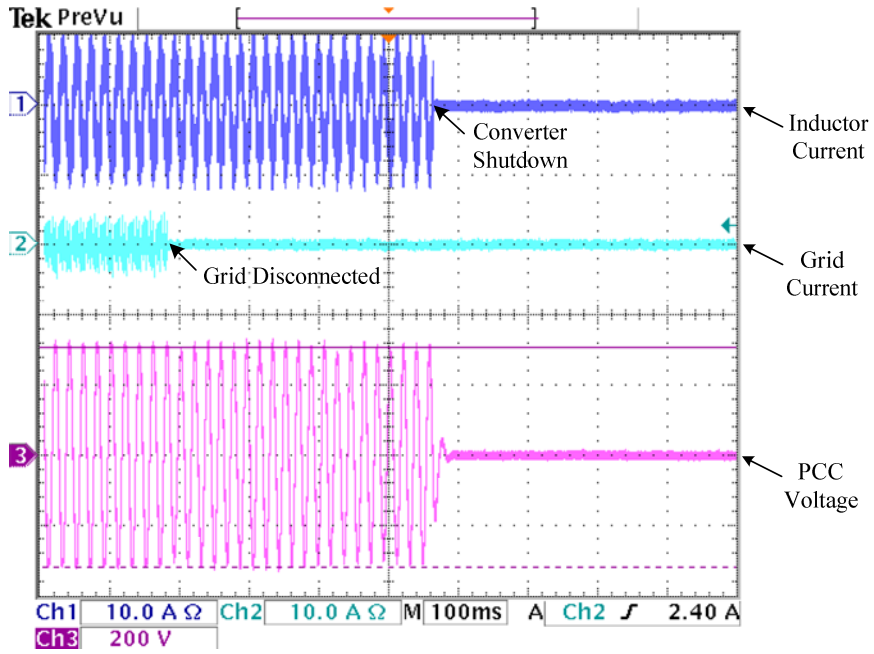

Figure 6.9 SMS test for load with $Q_f = 1.39$ and adjusted filter

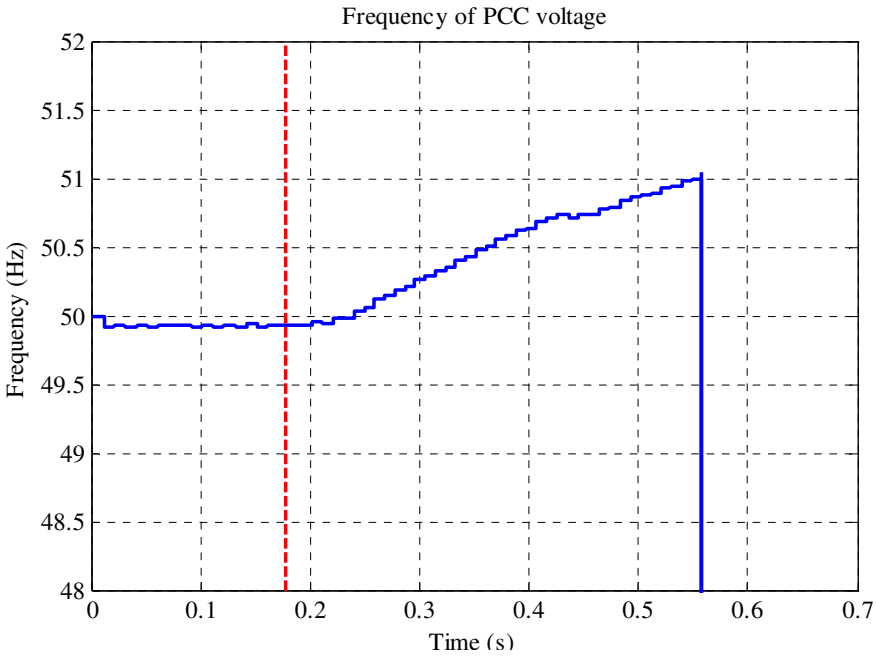

Figure 6.10 Filtered PCC voltage frequency for SMS test load with $Q_f = 1.39$ and adjusted filter

Energizing of the island is still prevented, but the shutdown time has increased to 380 ms. Adjusting the cut-off frequency of the low-pass filter, changes the response time of the SMS method.

During both SMS tests, the voltage amplitude remained within the compatibility levels of the grid.

The test result for the SVS is shown in Figure 6.11. The low-pass filter used on the voltage measurement has a cut-off frequency of 25 rad/s. The gain is set at 0.1 and the change in the reference is limited to 0.4 per unit and 1.9 per unit. The trip limits of the voltage are set at 207 V and 253 V. To prevent nuisance trips under normal operation the converter was set to trip if the voltage is outside the trip limits for four consecutive cycles.

After disconnecting from the grid, the amplitude of the current reference is decreased until it reaches its minimum limit. The converter is shut down approximately 80 ms after disconnecting from the grid.

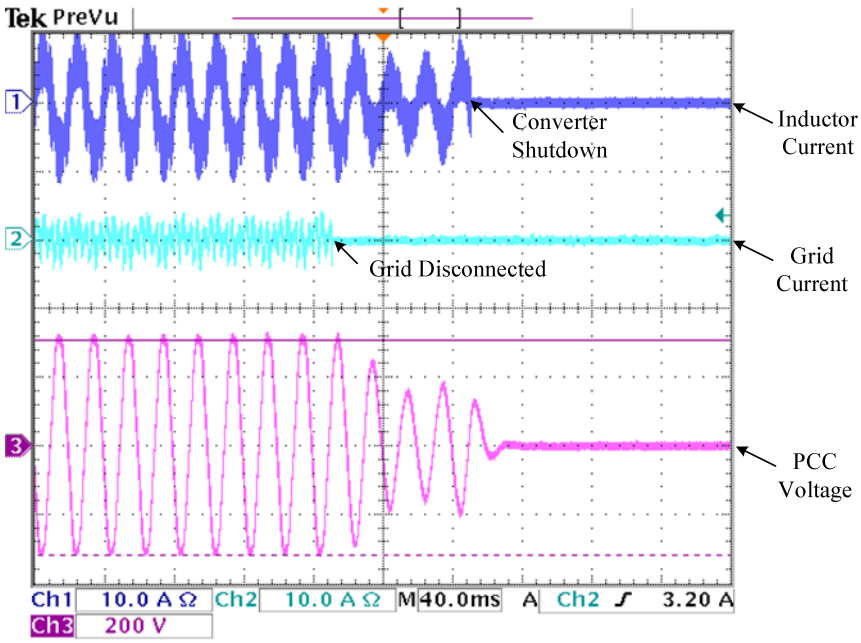

Figure 6.11 SVS test for load with $Q_f = 1.39$.

In both cases, the energizing of an island is prevented by either driving the voltage frequency or the amplitude outside the compatibility levels.

6.3.2 TESTING OF A LOAD WITH Q_F = 1.98

The parameters for the load in this test are listed in Table 6.2.

Table 6.2 Parameters for test load with Q_f = 1.98

Parameter	Value
L_{load}	73.9 mH
R_{load}	46 Ω
C_{load}	123.5 µF
C_{filt}	13.3 µF
Q_f	1.98
f_0	50.05 Hz

The inductor current, grid current and PCC voltage for the base case test are shown in Figure 6.12. After disconnecting from the grid at the indicated point in time, the voltage remains within the limits in terms of the amplitude and frequency. The filtered frequency of the PCC voltage is shown in Figure 6.13. Since no anti-islanding method is implemented, the converter continues to energize the local load. The trip levels of the frequency protection are set at 49 Hz and 51 Hz, and the voltage protection levels are set at 207 V and 253 V.

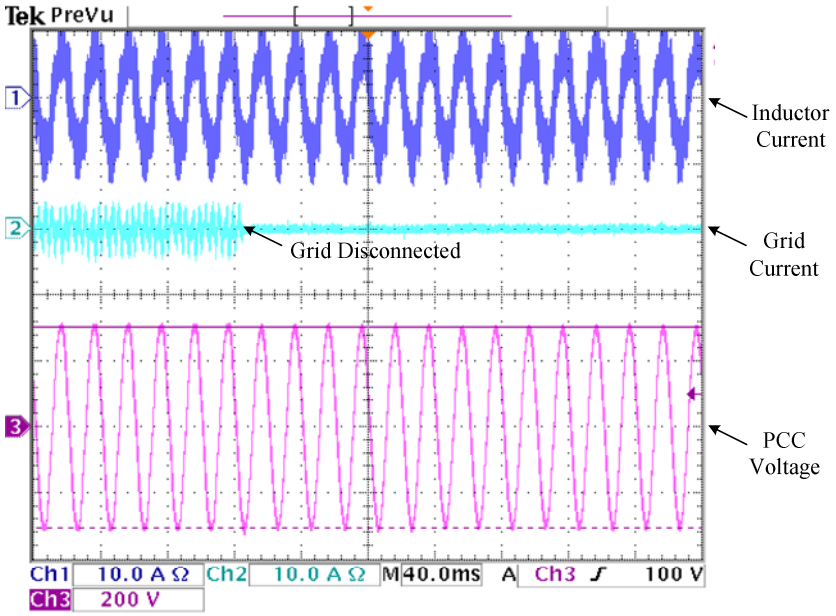

Figure 6.12 Base case test for load with Q_f = 1.98

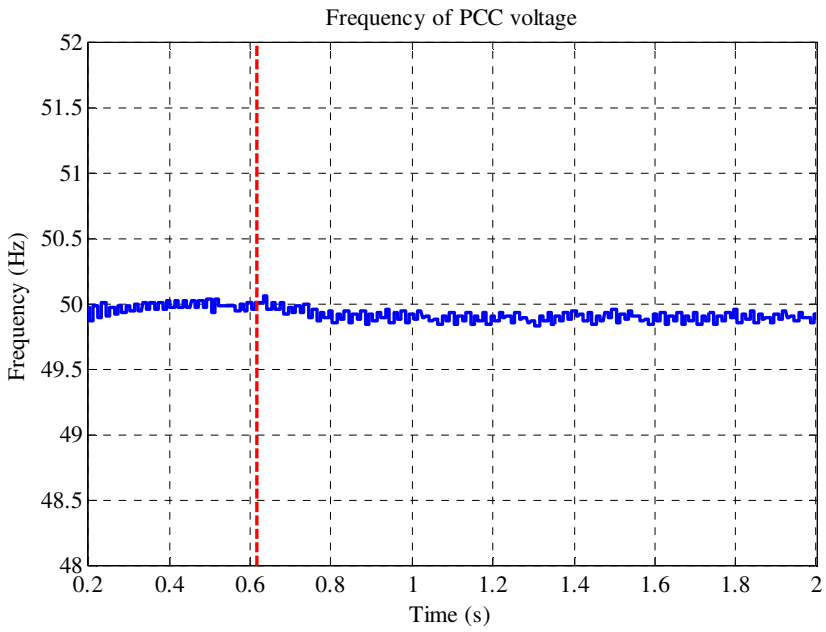

Figure 6.13 Filtered PCC voltage frequency for base case test load with Q_f = 1.98

The SMS method is implemented with the low-pass filter cuff-off frequency for the frequency measurement set at 160 Hz. The maximum phase deviation is set to 10º and the maximum frequency to 53 Hz. In Figure 6.14, the results of the SMS test are shown, and the filtered frequency measurement is shown in Figure 6.15. After disconnecting from the grid, it takes 65 ms for the filtered frequency to deviate outside the frequency limits and for the converter to shut down.

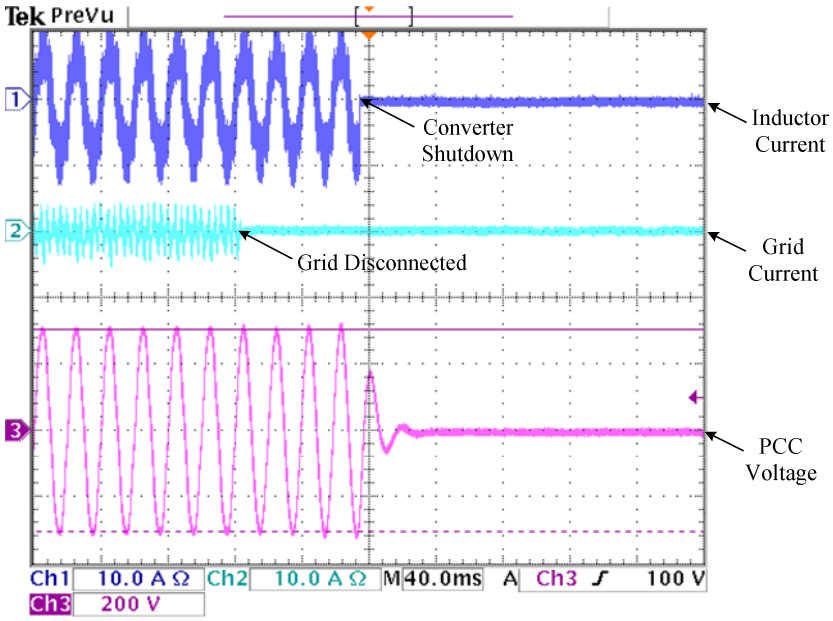

Figure 6.14 SMS test for load with Q_f = 1.98

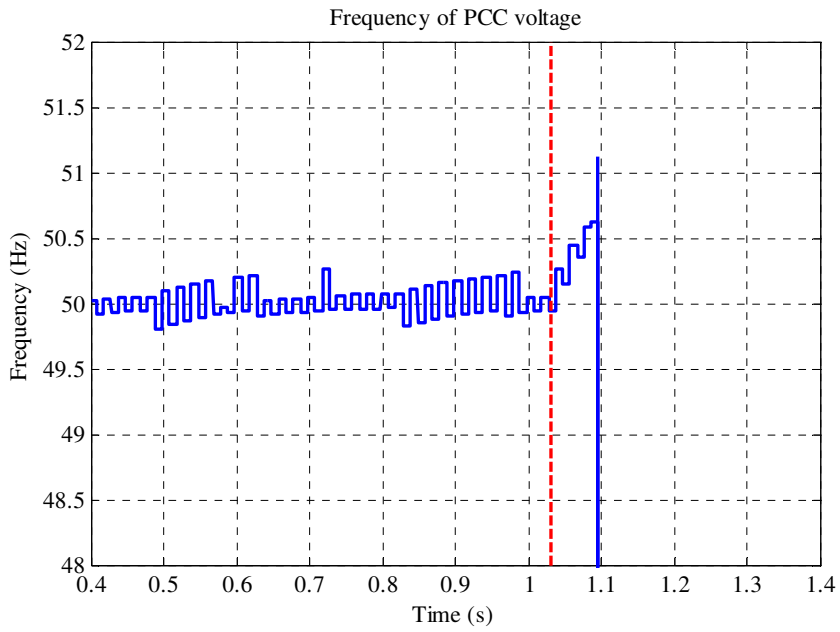

Figure 6.15 Filtered PCC voltage frequency for SMS test load with $Q_f = 1.98$

If the cut-off frequency of the low-pass filter is decreased to 16 Hz, the converter stays on for a longer time. Because of the lower cut-off frequency, the filtered frequency is less susceptible to changes in the measured frequency. This decreases the rate at which the phase deviation occurs, resulting in a longer response time. In Figure 6.16 the inductor current, grid current and PCC voltage are shown. The filtered frequency is shown in Figure 6.17. It takes 390 ms for the filtered frequency to deviate outside the limits and to de-energize the island.

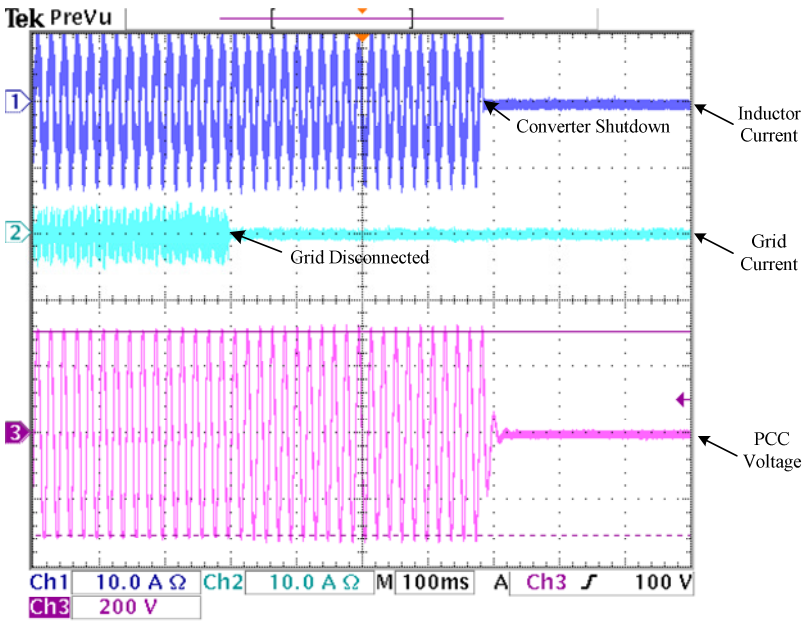

Figure 6.16 SMS test for load with $Q_f = 1.98$ and adjusted filter

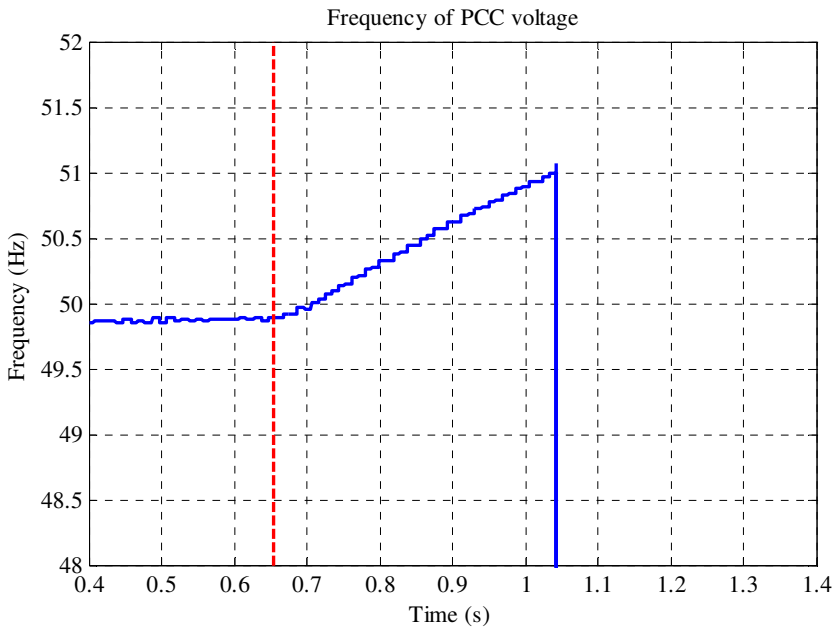

Figure 6.17 Filtered PCC voltage frequency for SMS test load with Q_f = 1.98 and adjusted filter

In Figure 6.18, the test results for the SVS method are shown. The cut-off frequency of the low-pass filter is set at 10 rad/s and the gain is set at 0.15. The reference amplitude limits are set at 0.1 per unit and 2.5 per unit. After disconnecting from the grid, it takes 65 ms before the converter shuts down. In this test, the converter shuts down if the voltage is below the limits for four consecutive cycles.

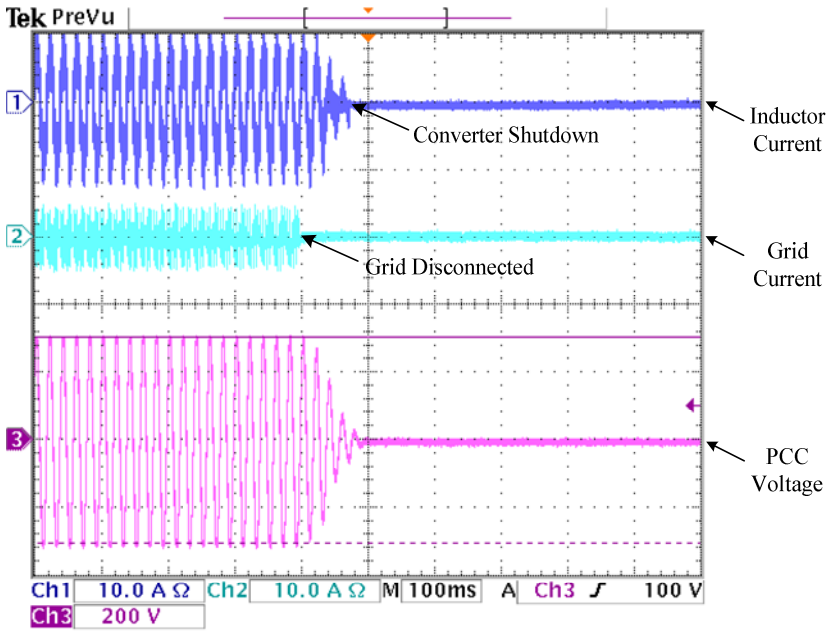

Figure 6.18 SVS test for load with Q_f = 1.98

In this test, the energizing of an island is prevented by using either the SMS method or the SVS method.

6.3.3 TESTING OF A LOAD WITH Q_F = 2.30

This load is close to the recommended test load as specified in the IEEE 1547:2003 standards. The load parameters are listed in Table 6.3.

Table 6.3 Parameters for test load with Qf = 2.30

Parameter	Value
L_{load}	122.47 mH
R_{load}	91 Ω
C_{load}	65.03 µF
C_{filt}	13.3 µF
Q_f	2.30
f_0	51.38 Hz

In Figure 6.19 the inductor current, grid current and PCC voltage of the base case test are shown. The filtered frequency of the PCC voltage is shown in Figure 6.20. After disconnecting from the grid, the voltage and frequency remain within the limits. Consequently, the island remains energized. The levels of the frequency protection are set to 49 Hz and 51 Hz, and the voltage protection levels are set to 207 V and 253 V.

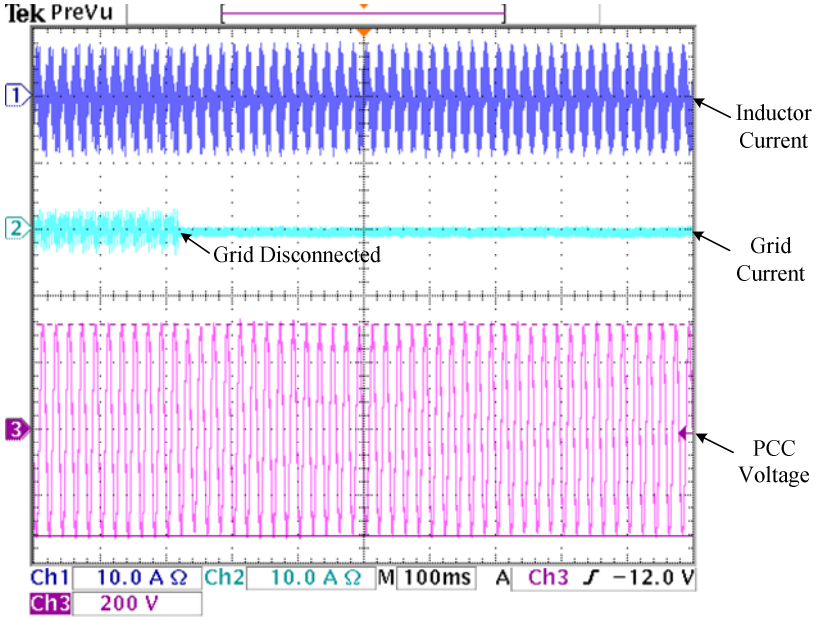

Figure 6.19 Base case test for load with Q_f = 2.30

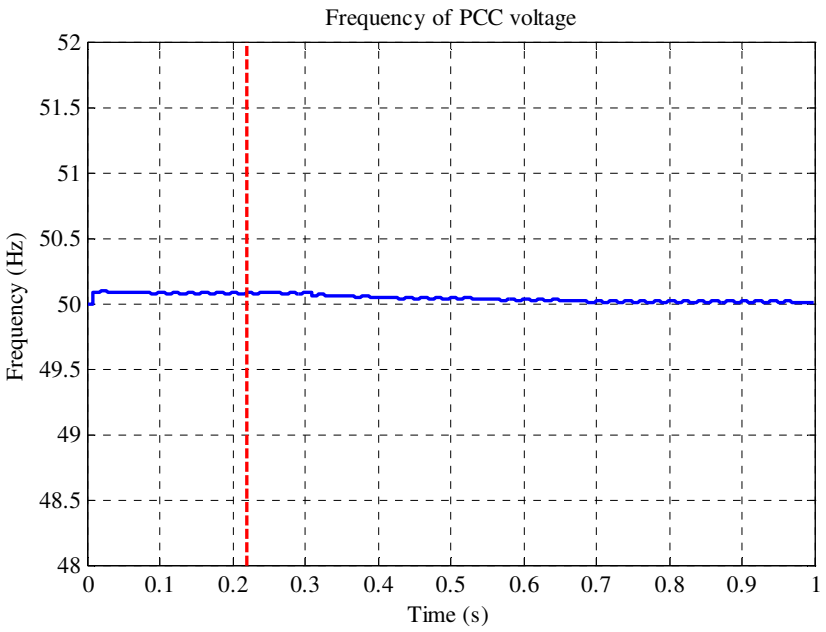

Figure 6.20 Filtered PCC voltage frequency for base case test load with $Q_f = 2.30$

To drive the frequency outside the compatibility levels, the SMS method is implemented. The maximum phase deviation is set at 10º and frequency deviation at 53 Hz. The low-pass filter on the frequency measurement has a cut-off frequency of 160 Hz. In Figure 6.21, the results of this test are shown. The filtered frequency is shown in Figure 6.22. After disconnecting from the grid, it takes 55 ms for the filtered frequency to deviate outside the limits.

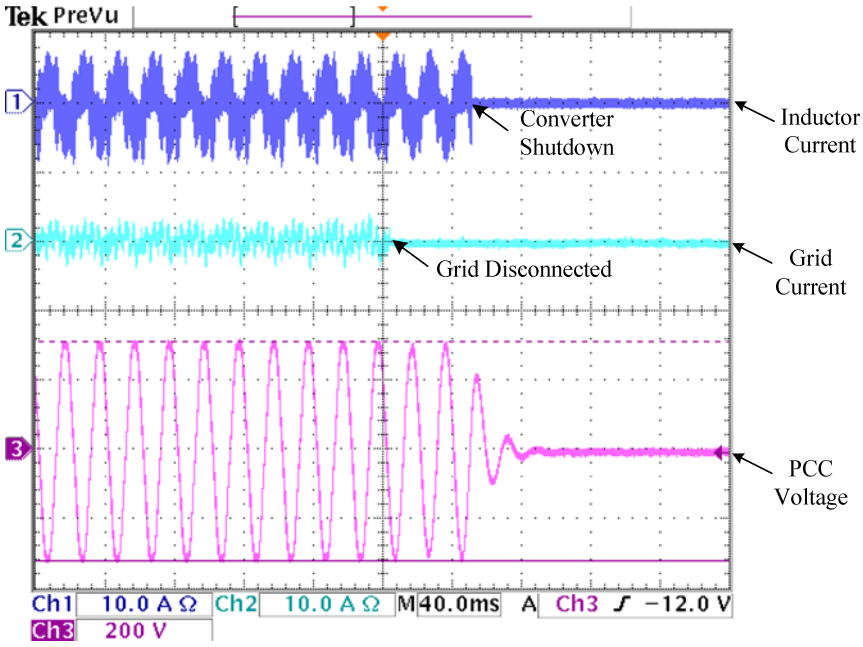

Figure 6.21 SMS test for load with $Q_f = 2.30$

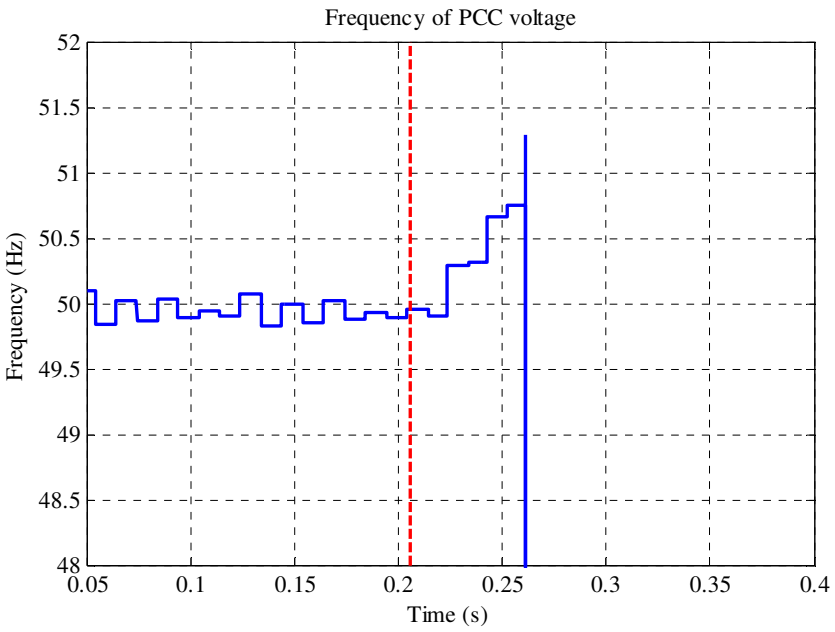

Figure 6.22 Filtered PCC voltage frequency for SMS test load with Q_f = 2.30

By lowering the cut-off frequency of the low-pass filter to 16 Hz, the time the converter stays on also increases, as shown in Figure 6.23. The filtered frequency shown in Figure 6.24 takes 650 ms to deviate outside the limits. The converter shuts down and the island is de-energized.

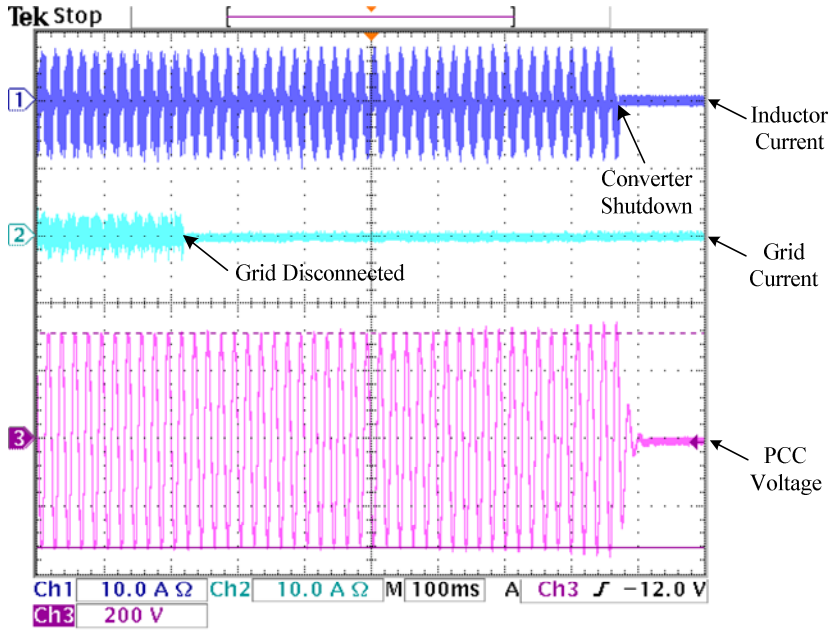

Figure 6.23 SMS test for load with Q_f = 2.30 and adjusted filter

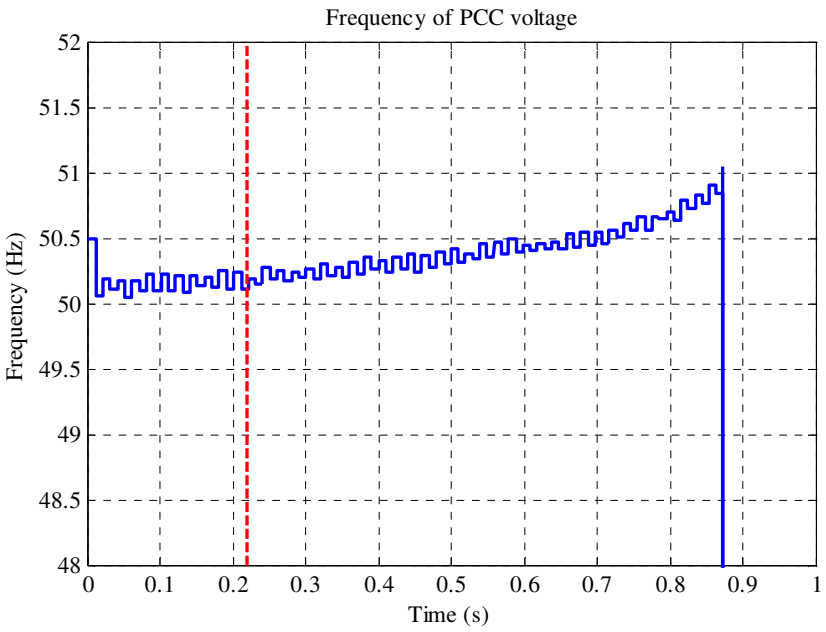

Figure 6.24 Filtered PCC voltage frequency for SMS test load with $Q_f = 2.30$ and adjusted filter

In both tests of the SMS method, the voltage amplitude remains inside the compatibility levels of the grid, but the frequency drifts outside.

The test results for the SVS method are shown in Figure 6.25. The gain is set to 0.8 and the filter cut-off frequency is at 25 rad/s. The converter is set to shut down if the voltage is outside the limits for six consecutive cycles. The grid is disconnected at the time interval indicated. After disconnecting from the grid, the reference is decreased to the minimum level of 0.1 per unit. The converter shuts down 120 ms after disconnecting from the grid.

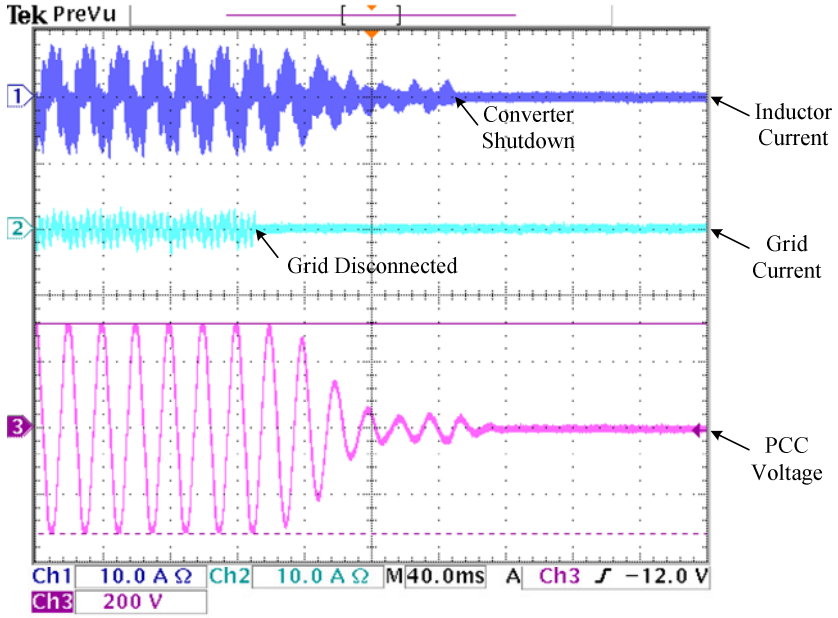

Figure 6.25 SVS test for load with $Q_f = 2.30$

In this test, the energizing of an island has been prevented successfully by using either the SMS or SVS method.

6.3.4 TESTING OF A LOAD WITH $Q_F = 3.88$

The load in this test is an extreme case. Although this load falls outside the specifications of the recommended test load specified in the IEEE 1547:2003 standard, it is still included to show that the anti-islanding methods can be also implemented in cases where loads with high quality factors are encountered. The parameters for this load are listed in Table 6.4.

Table 6.4 Parameters for test load with Qf = 3.88

Parameter	Value
L_{load}	73.9 mH
R_{load}	90.3 Ω
C_{load}	100.6 µF
C_{filt}	13.3 µF
Q_f	3.88
f_0	50.05 Hz

The results of the base case test shown in Figure 6.26 confirm that the voltage amplitude and frequency remain inside the trip limits after disconnecting from the grid. Consequently, the converter continues to energize the local load. The filtered frequency of the island is shown in Figure 6.27. After disconnecting from the grid, the frequency of the island increases slightly, but remains within the limits. The trip levels are set to 49 Hz and 51 Hz for the frequency and 207 V and 253 V for the voltage.

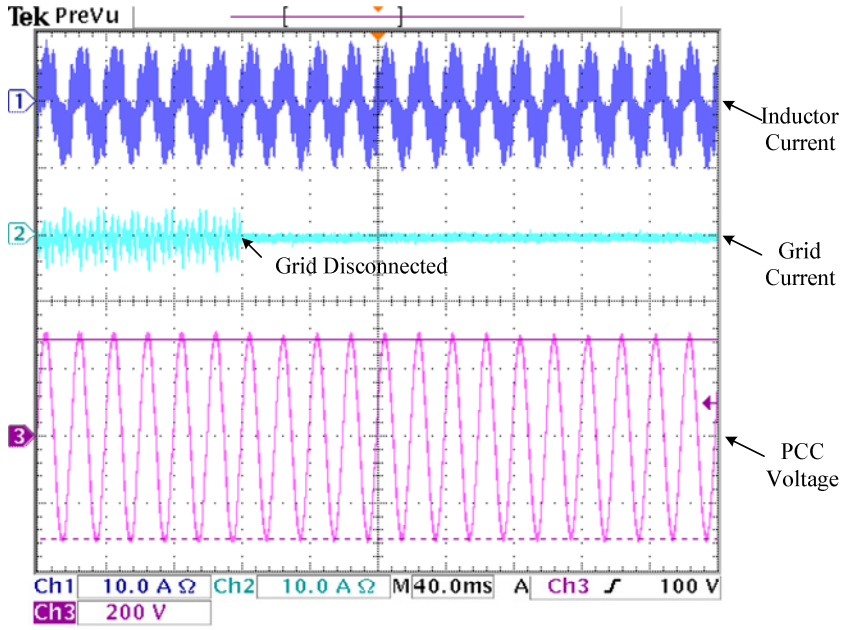

Figure 6.26 Base case test for load with $Q_f = 3.88$

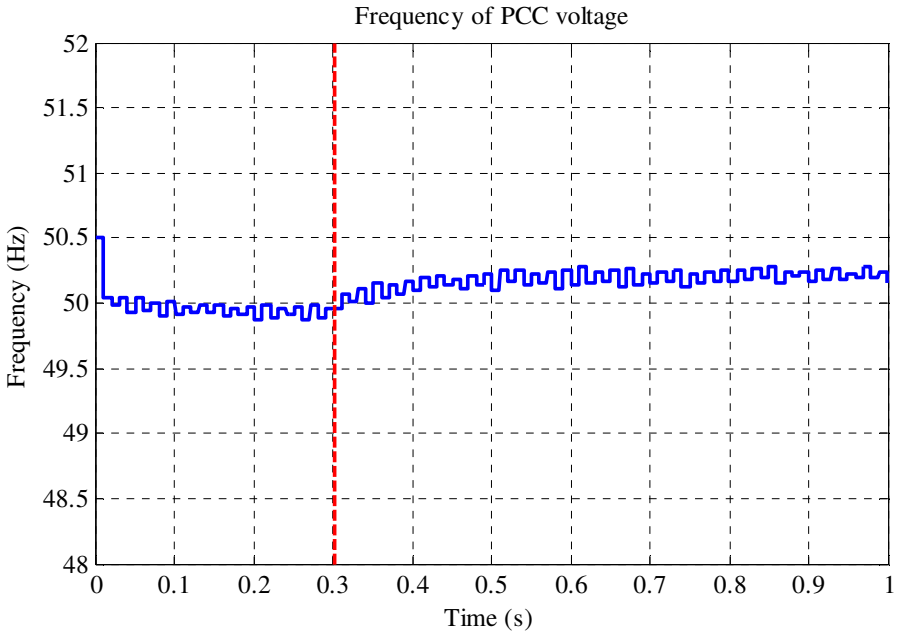

Figure 6.27 Filtered PCC voltage for base case test load with $Q_f = 3.88$

Because of the higher quality factor, the maximum phase deviation is increased. The maximum frequency deviation is kept the same, as it is still outside the limits. In the SMS test, the maximum phase deviation is set to 12°, whereas the maximum frequency deviation is 53 Hz. The results for the test with the filter set to 160 Hz are shown in Figure 6.28. It takes 75 ms for the filtered frequency shown in Figure 6.29 to drift outside the limits.

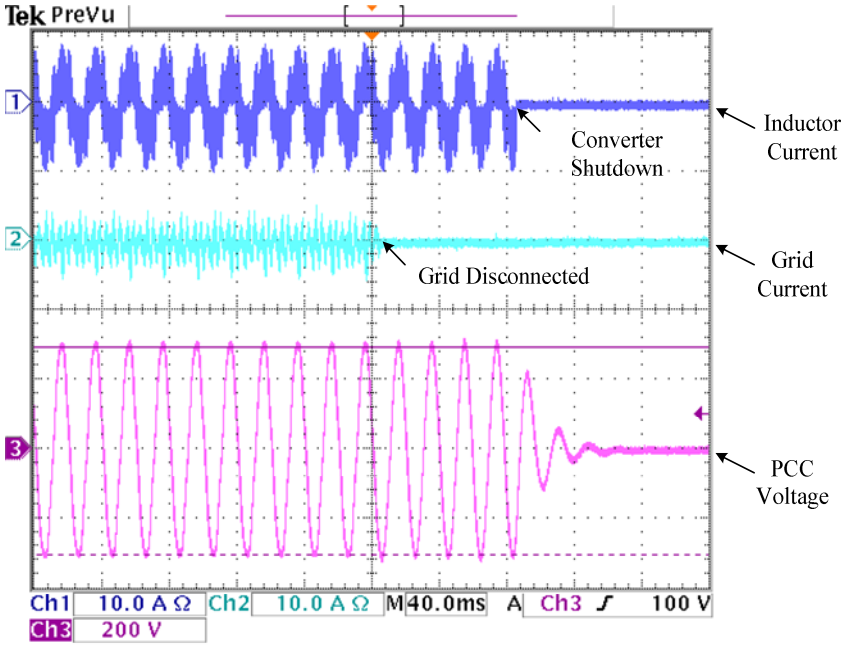

Figure 6.28 SMS test for load with Q_f = 3.88

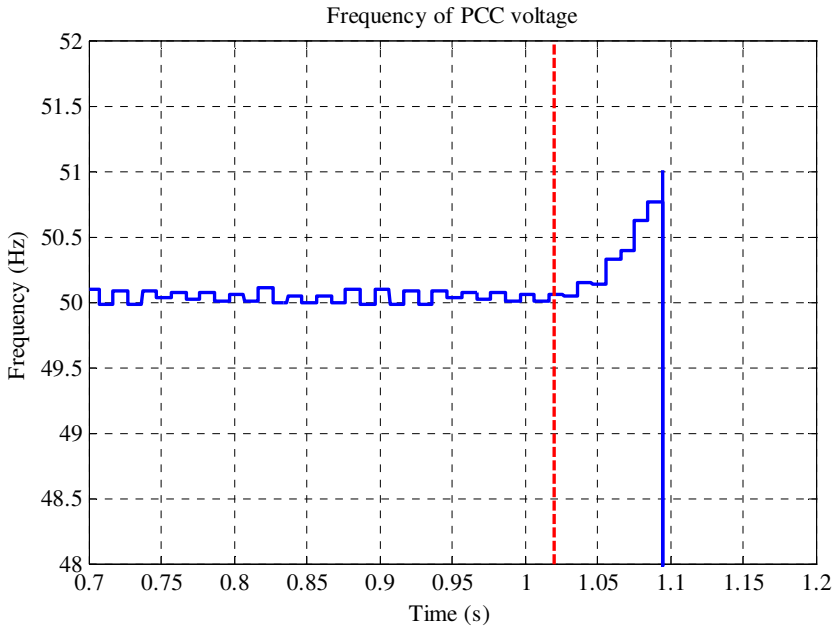

Figure 6.29 Filtered PCC voltage frequency for SMS test load with Q_f =3.88

A decrease in the low-pass filter increases the time the converter stays on, as shown in Figure 6.30. The cut-off frequency is decreased to 16 Hz. After 450 ms, the filtered frequency shown in Figure 6.31 deviates outside the limits and the island is de-energized.

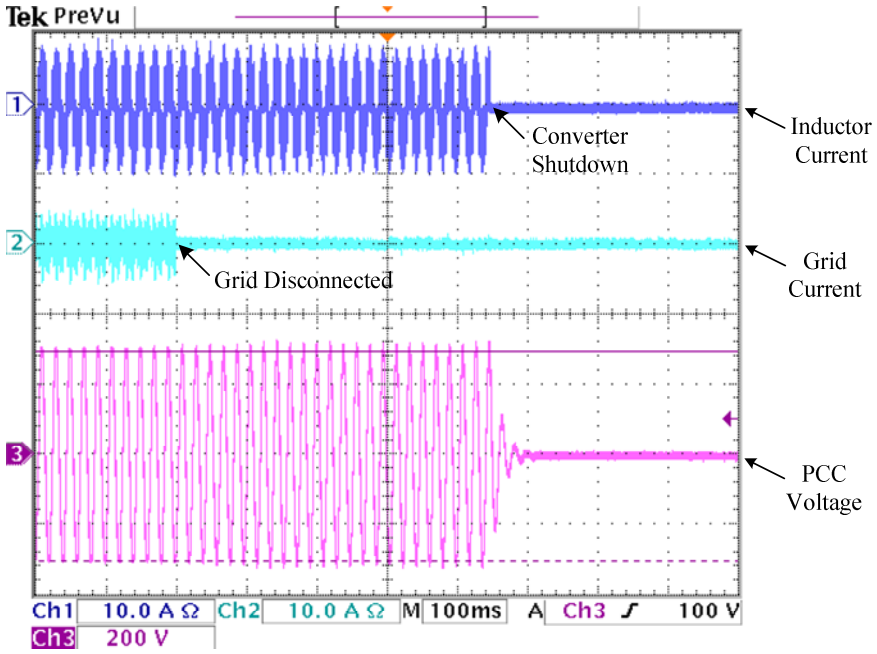

Figure 6.30 SMS test for load with Q_f = 3.88 and adjusted filter

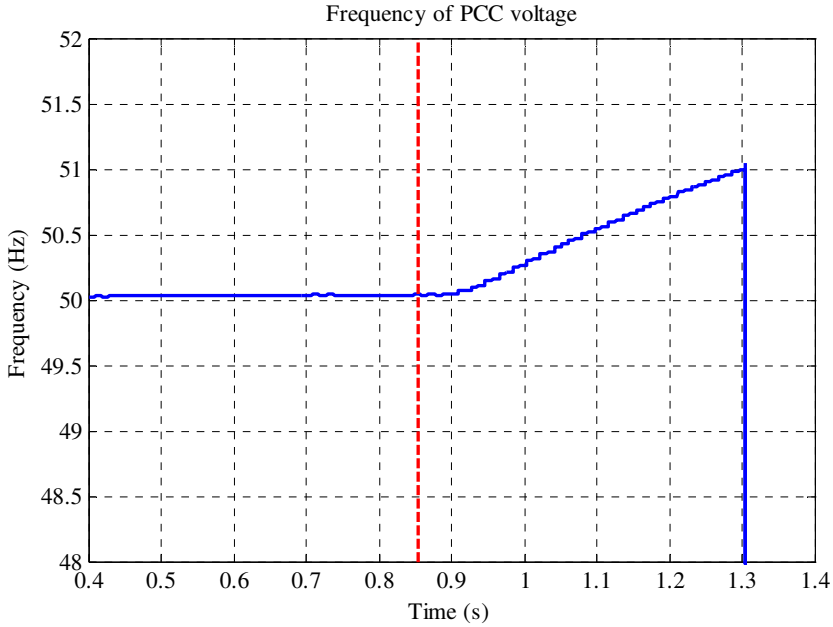

Figure 6.31 Filtered PCC voltage frequency for SMS test load with Q_f = 3.88 and adjusted filter

In Figure 6.32 the results of the SVS method are shown. The gain for this test is K_{svs} = 0.07, and the low-pass filter has a cut-off frequency of 25 rad/s. This limits to which the

reference can change are set to 0.1 per unit and 2.5 per unit. The converter shuts down 160 ms after disconnecting from the grid.

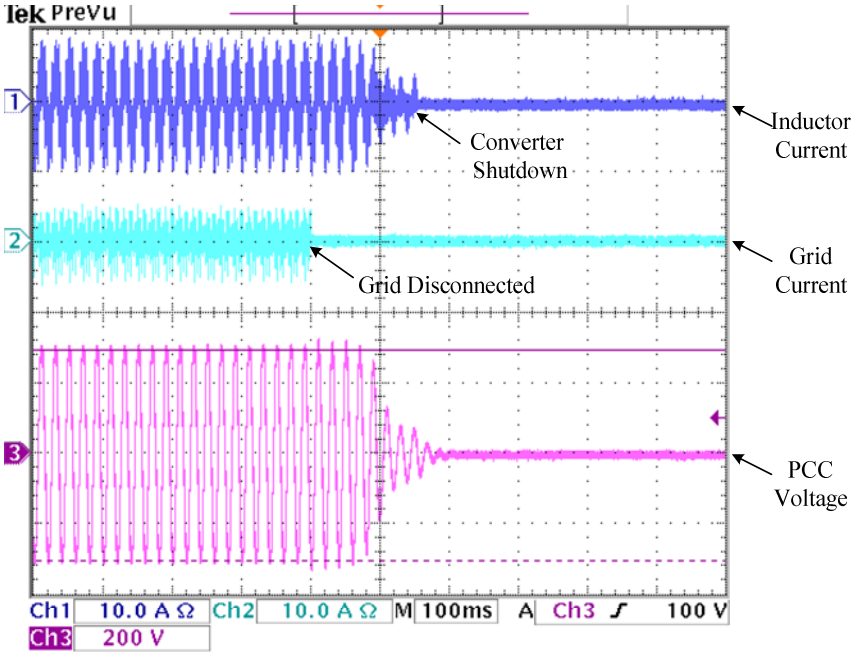

Figure 6.32 SVS test for load with Q_f=3.88

The test confirms that the SMS and SVS can also be implemented on loads with a quality factor that is higher than the recommended test load.

6.4 SUMMARY

In this chapter, the results of the practical anti-islanding tests were presented. The DC bus regulation algorithm was tested and the results were satisfactory. A change in the power reference was successfully tracked by the active rectifier. The active rectifier can also track the changes in the output voltage of the generator to keep the output power constant.

In the IEEE 1547:2003 standards, it is specified that the DG must seize to energize the load within two seconds of island formation. The response times of the anti-islanding methods under different load conditions were all faster than two seconds.

CHAPTER 7. CONCLUSIONS

7.1 INVESTIGATION OF ANTI-ISLANDING METHODS

In Chapter 2, the anti-islanding phenomenon, introduced in Chapter 1, was discussed in more detail. An overview was given of the various passive and active anti-island methods. Their modes of operation were explained as well as their strength and their weaknesses. It was found that most of the protection methods discussed in this chapter would provide some basis to prevent the formation of an island.

The over/under voltage and frequency protection methods were identified as default protection methods because they are easy to implement, as well as because they are deemed compulsory in term of the IEEE 1547:2003 standard.

Although the methods at utility level and the utility/inverter communication methods were shown to be very effective, they were not considered for further investigation due to the financial and administrative complications involved.

7.2 NON-DETECTION ZONES

The concept of non-detection zones was introduced in Chapter 3 as a method of representing graphically the range of loads that will cause a particular inverter-based anti-islanding method to fail. Passive methods were represented in the *power mismatch* plane and active methods in the $Q_f \; vs. \omega_0$ plane. A worst case test load, as specified in the IEEE 1547:2003 standard, was described and the compatibility levels of the grid, as specified in the NRS 048-2:2004 standard was given. An equation to calculate the gain of the SVS method was also derived and represented graphically.

It was shown that, if the active anti-islanding methods were designed correctly and used in combination with the voltage and frequency protection method, the continued energizing of an islanded section of the grid could be successfully prevented.

The slip mode frequency shift method was selected as the active method to drift the frequency of the voltage beyond the compatibility levels of the grid, and the Sandia

voltage shift method was selected to change the amplitude of the voltage beyond the compatibility levels of the grid.

7.3 ALGORITHM DEVELOPMENT AND SIMULATIONS

The algorithms required to simulate and test the anti-islanding methods were developed and discussed in Chapter 4. Predictive current control was discussed as a method of controlling the current through the filter inductors. The DC bus voltage was regulated by using a PI-controller. The PI-controller was also used to control the power flow from the generator to the grid.

The effects of dead-time on the output voltage of the converter was investigated and briefly discussed. A study was done to characterize the dead-time analytically in the zero-crossing region of the inductor current. A compensation method was proposed and implemented.

Simulations were done to verify the functionality of the designed DC bus regulation algorithm as well as the functionality of the active rectifier. The simulations of the SMS and SVS methods suggested that, if they were implemented together correctly, it would be possible to prevent DG units from energizing local loads once the grid was disconnected.

7.4 HARDWARE AND SOFTWARE DEVELOPMENT

The hardware and software used to confirm the functionality of the anti-islanding methods were discussed and developed in Chapter 5. Additional hardware was designed to interface with, and control the existing converter. A soft-start circuit was included to prevent damage to the IGBTs and bus capacitors of the converter. The soft-start procedure used was also explained.

An overview of the operational modes of the converter was given, along with the configuration of the ADC and PWM modules of the DSP. This was followed by flow diagrams of the interrupts where the control loops of the converter are executed. A modular approach was followed during the development of the software. This makes it easy to use the same software on similar converters in the future.

7.5 EXPERIMENTAL RESULTS

The experimental results obtained in Chapter 6 confirmed the functionality of the converter and the anti-islanding methods. It was possible to regulate the DC bus voltage to a pre-defined value as well as to adjust this value dynamically during the operation of the converter. The active rectifier successfully tracked changes in the power reference as well as in the output voltage of the generator. The response to these changes was nearly instantaneous.

Four different loads were used to test the anti-islanding method. The quality factors of these loads varied from 1.39 to 3.88. For each of the test loads a base case was tested to confirm the formation of an energized island once the grid was disconnected. Thereafter, the SMS and SVS methods were tested. In each case, the formation of an energized island was successfully prevented. The response times of the various methods varied from 55 ms to 650 ms, depending on the method or the parameters selected. These times were all well within the maximum of 2 s allowed for shut down, as specified in the IEEE 1547:2003 standard.

Both the SMS method and the SVS method will provide good protection against the formation of an energized island. The SVS method requires a larger change in active power, though, than the change in reactive power required by the SMS method. If it is not possible to implement both methods simultaneously, the SMS method is recommended for implementation.

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Appendix A. **LCD ERROR CODES**

The following table contains the list of error codes displayed on the LCD should an error occur.

Code #:	**Parameter**	**Description**
0	Err_NONE	There is no error.
1	Err_IGBT_A_TOP	Error on top IGBT of phase A during self test
2	Err_IGBT_A_BOT	Error on bottom IGBT of phase A during self test
3	Err_IGBT_B_TOP	Error on top IGBT of phase B during self test
4	Err_IGBT_B_BOT	Error on bottom IGBT of phase B during self test
5	Err_IGBT_C_TOP	Error on top IGBT of phase C during self test
6	Err_IGBT_C_BOT	Error on bottom IGBT of phase C during self test
7	Err_VDC_IGBT_TEST	DC bus voltage to low for self testing
8	Err_VDC_MIN	Over voltage on negative bus capacitor
9	Err_VDC_PLUS	Over voltage on positive bus capacitor
10	Err_Ia_OVR_CUR	Over current error on phase A
11	Err_Ib_OVR_CUR	Over current error on phase B
12	Err_Ic_OVR_CUR	Over current error on phase C
13	Err_Iu_OVR_CUR	Over current error on phase U
14	Err_Iv_OVR_CUR	Over current error on phase V
15	Err_Iw_OVR_CUR	Over current error on phase W
16	Err_VDC_SSTART_LIMIT	DC bus voltage over soft-start limit
17	Err_VDC_CHARGE_TIMEOUT	DC bus charging to slow during soft-start
18	Err_USER_SHUTDOWN	Converter is shutdown by user
19	Err_IGBT_OVERCUR_TZ_GEN	IGBT short circuit error on generator side
20	Err_IGBT_OVERCUR_TZ_GRID	IGBT short circuit error on grid side
21	Err_GRID_OVERVOLTAGE	Voltage on grid side over maximum level
22	Err_GRID_UNDERVOLTAGE	Voltage on grid side under minimum level
23	Err_GRID_OVERFREQ	Frequency on grid side over maximum level
24	Err_GRID_UNDERFREQ	Frequency on grid side under minimum level

Appendix B. CONTROLLER SOFTWARE

The two functions that control the grid side and generator side of the converter as well as the dead time compensation is contained in this appendix.

```
void controlGRID(){

        /*_____Alpha-Beta Convertions_____*/
        grid_mVA = Space3d(Va,Vb,Vc);
        grid_mVB = Space3q(Va,Vb,Vc);

        grid_mIA = Space3d(Ia,Ib,Ic);
        grid_mIB = Space3q(Ia,Ib,Ic);

        /*_____DC bus voltage and Filtered DC bus voltage_____*/
        mVdc = mVdc_plus + mVdc_min;
        fVdc = 0.99*fVdc + 0.01*mVdc;

        /*_____Calculation of Measrued Voltage and Current Magnitudes_____*/
        grid_mVmag = sqrt(grid_mVA*grid_mVA + grid_mVB*grid_mVB);
        grid_mImag = sqrt(grid_mIA*grid_mIA + grid_mIB*grid_mIB);

        /*_____Zero Crossing Detection on the alpha phase on the grid side_____*/
        grid_rIpuA_cnt++;
        if((grid_mVA >= 0) && (grid_rIpuA_sign == -1) && (grid_rIpuA_cnt > 50)){
                grid_rIpuA_sign = 1;
                /*_____Grid frequency calculation_____*/
                grid_mFreq = 1/(0.0002*(grid_rIpuA_cnt));
                grid_rIpuA_cnt = 0;
                grid_fFreq = grid_fFreq*0.99 + 0.01*grid_mFreq;

                if(ipMode == MODE_ONLINE){
                        #if (SVS)
                        if(grid_SVS_rIamp  < grid_SVS_upper && grid_SVS_rIamp  >
                        grid_SVS_lower){
                                grid_SVS_rIamp = 1.00 + prm_AI_Ksvs*cAB*(grid_fVmag -
                                grid_fVmag_prev);
                                grid_fVmag_prev = grid_fVmag;
                        }
                        grid_SVS_rIamp >= grid_SVS_upper ? grid_SVS_rIamp = grid_SVS_upper
                        : grid_SVS_rIamp;
                        grid_SVS_rIamp <= grid_SVS_lower ? grid_SVS_rIamp = grid_SVS_lower
                        : grid_SVS_rIamp;
                        #endif
                }
                else{
                        grid_SVS_rIamp = 1.00;
                }

                #if (SMS)
                grid_SMS_phase        = prm_SMS_phase*sin(1.5707*((fabs(grid_mFreq -
                prm_SMS_fg))/(prm_SMS_fm - prm_SMS_fg)));
                grid_SMS_cosx  = cos(0.01745*grid_SMS_phase);
                grid_SMS_sinx  = sin(0.01745*grid_SMS_phase);
                #endif
        }
        /*_____Zero crossing detection on the alpha phase on the grid side_____*/
        if((grid_mVA <= 0) && (grid_rIpuA_sign == 1) && (grid_rIpuA_cnt > 50)){

                grid_rIpuA_sign = -1;
                /*_____Grid frequency calculation_____*/
                grid_mFreq = 1/(0.0002*(grid_rIpuA_cnt));
                grid_rIpuA_cnt = 0;
                grid_fFreq = grid_fFreq*0.99 + 0.01*grid_mFreq;

                if(ipMode == MODE_ONLINE){
                        #if (SVS)
                        if(grid_SVS_rIamp  < grid_SVS_upper && grid_SVS_rIamp  >
                        grid_SVS_lower){
```

```
                        grid_SVS_rIamp = 1.00 + prm_AI_Ksvs*cAB*(grid_fVmag -
                        grid_fVmag_prev);
                        grid_fVmag_prev = grid_fVmag;
                }
                grid_SVS_rIamp >= grid_SVS_upper ? grid_SVS_rIamp = grid_SVS_upper
                : grid_SVS_rIamp;
                grid_SVS_rIamp <= grid_SVS_lower ? grid_SVS_rIamp = grid_SVS_lower
                : grid_SVS_rIamp;
                #endif
        }
        else{
                grid_SVS_rIamp = 1.00;
        }
}

/*_____Low-pass Filter on the voltage and current magnitudes_____*/
grid_fVmag = grid_fVmag*0.9975 + 0.0025*grid_mVmag;  //Cut-off at 25 rad/s
grid_fImag = grid_fImag*0.999 + 0.001*grid_mImag;    //Cut-off at 10 rad/s

/*_____Power Calculations and low pass filter_____*/
grid_mPower = 0.666666*grid_fVmag*grid_fImag;
grid_fPower = grid_fPower*0.999 +0.001*grid_mPower;

/*_____Limit the magnitude of the measured grid amplitude_____*/
(grid_mVmag < 1.00) ? (grid_mVmag = 1.00) : (grid_mVmag);

/*_____ANTI ISLANDING CALCULATIONS_____*/
/*___No Anti-Islanding Method___*/
#if (BASE_CASE)
grid_rIpuA              = grid_mVA/grid_mVmag;
grid_rIpuB              = grid_mVB/grid_mVmag;
grid_SVS_rIamp          = 1.00;
#endif

/*___Slip Mode Frequency Shift Method___*/
#if (SMS)
grid_rIpuA              = (grid_mVA*grid_SMS_cosx - grid_mVB*grid_SMS_sinx)
                           /grid_mVmag;
grid_rIpuB              = (grid_mVA*grid_SMS_sinx + grid_mVB*grid_SMS_cosx)
                           /grid_mVmag;
grid_SVS_rIamp          = 1.00;
#endif

/*___Sandia Voltage Shift Method___*/
#if (SVS)
grid_rIpuA = grid_SVS_rIamp*(grid_mVA/grid_mVmag);
grid_rIpuB = grid_SVS_rIamp*(grid_mVB/grid_mVmag);
#endif

/*_____OUTER CONTROL LOOP(PI Control)_____*/
Vdc_err = prm_ref_Vdc - fVdc;                       // Voltage Error
Vs += 0.13902*(Vdc_err - 0.998*Vdc_err_prev);
Vdc_err_prev = Vdc_err;

/*_____LIMITS OF THE AMPLITUDE OF THE CURRENT REFERENCE_____*/
(Vs >  prm_grid_current_limit) ? (Vs =  prm_grid_current_limit) : (Vs);
(Vs < -prm_grid_current_limit) ? (Vs = -prm_grid_current_limit) : (Vs);

grid_rIA = -1.5*Vs*grid_rIpuA;
grid_rIB = -1.5*Vs*grid_rIpuB;

/*_____INNER LOOP CONTROL(Predictive Current Control)_____*/
rValpha = 8.50*(grid_rIA - grid_mIA) + grid_mVA;
rVbeta  = 8.50*(grid_rIB - grid_mIB) + grid_mVB;

/*_____Space Vector Calculations_____*/
mVdc < 1.00 ? mVdc = 1.00 : mVdc;     //To prevent devision by zero in the SV
                                      calculations
imVdc = 1/mVdc;                       //Inverse of the grid voltage used for the
                                      Space Vector Calculations

SpaceVectorPWM();
DeadTimeComp(grid_rIA ,grid_rIB );
}
```

```
void controlGEN(){

        /*_____Alpha-Beta Convertions_____*/
        gen_mVA         = Space3d(Vu,Vv,Vw);
        gen_mVB         = Space3q(Vu,Vv,Vw);

        gen_mIA         = Space3d(Iu,Iv,Iw);
        gen_mIB         = Space3q(Iu,Iv,Iw);

        /*_____Calculation of Measrued Voltage and Current Magnitudes_____*/
        gen_mVmag       = sqrt(gen_mVA*gen_mVA + gen_mVB*gen_mVB);
        gen_mImag       = sqrt(gen_mIA*gen_mIA + gen_mIB*gen_mIB);

        /*_____Instatanious Power Calculation_____*/
        gen_mPower = gen_fVmag*gen_fImag*0.666666;

        /*_____Zero Crossing Detection on the Alpha Phase_____*/
        gen_rIpuA_cnt++;
        if((gen_mVA >= 0)&&(gen_rIpuA_sign == -1) && (gen_rIpuA_cnt >= 50)){
                gen_rIpuA_sign = 1;
                /*_____Frequency Calculation_____*/
                gen_mFreq = 1 / (gen_rIpuA_cnt*0.0002);
                gen_rIpuA_cnt = 0;                              //Counter Reset
                gen_fFreq       = gen_fFreq *0.99 + 0.01*gen_mFreq;
        }
        if((gen_mVA <= 0) && (gen_rIpuA_sign == 1) && (gen_rIpuA_cnt >= 50)){
                gen_rIpuA_sign = -1;
                /*_____Frequency Calculation_____*/
                gen_mFreq = 1 / (gen_rIpuA_cnt*0.0002);
                gen_rIpuA_cnt = 0;                              //Counter Reset
                gen_fFreq       = gen_fFreq *0.99 + 0.01*gen_mFreq;
        }

        /*_____Low Pass Filter on measurements_____*/
        gen_fVmag       = gen_fVmag *0.99 + 0.01*gen_mVmag;
        gen_fImag       = gen_fImag *0.999 + 0.001*gen_mImag;
        gen_fPower      = gen_fPower*0.999 + 0.001*gen_mPower;

        /*_____Reference Signals_____*/
        gen_rIpuA       = gen_mVA/gen_mVmag;
        gen_rIpuB       = gen_mVB/gen_mVmag;

        /*_____Adjust the current amplitude to deliver the reference power_____*/
        gen_fVmag < 1 ? gen_fVmag = 1 : gen_fVmag;
        gen_rIamp       = (gen_P_ref_3*0.333333)/(gen_fVmag*cAB);

        /*_____Limit the current amplitude_____*/
        gen_rIamp > prm_gen_current_limit ? gen_rIamp = prm_gen_current_limit : gen_rIamp;
        gen_rIamp < 0.00 ? gen_rIamp = 0.00 : gen_rIamp;

        /*_____Calculate the reference signals in the Alpha-Beta Plane_____*/
        gen_rIA = 1.5*(gen_rIamp*1.4142)*gen_rIpuA;
        gen_rIB = 1.5*(gen_rIamp*1.4142)*gen_rIpuB;

        /*_____Control Calculations_____(Predictive Current Control)*/
        rValpha = -8.50*(gen_rIA - gen_mIA) + gen_mVA;
        rVbeta  = -8.50*(gen_rIB - gen_mIB) + gen_mVB;

        /*_____Space Vector Calculations_____*/
        mVdc < 1 ? mVdc = 1 : mVdc;   //To prevent devision by zero in the SV calculations
        imVdc = 1/mVdc;               //Inverse of the grid voltage used for the Space
                                      Vector Calculations

        SpaceVectorPWM();
        DeadTimeComp(gen_rIA ,gen_rIB );

}
```

```
void DeadTimeComp(double V_alpha , double V_beta){

        /*_____DEAD TIME COMPENSATION_____*/
        dtIa = 0.6666*Spacedq0a(V_alpha,V_beta);
        dtIb = 0.6666*Spacedq0b(V_alpha,V_beta);
        dtIc = 0.6666*Spacedq0c(V_alpha,V_beta);

        if ((s_Da > DeadTime) && (s_Db > DeadTime) && (s_Dc > DeadTime)) {
                /*_____Mode 1_____*/
                /*_____When the current sign is defined_____*/
                if (dtIa >=  DeadTime_Theshold) { s_Da = s_Da + DeadTime; }
                if (dtIa <= -DeadTime_Theshold) { s_Da = s_Da - DeadTime; }
                if (dtIb >=  DeadTime_Theshold) { s_Db = s_Db + DeadTime; }
                if (dtIb <= -DeadTime_Theshold) { s_Db = s_Db - DeadTime; }
                if (dtIc >=  DeadTime_Theshold) { s_Dc = s_Dc + DeadTime; }
                if (dtIc <= -DeadTime_Theshold) { s_Dc = s_Dc - DeadTime; }

                /*_____In the area around 0 the dead time is undefined an linear approach
                is used to compensate for this_____*/
                if (dtIa <  DeadTime_Theshold && dtIa > 0.00 ) { s_Da = s_Da + (dtIa/
                        DeadTime_Theshold)*DeadTime; }
                if (dtIa > -DeadTime_Theshold && dtIa < 0.00 ) { s_Da = s_Da - (dtIa/-
                        DeadTime_Theshold)*DeadTime; }
                if (dtIb <  DeadTime_Theshold && dtIb > 0.00 ) { s_Db = s_Db + (dtIb/
                        DeadTime_Theshold)*DeadTime; }
                if (dtIb > -DeadTime_Theshold && dtIb < 0.00 ) { s_Db = s_Db - (dtIb/-
                        DeadTime_Theshold)*DeadTime; }
                if (dtIc <  DeadTime_Theshold && dtIc > 0.00 ) { s_Dc = s_Dc + (dtIc/
                        DeadTime_Theshold)*DeadTime; }
                if (dtIc > -DeadTime_Theshold && dtIc < 0.00 ) { s_Dc = s_Dc - (dtIc/-
                        DeadTime_Theshold)*DeadTime; }

                /*_____Mode 2_____*/
        } else if ((s_Da <= DeadTime) && (dtIa >= 0.0)) {
                if (dtIb>= 0.0) { s_Db = s_Db - (s_Da - DeadTime); }
                else { s_Db = s_Db - (s_Da + DeadTime); }
                if (dtIc >= 0.0) { s_Dc = s_Dc - (s_Da - DeadTime); }
                else { s_Dc = s_Dc - (s_Da + DeadTime); }
        } else if ((s_Da <= DeadTime) && (dtIa < 0.0)) {
                if (dtIb>= 0.0) { s_Db = s_Db - (s_Da - 3.0*DeadTime); }
                else { s_Db = s_Db - (s_Da - DeadTime); }
                if (dtIc >= 0.0) { s_Dc = s_Dc - (s_Da - 3.0*DeadTime); }
                else { s_Dc = s_Dc - (s_Da - DeadTime); }
        } else if ((s_Db <= DeadTime) && (dtIb >= 0.0)) {
                if (dtIa >= 0.0) { s_Da = s_Da - (s_Db - DeadTime); }
                else { s_Da = s_Da - (s_Db + DeadTime); }
                if (dtIc >= 0.0) { s_Dc = s_Dc - (s_Db - DeadTime); }
                else { s_Dc = s_Dc - (s_Db + DeadTime); }
        } else if ((s_Db <= DeadTime) && (dtIb < 0.0)) {
                if (dtIa >= 0.0) { s_Da = s_Da - (s_Db - 3.0*DeadTime); }
                else { s_Da = s_Da - (s_Db - DeadTime); }
                if (dtIc >= 0.0) { s_Dc = s_Dc - (s_Db - 3.0*DeadTime); }
                else { s_Dc = s_Dc - (s_Db - DeadTime); }
        } else if ((s_Dc <= DeadTime) && (dtIc >= 0.0)) {
                if (dtIa >= 0.0) { s_Da = s_Da - (s_Dc - DeadTime); }
                else { s_Da = s_Da - (s_Dc + DeadTime); }
                if (dtIb>= 0.0) { s_Db = s_Db - (s_Dc - DeadTime); }
                else { s_Db = s_Db - (s_Dc + DeadTime); }
        } else if ((s_Dc <= DeadTime) && (dtIc < 0.0)) {
                if (dtIa >= 0.0) { s_Da = s_Da - (s_Dc - 3.0*DeadTime); }
                else { s_Da = s_Da - (s_Dc - DeadTime); }
                if (dtIb>= 0.0) { s_Db = s_Db - (s_Dc - 3.0*DeadTime); }
                else { s_Db = s_Db - (s_Dc - DeadTime); }
        }
```