From high-speed superconducting devices to nanosensors

by

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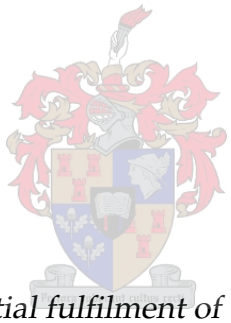

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Declaration

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Abstract

In this dissertation the story of a research career spanning 34 years is told.

It started in microelectronics in the early 1980's and focused on aspects of design and optimization of high-voltage diodes. Advanced simulation tools, such as Monte Carlo particle simulation algorithms, was also implemented, specifically for the design of microwave diodes.

During a sabbatical at *GEC Hirst Research Centre* in 1988, shortly after the discovery of high-temperature superconductors, an opportunity arose to work on superconducting devices. The research was focused on understanding and modeling the mechanisms of single particle (quasiparticle) tunnelling in NIS or SIS junctions. The ultimate goal was, as was the case for semiconductor electronics, to have a three-terminal switching device that can be utilized as a binary switch.

Back at Stellenbosch, the superconductivity laboratory was established, with the primary focus on the manufacture of high-temperature superconducting (YBCO) devices, including thin film deposition, photolithography and etching of micron-sized patterns.

In 1995 a sabbatical was spent at the University of California at Berkeley, in the research group of Professor Ted Van Duzer, one of the pioneers of superconducting technology. During this sabbatical the fastest superconducting voltage-state logic family, Complementary Output Switching Logic (COSL) was designed and successfully tested at a clock speed of 1 GHz. Towards the end of 1996 these devices were successfully tested at clock speeds up to 18 GHz, making it the fastest voltage-state logic family to this day. An alternative method to predict the circuit yield of superconducting circuits, incorporating all the imperfections of the manufacturing process, was also introduced. This method was based on a Monte Carlo analysis approach, and was extensively used to optimize the COSL circuits for maximum yield.

In 1996, back from Berkeley, the research focus of the group was extended (from the emphasis on the fabrication of high-temperature YBCO devices) to include the design of ultra-fast low-temperature superconducting devices, specifically COSL and Rapid Single Flux Quantum (RSFQ) circuits. The unique contributions in the low-T_c field included the conceptualization of the first Superconducting Programmable Gate Array and the design of such a circuit using a hybrid approach, mixing RSFQ and COSL gates. A major contribution was the advances made in the 3D-extraction of circuit parameters from the circuit layout, which incorporated the imperfections due to the fabrication processes. This effort led to the

establishment of a spin-off company, *NioCAD*, which focussed on advanced software for the layout of superconducting circuits. An important component of the software was the circuit extraction capabilities.

Due to the capabilities available in the superconductivity research laboratory, where submicron devices could be fabricated and also inspected, using the AFM and the tabletop SEM, the research focus gradually evolved to incorporate non-superconducting devices, with specific emphasis on nanosensors. An important aspect of the work on nanosensors is that it is, by nature, multidisciplinary. Very fruitful collaboration was thus established with researchers in microbiology, amongst others. Some of the unique contributions here were the successful design and testing of a piezoelectric nanogenerator (based on ZnO nanowires), and the incorporation of pathogens on the nanogenerator, using a protein scaffolding system, to form a biosensor. The successful testing of the biosensor proved that, by attaching antibodies on the piezoelectric nanogenerator, a specific pathogen (e.g. TB, *E. coli*, etc.) would attach to the antibody, thus generating a voltage that would confirm the presence of the specific pathogen. Significant advances have been made on alternative transducers, and electrospun microfibers, and also paper, have been successfully tested for the detection of bacteria.

Biosensor research is currently the main focus area of the research group.

Opsomming

In hierdie proefskrif word die storie vertel van 'n navorsingsloopbaan wat oor 34 jaar strek.

Dit het alles in mikroëlektronika in die vroeë 1980's begin, met die fokus op aspekte van die ontwerp en optimisasie van hoogspanningsdiodes. Gevorderde simulasiegereedskap, soos Monte Carlo partikelsimulasie algoritmes, is geïmplementeer, spesifiek vir die ontwerp van mikrogolfdiodes.

Kort na die ontdekking van hoë-temperatuur supergeleiers, gedurende studieverlof by *GEC Hirst Research Centre* in 1988, het die geleentheid hom voorgedoen om oor supergeleidende komponente navorsing te doen. Die fokus was om begrip te ontwikkel van die meganismes van enkelpartikel (kwasipartikel) tonnelling in NIS- en SIS vlakke, en ook om dit te modelleer. Die doel was om, soos die geval is by halfgeleier komponente, 'n drieterminaal komponent te vind wat as 'n binêre skakelaar kan optree.

Terug op Stellenbosch is die supergeleier navorsingslaboratorium gevestig. Die primêre doel was om hoë-temperatuur supergeleier (YBCO) komponente te vervaardig, en ook om dunfilm neerslag, fotolitografie en etsing te doen vir mikron-grootte komponente.

'n Studieverlofperiode is in 1995 by die Universiteit van Kalifornië in Berkeley, in die navorsingsgroep van die legendariese prof. Theodore Van Duzer, deurgebring. Gedurende hierdie tydperk is die vinnigste spanningstoestand logiese familie, Complementary Output Switching Logic (COSL), ontwerp en getoets by 'n klokspoed van 1 GHz. Teen die einde van 1996 is die komponente suksesvol getoets by 'n klokspoed van 18 GHz, wat dit, tot vandag toe nog, die vinnigste spanningstoestand logiese familie maak. 'n Alternatiewe metode om die opbrengs van vervaardigde supergeleidende bane, met al die imperfeksies van die vervaardigingsproses in ag geneem, te voorspel, is ook ontwikkel. Hierdie metode is gebaseer op die Monte Carlo analisemetode, en is ekstensief gebruik om die COSL bane se opbrengs te optimiseer.

In 1996, terug van die besoek aan Berkeley, is daar besluit om die navorsingsfokus van die groep te verbreed vanaf die enger klem op die vervaardiging van hoë-temperatuur YBCO komponente, en om ook te konsentreer op ultra-hoëspoed lae-temperatuur supergeleidende komponente, soos COSL en RSFQ bane. Unieke bydraes op die gebied van lae-temperatuur supergeleidende komponente gedurende hierdie tyd sluit die eerste 'Superconducting Programmable Gate Array' (SPGA) in, waar gebruik gemaak is van 'n hibriede benadering, wat beide COSL en RSFQ komponente ingesluit het. 'n Verdere wesenlike bydrae was die vordering wat gemaak is in die drie-dimensionele onttrekking van baanparameters

uit die uitleg van die baan, met inbegrip van die imperfeksies van die vervaardigingsproses. Hierdie navorsing het gelei tot die stigting van 'n afwentelmaatskappy, *NioCAD*, waar die fokus op gevorderde programmatuur vir die uitlê van supergeleierbane was. 'n Belangrike kompnoent van die programmatuur was uiteraard die vermoë om baanparameters te onttrek.

Die bestaande vermöe in die supergeleier navorsingslaboratorium om sub-mikron komponente te vervaardig en met die hulp van AFM en die kompakte SEM te inspekteer, het daartoe gelei dat die navorsingsfokus mettertyd verskuif het om ook nie-supergeleidende komponente, spesifiek nanosensors, in te sluit. 'n Belangrike aspek van die werk op nanosensors is dat dit uiteraard multidissiplinêr van aard is. Baie vrugbare samewerking het dus tot stand gekom met navorsers van, onder andere, mikrobiologie. Sommige van die unieke bydraes op hierdie gebied was die suksesvolle ontwerp en implementering van die ZnO nanodraad piesoëlektriese nanogenerator, en die suksesvolle integrering daarvan met patogene, deur gebruik te maak van 'n proteïenstellasie om 'n biosensor te vorm. Die sukses van die sensor het bewys dat, deur teenliggaampies aan die piesoëlektriese nanogenerator te koppel, 'n spesifieke patogeen (bv. TB, *E. coli*, ens.) kan koppel aan die teenliggaampie, om sodoende 'n elektriese spanning op te wek om die teenwoordigheid van die sepsifieke patogeen te verklik. Beduidende vordering is ook gemaak om alternatiewe omskakelaars te vind, en elektrostaties-geweefde mikrovesels, asook papier, is suksesvol gebruik om bakterieë op te spoor.

Biosensornavorsing is tans die hooffokus van die navorsingsgroep.

Acknowledgements

I do believe that anything meaningful is only possible through interaction with people, and in telling my little story, this was reconfirmed over and over again. I am indeed indebted to some many people on on so many different levels.

To Professor Christo Viljoen, thank you for planting the research seed in the fourth-floor electronics laboratory during a practical session in my final undergraduate year. Thank you for the guidance during my Master's and PhD studies. That was my first steps on my microelectronics path.

I am also extremely indebted to my early career mentors, Professors PW van der Walt and Johannes Cloete. I still remember the shared excitement when my first journal article had been accepted. I still remember how sweet the bitter *Castle Lager* at the Lanzerac Hotel tasted! To me, Johannes Cloete was the perfect academic. His Richard Feynman-like enthusiasm about science, and life in general, will always be an inspiration.

I have also been extremely blessed to rub shoulders with Professor Theodore Van Duzer. Through this humble giant of a man I came to the realization that even a boytjie from South Africa had something to say and could make some kind of a contribution.

My journey with Mark Jeffery will always be a highlight in my career. In addition, he introduced me to *Samuel Adams* and I introduced him to a true South African, *Grandpa Headache Powders*.

Now and then a person is lucky to meet some extraordinarily gifted people. Such a person is Ulrich Büttner. He is the most innovative technician I have ever met and virtually all our fabrication tools in the laboratory have the Ulrich signature, either by building if from scratch or modifying it for our specific purposes. He was instrumental in all the research that emanated from the laboratory. Thanks,Ulrich!

An then there are the students! I have learnt so much from extraordinary students such as Robert van Zyl, Coenrad Fourie, Graham Hardie, Akram Elkaseh, Retief Gerber, Wynand van Staden, Hennie de Villiers, Stanley van den Heever, Deon Neveling, Michael Maas and Frederic Isingizwe Nturambirwe.

A huge thank you to Leon Dicks, who started the exciting biosensor journey with me. Our collaboration is proof that something very interesting can come from meetings.

And then, lastly, my family. Thanks Mariechen for being part of the journey from the beginning – from midnight taxi rides to Edgeware General Hospital with a feverish child to road trips through California with our golden Ford Taurus with the less than reliable

braking system. Thanks for bearing with me! And thanks for shaping me to develop more shades of grey in my engineering thinking! Thanks Karolien, Philip, Dirk and Marika – you still are always interested in what I am doing, no matter how boring it may sound. Thank you all for the very interesting discussions on science, psychology and life in general that normally develop around the braai at home or at Keurboomstrand. Now and then I am even not the only one that agrees with myself. This truly gave substance to my journey!

Contents

Nomenclature

Abbreviations

RF	:	Radio frequency
UHF	:	Ultra-high frequency
VSWR	:	Voltage Standing Wave Ratio
DC	:	Direct Current
AC	:	Alternating Current
IMPATT	:	Impact Avalanche Transit Time
GaAs	:	Gallium Arsenide
GaN	:	Gallium Nitride
NDR	:	Negative Differential Resistance
PVM	:	Parallel Virtual Machine
NIS	:	Normal conductor-Insulator-Superconductor
SIS	:	Superconductor-Insulator-Superconductor
NS	:	Normal conductor-Superconductor
COSL	:	Complementary Output Switching Logic
MVTL	:	Modified Variable Threshold Logic
SQUID	:	Superconducting Quantum Interference Device
PRBSG	:	Pseudo-Random Bit-Sequence Generator
RSFQ	:	Rapid Single Flux Quantum
BER	:	Bit-error rate
JTL	:	Josephson Transmission Line
NDRO	:	Non-Destructive Readout Register
DRO	:	Destructive Readout Register
SR	:	Set-Reset
T	:	Toggle
DCRL	:	DC Resettable Latch
FPGA	:	Field Programmable Gate Array
SPGA	:	Superconducting Programmable Gate Array
HUFFLE	:	Hybrid Unlatching Flip-Flop Logic Element
CAD	:	Computer Aide Design
XML	:	Extensible Markup Language
RSFQ-AT	:	RSFQ-Asynchronous Timing

SEM	:	Scanning Electron Miroscope
AFM	:	Atomic Force Microscope
STM	:	Scanning Tunneling Microscope
YBCO	:	$YBa_2Cu_3O_{7-\delta}$
MgO	:	Magnesium Oxide
YSZ	:	Yttria-stabilized zirconia
PBCO	:	$PrBa_2Cu_3O_{7-\delta}$
IV	:	Current-Voltage
DUT	:	Device Under Test
ICM	:	Inverse Cylindrical Magnetron
VTB	:	Variable Thickness Bridge
3D	:	Three-dimensional
VLS	:	Vapor-Liquid-Solid
PMMA	:	Poly(methyl methacrylate)
SWCNT	:	Single-walled carbon nanotube
MWCNT	:	Multi-walled carbon nanotube
SSHI	:	Synchronized Switch Harvesting on Inductor
UV	:	Ultraviolet
EDS	:	Energy Dispersive X-ray Spectroscopy
TEM	:	Transmission Electron Microscopy
XRD	:	X-ray Diffraction
SAM	:	Self-Assembled Monolayers
EDC	:	Ethyl (dimethylaminopropyl) carbodiimide
NHS	:	N-hydroxysuccinimide
PBS	:	Phosphate Buffered Saline
RFU	:	Relative Fluorescence Unit
LOD	:	Limit of Detection
GPS	:	(3-glycidyloxy- propyl) 4 trimethoxysilane
LED	:	Light Emitting Diode
CFU	:	Colony Forming Unit
TB	:	Tuberculosis
HIV	:	Human Immunodeficiency Virus
3TAA	:	3-thiophene acetic acid
5SSA	:	5-sulfosalicylic acid
TIA	:	Technology Innovation Agency

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Chapter 1

Introduction

My academic career started in 1982 when I was appointed as Senior Lecturer in the Department of Electrical & Electronic Engineering at Stellenbosch University.

The aim of this dissertation is to tell the story of a research career spanning 34 years, starting with the design of high-voltage diodes and evolving to different aspects of superconductivity and finally shifting focus to nanosensors. The story will be contextualized by a trail of journal publications that will highlight the contributions along the way.

1.1 Layout of the dissertation

This dissertation will highlight a number of distinct phases in my research career:

- The semiconductor phase will be highlighted in Chapter 2 and will include the contributions relating to high-voltage diode design, a quick detour to microwave switches, and Monte Carlo particle simulation.
- In Chapter 3 the superconductor device research that was done during my sabbatical at *GEC Hirst Research Centre* is highlighted.
- The research that was done on low-T_C logical circuits during my sabbatical at the University of California at Berkeley is described in Chapter 4, as well as the subsequent research collaboration.
- In Chapter 5 the independent research on low-T_c superconductor research at Stellenbosch University is put in perspective. This includes the development of advanced CAD tools.
- The work that was done on the fabrication of high-T_c superconducting devices at Stellenbosch University is described in Chapter 6
- The nano-devices and biosensors story is told in Chapter 7

1.2 Summary

This dissertation is a narrative of the different phases in a research career of 34 years, and the relevant journal publications will give context to the contributions. A final conclusion will be given in Chapter 8.

Chapter 2

The semiconductor days

When I started my undergraduate studies in electronic engineering in 1972 at Stellenbosch University, calculations still had to be done with a slide rule and Johnson's baby powder, to ensure smooth operation with the required accuracy. The electronic revolution dawned on us when the first handheld scientific calculator, the HP-35, was announced by Hewlett-Packard in 1972 [1].

Professor Christo Viljoen, realizing the potential of microelectronics, established a small semiconductor fabrication facility in the Department of Electrical & Electronic Engineering during my undergraduate years. He persuaded me during my final year (in 1976) to continue with postgraduate studies, working on the characteristics of miniaturized printed spiral inductors on substrates, under his supervision. However, my decision to continue with my Master's degree probably had more to do with postponing military conscription than with an honest desire to learn.

Although it was a good decision, it also had quite an impact on my early career, as, towards the end of 1977, it was announced that military conscription was extended to two years, with a further obligation to do military camps over the ensuing twenty years. In order to get exemption from the obligatory military camps, I joined the Signal Corps of the SA Defense Force for four years, from 1978 to 1981, as a project engineer.

My academic career started in 1982 when I was appointed as Senior Lecturer in the Department of Electrical & Electronic Engineering at Stellenbosch University, earmarked to teach semiconductor physics – a topic that I knew very little of at that time.

2.1 High-voltage diodes

Upon my arrival at Stellenbosch an opportunity arose to investigate the viability of the local manufacture of high-voltage diodes. Keen to start a research career, I enrolled for a PhD with a focus on the design of high-voltage diodes, again with Professor Christo Viljoen as supervisor.

Typically, discrete high-voltage diodes are manufactured by taking a single silicon wafer, with a low n-type doping concentration, and then do a relatively shallow p-type diffusion to

establish the *pn*-junction. At high reverse bias voltages, most of the depletion region will be in the *n*-region, due to the low doping concentration, with a small portion of the depletion region in the highly doped *p*-region. A design challenge is that the diode should be thick enough to fully accommodate the depletion region at the maximum reverse bias voltage, but also thin enough to minimize the forward voltage when the diode is conducting.

Typically the depletion region width for high-voltage diodes can range from about 50 μm to more than 100 μm for reverse bias voltages from about 500 V to more than 1000 V. It is thus apparent that, at high reverse bias voltages, the electrical field (E) can be quite high, approaching the critical field, where the diode goes into reverse breakdown.

After the doping process, the whole wafer looks like a single diode with a very large area, and must thus be diced into thousands of smaller diodes. This is normally done by an etching process that must be deeper than the *pn*-junction, thus creating individual diodes on a single *n*-type substrate, which are then cut into completely separate diodes. A problematic consequence of the dicing process is that the E-field across the depletion region around the *pn*-junction can be substantially higher where the junction is exposed to air, than in the bulk region of the diode. Theoretically the etching process will create a smooth surface over the exposed part of the *pn*-junction, thus minimizing the increase in the E-field.

One of the main objectives of my doctoral research was to quantify the contribution of the edge geometry of the the diode, in order to optimize the breakdown voltage. To determine the potential distribution in a diode structure with a specific edge geometry, it was required to solve the two-dimensional Poisson equation, given by

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{q}{\epsilon_s} \left[\Gamma(x, y) + p - n \right] \tag{2.1.1}$$

where ψ is potential, q is electron charge, ϵ_s is the dielectric constant of silicon, Γ is the doping profile, and p and n is the hole- and electron concentration respectively. The electric field could then be calculated as

$$\vec{\mathbf{E}} = -\nabla \psi. \tag{2.1.2}$$

The algorithm was implemented on a VAX 11/785 minicomputer and it took about 1 to 2 hours to calculate the two-dimensional electric field distribution at a single reverse bias voltage value.

The simulated E-field distributions of a diode with three different edge geometries are shown in Figure 2.2. The reverse bias was 400 V and the E-field values were normalized with respect to the maximum electric field value (E_M).

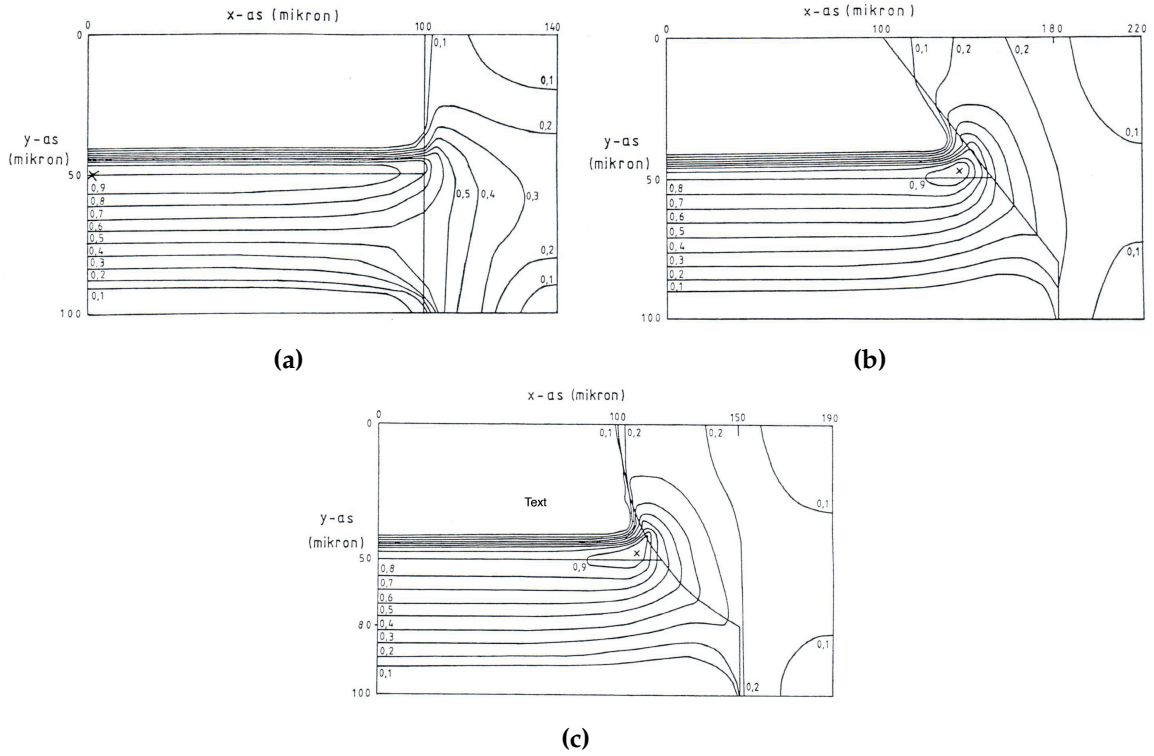


Figure 2.1: Normalized E-field distribution at a reverse bias of 400 V for (**a**) a diode structure with a 90° bevelled edge geometry, (**b**) a 45° bevelled edge geometry, and (**c**) an etched geometry. The maximum E-field point is indicated by $\times$. The pn-junction depth is 50 μm. From [2].

From Figure 2.1(a) it is apparent that, for a bevel angle of 90°, the maximum E-field occurs at the pn-junction and far removed from the edge. In Figure 2.1(b) and Figure 2.1(c) it can be seen that, as soon as the edge geometry changes from a 90° bevel angle, the point of maximum E-field moves towards the edge, and away from the actual pn-junction. The magnitude of the maximum E-field near the edge is always larger than the maximum bulk E-field. The edge geometry will thus always have a marked influence on the reverse breakdown voltage of a diode.

In order to determine the effect of edge geometries on the magnitude of the reverse breakdown voltage, the two-dimensional Poisson-solver was adapted to iteratively search for the avalanche breakdown point. Avalanche breakdown will occur when the so-called multiplication factor (M) becomes infinite. According to Kokosa and Davis [3] that will happen when

$$\int_{d'}^{d''} \alpha_i . \mathrm{d}\vec{x} = 1 \tag{2.1.3}$$

where d' and d'' are the depletion region edges at breakdown in the p- and n region, respectively, $\vec{x}$ a vector pointing in the direction of maximum change in potential, and α_i the

average ionization coefficient given by

$$\alpha_i = 1.07 \times 10^6 \, e^{-1.65\times 10^6/|E|}. \tag{2.1.4}$$

The reverse breakdown voltage was determined by iteratively changing the reverse voltage, and then solving for E, until (2.1.3) was satisfied. The execution time for the calculation of the breakdown voltage of a diode structure was about 10 hours on a VAX 11/785 minicomputer.

The very long execution times of the computer simulations made it somewhat impractical as a design tool. It was thus decided to try to look whether simpler design procedures could not be found that would speed up the design process, but were still accurate enough when compared to the computer simulation results.

In two journal publications [4, 5] an approximation procedure is described to estimate the E-field in diode structures with bevelled edge geometries, when the one-dimensional breakdown voltage is known. The one-dimensional breakdown voltage was obtained by solving Poisson's equation in one-dimension, similar to the procedure that was discussed above for the two-dimensional case, but in a fraction of the time. One-dimensional breakdown voltage values can also be obtained from graphs [6].

The value of the E-field at reverse breakdown was now required and would normally entail that the one-dimensional Poisson equation be solved at the breakdown voltage. A much faster procedure was proposed, where the one-dimensional E-field (E_N) could be approximated by

$$E_N = \frac{qN_{av}d}{\epsilon_s} \tag{2.1.5}$$

where d is the depletion region width on the p-side of the junction, and N_{av} the average doping concentration in the depletion region on the p-side of the junction. The average doping concentration was calculated as

$$N_{av} = \frac{1}{d} \int_{x_j-d}^{x_j} N(x).\mathrm{d}x \tag{2.1.6}$$

where x_j is the junction depth and $N(x)$ the doping profile. The approximated values of E_N were in very good agreement with the exact values that were calculated with the one-dimensional Poisson solver (within 2.1%), for a range of one-dimensional diode profiles at numerous reverse bias voltages.

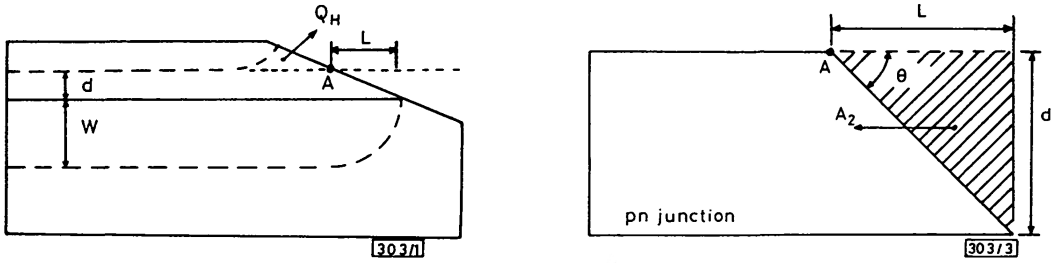
It was postulated [4] that the maximum E-field in a two-dimensional diode structure with a specified edge geometry (E_B) could be calculated as

$$E_B = E_N + \delta E \tag{2.1.7}$$

where δE is the increase in the E-field above the one-dimensional value (E_N), as approxi-

mated by (2.1.5).

A reverse biased diode structure with a negative bevel angle is shown in Figure 2.2(a), where W and d are the widths of the depletion region in the n- and p-region, respectively. In theory all charge within a coupling distance (L) from point A will be redistributed and appear as Q_H, as shown in Figure 2.2(a).



(a) **(b)**

Figure 2.2: Diode structure with negative bevel angle, showing (**a**) the depletion region parameters, and (**b**) the depletion region on the p-side of the junction at the critical angle (θ_c). From [4].

Furthermore, a critical angle (θ_c) was defined [4] as

$$\theta_c = \tan^{-1}(d/L), \tag{2.1.8}$$

when the area (A_2) is a maximum, as is shown in Figure 2.2(b). The coupling distance was defined as

$$L = (W - d)/2. \tag{2.1.9}$$

Theoretically the maximum E-field point will start to shift away from the pn-junction for all negative bevel angles where $\theta > \theta_c$. It was shown in [4] that, for $\theta > \theta_c$, the increase in E-field could be modelled by

$$\delta E = \left[\frac{qN_{av}}{2\pi\epsilon_s d \tan(\theta_c)}\right] A_2 \tag{2.1.10}$$

where A_2 is the area defined as

$$A_2 = \frac{d^2}{2\tan(\theta)} \tag{2.1.11}$$

and shown in Figure 2.2(b).

The approximated values for the increase in E-field were within 2% of the values obtained from two-dimensional simulations for all structures that were analyzed.

In [4] negative bevel angles were classified as either large ($\theta > \theta_c$) or small ($\theta \leq \theta_c$). For large angles the increase in E-field is given by (2.1.10), which can be simplified from (2.1.8)

and (2.1.11) to give

$$\delta E_L = \frac{qN_{av}L}{4\pi\epsilon_s \tan(\theta)}, \tag{2.1.12}$$

and for small negative bevel angles it was shown that the increase in E-field could be calculated from

$$\delta E_S = \frac{qN_{av}L^2 \tan(\theta)}{4\pi\epsilon_s d}. \tag{2.1.13}$$

Further investigation [5] showed that the accuracy of the prediction model was reduced markedly in the interval from θ_c to 45°. This was attributed to the discontinuity in the predictions of the two models at the critical angle, as is shown in Figure 2.3(a).

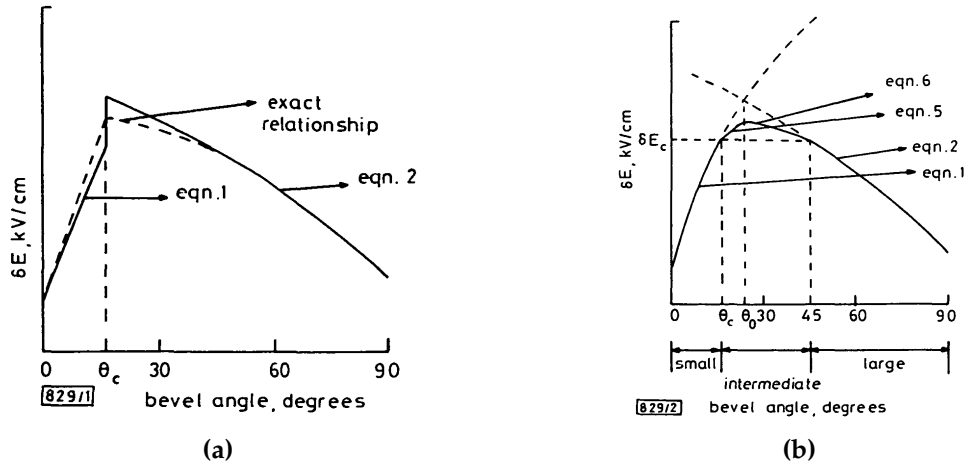


Figure 2.3: The increase in E-field as a function of the negative bevel angle at a constant reverse bias voltage, showing (**a**) the discontinuity in the predicted values at θ_c, and (**b**) the predicted values when the discontinuity is removed. From [5].

An approximation model was proposed for the mentioned interval by definition of a transition angle (θ_o) where the values of the two prediction models are the same, i.e. where $\delta E_L = \delta E_S$, as is shown in Figure 2.3(b). The transition angle is given by

$$\theta_o = \tan^{-1}(\sqrt{d/L}) = \tan^{-1}\left[\sqrt{\tan(\theta_c)}\right]. \tag{2.1.14}$$

In order to make the prediction model continuous for all negative bevel angles, ranging from small-, to intermediate-, to large bevel angles. The increase in the E-field over the

whole range of bevel angles was modelled as

$$\delta E = \begin{cases} \delta E_S & \theta \leq \theta_c \quad \text{(eqn. 1 in Figure 2.3)} \\ (\delta E_S + \delta E_C)/2 & \theta_c < \theta \leq \theta_o \quad \text{(eqn. 5 in Figure 2.3)} \\ (\delta E_L + \delta E_C)/2 & \theta_o < \theta < 45^\circ \quad \text{(eqn. 6 in Figure 2.3)} \\ \delta E_L & \theta \geq 45^\circ \quad \text{(eqn. 2 in Figure 2.3)} \end{cases} \tag{2.1.15}$$

where δE_C was defined as the value of the increase of the E-field when $\theta = \theta_c$.

The predicted values for the total E-field were within 5% of the simulated values for all the test structures with small and intermediate negative bevel angles.

A computer programme was developed that implemented the approximate procedures to efficiently determine the two-dimensional breakdown voltage of diodes with negative bevel angles ranging from small to large. Diodes with etched geometries, as shown in Figure 2.1(c), was also successfully incorporated by the calculation of an equivalent negative bevel angle [2].

2.2 High-frequency diode applications

After graduating with my PhD in March 1986 my research started branching out to other diode related areas, such as high-frequency diode applications and also more advanced diode simulation techniques.

In 1987 a need was identified by my PhD co-supervisor, Prof PW van der Walt, to develop an RF switch for use in a television repeater station, where two receiving antennas had to be connected to the system by a double-pole change-over RF switch, depending on the quality of the receiving antenna's signal. A schematic of the system is shown in Figure 2.4.

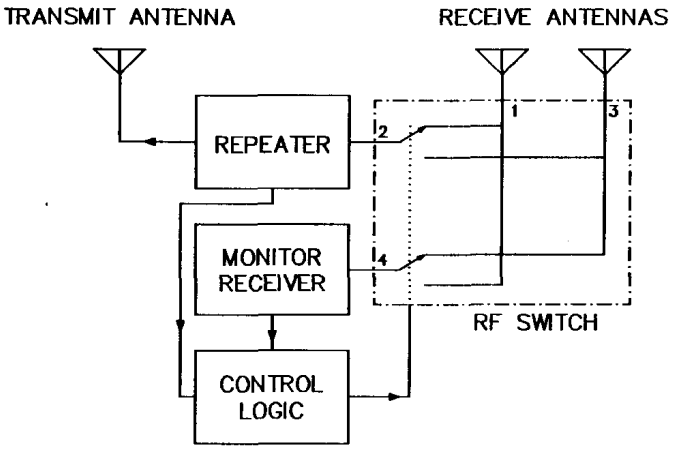


Figure 2.4: Space diversity switching system for television repeater station. From [7].

The switch had to be designed for use in UHF Band V (typically from 580 MHz to 860 MHz). It was specified that one should be able to add monitoring equipment to an existing

repeater station, as shown in Figure 2.4, without retuning of the RF circuits. This required a VSWR less than 1.1:1. In order to eliminate co-channel interference it was also specified that the channel isolation should be more than 60 dB when the isolation is in the off position.

It was decided to implement a distributed bandpass filter with PIN-diodes as switching elements, roughly covering UHF Band V, with the necessary elements to provide DC biasing paths and elements to compensate for PIN-diode parasitics when forward- or reverse biased. The general bandpass filter concept is shown in Figure 2.5.

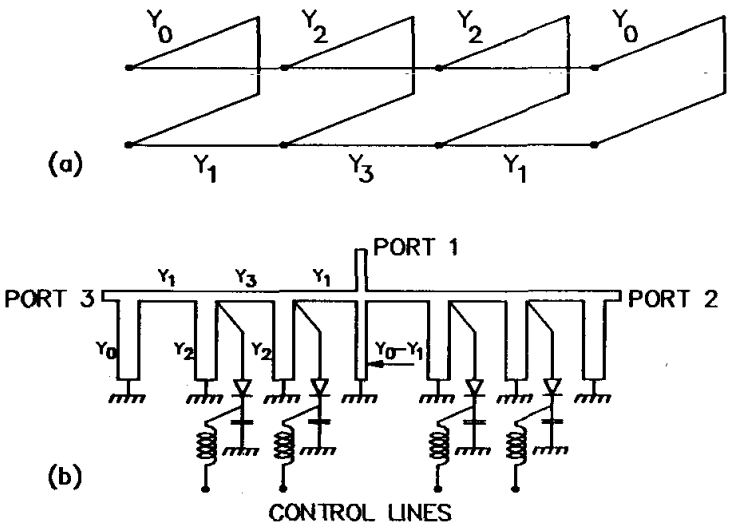


Figure 2.5: Basic bandpass filter concept. (**a**) Structure for PIN-diode switch. The electrical length of the transmission line elements is 90° at the centre frequency. (**b**) Stripline layout of matched PIN-diode switch, based on the filter in (a). From [7].

The filter design, however, was not a practical proposition for UHF implementation, as each section of the filter is a quarter wavelength long (i.e. an electrical length of 90°) [8]. For example, for a filter with a centre frequency of 600 MHz, that would result in section lengths of 125 mm each, and arm lengths of 375 mm each, for a switch with two shunt diodes per arm.

In our case, a compact version of the filter shown in Figure 2.5, was designed and constructed [7], with electrical section lengths of 30°. The stripline implementation of the four port double-pole PIN-diode switch is shown in Figure 2.6. The diodes were separated by a sixth of a wavelength, which is close to optimum for maximum isolation. The short circuit stubs provided the DC bias to the diodes and also served as protection against lightning discharges. The open circuit stubs provided the ability to compensate for the junction capacitances of reverse biased diodes.

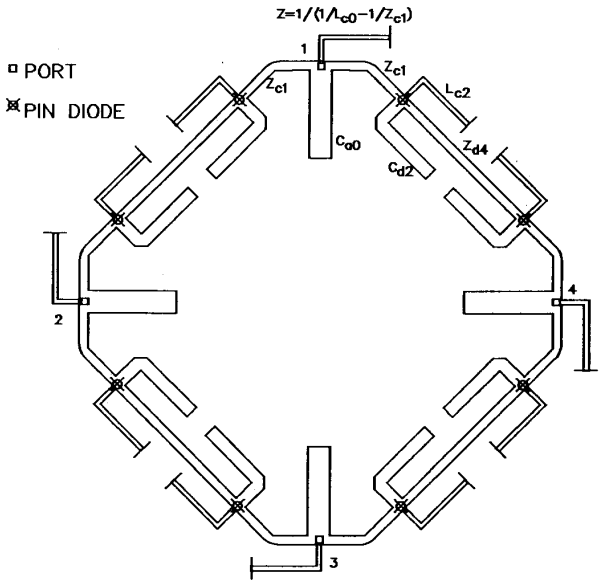


Figure 2.6: Stripline form of a four port double-pole PIN-diode switch. The electrical length of the transmission line elements is 30° at the centre frequency of the filter. Element values relate to Figure 2.7(d). From [7].

The steps in the design of the 8^{th} order Chebychev filter is shown in Figure 2.7(a)–(d). The equivalent circuit of the filter on which the final design is based, is shown in Figure 2.7(d).

The physical construction of the final switch is shown in Figure 2.8. All lines were in 10×10 mm square channels that were machined in aluminum. Square brass centre conductors were used for the open circuit stubs, while copper wire was used for the centre conductors of the other lines. The open circuit stubs were kept in place by shims of low-loss foam, which, in turn, supported the copper wire lines. The port connections were made with *N* connectors.

The parasitic series inductance of the shunt mounted diodes was resonated out at the centre frequency of the switch by mounting the diode in series with a capacitor, as shown in Figure 2.6. Mylar plastic film was used as dielectric for disc capacitors, which formed part of the diode mounts. The junction capacitance of the shunt-mounted diodes was compensated for by the reduction of the length of the open circuit stub next to the diode. HP5082-3101 PIN-diodes were used in the switch.

The best and worst measured port reflection coefficients of the four-port switch are shown in Figure 2.9, and the measured isolation between two ports in Figure 2.10.

A four-port two-pole RF switch for television broadcasting was successfully designed and constructed. The measured reflection coefficients (Figure 2.9) confirmed that the target VSWR of 1.1:1 was achieved over an operating bandwidth of 650–860 MHz. The measured isolation between arms in the blocking state was better than 65 dB (Figure 2.10), while the measured insertion loss was less than 0.3 dB over the operating bandwidth.

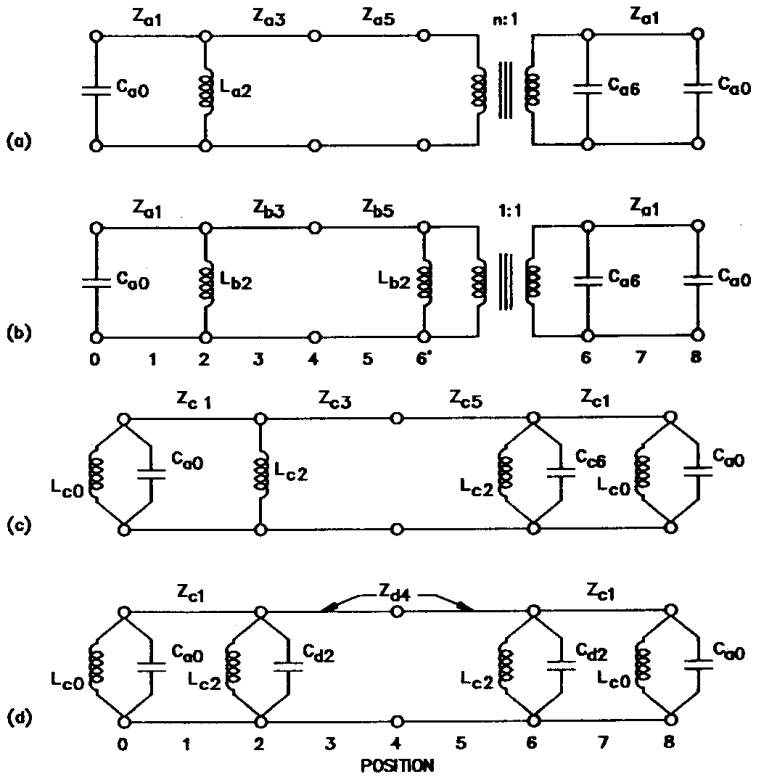


Figure 2.7: Steps in the synthesis of the filter. (**a**) Synthesized prototype. (**b**) Transformer removed with Kuroda transformation. (**c**) Further Kuroda transformation to obtain shorted stubs at the ends of the filter. (**d**) Final symmetrical filter with resonators spaced 60° (electrical) apart at the centre frequency. The capacitive elements are used to compensate for PIN-diode junction capacitance. From [7].

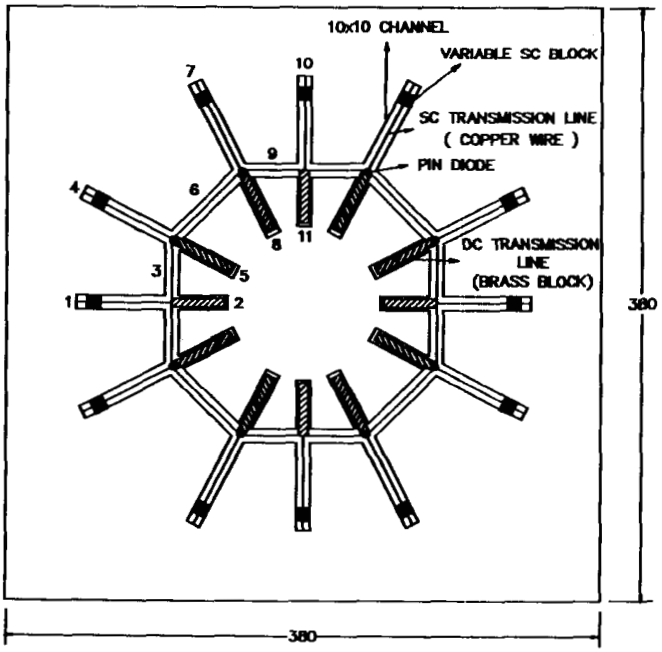


Figure 2.8: Physical construction of the PIN-diode RF switch. From [7].

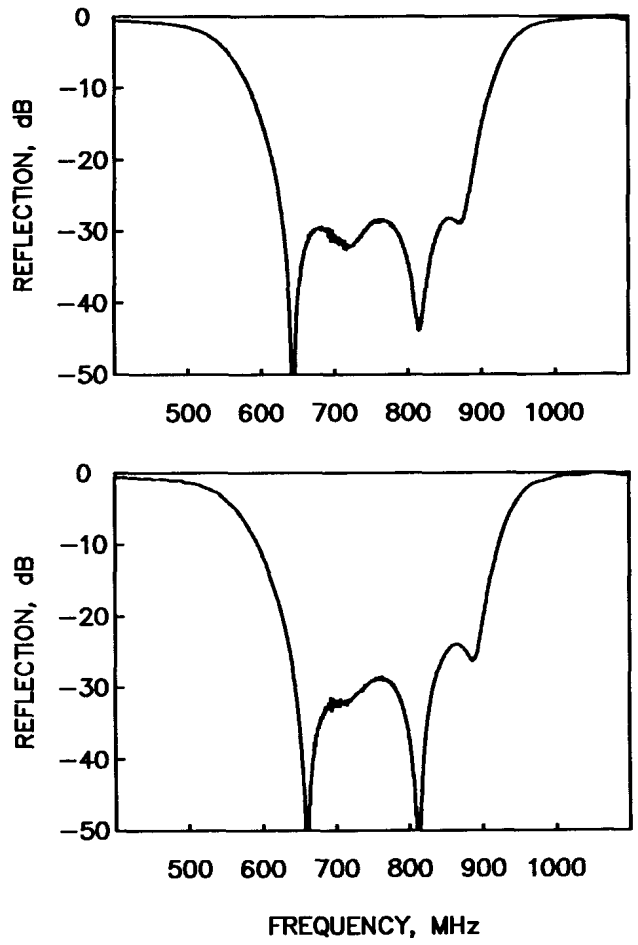


Figure 2.9: The best and worst measured port reflection coefficients of the switch. From [7].

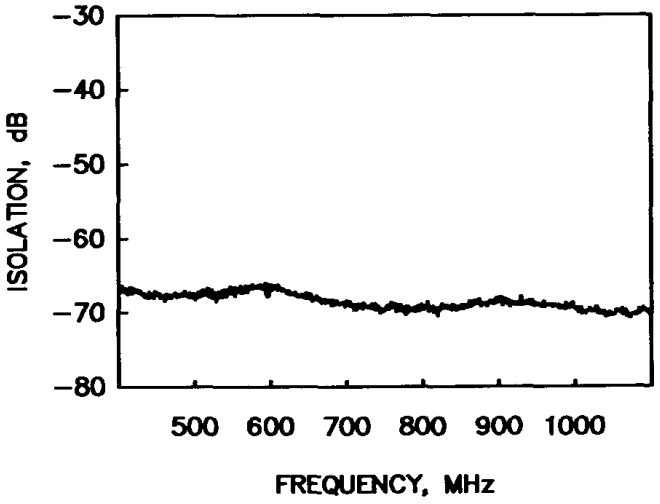


Figure 2.10: Measured isolation between two ports. From [7].

2.3 Monte Carlo particle simulation of microwave diode structures

Our research on high-frequency diode applications almost naturally branched out to more sophisticated simulation methods, to get a more fundamental understanding of semiconductor device behavior, specifically devices that can be used for the generation of AC power, such as Gunn- and IMPATT diodes [9].

In order to understand the inherent oscillatory capabilities of (say) a Gunn-diode, it is important to understand and also simulate the fundamental properties of the applicable semiconductor materials, something that is not possible using conventional simulation techniques, as was used in the simulation of the high-voltage diodes that were discussed in Section 2.1.

Kurosawa [10] first reported on the use of the Monte Carlo particle simulation technique for semiconductor materials and devices in 1966. The Monte Carlo technique is used to model physical processes that are based on probability distributions, such as in the case of semiconductor materials. In semiconductor devices this technique tracks the dynamics of charge carriers in a specified device geometry, when subjected to external forces, such as an applied voltage or current. The technique is inherently computationally intense, as a large number of charge carriers (typically more than 25 000) have to be tracked for the full duration of the simulation, for the results to be accurate. This entails that the electric field needs to be determined throughout the structure and that the effect of the field on each charge carrier has to be determined. The latter includes the movement of a charge carrier under the influence of the electric field and also the statistical determination of the possible particle scattering process that may take place. These calculations will put the charge carriers statistically at a different position at time $t + \delta t$, which will have an influence on the electric field throughout the structure. The new electric field values thus need to be calculated again and the process is thus repeated for the duration of the simulation period. In this way all the charge carriers are tracked and terminal characteristics, such as current and/or voltage, can be determined. A flow diagram of the simulation process [11] is shown in Figure 2.11.

A PhD student, Robert van Zyl, developed Monte Carlo particle simulation software and successfully used it in the design and optimization of GaAs Gunn-diodes [12]. It was shown that a fundamental understanding of the energy band structure of a semiconductor, i.e. an electron's energy with respect to its wave vector $\mathbf{k}$, was important, as that was indicative of the energy states that electrons can occupy, and thus the dynamic behavior of a device.

When electron transport is studied it is sufficient to look at the local band minima, as electrons are usually located near the bottom of the energy band valleys. At low electron energy values the energy-wave vector ($E - \mathbf{k}$) relationship can be approximated by parabolas [13].

In Figure 2.12 [14] a two-valley parabolic approximation is shown for GaAs. This approximation was implemented in the Monte Carlo simulation software and is sufficient for most moderate-field applications.

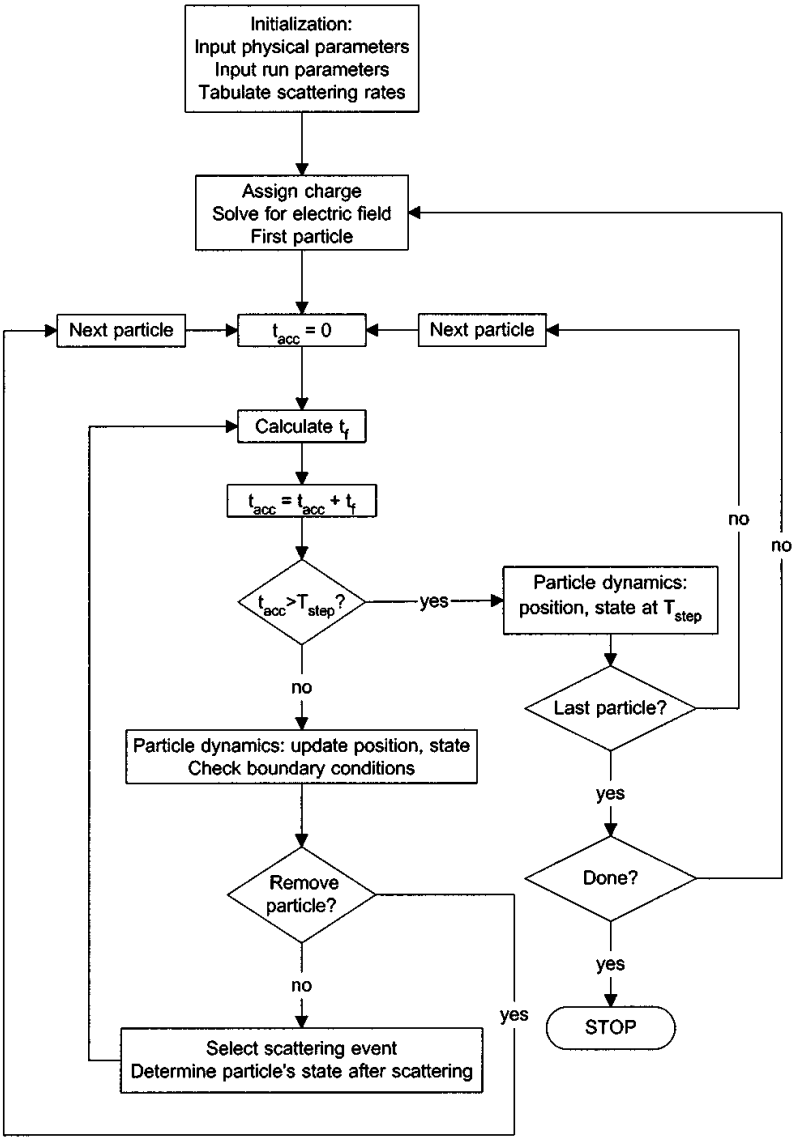


Figure 2.11: Flow diagram of a typical Monte Carlo device simulation algorithm. From [11].

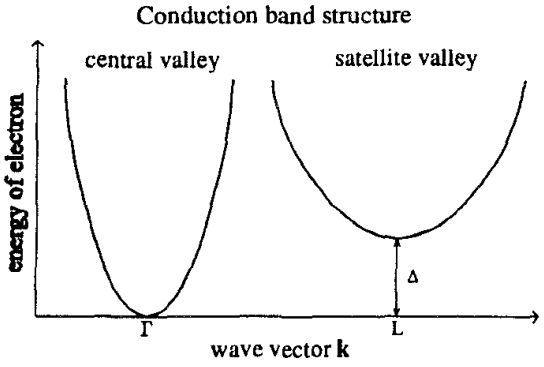


Figure 2.12: Parabolic two-valley approximation of the energy band structure of GaAs, showing the central valley (Γ) and one satellite (L) valley. The energy gap (Δ) is the energy that is required for an electron to jump from the central valley to the satellite valley. From [14].

With no bias applied to the GaAs, virtually all the electrons will occupy the Γ-valley, because their individual thermal energy values will be less than the energy gap (Δ). With an increase in bias an increasing number of electrons are accelerated and they may gain sufficient energy ($> \Delta$) to be transferred to the L-valley. This phenomenon is known as the *transferred electron mechanism*.

A bulk GaAs sample (Δ=0.36 eV) was simulated at different bias values to verify the transferred electron mechanism [14], by looking at the electron occupancy of the Γ- and L-valley. The simulated results are shown in Figure 2.13 at electric field values of 0.1 MV/m, 0.4 MV/m and 1 MV/m, respectively.

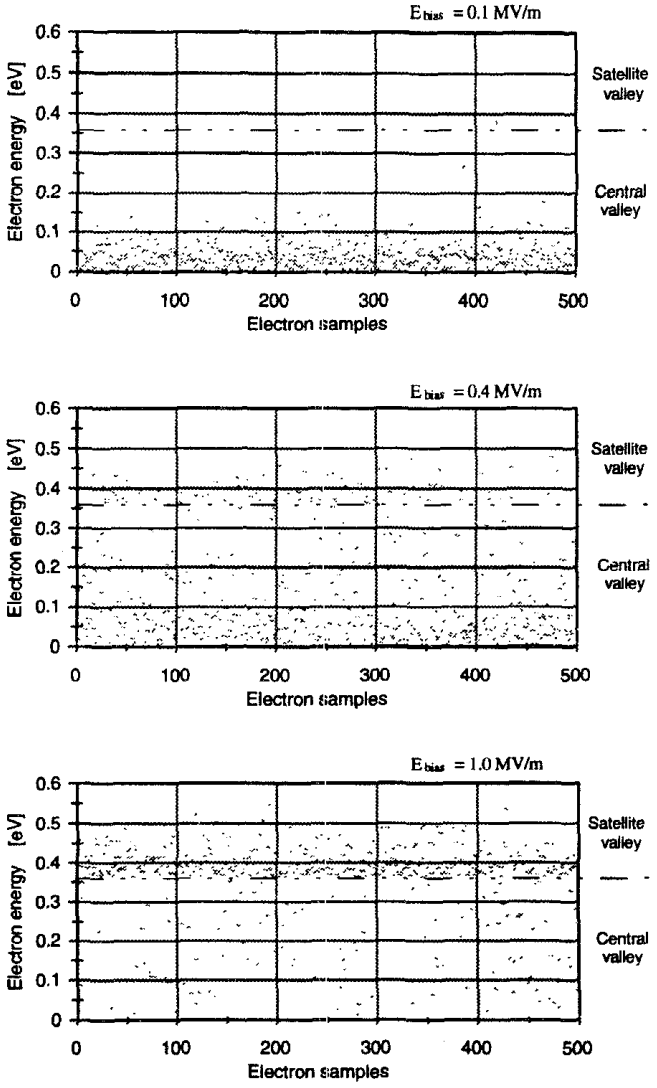


Figure 2.13: Valley occupation of electrons in bulk GaAs for three applied electric field values, namely 0.1 MV/m, 0.4 MV/m and 1 MV/m, respectively. From [14].

It is quite clear from Figure 2.13 that an ever increasing number of electrons will gain enough energy (0.36 eV for GaAs) to be transferred from the Γ- to the L-valley as the bias is increased, with a significant electron population in the L-valley at 1 MV/m.

The electrons that have been transferred to the L-valley will immediately move slower, due to an increase in their effective mass. This will result in a decrease in the average drift velocity, and thus the current, as the electric field is increased. A region of negative differential resistance (NDR) can thus occur for electric fields above a certain threshold value. This phenomenon is important as it is the fundamental reason why oscillatory behavior is possible in these type of devices. The simulated steady-state average electron drift velocity of a bulk sample of GaAs at room temperature (T=300 K) is shown in Figure 2.14.

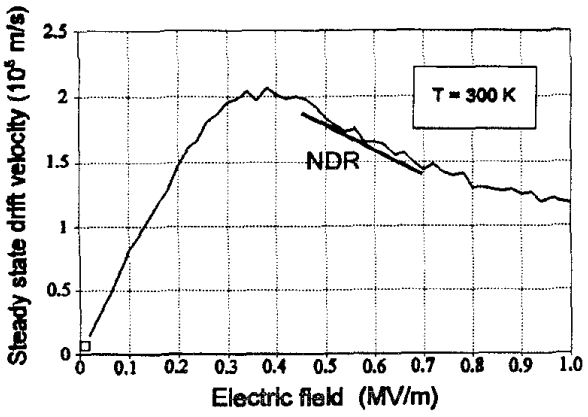


Figure 2.14: Simulated steady-state average electron drift velocity of a bulk sample of GaAs at room temperature (T=300 K). The NDR region is shown. From [14].

It is clear that a negative differential resistance (NDR) region is starting to form at an electric field value of about 0.4 MV/m for a bulk GaAs sample.

An excerpt from a laboratory notebook of J.B. Gunn is shown in Figure 2.15. On the line for 704 V, he has written the word "noisy" (underlined in red). He later described it as the "most important single word" he has ever written. He had inadvertently observed the NDR region when the applied voltage was increased to 704 V.

The reason why the formation of an NDR region can lead to oscillations is not straightforward, but depends on the formation of so-called Gunn-domains that sustainably traverse a biased GaAs sample with length L, as shown in Figure 2.16. For Gunn-domains to develop, the electric field ($E_o = V_o/L$) must be high enough to bias the device in the NDR region. For a Gunn-domain to form, it is assumed that a local charge perturbation occurs at a specific time instance. The perturbation can be, for example, the result of local thermal drift of electrons. The charge perturbation may lead, for example, to a local increase in electric field at a specific point, and thus a local increase in drift velocity (see Figure 2.14). This will cause a local pileup of charge, due to the slower drift velocity of the electrons immediately to the right of the perturbation. The initial charge perturbation will grow as it drifts towards the anode and will eventually form a stable charge dipole domain, known as a Gunn-domain. As the Gunn-domain is absorbed by the anode, the average electric field will rise, and domain formation will start again. The sustained formation and absorption of Gunn-domains

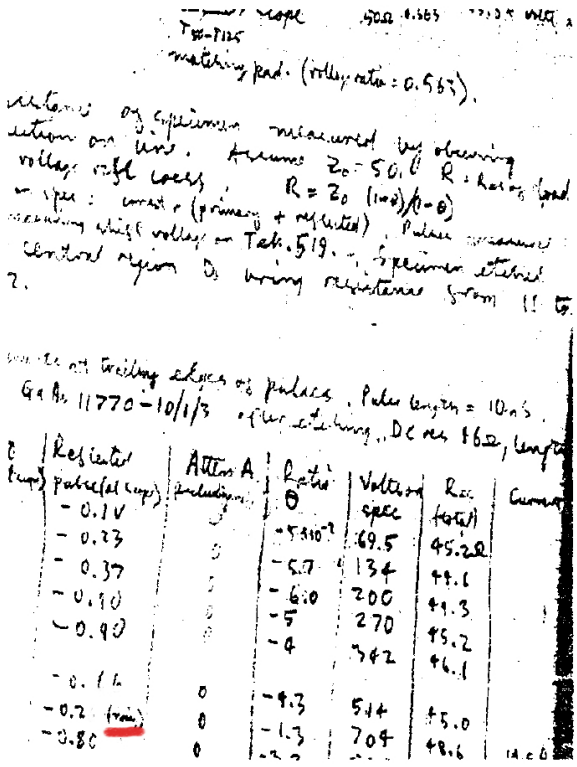


Figure 2.15: An excerpt from a laboratory notebook of J.B. Gunn on which he made the discovery of the Gunn-effect. The word "noisy" is underlined in red. From [14].

are known as the Gunn-mode, and the frequency of oscillation is determined by the length of the device (L) and also the applied bias voltage.

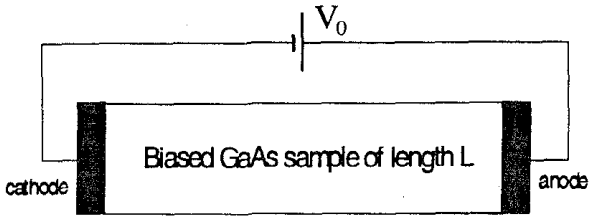


Figure 2.16: Schematic of a biased GaAs device with length L. From [14].

The Gunn-mode was verified by Monte Carlo simulation for a 5 μm GaAs device, uniformly doped with a concentration of 10^{15} cm^{-3} and at a bias voltage of 5 V. The oscillation frequency was approximately 25 GHz.

The simulation results are shown in Figure 2.17. In Figure 2.17(a) the formation and drift of the charge dipole (Gunn-domain) is clearly observed at t=90 ps and t=110 ps, respectively. At t=130 ps the absorption of the Gunn-domain is observed at the anode (on the right), while a new Gunn-domain is being formed at the cathode (on the left). At t=150 ps the newly formed Gunn-domain is seen drifting towards the anode again. In Figure 2.17(b) the electric

field formation is observed as a result of the charge dipole formation, again verifying that the device is operating in the Gunn-mode.

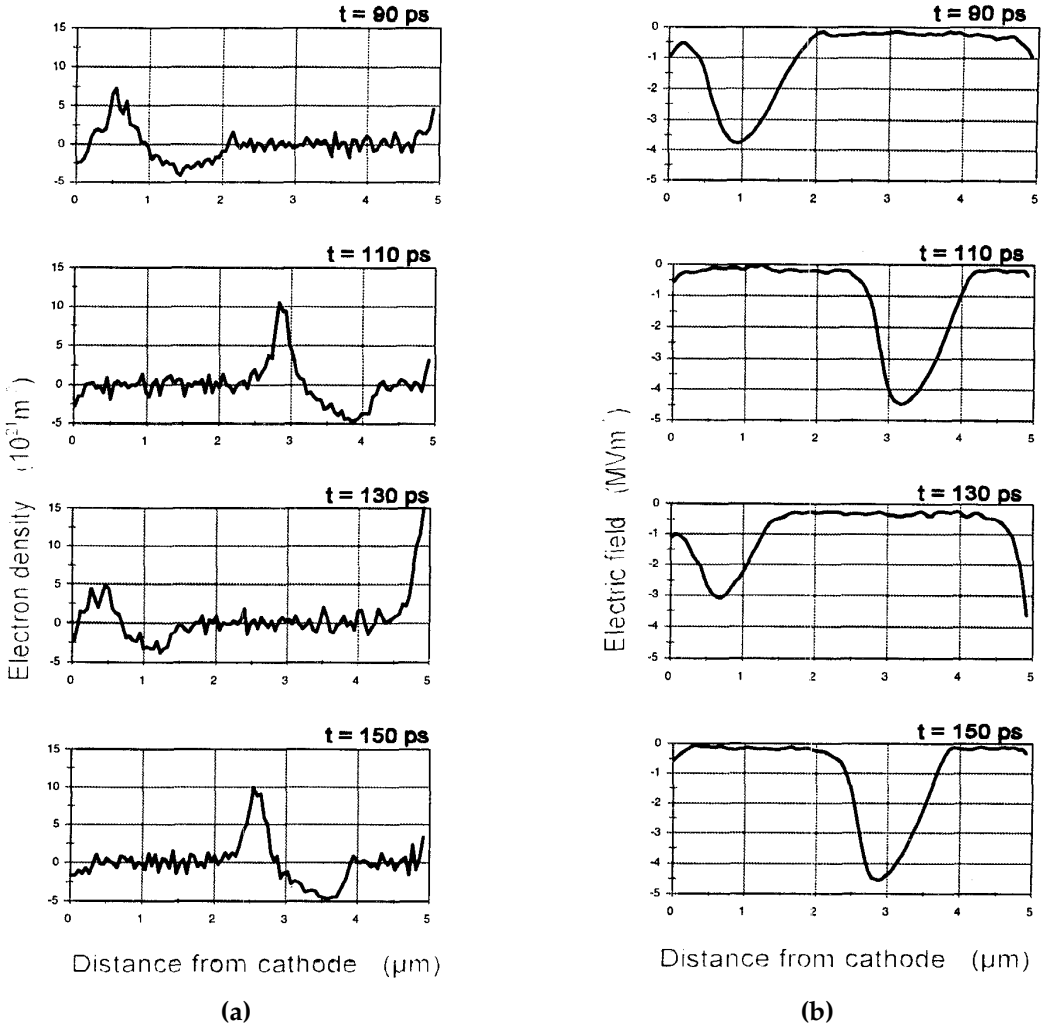


Figure 2.17: Simulated Gunn-domain formation for a 5 μm GaAs device, uniformly doped with a concentration of 10^{15} cm^{-3} and at a bias voltage of 5 V. (**a**) Simulated charge distribution at 4 different time instances. (**b**) Simulated electric field formation at 4 different time instances as a result of the charge dipole formation. From [14].

As was previously mentioned, the Monte Carlo simulation of semiconductor devices is inherently computationally intensive, leading to excessively long execution times. That was especially true when the research was conducted during the 1990's. However, the fact that the dynamics of every individual electron can be calculated separately, makes the Monte Carlo method suitable for parallel implementation in order to reduce computation time.

As part of his PhD research, Robert van Zyl, implemented an efficient parallel implementation of the Monte Carlo method on a network of personal computers [11]. The implementation was based on a parallel virtual machine (PVM) master-slave model, where the particles were divided into sub-ensembles en then sent to separate processors (slaves). The

slaves were dedicated to solving the particle dynamics. The results were sent to the master, which used the results to compute the new electric field distribution (by solving Poisson's equation). The updated field distribution was then redistributed to the slaves to calculate the particle dynamics again. A flow diagram of the parallel implementation is shown in Figure 2.18.

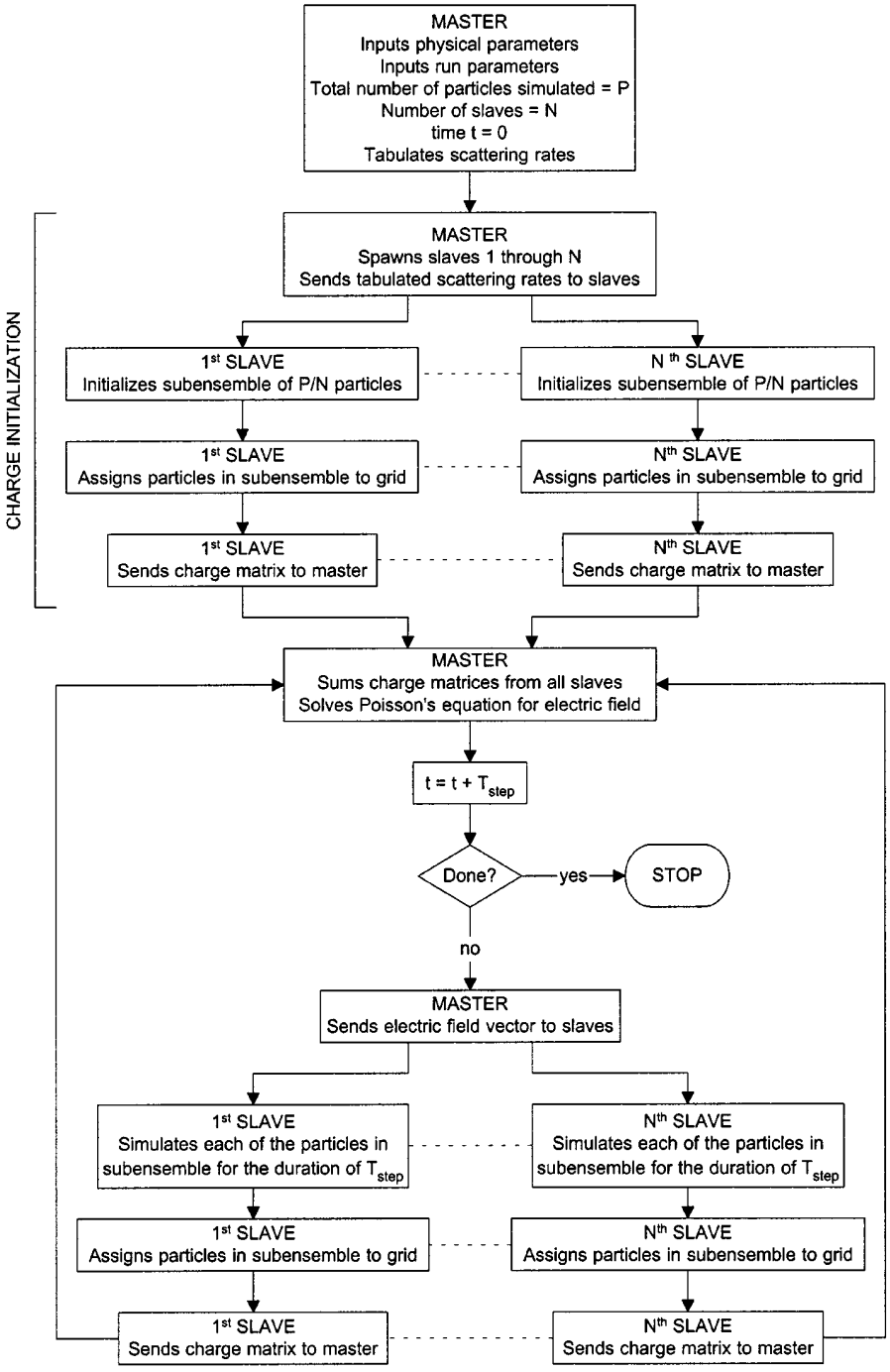


Figure 2.18: Flow diagram of the parallel implementation of the Monte Carlo device simulation algorithm. From [11].

One of the negative consequences of the mentioned parallel implementation, was that the slaves were idle while the master was updating the electric field distribution. A novel leap-frog (LF) algorithm was proposed to address this problem [11]. The algorithm was based on the consecutive assignment of charge and the updating of the electric field distribution at intermediate points in time. This led to a leap-frog arrangement of the two processes, and resulted in less time wasted, because the master solved Poisson's equation concurrently with the charge simulations by the slaves.

The efficiency and accuracy of the parallel implementation and the leap-frog implementation were investigated by comparing the results for a one-dimensional millimeter-wave Gunn-effect relaxation oscillator to those obtained by Tully [15]. An ensemble of 25 000 particles was divided equally among the slave processors, where each simulated particle actually represented 10 900 actual charge particles. The terminal currents were calculated by taking the cross section area as 5×10^{-5} cm^2.

The doping profile of the Gunn-diode is shown in Figure 2.19(a). The complete relaxation oscillator was modelled as a parallel resonant circuit and is shown in Figure 2.19(b). The diode was divided into 128 segments for the calculation of the electric field distribution, and 5 fs time steps were used. The 30 ps Monte Carlo simulation was implemented on 19 slaves (Pentium computers running at 60 MHz clock speeds) and both the PVM and leap-frog algorithms were tested.

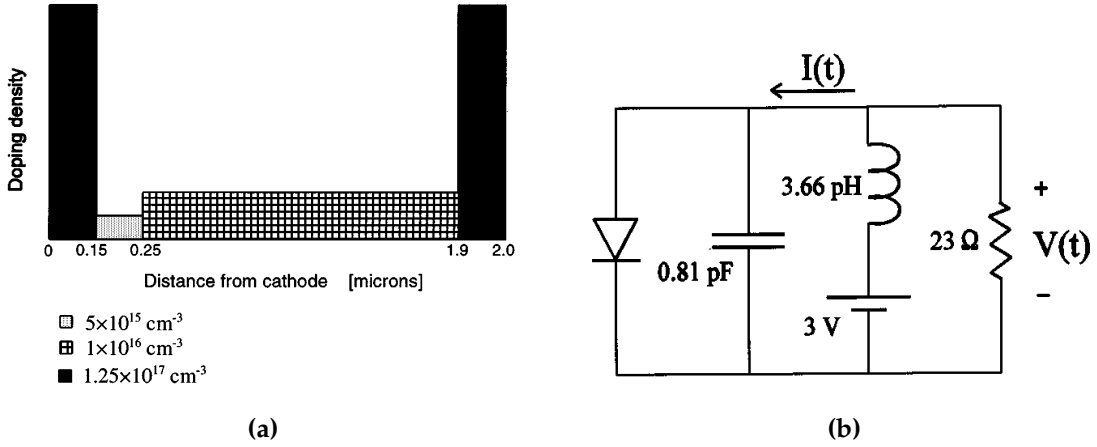


Figure 2.19: (**a**) The doping profile of the simulated Gunn-diode. The active region is sandwiched between the highly doped cathode and anode regions. (**b**) The equivalent circuit of the simulated relaxation oscillator. The diode represents the Monte Carlo simulation. The Gunn-diode is biased with a 3 V battery. The oscillator is connected to a 23 Ω load resistance. From [11].

The simulated values for the voltage, $V(t)$, and the current, $I(t)$, as defined in Figure 2.19(b) and obtained by the implementation of the leap-frog algorithm, are shown in Figure 2.20. The results were identical to the values predicted by the PVM algorithm and also in excellent agreement with the results obtained by Tully [15].

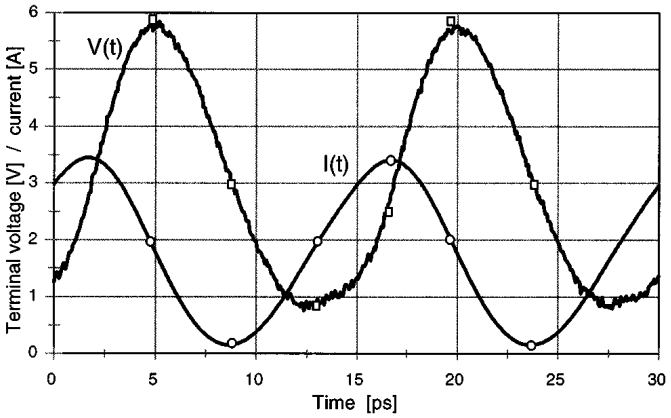


Figure 2.20: The simulated voltage, $V(t)$, and current, $I(t)$, waveforms, as obtained by implementation of the leap-frog algorithm. The voltage and current waveforms obtained by Tully [15] are indicated by the squares and circles, respectively. From [11].

With the 19 slaves, the leap-frog implementation completed the 30 ps simulation in 2825 s, while the PVM algorithm required 3383 s to complete[1]. The much better efficiency of the leap-frog implementation is also apparent from the speed-up curves, shown in Figure 2.21. Also noticeable is the flattening of the speed-up curves as the number of slaves are increased. This was due to the ever increasing master-slave communication time as the number of slaves were increased.

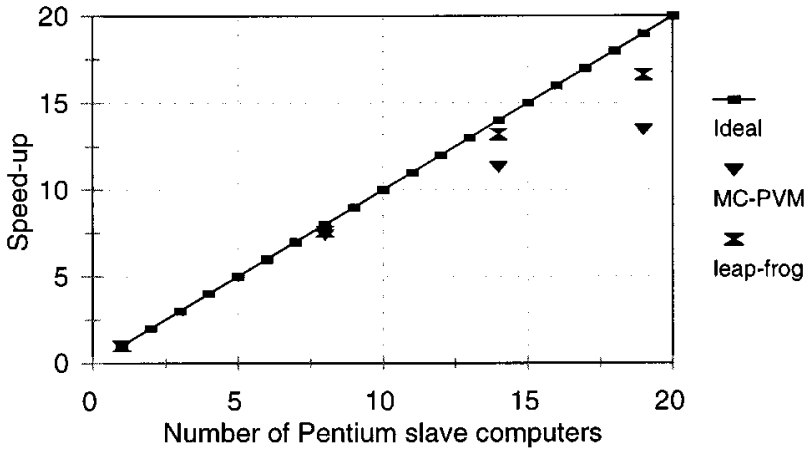


Figure 2.21: Speed-up comparison between the PVM and leap-frog algorithms, as a function of the number of slaves. The ideal (linear) speed-up curve is also shown. From [11].

One of the unique contributions from the dissertation of Robert van Zyl [12] was the incorporation of temperature as an integral part of the Monte Carlo particle simulation model. This model was used to develop an empirical prediction model for the operational frequency limits in bulk GaAs and GaN [16]. The model was based on the observation that the negative

[1] It is interesting to note that the same setup would execute in about a minute when current technology is used running at clock speeds of about 3 GHz.

differential resistance (NDR) phenomenon in the drift velocity-electric field relationship (see Figure 2.14) started to exhibit hysteretic behavior close to the operational frequency limit of the Gunn-effect. A positive slope in the NDR region of the curve would thus suggest that the operational frequency limit of a device has been exceeded. The simulated velocity-electric field relationships of GaAs (at different operating conditions) are shown in Figure 2.22. From Figure 2.22(a) it is apparent that, in the NDR region of the curve, the slopes remain negative, even in the hysteretic part of the curve. That would suggest that the device would be operational at 40 GHz and a temperature of 300 K. However, from Figure 2.22(b), it is clear that there is a portion of the hysteretic part of the curve, from 0.7×10^6 V/m to 0.8×10^6 V/m, that exhibits a positive slope. The device would thus not be operational at 100 GHz and a temperature of 500 K.

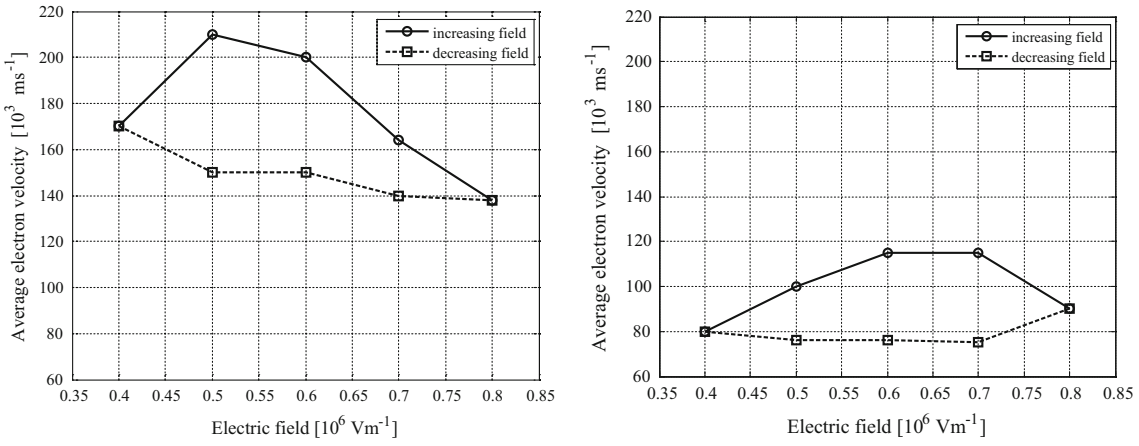


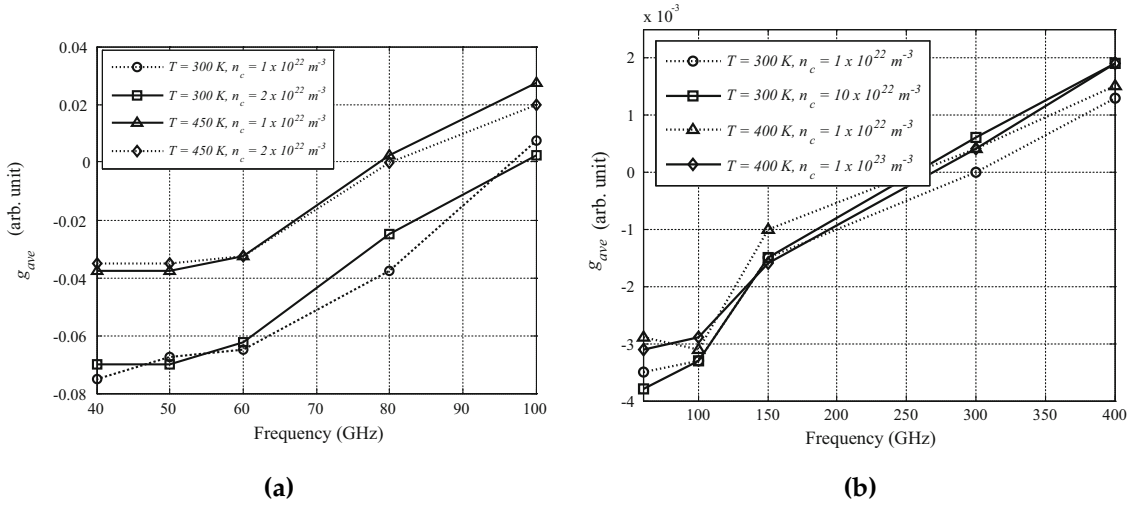
Figure 2.22: (**a**) Velocity-electric field characteristic curve of GaAs at 40 GHz, 300 K and doped at 1×10^{22} m^{-3}. (**b**) Velocity-electric field characteristic curve of GaAs at 100 GHz, 500 K and doped at 1×10^{22} m^{-3}. From [16].

In order to simplify the procedure, an average slope parameter was defined as

$$g_{ave} = \frac{1}{N} \sum_{i=1}^{N} \frac{\Delta v_i}{\Delta E_i} \tag{2.3.1}$$

where v is the average drift velocity of electrons, E the electric field and N the number of samples. The samples were taken over a complete cycle of the applied alternating electric field. This parameter gives a quantitative indication of the strength of the NDR mechanism and a negative value an indication that NDR does indeed exist in the material.

The simulated average slopes (g_{ave}) of the drift velocity-electric field (vE) relationship are shown in Figure 2.23 for bulk GaAs and GaN, respectively, as a function of frequency, temperature and doping level.



(a) **(b)**

Figure 2.23: (**a**) Average slope g_{ave} of the vE-curves of bulk GaAs as a function of operating frequency, temperature and doping level. (**b**) Average slope g_{ave} of the vE-curves of bulk GaN as a function of operating frequency, temperature and doping level. From [16].

It is clear from Figure 2.23(a) that the GaAs device reach its upper frequency limit of operation at about 80 GHz at 450 K and about 100 GHz at 300 K. The GaN device, on the other hand, will reach its upper frequency limit of operation between 255 GHz and 300 GHz, depending on the operating conditions.

2.4 Summary

A brief overview was given of my research contributions and the contributions of some of the research students that I supervised during the earlier parts of my academic career, with emphasis on semiconductor devices. My own PhD research contributions focussed on aspects of design optimization of high-voltage diodes, specifically the reverse breakdown voltage, while the research focus of my postgraduate students was steered towards the development of more sophisticated and accurate simulation tools for the design of microwave devices [17, 18]. These students paved the way for the excellent contributions on Monte Carlo particle simulation by Robert van Zyl during his Master's and PhD studies [19, 12].

Chapter 3

Superconducting device research – The start of a new chapter

Looking back, the 1987 visit of Dr Karl Gehring of *GEC Hirst Research Centre* in London had a life changing influence on my academic career. At the time he was the leader of the Instrumentation Group at *GEC Hirst Research Centre* and I remember our discussion about a possible sabbatical in front of our clean room facility quite vividly. I had just finished my PhD and the plan was to continue in the semiconductor field, possibly looking at advanced diffusion techniques. Dr Gehring persuaded me to come to *GEC Hirst Research Center*, as they had a well established VLSI Process Techniques Research Laboratory.

Our family arrived in London in January 1988, eager for the new adventure. Our enthusiasm was severely suppressed when we found out that I had made a little mistake with regards to the price of accommodation, not realizing that the apartment rent was quoted per week, and not per month. Our accommodation thus consumed quite a substantial chunk of my available *GEC* salary, £607 of the available £625. Our then Prime Minister, Mr PW Botha, did not help either, as the exchange rate dropped drastically every time that he spoke in public, making my Stellenbosch salary that was transferred to England less every month.

However, the year turned out to be quite successful – something that we could not envisage early in January 1988.

3.1 Superconducting tunnelling devices

Upon my arrival at *GEC Hirst Research Centre* I was ready to start the next step in my research career, but I did not realize that the discovery of high-temperature superconductivity in 1986 [20] would make the first step quite different to what was anticipated.

One of the activities in the Instrumentation Group, the group that Dr Gehring was leader of, was SQUID magnetometers. During our first meeting after my arrival Dr Gehring suggested that, in anticipation of the new possibilities of employing high-temperature superconductors, I should consider joining his group with the specific task to investigate alternatives to the standard in low-temperature superconducting switching devices, the Josephson

junction. The decision to join his group steered my career in a completely different direction.

3.1.1 Single-junction tunnelling

Virtually all superconducting devices are based on particles tunnelling through a very thin insulation layer. The tunnelling can either take place from a normal metal to a superconductor (NIS junction) or from superconductor to superconductor (SIS or Josephson junction). My first task was to study the current-voltage characteristics of single particle tunnelling. Tunnelling through SIS junctions was quite well understood [21], but the same could not be said for NIS junctions, due to phenomena such as subharmonic gap structures, branch imbalance and excess current (Andreev reflections). The intricate transport of so-called quasiparticles through NS and NIS junctions was eventually solved by using the solution of the Bogoliubov equations [22, 23, 24].

The stationary one-dimensional Bogoliubov equations for electrons and holes are given by

$$-(\hbar^2/2m)\frac{\partial^2 f(x)}{\partial x^2} - \mu f(x) + V f(x) + \Delta g(x) = E f(x) \tag{3.1.1}$$

and

$$(\hbar^2/2m)\frac{\partial^2 g(x)}{\partial x^2} + \mu g(x) - V g(x) + \Delta f(x) = E g(x) \tag{3.1.2}$$

respectively, where $f(x)$ and $g(x)$ are the wave function for electrons and holes, V the applied voltage, μ the chemical potential, $\hbar$ the reduced Planck constant, m the electron mass, Δ the superconductor band gap and E the energy.

From the equations it is evident that the superconductor band gap is the link between the two equations. Therefore, for a normal metal (Δ=0), there will be no coupling between the two wave functions, and the Bogoliubov equations will simplify to the Schrödinger equation for electrons and holes, respectively.

In [25], a solution for the Bogoliubov equations was presented for the equilibrium case (V=0), by using the Laplace transforms of the respective wave functions. If it is assumed that the Laplace transforms of the respective wave functions for electrons and holes are given by $F(s)$ and $G(s)$, the transformed Bogoliubov equations could be expressed as

$$-(\hbar^2/2m)[s^2F(s) - sf(0) - f'(0)] + \Delta G(s) = (\mu + E)F(s) \tag{3.1.3}$$

and

$$(\hbar^2/2m)[s^2G(s) - sg(0) - g'(0)] + \Delta F(s) = -(\mu - E)G(s). \tag{3.1.4}$$

For a *normal metal* the energy gap is zero (Δ=0) and, from (3.1.3) and (3.1.4), the respective

Laplace transforms could be written as

$$F(s) = \frac{sf(0) + f'(0)}{s^2 + 2m(\mu + E)/\hbar^2} = \frac{F_{n1}}{s + jq_+} + \frac{F_{n2}}{s - jq_+} \tag{3.1.5}$$

and

$$G(s) = \frac{sg(0) + g'(0)}{s^2 + 2m(\mu - E)/\hbar^2} = \frac{G_{n1}}{s + jq_-} + \frac{G_{n2}}{s - jq_-} \tag{3.1.6}$$

where

$$\begin{aligned} q_\pm^2 &= (2m/\hbar^2)(\mu \pm E) \\ F_{n1,2} &= \frac{\mp jq_+ f(0) + f'(0)}{\mp 2jq_+} \\ G_{n1,2} &= \frac{\mp jq_- g(0) + g'(0)}{\mp 2jq_-}. \end{aligned} \tag{3.1.7}$$

and where the factors q_- and q_+ are the wave numbers of the wave function of the normal metal.

The general solution of the Bogoliubov equations for a *normal metal* was then obtained by taking the inverse Laplace transforms of (3.1.5) and (3.1.6), which rendered

$$f(x) = F_{n1}e^{-jq_+x} + F_{n2}e^{jq_+x} \tag{3.1.8}$$

and

$$g(x) = G_{n1}e^{-jq_-x} + G_{n2}e^{jq_-x} \tag{3.1.9}$$

where the coefficients were defined by (3.1.7).

In the case of a *superconductor* ($\Delta \neq 0$), (3.1.3) and (3.1.4) could be expressed as

$$F(s) = \frac{(s^2 + q_-^2)[sf(0) + f'(0)] + (2m\Delta/\hbar^2)[sg(0) + g'(0)]}{(s^2 + k_+^2)(s^2 + k_-^2)} \tag{3.1.10}$$

and

$$G(s) = \frac{(s^2 + q_+^2)[sg(0) + g'(0)] + (2m\Delta/\hbar^2)[sf(0) + f'(0)]}{(s^2 + k_+^2)(s^2 + k_-^2)} \tag{3.1.11}$$

with

$$k_\pm^2 = (2m/\hbar^2)[\mu \pm (E^2 - \Delta^2)^{1/2}], \tag{3.1.12}$$

the wave numbers of the superconductor.

The two expressions above were simplified to give

$$F(s) = \frac{F_{s1}}{s + jk_+} + \frac{F_{s2}}{s - jk_+} + \frac{F_{s3}}{s + jk_-} + \frac{F_{s4}}{s - jk_+} \tag{3.1.13}$$

and

$$G(s) = \frac{G_{s1}}{s + jk_+} + \frac{G_{s2}}{s - jk_+} + \frac{G_{s3}}{s + jk_-} + \frac{G_{s4}}{s - jk_+}. \tag{3.1.14}$$

The definition of the coherence factors in the BCS theory for superconductivity [26],

$$u_o^2 = 1 - v_o^2 = \frac{1}{2}\left[1 + \frac{\sqrt{E^2 - \Delta^2}}{E}\right], \tag{3.1.15}$$

were used for the calculation of the coefficients as

$$\begin{aligned}
F_{s1,2} &= \frac{u_o^2[\mp jk_+ f(0) + f'(0)] - u_o v_o[\mp jk_+ g(0) + g'(0)]}{\mp 2jk_+(u_o^2 - v_o^2)} \\
F_{s3,4} &= \frac{-v_o^2[\mp jk_- f(0) + f'(0)] + u_o v_o[\mp jk_- g(0) + g'(0)]}{\mp 2jk_-(u_o^2 - v_o^2)} \\
G_{s1,2} &= \frac{-v_o^2[\mp jk_+ g(0) + g'(0)] + u_o v_o[\mp jk_+ f(0) + f'(0)]}{\mp 2jk_+(u_o^2 - v_o^2)} \\
G_{s3,4} &= \frac{u_o^2[\mp jk_- g(0) + g'(0)] - u_o v_o[\mp jk_- f(0) + f'(0)]}{\mp 2jk_-(u_o^2 - v_o^2)}.
\end{aligned} \tag{3.1.16}$$

The wave fuctions were again solved by taking the inverse Laplace transforms of $F(s)$ and $G(s)$ respectively, to render

$$f(x) = F_{s1}e^{-jk_+x} + F_{s2}e^{jk_+x} + F_{s3}e^{-jk_-x} + F_{s4}e^{jk_-x} \tag{3.1.17}$$

and

$$g(x) = G_{s1}e^{-jk_+x} + G_{s2}e^{jk_+x} + G_{s3}e^{-jk_-x} + G_{s4}e^{jk_-x} \tag{3.1.18}$$

where the coefficients were defined by (3.1.16).

The general solutions for the Bogoliubov equations for *normal metals* and *superconductors* were derived in (3.1.8) and (3.1.9), and (3.1.17) and (3.1.18), respectively.

These solutions were applied to a normal metal/superconductor (NS) interface, and compared to the results that were obtained by Blonder *et al* [27]. Not all the components of the general solutions can exist in a NS interface due to physical constraints. Transmission through an interface will only be possible if the sign of the group velocity ($dE/d\hbar k$) of the wave function is preserved through the interface. For example, if an incident electron with energy E is described by $F_{n2}e^{jq_+x}$ on the N-side, then the only possible wave function components on the S-side would be $F_{s2}e^{jk_+x}$ and $F_{s3}e^{jq_-x}$, due to their positive group velocities, representing electron-like and hole-like behavior, respectively. The reflected component on

the N-side has a negative group velocity, and is thus represented by $F_{n1}e^{-jq_+x}$. An incident electron can also be Andreev reflected, emerging as a hole with energy $-E$, while two electron charges are transferred to the S-side. This wave function component is described as $G_{n2}e^{jq_-x}$. In order to exclude all the non-allowed states, the appropriate coefficients had to be set to zero. We thus had that $G_{n1} = G_{s1} = G_{s4} = F_{s1} = F_{s4} = 0$.

The elastic scattering at the NS interface was modelled as a δ-function potential $V(x) = H\delta(x)$ [27]. In order to guarantee continuity of the wave functions at the NS interface, the boundary conditions

$$\begin{aligned} f_N(0) &= f_S(0) = f(0) \\ g_N(0) &= g_S(0) = g(0), \end{aligned} \tag{3.1.19}$$

and the derivative boundary conditions

$$\begin{aligned} (\hbar^2/2m)[f'_S(0) - f'_N(0)] &= Hf(0) \\ (\hbar^2/2m)[g'_S(0) - g'_N(0)] &= Hg(0) \end{aligned} \tag{3.1.20}$$

were applied. After setting F_{n2}=1 and $k_+ = k_- = q_+ = q_- = k_F$ (the wave number on the Fermi surface), the respective relevant coefficients were determined as

$$\begin{aligned} F_{n1} &= -(u_o^2 - v_o^2)(Z^2 + jZ)/\gamma \\ F_{s2} &= u_o^2(1 - jZ)/\gamma \\ F_{s3} &= jv_o^2 Z/\gamma \\ G_{n2} &= u_o v_o/\gamma \\ G_{s2} &= u_o v_o(1 - jZ)/\gamma \\ G_{s3} &= ju_o v_o Z/\gamma \end{aligned} \tag{3.1.21}$$

where

$$\gamma = u_o^2 + Z^2(u_o^2 - v_o^2) \tag{3.1.22}$$

and

$$Z = mH/\hbar^2 k_F, \tag{3.1.23}$$

the definition of the barrier strength.

The system of equations were then expressed in matrix form as

$$\psi_N = \begin{bmatrix} 1 \\ 0 \end{bmatrix} e^{jq_+x} + F_{n1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} e^{-jq_+x} + G_{n2} \begin{bmatrix} 0 \\ 1 \end{bmatrix} e^{jq_-x} \tag{3.1.24}$$

$$\psi_S = (F_{s2}/u_o) \begin{bmatrix} u_o \\ v_o \end{bmatrix} e^{jk_+x} + (F_{s3}/v_o) \begin{bmatrix} v_o \\ u_o \end{bmatrix} e^{-jk_-x} \tag{3.1.25}$$

where ψ_N and ψ_S are the wave functions in the normal metal and superconductor, respectively.

The coefficients of the column matrices were identical to the coefficients that were reported in [27].

3.1.2 Double-junction tunnelling

In order to make superconductor technology viable as a circuit element, a switching element is required that is controlled by a third terminal. In silicon technology the transistor provided the solution, but in superconducting technology the Josephson junction, being a two-terminal element, was not an obvious candidate.

A three-terminal device was perceived as being the holy grail for superconducting switching circuits and it was decided that I should focus on these types of devices during my sabbatical. That would entail that I understand the dynamics of tunnelling in superconductor three-terminal geometries and also be able to model the current-voltage characteristics.

A three-terminal device that was used to study the non-equilibrium state in superconductors is shown in Figure 3.1. In the device, quasiparticles can be injected through a normal metal-insulator-superconductor (N_1IS_2) or superconductor-insulator-superconductor (S_1IS_2) and then detected by a subsequent superconductor-insulator-superconductor (S_2IS_3) junction.

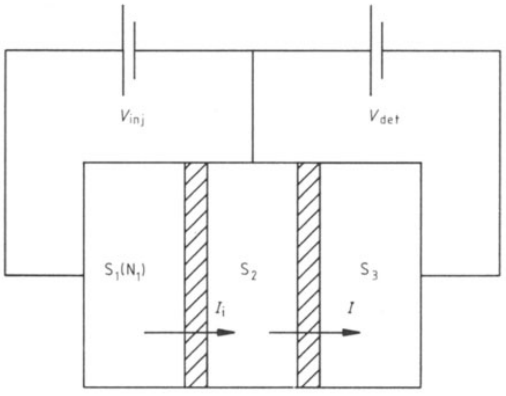


Figure 3.1: A superconductor double-junction structure. From [28].

A computer model was implemented where different interfaces could be selected as

quasiparticle injectors, and the transport between the injector and the detection of the particles at the second junction be quantified.

3.1.2.1 Quasiparticle injection

The tunnelling Hamiltonian approach was used to calculate the current-voltage characteristics of the injector junctions, ranging from NS junctions to SIS junctions [29]. The general expression for the single particle tunnelling current was modelled as

$$I = \frac{G_{NN}}{q} \int_{-\infty}^{\infty} \rho_2(E - qV)\rho_1(E)\psi(E, qV)\mathrm{d}E \tag{3.1.26}$$

where E is the energy, V the applied voltage, ρ the normalized density of states and G_{NN} the normal state tunnelling conductance. The function $\psi(E, qV)$ gives the difference of the Fermi function on either side of the barrier due to the applied voltage and can be expressed as

$$\psi(E, qV) = \frac{1}{1 + e^{(E-qV)/kT}} - \frac{1}{1 + e^{E/kT}}. \tag{3.1.27}$$

For a superconductor the normalized density of states function is expressed as

$$\rho(E) = \frac{|E|}{\mathrm{Re}\left[\sqrt{E^2 - \Delta^2(T)}\right]} \tag{3.1.28}$$

where $\Delta(T)$ is the temperature dependent superconductor band gap. For a normal metal the normalized density of states function is 1.

The discontinuity in the range of integration for a NIS junction was removed by splitting the current into two components [29], given by

$$\begin{aligned} I_1 &= \frac{G_{NN}}{q} \int_0^{\infty} \frac{e^{qV/kT} - 1}{(1 + e^{r/KT})[1 + e^{(qV-r)/kT}]}\mathrm{d}u, \text{ and} \\ I_2 &= \frac{G_{NN}}{q} \int_0^{\infty} \frac{e^{qV/kT} - 1}{(1 + e^{-r/KT})[1 + e^{(qV+r)/kT}]}\mathrm{d}u \end{aligned} \tag{3.1.29}$$

where $r = \sqrt{u^2 + \Delta^2}$. The total current is given by $I = I_1 + I_2$.

The quasiparticle injection efficiency is expresses as

$$\eta = \frac{I_{qp}}{I} = \frac{I_1 - I_2}{I_1 + I_2}. \tag{3.1.30}$$

For the SIS case the removal of the discontinuities rendered

$$I = \begin{cases} I_1 + I_2 & 0 < qV < \Delta_2 - \Delta_1 \\ I_2 + I_3 & \Delta_2 - \Delta_1 < qV < \Delta_1 + \Delta_2 \\ I_2 + I_3 + I_4 & qV > \Delta_1 + \Delta_2 \end{cases} \tag{3.1.31}$$

where

$$\begin{aligned} I_1 &= \frac{G_{NN}}{q} \int_0^{\infty} \frac{E(E+qV)\psi(-E,qV)}{\sqrt{(E+\Delta_1)(E+qV+\Delta_2)}} \mathrm{d}u \\ I_2 &= \frac{G_{NN}}{q} \int_0^{\infty} \frac{E(E-qV)\psi(E,qV)}{\sqrt{(E-\Delta_1)(E-qV+\Delta_2)}} \mathrm{d}u \\ I_3 &= \frac{G_{NN}}{q} \int_0^{\infty} \frac{E(E+qV)\psi(-E,qV)}{\sqrt{(E+\Delta_1)(E+qV-\Delta_2)}} \mathrm{d}u \\ I_4 &= \frac{G_{NN}}{q} \int_{-\pi/2}^{\pi/2} \frac{E(qV-E)\psi(E,qV)}{\sqrt{(E+\Delta_1)(qV-E+\Delta_2)}} \mathrm{d}u \end{aligned} \tag{3.1.32}$$

The relationship between E and I_1, I_2 and I_3 was given by $E = \alpha \cosh(u) + \beta$, and for I_4 by $E = \alpha \sinh(u) + \beta$. The values for α and β were given as

$$\alpha = \begin{cases} \frac{1}{2}(\Delta_2 - \Delta_1 - qV) & \text{for } I_1 \\ \frac{1}{2}(\Delta_2 + \Delta_1 + qV) & \text{for } I_2 \\ \frac{1}{2}(\Delta_1 + \Delta_2 + qV) & \text{for } I_3 \\ \frac{1}{2}(qV - \Delta_1 - \Delta_2) & \text{for } I_4 \end{cases} \tag{3.1.33}$$

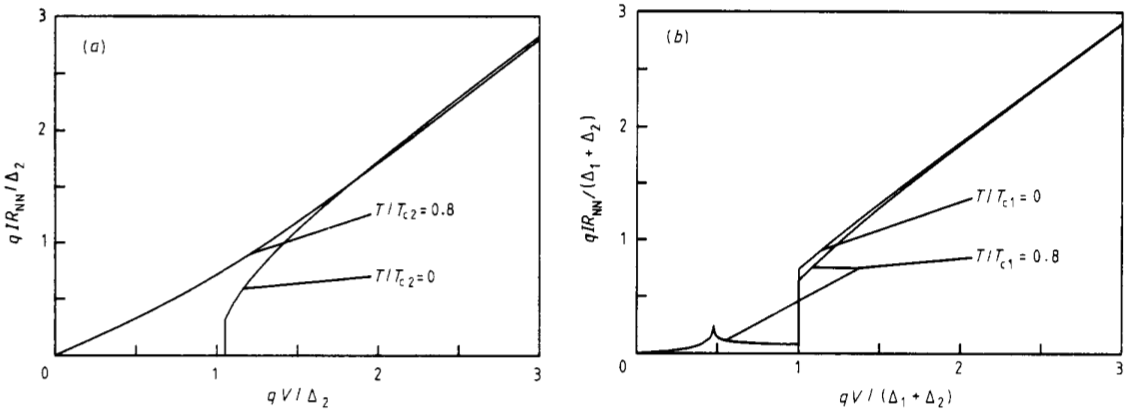
and

$$\beta = \begin{cases} \frac{1}{2}(\Delta_2 + \Delta_1 - qV) & \text{for } I_1 \\ \frac{1}{2}(\Delta_2 - \Delta_1 + qV) & \text{for } I_2 \\ \frac{1}{2}(\Delta_1 - \Delta_2 - qV) & \text{for } I_3 \\ \frac{1}{2}(qV + \Delta_1 - \Delta_2) & \text{for } I_4 \end{cases} \tag{3.1.34}$$

The quasiparticle injection efficiency was calculated as

$$\eta = \begin{cases} (I_1 - I_2)/(I_1 + I_2) & 0 < qV < \Delta_2 - \Delta_1 \\ (I_3 - I_2)(I_2 + I_3) & \Delta_2 - \Delta_1 < qV < \Delta_1 + \Delta_2 \\ (I_3 + I_4 - I_2)(I_2 + I_3 + I_4) & qV > \Delta_1 + \Delta_2 \end{cases} . \tag{3.1.35}$$

All the integrals were solved numerically and the calculated current-voltage characteristics of typical NIS and SIS junctions are shown in Figure 3.2 for T/T_c=0 and T/T_c=0.8 respectively, where T_c is the critical temperature of the superconductor [28].



(a) **(b)**

Figure 3.2: Current voltage characteristics at T/T_c=0 and T/T_c=0.8 for (**a**) an NIS interface, and (**b**) an SIS interface with $\Delta_2/\Delta_1 = 2$. From [28].

The calculations to determine the current-voltage characteristics of an NS junction was based on the work of Blonder *et al* [27] and my own [25], where the solution of the Bogoliubov equations were solved in a normal metal and a superconductor. This method is versatile in the sense that interfaces ranging from a pure metal to an insulator can be modelled by adjustment of the dimensionless barrier strength parameter (Z), defined in (3.1.23).

The tunnelling current was modelled as

$$I = \frac{G_{NN}}{q}\int_{-\infty}^{\infty}[1 + A(E) - B(E)]\psi(E, qV)\mathrm{d}E \tag{3.1.36}$$

where $A(E)$ and $B(E)$ are the probabilities of Andreev and normal reflection, respectively, and defined in [27] as

$$\begin{aligned} A(E) &= u_o^2 v_o^2/\gamma^2 \\ B(E) &= (u_o^2 - v_o^2)Z^2(1 + Z^2)/\gamma^2. \end{aligned} \tag{3.1.37}$$

The coherence factors (u_o and v_o), barrier strength parameter (Z) and γ were defined in (3.1.15), (3.1.23) and (3.1.22), respectively.

The computer generated current-voltage characteristics of a number of NS junctions, at T=0 K, are shown in Figure 3.3. The barrier strengths were chosen to range from a pure metal (Z=0) to an insulator ($Z = 100 \gg 1$). The resemblance between a pure NIS junction and an NS junction with a large barrier strength parameter ($Z \gg 1$) is quite clear.

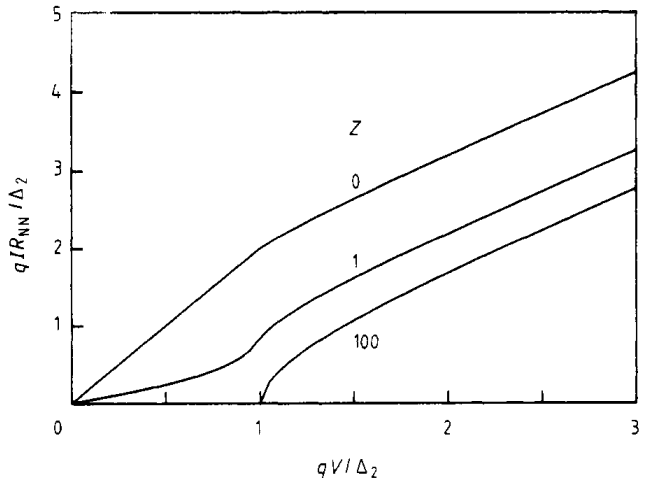


Figure 3.3: Current-voltage characteristics of NS interfaces at T=0 K with different barrier strength parameters. From [28].

3.1.2.2 Non-equilibrium quasiparticle transport

To calculate the current through the detection barrier, the transport from the injector to the detection barrier must be modelled, which will give an indication of the quasiparticle density at the detection barrier. The model is based on a modified version of the Rothwarf-Taylor rate equation [30], where the change in quasiparticle density (N) is expressed by the differential equation

$$\frac{\partial^2 N}{\partial x^2} = R_{eff}(N^2 - N_T^2), \tag{3.1.38}$$

where N_T is the steady-state equilibrium quasiparticle density and R_{eff} the effective recombination rate constant given by

$$R_{eff} = \kappa/(1 + \tau_\gamma/\tau_B), \tag{3.1.39}$$

where κ is the intrinsic quasiparticle recombination rate constant, τ_B the phonon lifetime against pair breaking, and τ_γ the phonon escape time. The quasiparticle density on the edge of the injector interface ($x = 0$) was derived from the boundary condition $\partial^2 N/\partial x^2 = 0$ as

$$N_o^2 = N_T^2 + (I_o/\kappa)(1 + f\tau_\gamma/\tau_B), \tag{3.1.40}$$

where I_o is the quasiparticle injection rate, and $f = F(qV - \Delta)/2\Delta$, where F gives an indication of the fraction of the energy which is converted to quasiparticles. The other boundary condition requires that no excess quasiparticles exist at $x \to \infty$. Wong *et al* [31] proposed an analytical solution for (3.1.38), which satisfied both boundary conditions,

$$\frac{N}{N_T} + 2 = 3\left[\frac{(\sqrt{N_o/N_T + 2} + \sqrt{3}) + (\sqrt{N_o/N_T + 2} - \sqrt{3})e^{-x/\lambda}}{(\sqrt{N_o/N_T + 2} + \sqrt{3}) - (\sqrt{N_o/N_T + 2} - \sqrt{3})e^{-x/\lambda}}\right]^2 \tag{3.1.41}$$

where $\lambda = \sqrt{D/2R_{eff}N_T}$, the quasiparticle diffusion length, and D the quasiparticle diffusion constant. The computed quasiparticle density characteristic between the injector and detector interfaces is shown in Figure 3.4 for τ_γ=10 ps, τ_B=5 ps, $\kappa = 10^{-12}$ cm^3/s, D=20 cm^2/s and $n_o = (N_o - N_T)/4N(0)\Delta$=0.2244. $N(0)$ is the single-spin density of states and was taken as 3×10^{22} cm^{-3}eV^{-1}.

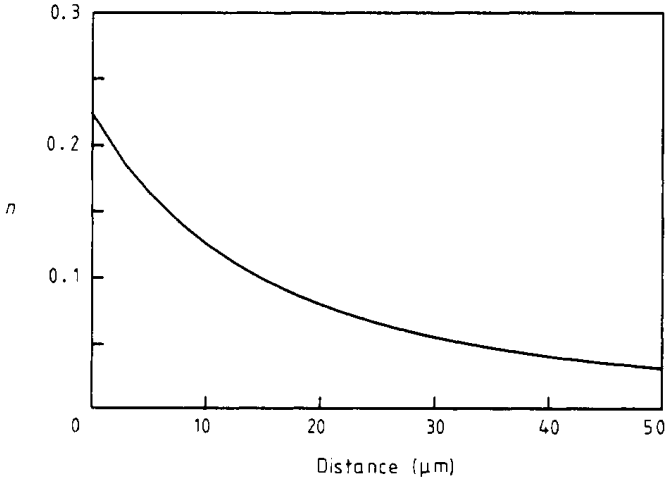


Figure 3.4: Normalized excess quasiparticle concentration as a function of distance. From [28].

3.1.2.3 Quasiparticle detectors

When excess quasiparticles are present at an SIS interface, the current-voltage characteristics of the interface will be modified. The excess quasiparticles can be present due to external stimuli, such as injection from a preceding interface, as shown in Figure 3.1.

When excess quasiparticles are present, the superconductor band gap is suppressed. Owen and Scalapino [32] developed a model which made the assumption that the excess quasiparticles would disturb the chemical equilibrium of the interface, but not the thermal equilibrium. The excess quasiparticles would thus introduce an effective chemical potential μ^*.

The effective superconducting band gap at a specific temperature and quasiparticle injection level was calculated numerically by the simultaneous solution of the normalized excess quasiparticle concentration (n), given by

$$n = \frac{N - N_T}{4N(0)\Delta_o} = \frac{1}{\Delta_o}\int_0^\infty \left[\frac{1}{1 + e^{(E-\mu^*)/kT}} - \frac{1}{1 - e^{E/kT}}\right] \mathrm{d}\epsilon, \tag{3.1.42}$$

where $E = \sqrt{\epsilon^2 + \Delta^2}$ and Δ_o the superconductor band gap at T=0 K and n=0, and the BCS

gap equation that was modified by μ^* to become

$$\frac{1}{N(0)V} = \int_{-\hbar\omega_c}^{\hbar\omega_c} \tanh\left[\frac{(E-\mu^*)/kT}{2E}\right] d\epsilon \tag{3.1.43}$$

where $\hbar\omega_c$ is the cut-off energy for the assumption that the band gap stays constant for weakly coupled superconductors.

The computed values for the relative band gap (Δ/Δ_o) is shown in Figure 3.5(a) as a function of temperature at different injection levels. It is apparent that, when n=0, the graph shows the BCS equilibrium (μ^*=0) dependence of the band gap on temperature. The effective chemical potential was also numerically calculated from (3.1.42) and is shown as a function of the normalized excess quasiparticle concentration in Figure 3.5(b).

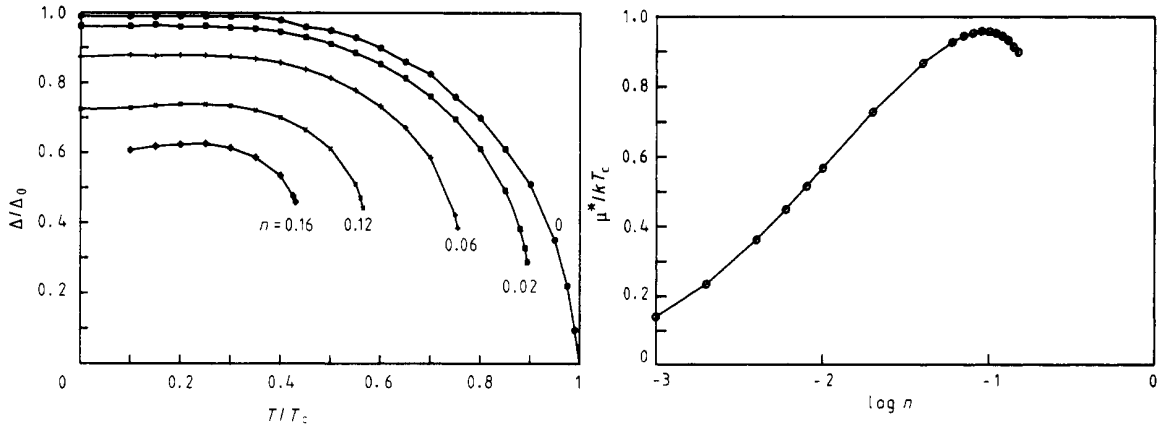


Figure 3.5: (**a**) Relative superconductor band gap as a function of temperature at different quasiparticle injection levels. (**b**) Effective chemical potential as a function of normalized excess quasiparticle concentration at $T/T_{c2} = 0.3$. From [28].

The suppressed values for the band gap and the effective chemical potential was then used to calculate the resulting tunnelling current of the detector interface, using (3.1.32), but with $\psi(E, qV)$ modified to include μ^* as

$$\psi(E, qV) = \frac{1}{1 + e^{[E-(\mu^*+qV)]/kT}} - \frac{1}{1 + e^{E/kT}}. \tag{3.1.44}$$

The computed current-voltage characteristics of typical SIS detectors are shown in Figure 3.6, at T/T_{c2}=0.8, for n=0 and n=0.4, for Δ_3/Δ_2=1, Δ_3/Δ_2=2 and Δ_3/Δ_2=10, respectively. The band gap suppression of Δ_2 is clearly observed as the shift in the points of discontinuity.

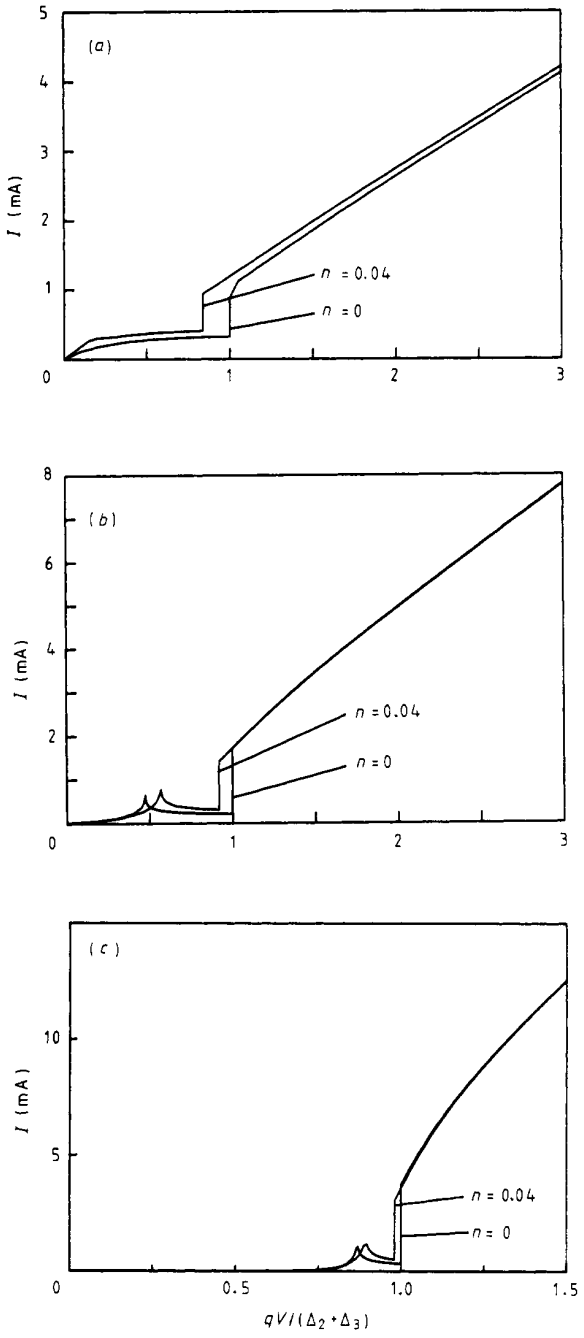


Figure 3.6: Current-voltage characteristics of an SIS detector junction at T/T_{c2}=0.8 and different quasiparticle injection levels. (**a**) Δ_3/Δ_2=1, (**b**) Δ_3/Δ_2=2, and (**c**) Δ_3/Δ_2=10. From [28].

An overview article about non-equilibrium quasiparticle processes in superconducting tunnelling structures was also published in a South African journal [33].

3.1.3 The superconducting Gray-transistor

In the 1980's the description of the Gray transistor [34] was seen as a major breakthrough in the search of a superconducting three-terminal device with transistor-like behavior.

A typical Gray transistor structure is shown in Figure 3.7. It comprises a stack of two tunnelling junctions, with the middle superconducting layer common to both junctions. All the superconducting layers are made from the same material and thus have the same superconducting band gap (Δ).

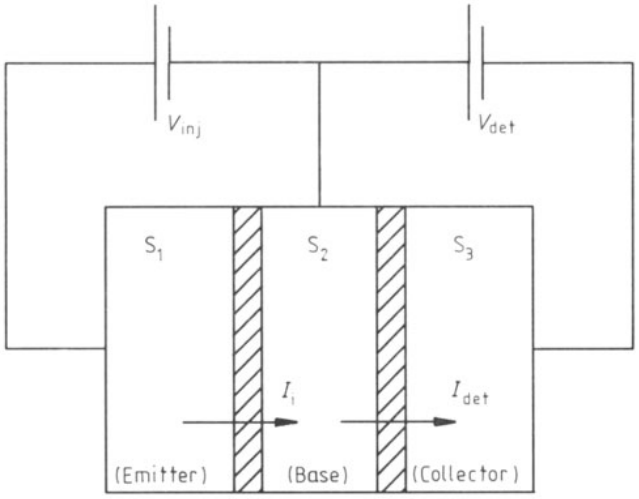


Figure 3.7: Structure of a Gray transistor. From [35].

The first junction is biased above the sum gap (2Δ), which will result in a high concentration of quasiparticles that will tunnel through the junction. The injected quasiparticles will then traverse the 'base' region of the device and will impinge on the second tunnelling junction, which is biased below the sum gap, and is used as a quasiparticle detector.

The current gain of the Gray transistor is defined as

$$A_i = \Delta I / I_i \tag{3.1.45}$$

where ΔI is the excess collector current, and I_i the injected current from the first junction. Furthermore, the relationship between I_i and the injection rate (I_o) was defined by Iguchi [36] as

$$I_o = I_i / qAd \tag{3.1.46}$$

where q is electron charge, A the area of the injection junction and d the thickness of the injection insulation layer.

If the bias voltage of the first junction is chosen to be low enough, the excess quasiparticle concentration (ΔN) will be negligible when compared to the steady-state equilibrium concentration (N_T). The excess collector current will then be directly proportional to the excess quasiparticle concentration. It thus follows that

$$\Delta I = \alpha \Delta N \tag{3.1.47}$$

where α is the constant of proportionality.

The excess quasiparticle concentration is approximated from the solution of the Rothwarf-Taylor rate equation [30] and can be expressed as

$$\Delta N = (I_o/2\kappa N_T)(1 + \tau_\gamma/\tau_B). \tag{3.1.48}$$

The theoretical recombination lifetime is defined as

$$\tau_r = 1/\kappa N_T \tag{3.1.49}$$

and the effective recombination lifetime as

$$\tau_{eff} = \tau_r(1 + \tau_\gamma/\tau_B)/2. \tag{3.1.50}$$

By using (3.1.45)–(3.1.50) the current gain can be expressed as

$$A_i = \frac{\alpha\tau_{eff}}{qAd}. \tag{3.1.51}$$

It is clear from the expression of the gain that the geometry of the junction and the time constant are critical parameters.

Gray's original transistor structure [34] was simulated with the software that was developed at *Hirst Research Centre* [28]. The values were then compared with the reported measured values.

Gray used three 300 Å thick aluminum layers for the superconductors, and the normal state resistance values of the injector and detector junctions were 16 Ω and 0.016 Ω, respectively. The detector area (A) was calculated from the specified product $RA \simeq 3.75 \times 10^{-4}$ Ω-cm^2, as 3.75×10^{-4} cm^2. The appropriate time constants were approximated in the software [28], based on published data [37, 38].

The computed values of ΔI were plotted against I_i at different temperatures in Figure 3.8. The slope of the graph thus represents the current gain as was defined in (3.1.45). The temperature values were chosen to correspond to the values used by Gray to measure the gain of his transistor. The detector bias was chosen as $qV/2\Delta(T) = 0.75$ for all calculations.

It is clear from Figure 3.8 that the gain curve did not extrapolate back to the origin at low injection levels. The assumption was made that the nonlinearity in gain could probably be attributed to the fact that the injection current did not increase linearly for injector bias voltages close to the sum gap. In order to test the assumption, gain values were recalculated at injector bias voltages that were well above the region of nonlinearity. Low values of injector current were obtained by increasing the normal state resistance R_{NN}.

The recalculated gain curves are shown in Figure 3.9. The least-squares straight-line fits all extrapolate to the origin, validating the assumption of nonlinearities in the injection current at low injector bias values.

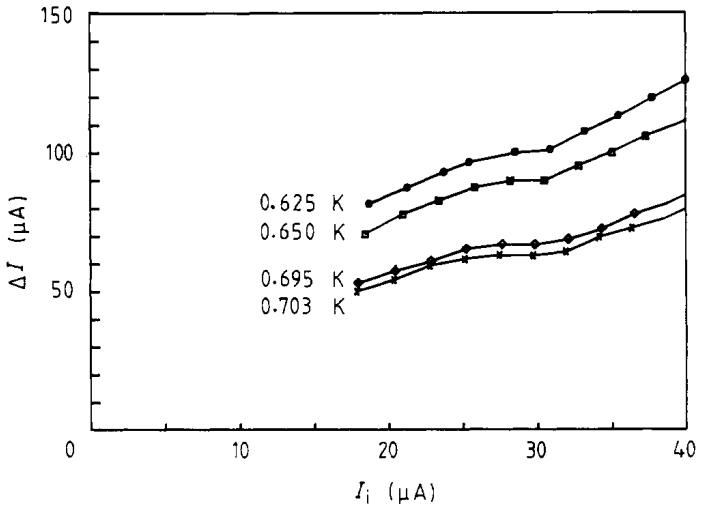


Figure 3.8: Simulated current gain of Gray transistor at different temperatures. From [35].

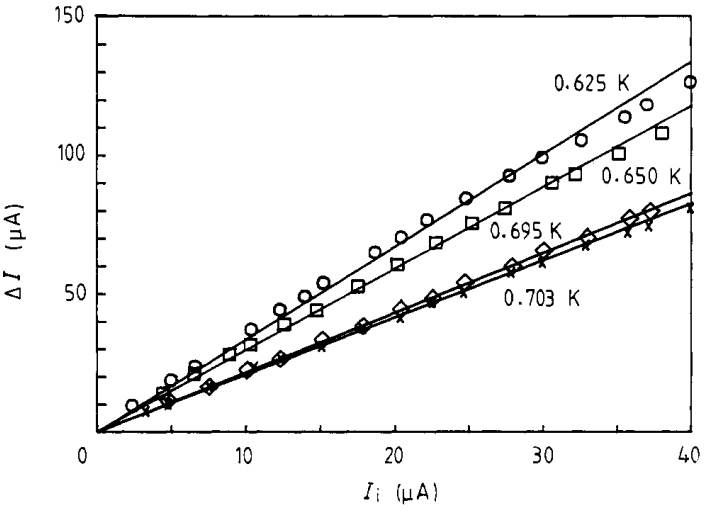


Figure 3.9: Simulated current gain of Gray transistor for linearized injector current at different temperatures. From [35].

The current gain values were calculated as 3.35, 2.94, 2.16 and 2.06 at temperature values of 0.625 K, 0.650 K, 0.695 K and 0.703 K, respectively. These values were in reasonable agreement with the measured gain values of 4, 2.25, 1.8 and 1.5, as reported by Gray [34].

An inherent feature of the Gray transistor is the fact that the current gain is strongly influenced by temperature due to the exponential decay of the quasiparticle recombination lifetime (τ_r) with increasing temperature [37]. This will be an inherent characteristic for any Gray transistor if the same superconducting material is used for all the layers.

In [39] the notion, that the decline in current gain with increasing temperature could be countered by substitution of the 'collector' material with a superconductor with a larger band gap, was tested. In theory such a material would counter the decaying current gain if temperatures were increased.

The original Gray transistor structure [34, 35] was used as reference structure. In the test structure the 'collector' was replaced with a 300 Å layer of niobium.

The computed temperature dependence of the current gain of the reference structure is shown in Figure 3.10 for different detector bias voltages.

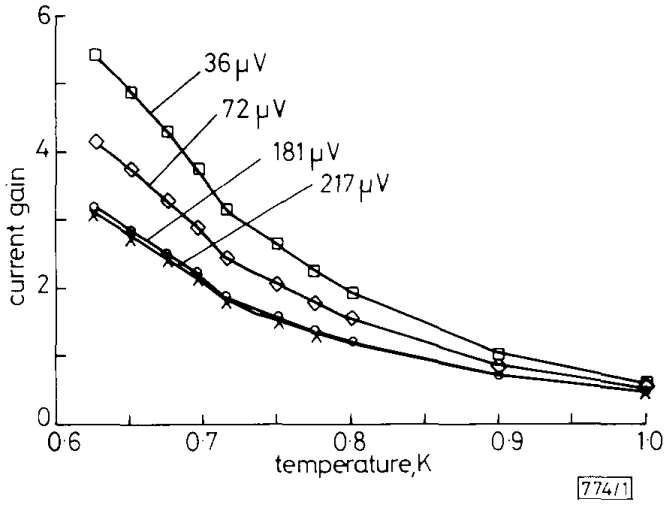


Figure 3.10: Calculated current gain of reference Gray transistor with Al-Al detector as function of temperature, for different detector bias voltages. From [39].

The computed current gain of the test structure, as a function of the temperature for different detector bias voltages, is shown in Figure 3.11. A vast improvement in current gain stability was observed when compared to the values that were shown in Figure 3.10. It was, however, also observed that, in order to obtain the additional current gain stability, the operational temperature range became smaller. That was true for temperatures below 0.625 K, which was confirmed by additional simulations, as well as higher temperatures, as observed in Figure 3.11.

The gain stabilized Gray transistor has some sentimental value for me, as it was patented by *GEC Hirst Research Centre* – a first for me at that time. The letter from the *GEC Patent Department* confirming that the patent will be filed in the USA, Japan and Europe is shown in Figure 3.12.

A review article on three-terminal superconducting devices that utilized quasiparticle tunnelling as basic operational principle, such as the Gray transistor and the Quiteron, was published in a South African journal [40].

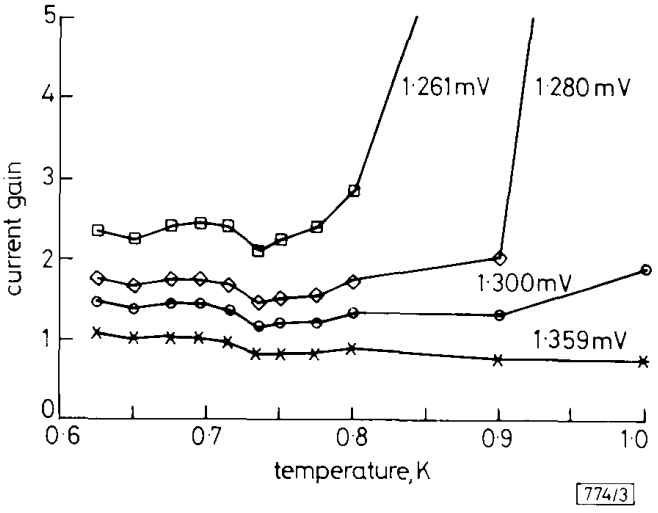


Figure 3.11: Calculated current gain of test Gray transistor with Al-Nb detector as function of temperature, for different detector bias voltages. From [39].

THE GENERAL ELECTRIC COMPANY, p.l.c.
GEC PATENT DEPARTMENT WEMBLEY

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Facsimile: 01-904 7582

Our Ref. T/HRF/3522 US

Your Ref.

Dr. W. J. Perold,
35 Dummer Street,
Somerset West 7130,
SOUTH AFRICA.

5th October 1989

SWIFTAIR

Dear Dr. Perold,

United States Application
corresponding to British Application No: 8823399.4
"Stabilised Superconducting Transistor"

We are filing US, Japanese and European patent applications in respect of this invention.

I would be grateful if you would sign the enclosed US declaration and power of attorney document, and return it to me as soon as possible. Please sign with your full names and insert the date, where indicated.

Many thanks.

Yours sincerely,

S. A. George,
Chartered Patent Agent.

Figure 3.12: Letter from *GEC Patent Department* confirming that patent applications will be filed in the USA, Japan and Europe in respect of the gain stabilized Gray transistor.

3.2 Summary

In this chapter my first steps in superconductivity research were described. The main thrust of my research at *GEC Hirst Research Centre* was focused on understanding and modeling the mechanisms of single particle (quasiparticle) tunnelling in NIS or SIS junctions [25, 28, 35, 39]. That was important, because the ultimate goal in superconducting electronics was, as was the case for semiconductor electronics, to have a three-terminal switching device that can be utilized as a binary switch.

Upon my return to Stellenbosch in 1989 I decided to see whether it was possible to establish a research activity in superconducting devices alongside the semiconductor research on advanced simulation techniques. The initial progress was slow, but I managed to get a few postgraduate students interested in superconductivity, mainly looking at simulation aspects of Josephson junctions, SQUIDs and three-terminal devices [41, 42, 43, 44].

In the early 1990's superconductivity research in South Africa was done at some universities, but the focus was on materials and the theory of superconductivity. In an effort to introduce superconducting device electronics to the South African research fraternity a number of review articles on tunnelling, three-terminal devices and SQUID magnetometers were published in South African journals [33, 40, 45].

Chapter 4

Low-temperature superconductor devices – Collaboration with UC Berkeley

At Stellenbosch University academics are entitled to take a one year sabbatical every seven years. Realizing that I was due for my next sabbatical in 1995, I decided to send my CV to a number of research groups working in the superconductivity field, amongst others a letter to Prof Theodore Van Duzer at the University of California at Berkeley. Prof Van Duzer's group was one of the leaders in superconductivity device research, with a very high international reputation. That is why I considered that specific application as a very long shot. I was thus thrilled, and a little shocked, when I heard that I was welcome to join the group for my 1995 sabbatical.

The *IEEE AP/MTTS '94* conference was scheduled to be hosted at Stellenbosch University, with a special session on superconducting devices. As I was already accepted to go to UC Berkeley the next year, and keen to meet Prof Van Duzer, he was invited for a keynote speech, and also to chair the superconductivity session at *IEEE AP/MTTS '94*. Our first coffee shop outing to Julian's Coffee shop in Stellenbosch is depicted in Figure 4.1.

Meeting this larger than life, humble and inspiring man was the start of the most rewarding journey of my academic career. It was thus with a lot of excitement and apprehension that our family started this journey to Berkeley early in January 1995.

4.1 Complementary Output Switching Logic

In January 1995 Prof Van Duzer's research group at UC Berkeley was an interesting selection of researchers and students from all over the world. The group was about 20 strong, with students from India, China and Japan, one research fellow from the USA and one very apprehensive South African academic on sabbatical.

The whole group was accommodated in one laboratory area, everyone in front of a UNIX terminal, back-to-back with a fellow researcher. The shielded room, where the low-T_c de-

Figure 4.1: Coffee with Prof Van Duzer (right) and colleague, Howard Reader (middle), at Julian's Coffee Shop in Stellenbosch.

vice measurements were done, was on the left as one entered the room. As it turned out, my back-to-back fellow researcher was Mark Jeffery, the research fellow. His first words to me were "I want to show you something that we have done, and I think it is kind of cool". I was somewhat taken aback by his bold statement, but then he showed me the results, and it was very, very cool indeed. They were the first to show how efficiently different moat structures could be used to trap stray flux, thus avoiding the malfunctioning of superconducting circuits [46].

In early 1995 the maximum clock speed of the *Intel*® *Pentium*® processor was 120 MHz. The state of the art with regard to clock speed of superconducting voltage-state logic circuits was 2.3 GHz, which was achieved by the Modified Variable Threshold Logic (MVTL) family of gates [47], more than an order of magnitude faster than their semiconductor counterparts. Prof Van Duzer challenged me to investigate other implementations of voltage-state gates that could possibly push the boundaries as far as clock speeds were concerned.

The MVTL family of gates was the most widely used at the time, due to its relatively large static operating margins. It consisted of an OR gate, complimented by a 2 OR/AND combination and a timed inverter. The timed inverter was generally considered to be the least reliable of the family of gates.

I started looking at the work of Fang [48] and Luong [49]. The Fang-Luong gates were thoroughly tested by simulation and serious problems were identified, especially as clock frequencies moved into the GHz range. Subsequently a new voltage-state logic family, Complementary Output Switching Logic (COSL), was proposed [50]. It was based on the Fang-Luong family, but with a range of fundamental design changes to make the family more robust and versatile.

4.1.1 Functionality principles of the OR/AND, NOR/NAND and XOR gates

A basic COSL OR/AND gate is shown in Figure 4.2. It is clear that the input of the gate is a one-junction SQUID, which drives a two-junction SQUID at the output. The gate is clocked by a three-phase clocking scheme, of which Clock 1 and Clock 2 in Figure 4.2 are the first two

clocks in the scheme. The Josephson junctions in the clock shaper circuits, driven by Clock 1 and Clock 2, respectively, are designed to switch for the positive portion of every clock cycle, thus giving a very stable bias reference of 2.5 mV at the input and the output. The one-junction SQUID will be reset by the negative portion of every clock cycle. The choice of the input bias resistor at the input will determine whether the gate functions as an OR, or an AND gate.

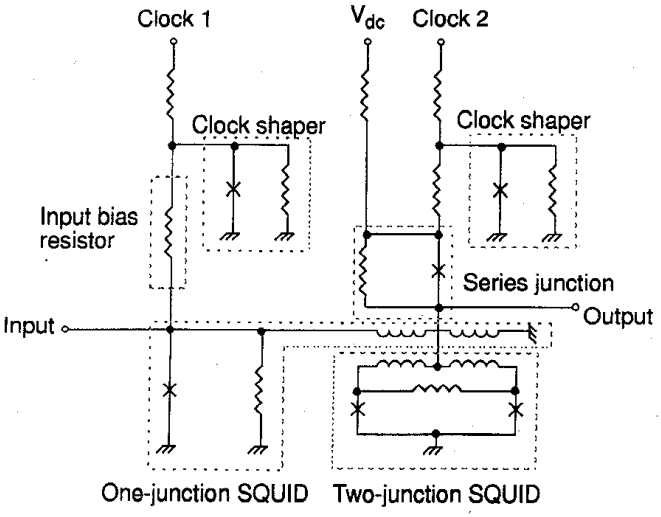


Figure 4.2: Schematic diagram of a basic COSL OR/AND gate. From [50].

The input one-junction SQUID will switch as soon as the sum of the input current from the driving circuit and the reference current from the clock exceeds the threshold current (I_{th}) of the one-junction SQUID, as is shown in Figure 4.3(a). The circuit was designed so that the current from the clock during the negative clock cycle will exceed I_{min}, thus resetting the one-junction SQUID. As can be seen from Figure 4.3(a), a large inductor current (I_L) will be induced in the inductive loop of the one-junction SQUID, which will serve as control current (I_{con}) for the two-junction SQUID. An increase in the control current (I_{con}) will suppress the critical current (I_{max}) of the two-junction SQUID, as can be derived from the the threshold curve shown in Figure 4.3(b).

The critical current of the series Josephson junction (see Figure 4.2) was designed to be less than $2I_{max}$, the critical current of the two-junction SQUID when $I_{con} = 0$, but larger than the suppressed value of the critical current of the two-junction SQUID, when I_{con} is flowing in the inductive loop of the one-junction SQUID. When the one-junction SQUID has switched ($I_{con} > 0$), the two-junction SQUID will switch first, due do the suppressed critical current, but the series junction will not switch, thus giving a high output voltage. On the other hand, when the the one-junction SQUID has not switched ($I_{con} = 0$), the critical current of the two-junction SQUID is not suppressed, and the series junction will switch first, leaving the two-junction SQUID in a non-switched state, giving a low output voltage. The gate was designed to switch into a 5 Ω load with a 1 mV output voltage, giving a 200 μA load current.

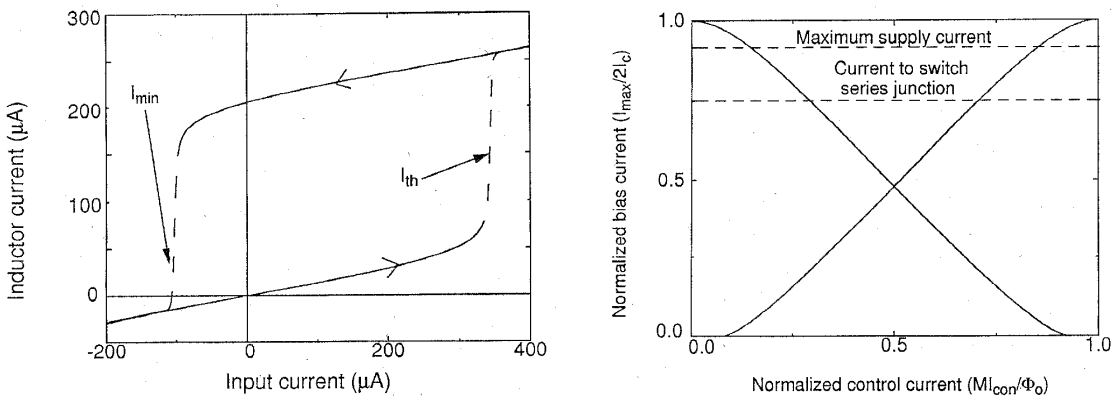


Figure 4.3: (**a**) Current transfer curve of one-junction SQUID, and (**b**) threshold curve of the two-junction SQUID. From [50].

The term "complementary" in the name of the logic family was derived from the fact that either the series junction or the two-junction SQUID could be in the switched state, depending on the input. This has the benefit that the current supplied by Clock 2 (see Figure 4.2) would be the same, whether the output is high or low.

One of the novel aspects of the COSL family of gates is that the series Josephson junction can be placed below the two-junction SQUID and not above, as is the case for the OR/AND configuration. This will automatically lead to the inverse logic functions, thus rendering a NOR/NAND configuration.

An XOR logic function $A\overline{B} + \overline{A}B$ can be implemented with a minimum of 7 gates if the complements of A and B are not available. In the COSL family of gates, it was possible to implement the XOR function with a single OR gate. The only difference being a single series Josephson junction at the input of the gate to limit the input current. An important feature of the gate is that the normal clocking scheme is different from the normal scheme in that the input clock of the XOR gate is not in phase with the output clock of the driver gate, but lags by one clock cycle. The input to the XOR gate requires two nominal drives of 200 μA each to implement two logical ones, and no current for logical zeros. The series junction of the XOR gate was designed to be less than the full drive of 400 μA. The series junction will thus block the current and prevent the one-junction SQUID from switching when two logical ones are applied to the input, as is required for proper XOR functioning.

4.1.2 Calculation of the theoretical yield of gates

The reliability of gates are normally predicted by margin analyses, where one or two circuit parameters are changed in consecutive simulation runs, while the functionality of the gate is observed. By doing that, the sensitivity of a gate to certain parameter changes is obtained. This method is deficient in the sense that simultaneous changes of multiple circuit parameters, which may influence the reliability of a gate, cannot be predicted.

For the COSL family a different approach was followed. A Monte Carlo yield prediction process was followed to predict the reliability of the gates. All the parameter values were statistically varied around their optimum values. Parameter variations depend on the quality of the fabrication process, and the parameter spreads are normally larger between wafers and not so large on the same wafer. In order to emulate this realistically a global (chip-to-chip) parameter variation and a local (on-chip) parameter variation were defined, all with Gaussian distributions.

The circuit yields were determined by doing HSPICE[1] Monte Carlo analyses. Global and local variations of resistors and inductors were considered. Global changes in critical current were considered to originate from changes in the critical current density, while local variations were ascribed to variations in the areas of the Josephson junctions. The spreads in the capacitance and resistance values of the Josephson junctions were, in turn, ascribed to the changes in critical current.

The true statistical circuit yield of a gate (y) is defined as

$$y = y' \pm L \tag{4.1.1}$$

where y' is the observed yield and L the confidence interval [51]. The confidence interval is defined as

$$L = k\sqrt{\frac{y'(1-y')}{N}}, \tag{4.1.2}$$

where N is the number of Monte Carlo cycles and k a constant which depends on the confidence level of the prediction. The value of k varies from 2 for a confidence level of 95% to 2.6 for a confidence level of 99%.

4.1.3 Implementation of circuit trim

In practice a non-functional COSL gate can be tweaked to become operational by slight adjustments of the DC bias to either the input one-junction SQUID or the output two-junction SQUID, or both. The trim facility was implemented as a subcircuit in HSPICE to compensate for global parameter variations, and input and output trim voltages were calculated for every set of global parameters of each Monte Carlo subcycle over sets of local parameter values.

For the input one-junction SQUID the trim voltage was calculated as that voltage that would make the ratio of the total bias current and the threshold current of the one-junction SQUID the same as it would be with nominal circuit parameters with no trim. The threshold current was calculated from

$$I_{th} = I_c \sin[\arccos(-1/\beta)] + \frac{I_c}{\beta}\arccos(-1/\beta) \tag{4.1.3}$$

[1] *Meta-Software Inc.*

where

$$\beta = \frac{2\pi L I_c}{\Phi_o} \tag{4.1.4}$$

and L the inductance of the one-junction SQUID, I_c the critical current of the Josephson junction and Φ_o a magnetic flux quantum or fluxon (2.07×10^{-15} Wb).

For the output trim circuit the ratio between the total bias current and the critical current of the two-junction SQUID was calculated for the nominal case, when the one-junction SQUID was in the switched state. The same ratio was then calculated when the global parameter spreads were introduced. The output trim voltage was calculated as that voltage that would restore the ratio to the nominal value.

4.1.4 Calculated yield of optimized gates

All the COSL gates were optimized for optimum yield by Monte Carlo analyses at 10 GHz. The 3σ global variation for resistors were chosen to be 15%, and the 3σ local variations as 5%. For inductors the respective spreads were 15% and 5%. The global variation in the critical current density of the *HYPRES* 1 kA/cm^2 fabrication process was taken as 10%, and the local spread in the Josephson junction area as 5%. The gates were also analyzed with the same global parameter spreads, but with the 3σ local variation increased to 10%. The optimized gates are shown in Figure 4.4.

All the gates were tested at 5 GHz and 10 GHz, and 50 Monte Carlo cycles were used for the optimization process. The 99% confidence level theoretical yields of the gates, without trimming, are shown in Table 4.1.

Table 4.1: Theoretical yield of COSL family without trimming

Gate	YIELD			
	5% 3σ local variation		10% 3σ local variation	
	5 GHz	10 GHz	5 GHz	10 GHz
OR	98^{+2}_{-5} %	98^{+2}_{-5} %	96^{+4}_{-7} %	94^{+6}_{-9} %
NOR	96^{+4}_{-7} %	98^{+2}_{-5} %	94^{+6}_{-9} %	86^{+13}_{-13} %
XOR	98^{+2}_{-5} %	100^{+0}_{-0} %	98^{+2}_{-5} %	100^{+0}_{-0} %
AND	100^{+0}_{-0} %	100^{+0}_{-0} %	98^{+2}_{-5} %	100^{+0}_{-0} %
NAND	98^{+2}_{-5} %	98^{+2}_{-5} %	94^{+6}_{-9} %	86^{+13}_{-13} %

From Table 4.1 it is clear that very good yields were obtained at high frequencies, even with large 3σ local variations and without trimming.

To put the performance of the COSL gates in perspective, the yields were compared with the basic MVTL family. The MVTL gates were optimized in similar fashion than the COSL gates. The MVTL family consisted of the OR gate, the two OR/AND combination and the OR/TI (timed inverter) combination. The 99% confidence level theoretical yield of the MVTL gates is shown in Table 4.2.

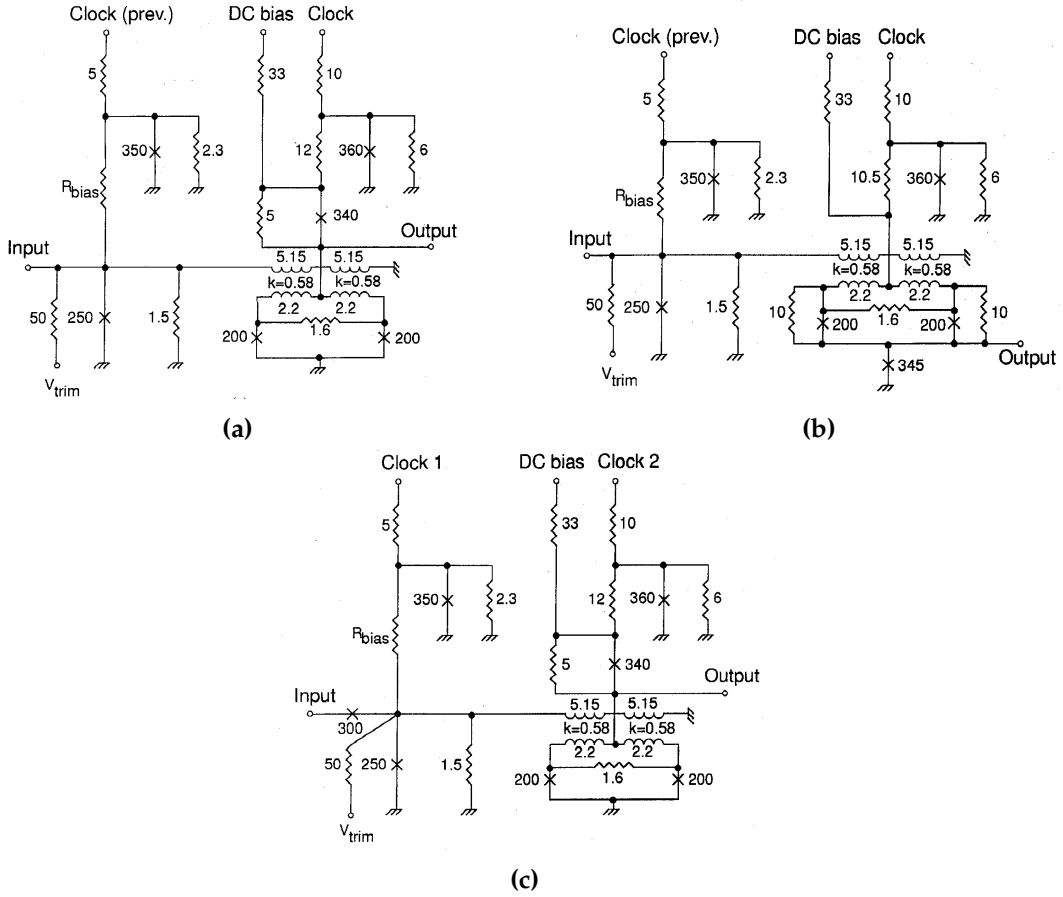


Figure 4.4: Configurations of the optimized COSL (**a**) non-inverting AND and OR gates, (**b**) the inverting NAND and NOR gates, and (**c**) the XOR gate. The value for R_{bias} is 14.3 Ω for the AND and NAND gates, 8.8 Ω for the OR and NOR gates, and 9.8 Ω for the XOR gate. Units of resistance, inductance, and critical current of junctions are Ω, pH, and μA, respectively. From [50].

Table 4.2: Theoretical yield of MVTL family without trimming

Gate	YIELD			
	5% 3σ local variation		10% 3σ local variation	
	5 GHz	10 GHz	5 GHz	10 GHz
OR	100^{+0}_{-0} %	94^{+6}_{-9} %	100^{+0}_{-0} %	94^{+6}_{-9} %
2 OR/AND	100^{+0}_{-0} %	92^{+8}_{-10} %	100^{+0}_{-0} %	88^{+12}_{-12} %
OR/TI	100^{+0}_{-0} %	56^{+18}_{-18} %	92^{+8}_{-10} %	46^{+18}_{-18} %

From Table 4.2 it is clear that the yield of the gates are very high at 5 GHz, but that the yield drops markedly at 10 GHz, especially in the case of the OR/TI combination.

The new COSL family was presented for the first time at the *Bi-annual American Workshop on Superconducting Electronics* in Farmington, Pennsylvania in October 1995 [52]. At that time the gates had not been fabricated yet, and only the theoretical principles of operation and the simulations were presented. It was met a lot of skepticism, specifically with regard to

the capability of the gates to operate at GHz frequencies.

4.1.5 Low frequency tests of gates

The correct operation of the COSL family was verified by fabricating chips with the various gates, using the 1 kA/cm^2 current density *HYPRES* process. The layout of the XOR gate is shown in Figure 4.5. The moats for stray flux trapping can clearly be observed, as well as the output amplifier to convert the 1 mV output signal to a 2.5 mV output signal (the gap voltage) into a 50 Ω external load.

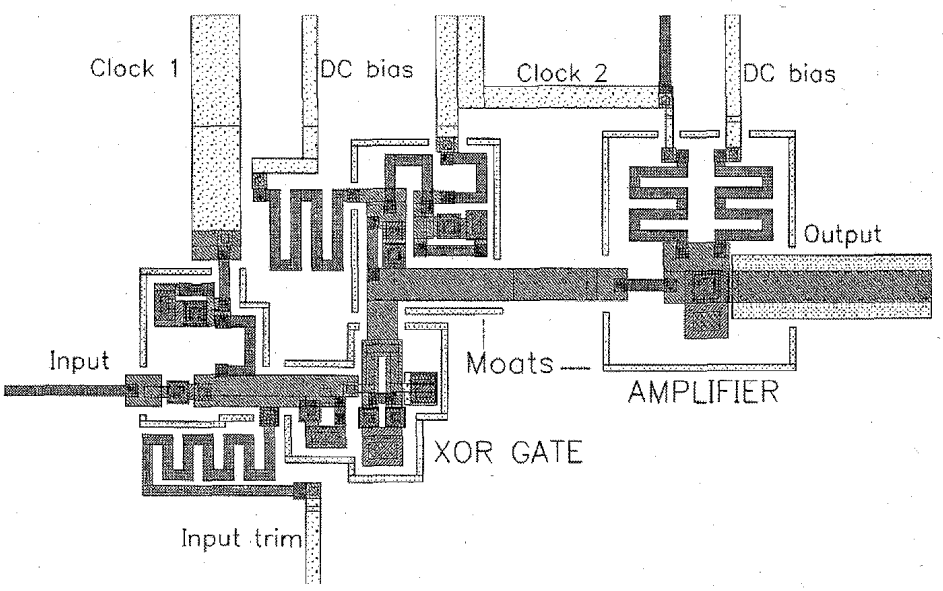


Figure 4.5: Layout of COSL XOR gate. From [50].

The fabricated chips were delivered in November 1995, just before I had to return to Stellenbosch.

On 10 November 1995 we achieved our first operational COSL gates. The clocks and the multiple input signals were generated by an *HP 8175 A Digital Signal Generator*. The input signals were sent through a series of monostable multivibrators to control the pulse width and phase relative to the clock signals. The input signals were also attenuated to obtain the correct amplitude values.

The gates were tested at 5 kHz for proper operation. The measured results of the OR, AND, XOR and NAND gates are shown in Figure 4.6. The gates were quite insensitive to amplitude variations of the clocks and margins of the order ±30% were obtained. Input trimming was never required, but output trimming was successfully used to optimize the margins on the clock amplitudes.

As can be seen from the measured results, the functionality of the COSL family of gates was verified at low clock frequencies. Even though we realized that 5 kHz operation was not

really earth shattering, we (Mark Jeffery and myself) celebrated in the company of *Samuel Adams* at our favorite watering hole, *Jupiter's*.

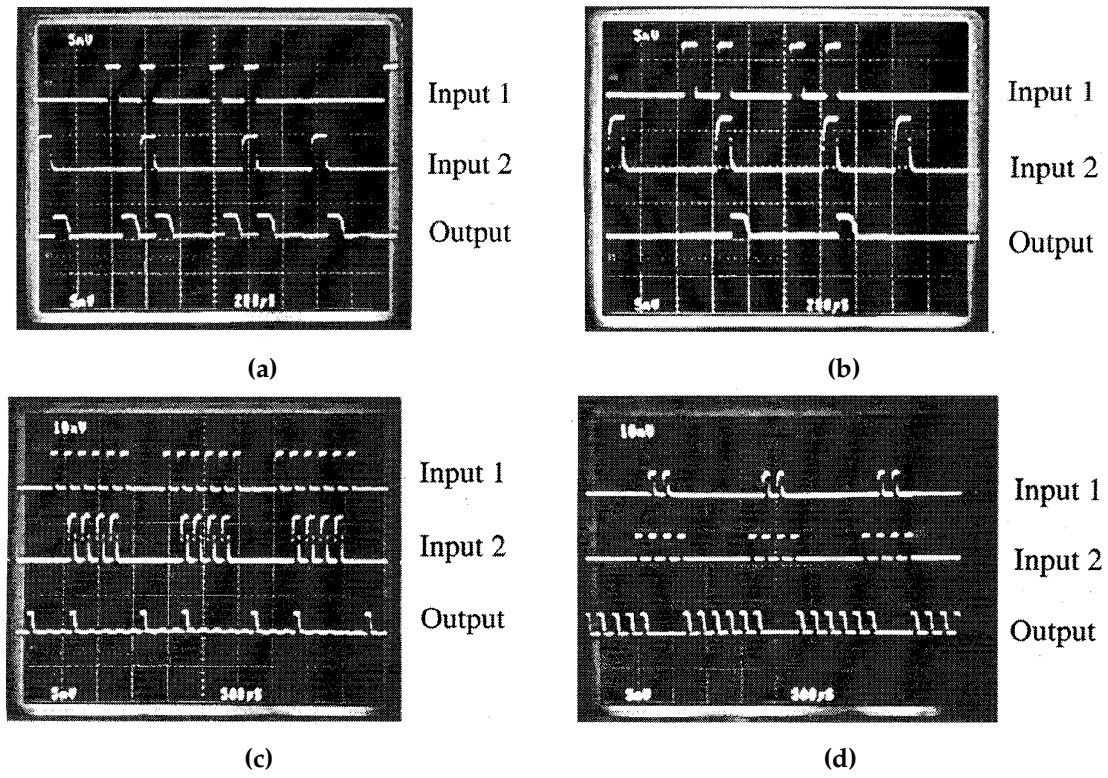


Figure 4.6: Low-speed measured functionality of COSL (**a**) OR, (**b**) AND, (**c**) XOR, and (**d**) NAND gates. A 50 Ω resistive matching network was used for all inputs to prevent signal degradation. From [50].

4.1.6 High-frequency operation of COSL gates

As was mentioned before, the screened room with the high-frequency signal generator and the measurement equipment was on the left as one entered the laboratory area (Figure 4.7).

The fabricated chips were mounted on the tip of a Petersen probe and contact to the pads of a chip was made by spring-loaded conductive fingers. The probe was then slowly inserted into the liquid helium dewar, sealed, and then connected to the room temperature electronics. In Figure 4.8 the new liquid helium dewar is shown. The *MuMETAL*® magnetic shield is clearly visible[2].

[2] A *MuMETAL*® magnetic shield will become manetized over time and need to be demagnetized on a regular basis. Demagnetization (or degaussing) is done by wrapping a coil around the cylinder and then applying a slowly decaying sinusoidal current at a low frequency, typically around 6 Hz. A degaussing amplifier was required for the new dewar and, based on the fact that my third year electronics class at Stellenbosch designed a 5 W push-pull amplifier for a practical the previous year, I volunteered to design and build the amplifier. The only small complicating factor was that the required 1.5 kW power requirement was slightly more than my 5 W comfort zone. However, I designed the circuit and, with the help of an undergraduate student, Armando, the circuit was built as well. I remember quite vividly how the power transistors exploded at the first switch-on, luckily without loss of eyes or arms. Fortunately the problem was easily solved and the degaussing amplifier served the group well for a number of years. Prof Van Duzer insisted, however, that the ugly electronics and heat sinks be hidden in a nice grey box.

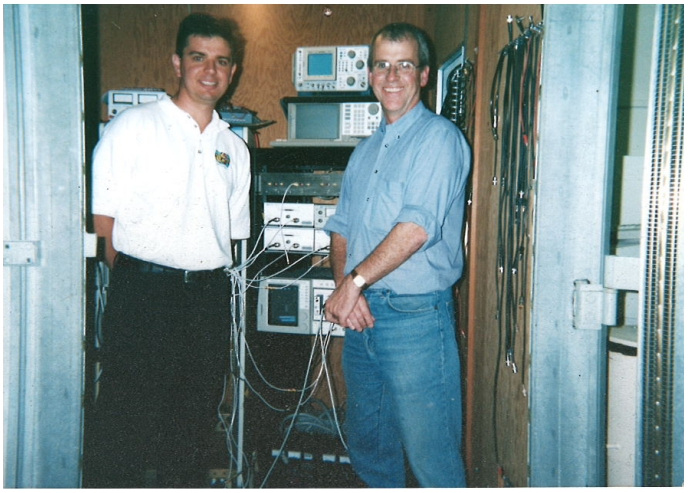


Figure 4.7: Mark Jeffery (left) and myself (right) in the screened room, with the instrumentation at the back.

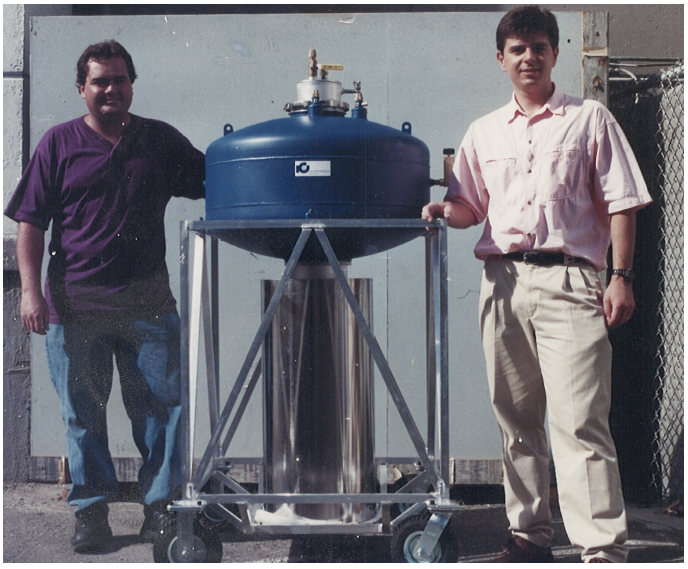


Figure 4.8: The brand new liquid helium dewar, with Mark Jeffery (right) and a technician, Ben (left). The *MuMETAL*® magnetic shield is clearly visible.

In early 1996 Mark started testing the COSL family at GHz frequencies in the laboratory at UC Berkeley. The following E-mail interchanges described the progress:

18 January 1996 "COSL at 1GHz!!!!!!"

1 February 1996 "We did it!!!!!!!!!!!!!!!!!!!! We have 8 GHz!!!!!!!!!!!!"

8 March 1996 "I got an OR gate to work at 10 GHz today with a 1 GHz pulse input."

For the high-frequency testing an *HP 80000 Data Generator* was used for the input signals, an *HP 86735 Signal Generator* for the sinusoidal clocks and an *NEL NG4218 Multiplexer* with a clock divide-by-four to phase lock all components. The experimental data of a COSL

OR gate, clocked at 10 GHz, was directly observed by a *Tektronics 11801 Digital Sampling Oscilloscope*, as is shown in Figure 4.9 [53]. The input was a 625 MHz return to zero (RZ) signal. The 10 GHz results were significant, because it made COSL the fastest voltage-state family in the world, by a factor of 5, at that time.

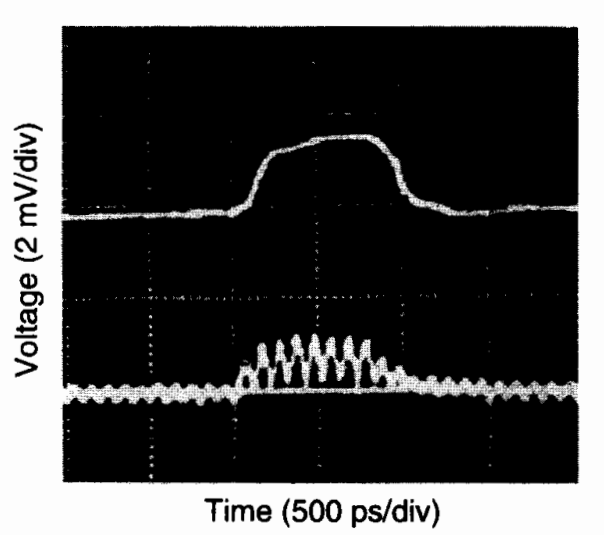
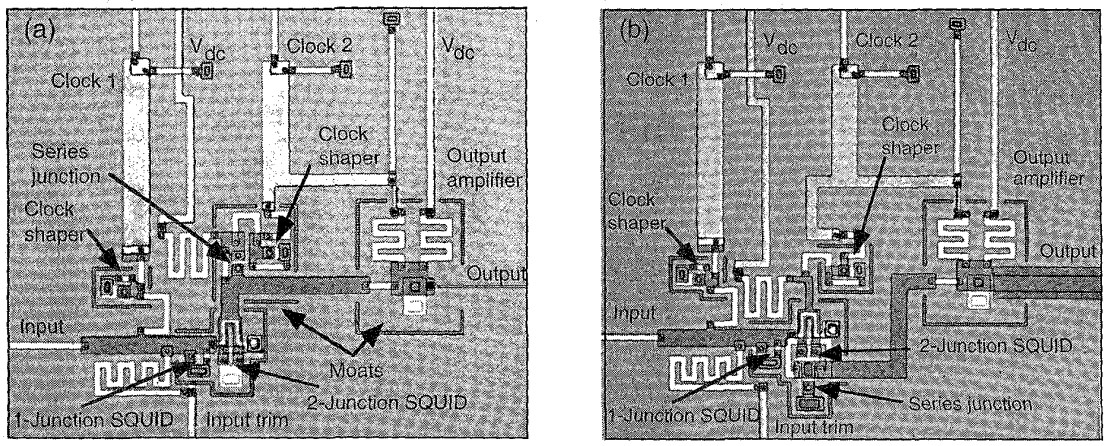


Figure 4.9: Experimental data for a COSL OR gate operating at 10 Gb/s. The input (top) was phase shifted and scaled for direct comparison with the output (bottom). From [53].

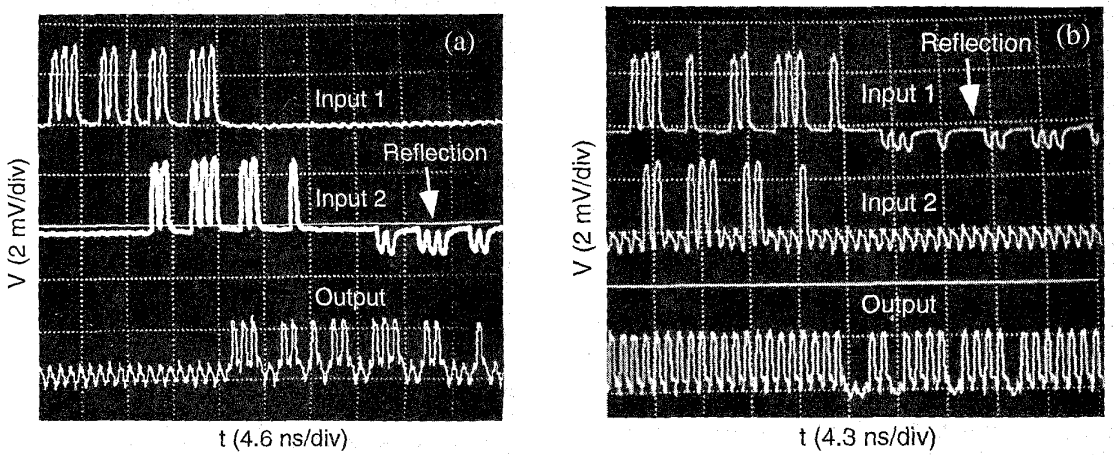
More extensive experimental data was later reported for the COSL OR gate and NAND gate at clock frequencies approaching 10 GHz [54]. The layouts of the gates are shown in Figure 4.10. The experimental data of the OR gate and the NAND gate is shown in Figure 4.11 for a clock frequency of 1 Gb/s. A delay of approximately 15 ns was observed between the input and output data pulses. That was in correspondence to the propagation delay of the cables from the the chip, through the probe, to the sampling oscilloscope. The original gate layouts, shown in Figure 4.10, had only one impedance matched input. For the test data shown in Figure 4.11, a second input was applied through the input trim bias connection (see Figure 4.10). This input was thus not impedance matched, and a large reflected component was observed, as shown in Figure 4.11.

In Figure 4.12 the responses of the OR gate and NAND gate are shown again, but this time at clocks speeds of 8 Gb/s and 7 Gb/s, respectively. Some of the outputs in Figure 4.11 and in Figure 4.12 showed some background oscillations, specifically at frequencies higher than 5 GHz. This could be attributed to the fact that the third clock phase was not required for the gates. It was found that the addition of the third clock phase eliminated the background oscillations almost completely.



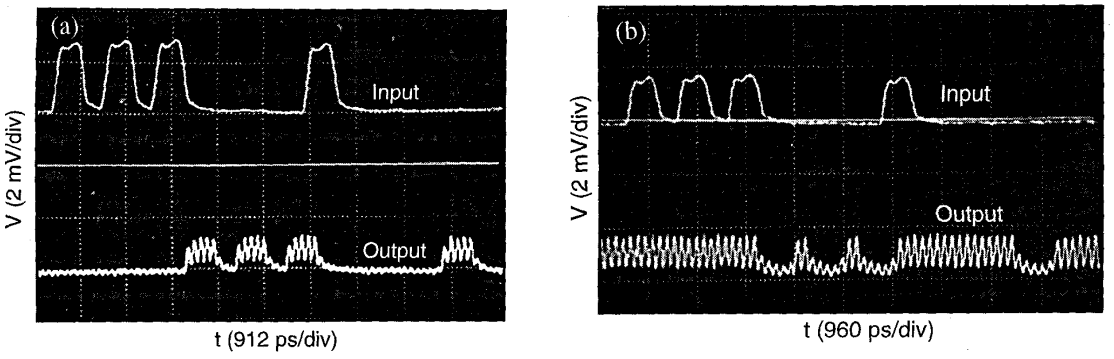
(a) **(b)**

Figure 4.10: Photographs of COSL gates fabricated using the *HYPRES* 1 kA/cm^2 process. (**a**) OR gate, and (**b**) NAND gate. From [54].



(a) **(b)**

Figure 4.11: Sampling oscilloscope photograph of (**a**) the OR gate, and (**b**) the NAND gate, at a clock frequency of 1 GHz. The reflections were due to an impedance mismatch on one of the inputs. From [54].



(a) **(b)**

Figure 4.12: Sampling oscilloscope photograph of (**a**) the OR gate, clocked at 8 GHz, and (**b**) the NAND gate, at a clock frequency of 7 GHz. From [54].

The bit error rate is an important parameter in all digital logic circuits. The very clear measured eye pattern of the COSL OR gate, with a clock frequency of 6 GHz, is shown in Figure 4.13.

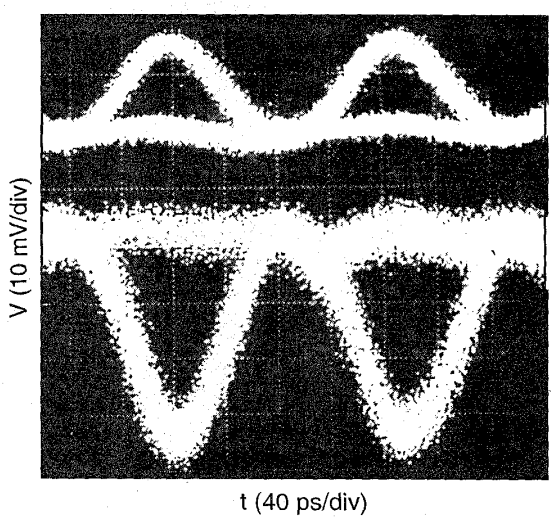


Figure 4.13: The return-to-zero eye pattern for the COSL OR gate operating at 6 GHz. The 12 GHz input is shown on the top, and the gate output, after the low noise inverting amplifier, is shown on the bottom. From [54].

The bit error rate of the OR gate was measured as 10^{-12} at 2 GHz, and 10^{-9} at 5 GHz. To our knowledge these bit error measurements were the first to directly interface a superconducting circuit to a room temperature bit error rate measuring system, in order to ensure that every bit at the output was sampled for errors.

To investigate whether the COSL gate family could be operated at clock frequencies beyond 10 GHz, the layouts of the gates were adapted for the new 2.5 kA/cm^2 *HYPRES* process. The new layout of the COSL OR gate is shown in Figure 4.14.

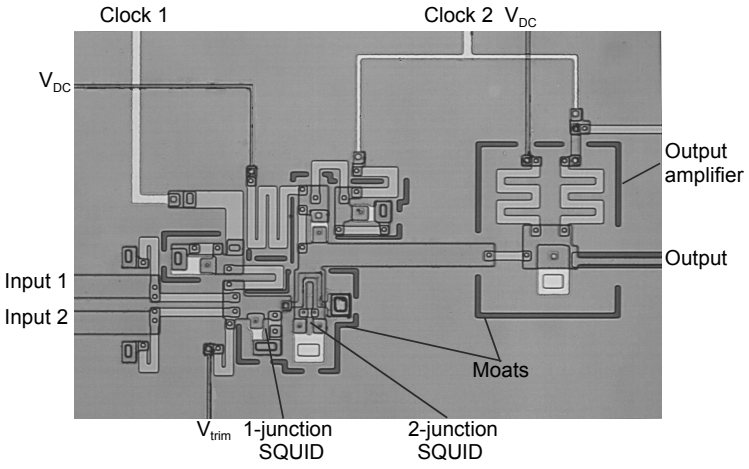


Figure 4.14: Photograph of COSL OR gate adapted for the new *HYPRES* 2.5 kA/cm^2 fabrication process. From [55].

The gates were optimized by the Monte Carlo method for 20 – 30 GHz operation. In the layout the moats surrounding the active components can clearly be seen. The moats shield the circuit from stray magnetic flux.

The circuits were tested at UC Berkeley and in early September 1997 I received the following E-mail from Mark Jeffery:

10 September 1997 "18 GHz!!!!!! I got the basic gate to go at 18 GHz..."

The 18 GHz operation of the COSL gate family was first reported at *The American Physical Society March Meeting* in Los Angeles in 1998 [55]. In Figure 4.15 the measured output data of an OR and AND gate is shown at a clock frequency of 15 GHz, for overlapping input test data at 4 GHz. The measured performance of a COSL OR gate at a clock frequency of 18 GHz, with a 12 GHz input signal, is shown in Figure 4.16. The measured data in the two figures confirmed the correct operation of the gates at 15 GHz and 18 GHz clock frequencies, respectively.

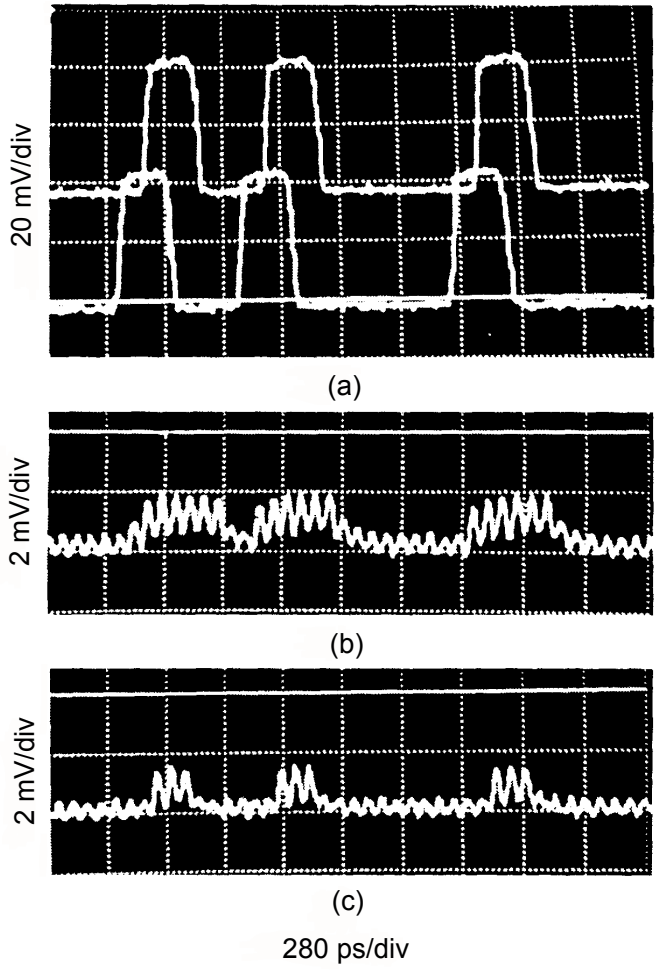


Figure 4.15: Measured performance of a COSL OR/AND gate at a clock frequency of 15 GHz. (**a**) Overlapping test data at 4 GHz input frequency. (**b**) OR gate output data. (**c**) AND gate output data. From [55].

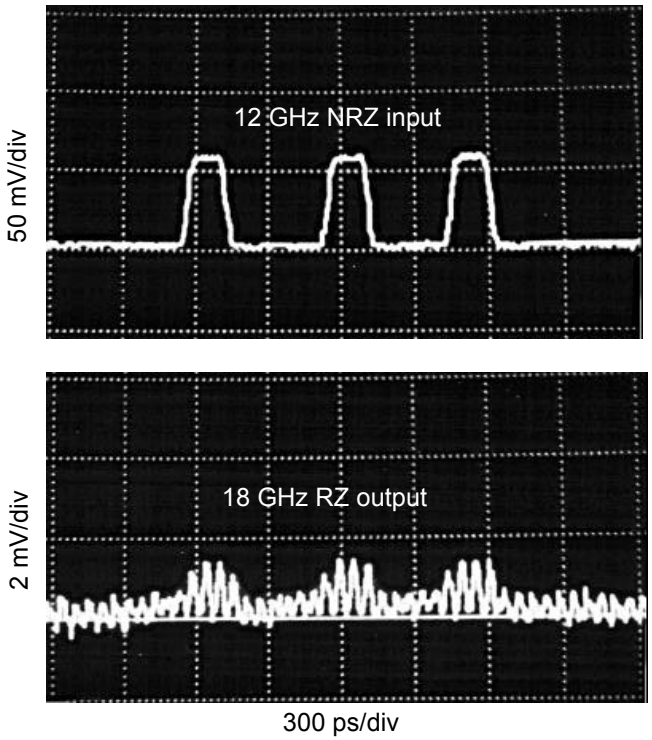


Figure 4.16: Measured performance of a COSL OR gate at a clock frequency of 18 GHz. The input data is a 12 GHz signal. From [55].

The results were obviously very gratifying, because it served as confirmation that COSL was the fastest superconducting voltage-state logic devices ever reported by quite a large margin.

4.1.7 High-frequency operation of encoding circuits for flash analog-to-digital converters

The original COSL gates were optimized by doing Monte Carlo yield approximations, as was described in Section 4.1.4. The global and local circuit parameter variations were estimations and not based on real data. In order to gauge the accuracy of the assumptions, the real parameter variations of the *HYPRES* 1 kA/cm^2 fabrication process, the process that was used to fabricate the original COSL family of gates, was investigated [56].

4.1.7.1 Measured process variations of *HYPRES* 1 kA/cm^2 process

The *HYPRES* global variation data for critical current density and resistance is shown in Figure 4.17(a) and 4.17(b), respectively. The data was obtained from measured values that were reported by *HYPRES* for chips bought by the University of Rochester. The average values of critical current density for 106 wafers are given in the bar graphs, as well as the average values of resistance for 95 wafers. The target critical current density was 1 kA/cm^2 and the target resistance was 1 $\Omega/\square$. The dashed lines in Figure 4.17(a) give the range of values of critical current density that was within specifications, according to the *HYPRES*

design rules. All the resistance values shown in Figure 4.17(b) were within *HYPRES* specifications. From the data the standard deviation for critical current density was σ=12.5%, with an average of 1.038 kA/cm^2. The standard deviation for resistance was σ=7.8%, with an average of 0.953 Ω/□.

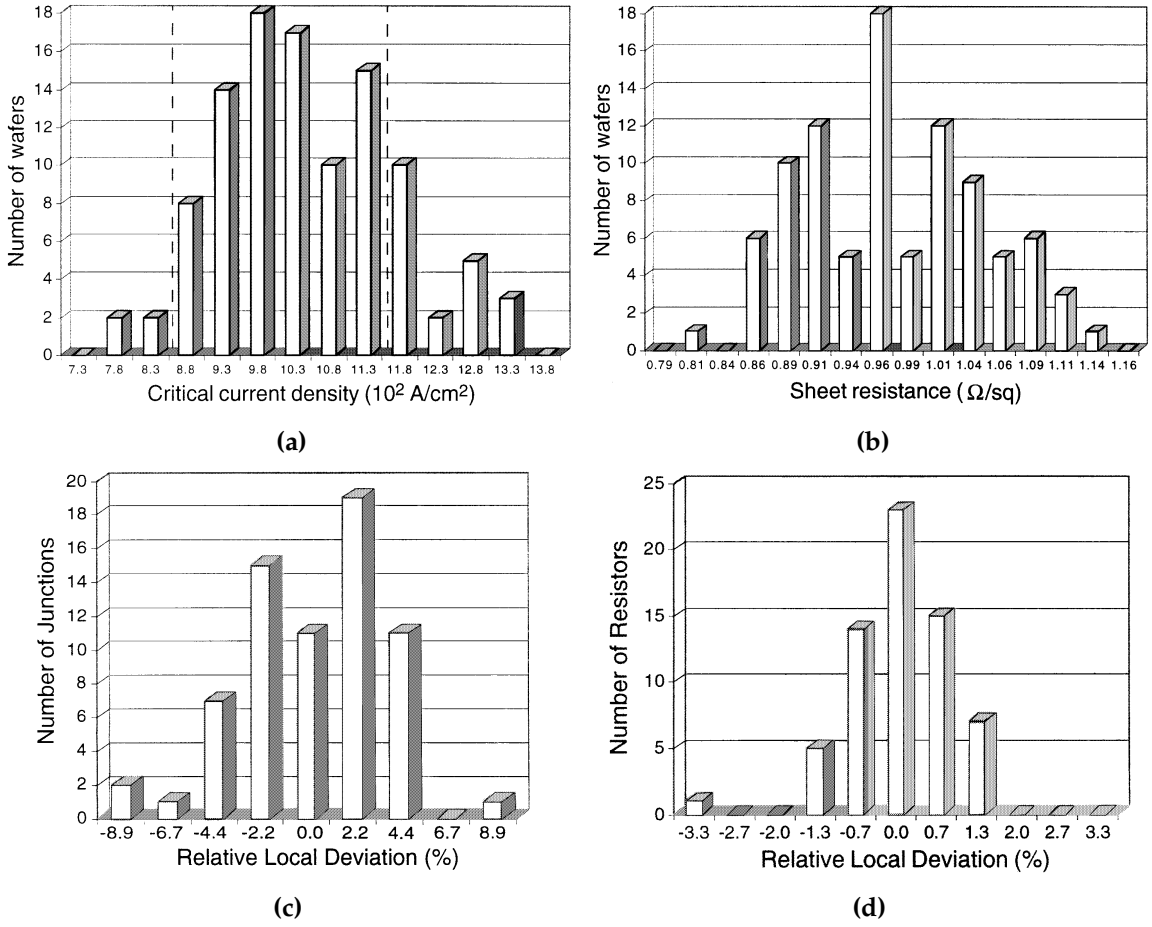


Figure 4.17: Measured process variations in (**a**) global critical current density, (**b**) global resistance, (**c**) local variations in critical current density, and (**d**) local variations in resistance. Global data values (a) and (b) courtesy of M. Feldman and D. K. Brock. From [56].

In order to quantify local variations, test chips were designed at UC Berkeley with identical resistors and Josephson junctions, all evenly distributed over the chip surface. Five resistance chips, with thirteen 5 Ω resistors, and five chips with fifteen 200 μA Josephson junctions were fabricated by *HYPRES*. The measured standard deviation for critical current was σ=3.7%, with an average of 186 μA, while the standard deviation for resistance was σ=0.82%, with an average of 4.6 Ω.

Inductance variations were not explicitly measured. Global variations were based on the work of Gaj and coworkers from the University of Rochester, who estimated that the *HYPRES* process had a 3σ variation of 8.5% [57]. The local variations were based on mea-

surements by Polonsky from the State University of New York, who found that the values were well within 5% [58].

A graphical representation of how global and local parameter variations were used in the Monte Carlo optimization of circuit yield is shown in Figure 4.18.

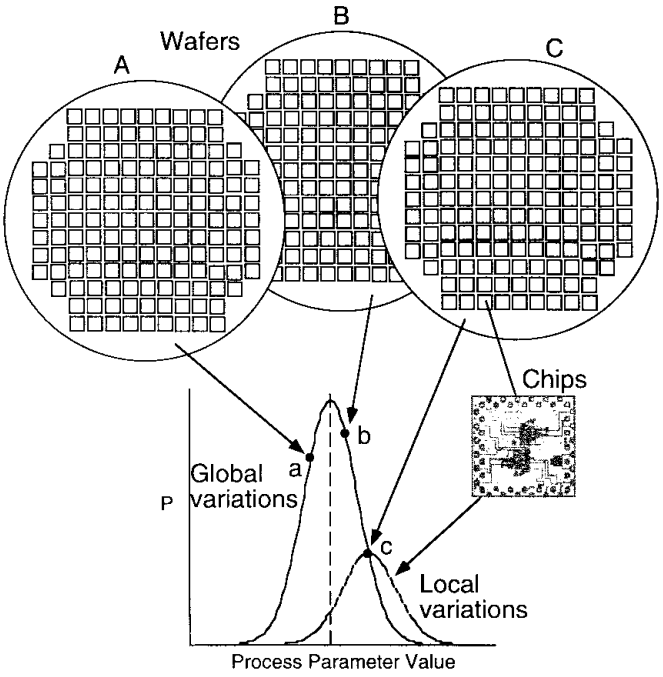


Figure 4.18: Schematic of global and local process variations used in a Monte Carlo optimization process. From [56].

Each chip has a global deviation approximated by wafer-to-wafer Gaussian distributions. In addition to global variations, components fabricated on the same chip have different local variations, which are also Gaussian distributed. These local variations are in addition to the global variations, shown schematically for the wafer C. The process deviations on a single chip are therefore described statistically by the multiplication of the global and local Gaussian distribution functions.

4.1.7.2 Monte Carlo yield calculations of 2-bit and 3-bit encoder circuits

In order to test the performance of the COSL gates in more complicate circuits, a 2-bit and 3-bit encoder were designed. These encoders are used in flash analog-to-digital (A-to-D) converters. An n-bit flash A-to-D converter consists of $2^n - 1$ comparators, each comparator switching at a higher input value, rendering so-called thermometer code. The n-bit encoder converts the thermometer code to a binary output. As an example, the simulation results of 2-bit flash A-to-D converter is shown in Figure 4.19, at a clock frequency of 10 GHz.

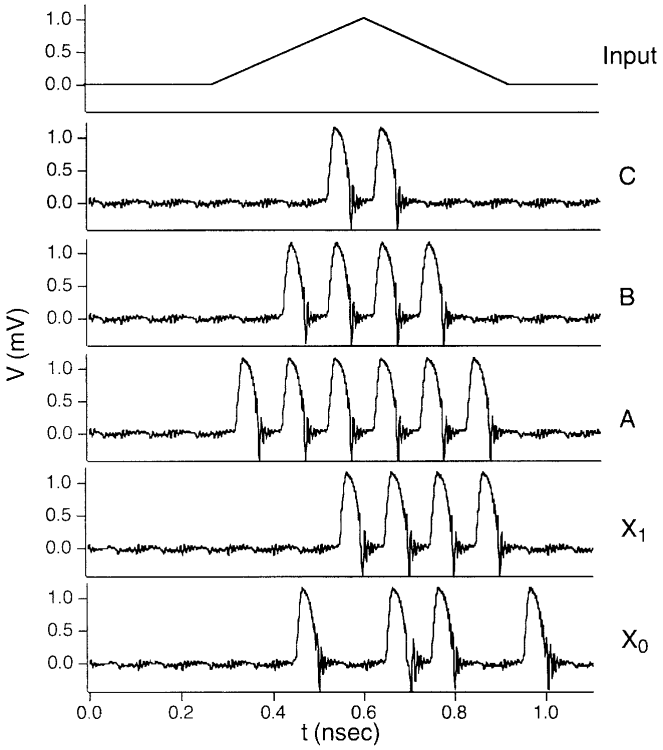


Figure 4.19: Simulation results of a 2-bit A-to-D converter at 10 GHz, showing the input, the outputs of the comparators (A, B, C) and the digital outputs (X_o, X_1). From [56].

The Boolean expressions for the two outputs of the 2-bit encoder are given by

$$X_1 = B \tag{4.1.5}$$

$$X_0 = A\overline{B} + C = A \oplus B + C \tag{4.1.6}$$

where $\oplus$ denotes the XOR function.

The two logic implementations and the COSL implementation of the 2-bit encoder are shown in Figure 4.20.

For a 3-bit encoder, there are seven comparator outputs (A, B, C, D, E, F, G), which are encoded into three digital output bits (X_0, X_1, X_2). The logic expressions for the output bits can be written as

$$X_2 = D \tag{4.1.7}$$

$$X_1 = D\overline{B} + DF \tag{4.1.8}$$

$$= \overline{\overline{D} + \overline{B}} + \overline{\overline{D} + \overline{F}} \tag{4.1.9}$$

$$X_0 = \overline{D}(A \oplus B + C) + D\overline{D \oplus E + F} + G \tag{4.1.10}$$

$$= \overline{D + \overline{A \oplus B + C}} + \overline{\overline{D} + D \oplus E + F} + G. \tag{4.1.11}$$

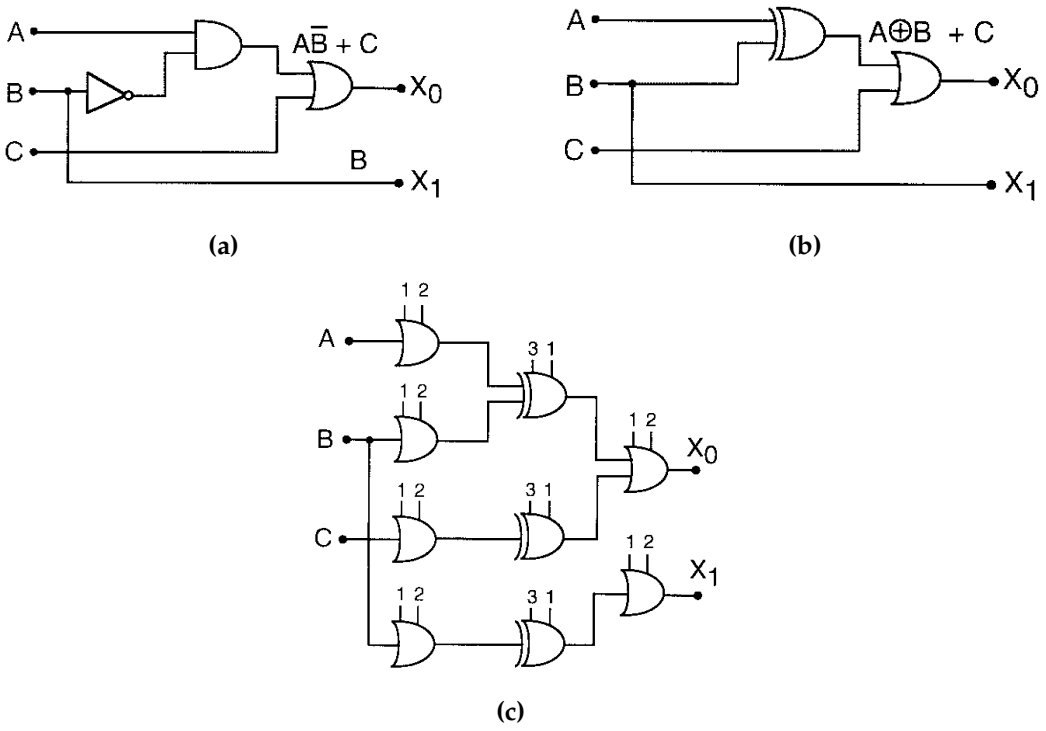


Figure 4.20: The 2-bit encoder logic. (**a**) OR/AND implementation, (**b**) XOR/OR implementation and, (**c**) the XOR/OR COSL gate implementation, including the buffers, and showing the clock phasing. From [56].

The logic implementation of the 3-bit encoder, using OR, AND and XOR gates, is shown in Figure 4.21(a) and the COSL implementation is shown in Figure 4.21(b). The inverter function was implemented by an XOR gate, with one input continuously clocked high.

Monte Carlo yield analyses were performed on the COSL implementations for the 2-bit and 3-bit encoders, as well as for the 2-bit MVTL implementation of the encoder. The global variations were chosen as 3σ=15% for R and L, and 3σ=10% for J_c, while the 3σ local parameter variations were chosen as 5% for the first data set, and 10% for the second data set. The third data set was calculated with the measured 3σ parameter variations, i.e. global variations of 37% for J_c, 23% for resistance and 15% for inductance, and local variations of 11% for J_c, 2.5% for resistance and 5% for inductance.

The calculated yields for the 2-bit encoder implementations, for 100 Monte Carlo cycles, are shown in Figure 4.22 at 5 GHz and 10 GHz clock frequencies. The yields of the COSL implementation, with trimming, were also calculated.

From Figure 4.22 it was clear that the MVTL implementation showed the lowest yield at 5 GHz and at 10 GHz clock frequencies. As expected, an increase in local parameter variations had a marked influence on yield, as was the case for the high global and local variations that were measured. Also noticeable was that trimming of the circuits had a marked positive influence on the yield.

In Figure 4.23 the calculated circuit yield for the COSL 3-bit encoder, for 50 Monte Carlo

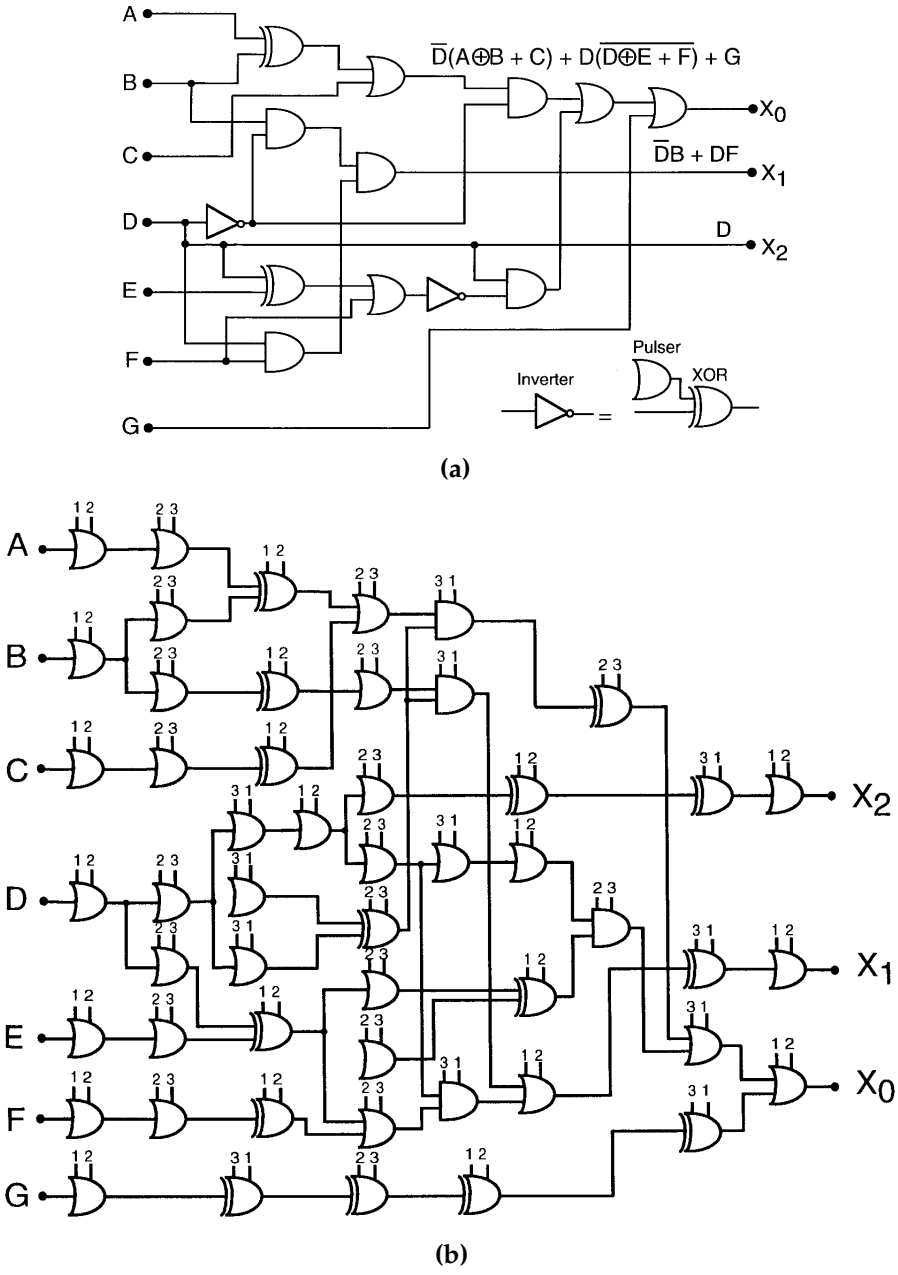
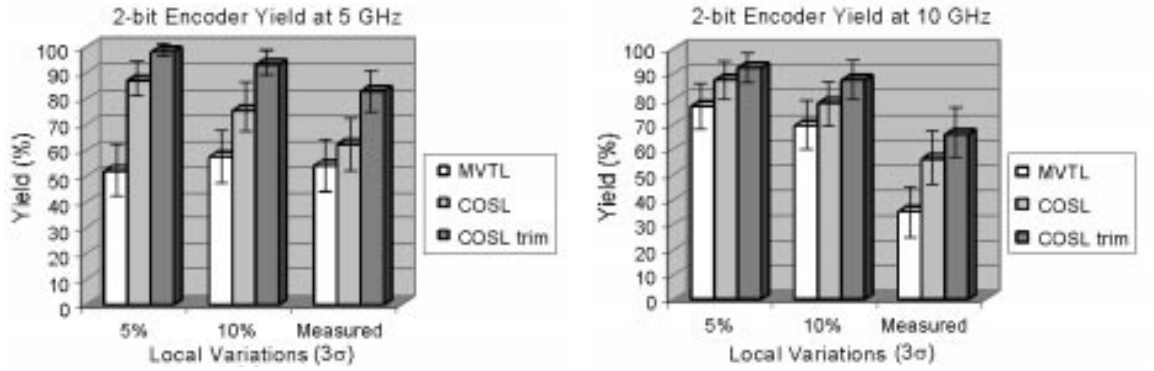


Figure 4.21: The 3-bit encoder logic. (**a**) XOR/OR/AND logic implementation, and (**b**) COSL gate implementation, including the buffers, and showing the clock phasing. From [56].

cycles, is shown, for the same parameter spreads as was the case for the 2-bit encoder, at a clock frequency of 10 GHz. For the first two parameter sets the calculated yields are also shown for no global parameter variations.

The calculated yields in Figure 4.23 clearly demonstrated that large global parameter variations, as was the case with the measured data, had a large influence on the probability that practical circuits would operate at high clock frequencies (e.g. 10 GHz).



(a) **(b)**

Figure 4.22: Simulated yield of 2-bit encoder at (**a**) 5 GHz clock frequency, and (**b**) 10 GHz clock frequency. Errors bars reflect the statistical uncertainty. From [56].

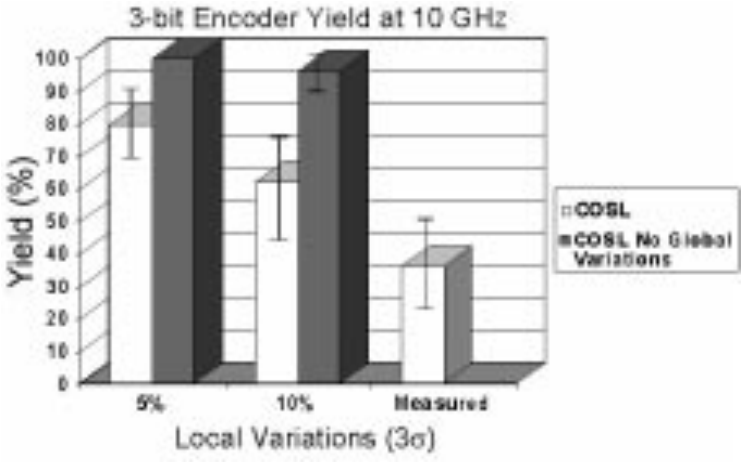


Figure 4.23: Simulated yield of COSL 3-bit encoder at 10 GHz clock frequency. Errors bars reflect the statistical uncertainty. From [56].

4.1.7.3 Layout and measured test results of a COSL 2-bit encoder

The COSL 2-bit encoder was fabricated using the 1 kA/cm^2 *HYPRES* process. A photograph of the 5 mm $\times$ 5 mm chip is shown in Figure 4.24. The chip contains two 2-bit encoders. All the transmission lines were impedance matched.

The measured test results at a clock frequency of 1 GHz are shown in Figure 4.25(a), and in Figure 4.25(b) when the circuit was clocked at 4 GHz. In the latter case the inputs were 1 GHz return-to-zero pulses, which explains the two pulses at the output for every single input pulse.

The thermometer code corresponding to a linear upwards and downwards sweep (see Figure 4.19 for simulation results) is shown in the three top traces of every graph, and the correctly encoded digital outputs in the bottom two traces.

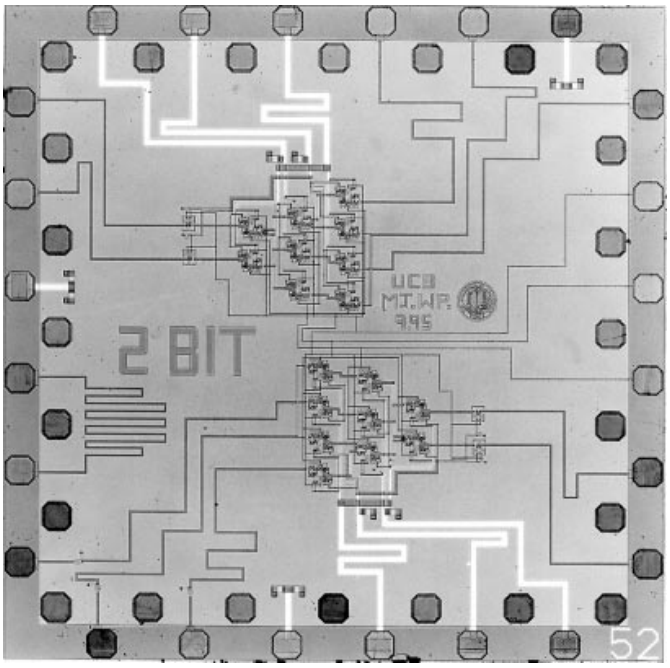


Figure 4.24: Photograph of the 5 mm × 5 mm 2-bit encoder chip fabricated using the 1 kA/cm^2 *HYPRES* process. From [56].

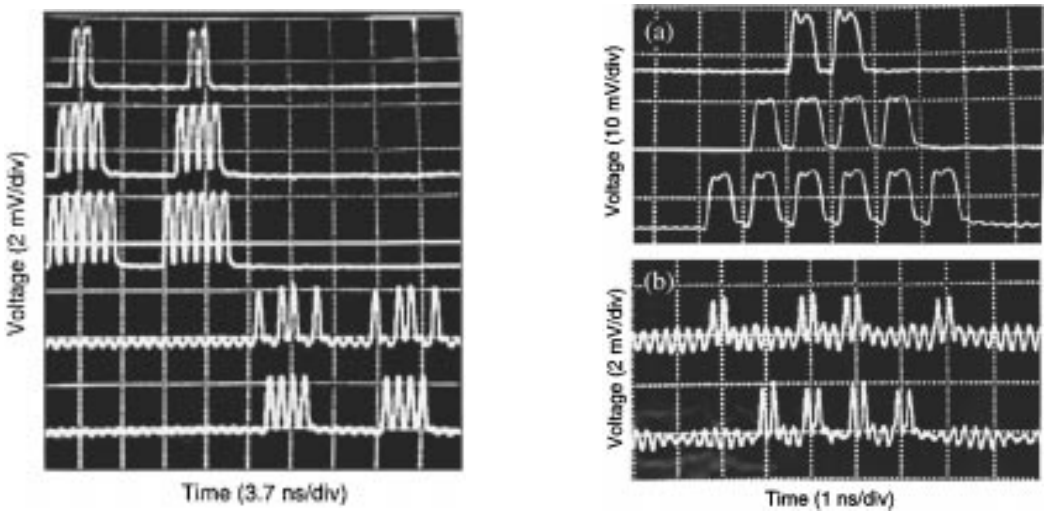


Figure 4.25: Measured results of 2-bit encoder (**a**) with 1 GHz clock frequency, and (**b**) with a 4 GHz clock frequency and 1 GHz RZ input pulses. From [56].

4.1.8 A COSL pseudo-random bit-sequence generator

To further explore the applicability of COSL gates to more complex circuits at GHz frequencies, a 4-bit pseudo-random bit-sequence generator (PRBSG) was designed [59].

The block diagram of a 4-bit PRBSG is shown in Figure 4.26, as well as the schematic of the COSL implementation.

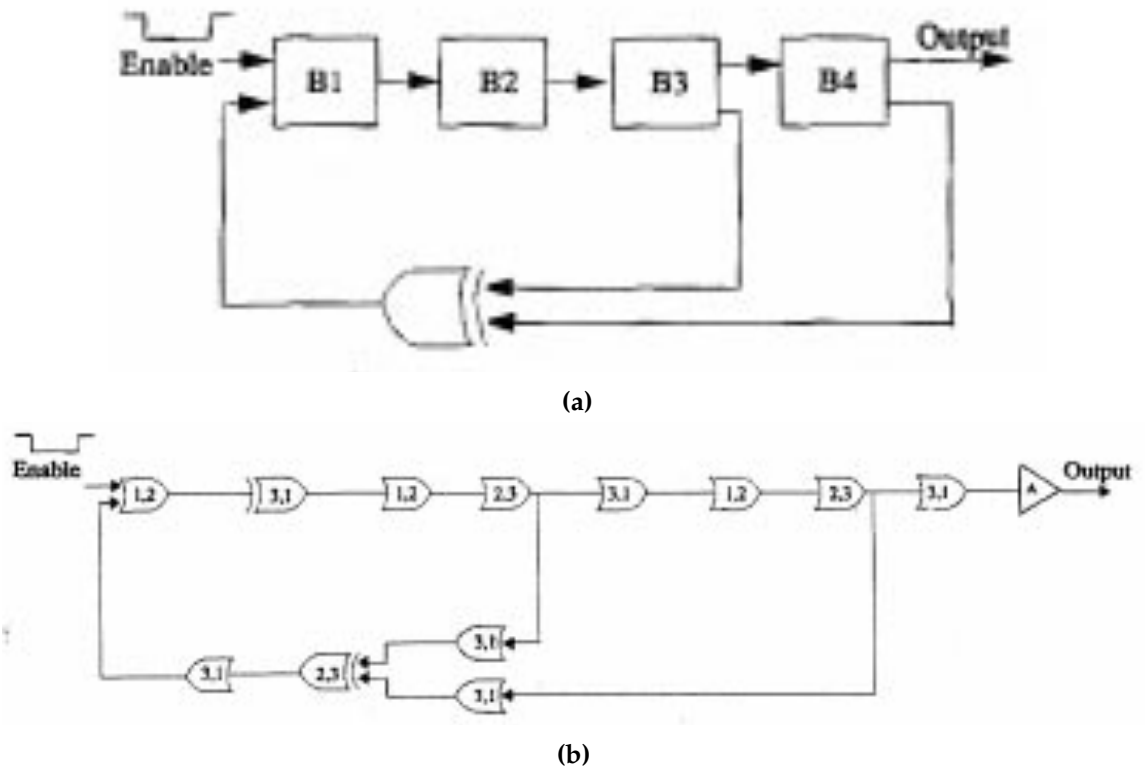


Figure 4.26: (**a**) Block diagram of 4-bit PRBSG, and (**b**) schematic of COSL implementation. From [59].

The PRBSG was implemented with the COSL gates that were optimized for optimum yield [56]. The gates in the forward path of the PRBSG, shown in Figure 4.26(b), are only equivalent to a 3-bit shift register, but the latency of the XOR gate and the buffers in the feedback path is equivalent to a 1-bit shift register, making the delay in the loop equivalent to a 4-bit shift register. In order to to start generating the periodic 4-bit pseudo-random bit sequence, it was required to zero the *Enable* input after at least four clock cycles at a logical "1". That was due to the latching nature of the COSL gates. The output of the PRBSG was fed to an on-chip COSL amplifier circuit, which switched the output to the gap voltage (2.5 mV) into a 50 Ω load. The correct output sequence of the circuit was 0,0,0,1,0,0,1,1,0,1,0,1,1,1,1.

The simulated results of the 4-bit PRBSG is shown in Figure 4.27 at a clock frequency of 10 GHz, confirming the correct sequence (starting at about t=1 ns).

The layout consisted of 12 gates and one amplifier, which converted the output voltage level form 1 mV to 2.5 mV (the gap voltage), switching into the 50 Ω input resistance of the measuring equipment. A total of 136 resistors and 75 Josephson junctions were used. The dimensions of the PRBSG were 1530 × 950 μm^2 and it was fabricated in the 1 kA/cm^2 *HYPRES* process. The layout of the circuit is shown in Figure 4.28.

The non-averaged measured output of the 4-bit PRBSG is shown in Figure 4.29(a) for three periods of the bit sequence, at a clock frequency of 1 GHz. The output was amplified by a microwave amplifier (*HP 8347A*) with a gain of 25 dB and a 3 GHz bandwidth. The

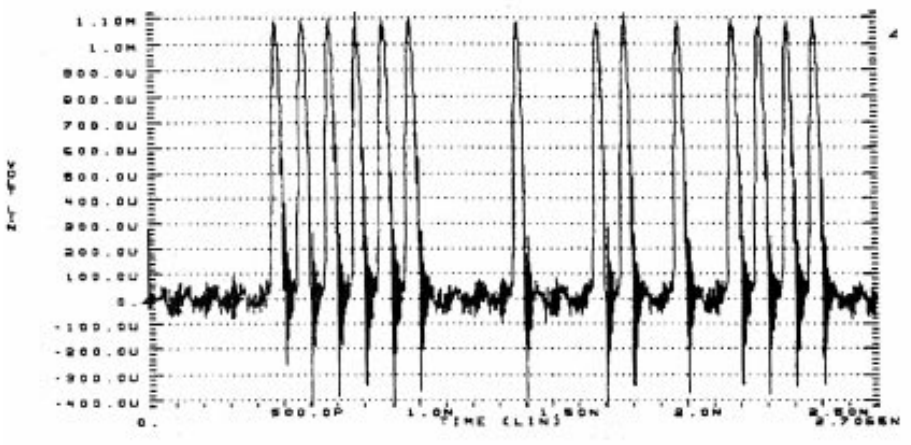


Figure 4.27: Simulation results of the 4-bit PRBSG at a clock frequency of 10 GHz. From [59].

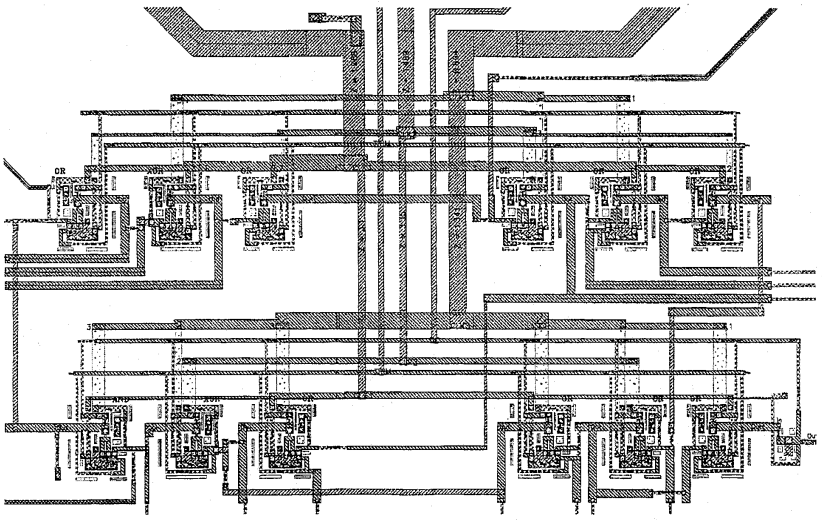


Figure 4.28: Layout of the 4-bit PRBSG. From [59].

clean eye pattern is shown in Figure 4.29(b) at a clock frequency of 1 GHz. The horizontal width of the lines gives an indication of the jitter (phase noise) of the circuit. The eye pattern was obtained from the PRBSG output by triggering on every eighth clock cycle.

The output of the PRBSG at a clock frequency of 2 GHz is shown in Figure 4.30. The output voltage was about 2 mV and was obtained by averaging, and without amplification. The measured results confirmed the correct and stable operation of the PRBSG at 2 GHz.

4.1.9 COSL amplifier circuits

Typical output voltages of superconducting logic circuits range from about 0.1 mV to approximately 2.5 mV. In Rapid Single Flux Quantum (RSFQ) circuits [60], output voltages of about 0.1 mV are typically generated.

With the COSL configuration the capability to interface with room temperature electronics by amplification of the on-chip voltage levels was demonstrated. An on-chip single-junction amplifier was provided to convert the nominal 1 mV output voltage to a 2.5 mV

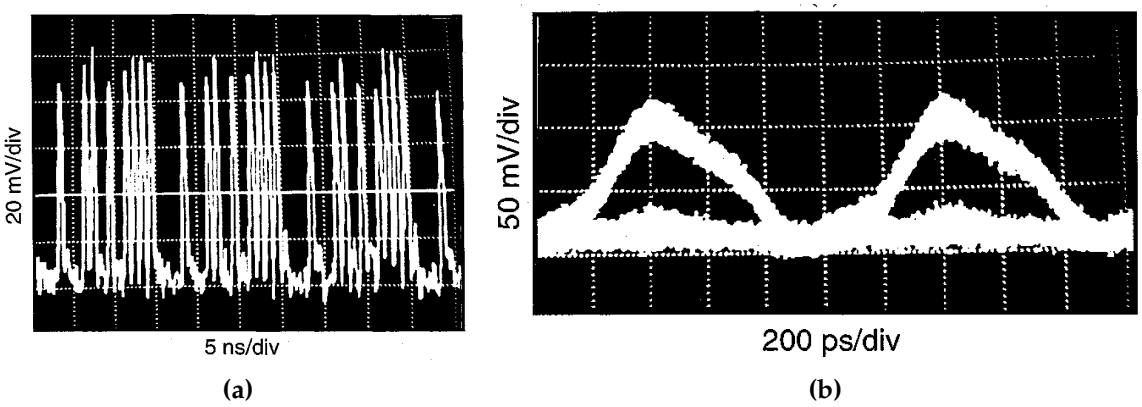


Figure 4.29: (**a**) Measured output of 4-bit PRBSG at a 1 GHz clock frequency, showing three periods of the bit sequence. (**b**) The eye pattern of the 4-bit PRBSG at a 1 GHz clock frequency. From [59].

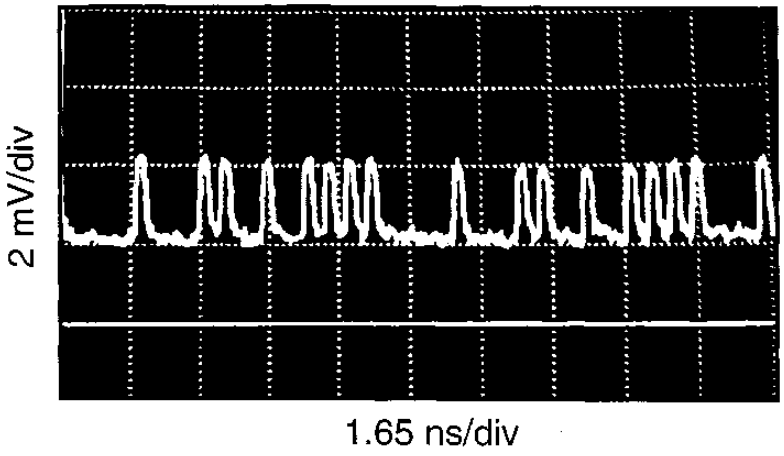


Figure 4.30: Averaged output of the 4-bit PRBSG at 2 GHz. From [59].

output voltage, switching into a 50 Ω external load (Figure 4.5). It was thus decided to explore the amplification capabilities of the COSL configuration further, to see whether on-chip amplification was practical, especially at frequencies in excess of 5 GHz.

The first attempt at on-chip amplification was the Suzuki stack [61], as is shown in Figure 4.31. Every Josephson junction in the stack is designed to switch to the gap voltage (V_G), giving a theoretical output voltage of nV_G, where n is the number of junctions in the stack.

One of the main problems of a Suzuki stack is the fact that it is very sensitive to variations in the critical current of the Josephson junctions. If, for example, the critical current of one of the Josephson junctions in the output series branch is notably smaller than the rest, that junction will switch first to the high impedance state. This will limit the current to such an extent that none of the other series junctions will be able to switch. The output voltage will thus be limited to the gap voltage V_G.

Another serious drawback of the Suzuki stack is the inability to switch off at high fre-

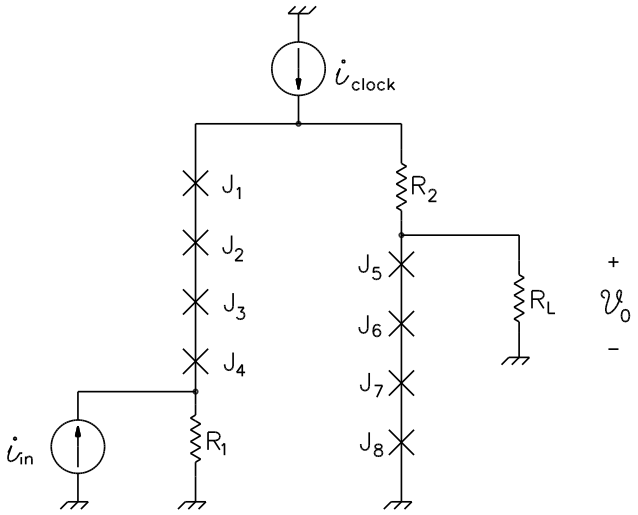


Figure 4.31: Circuit diagram of a typical Suzuki stack amplifier. From [62].

quencies when the clock goes negative. This is due to the relatively high shunt capacitances of the Josephson junctions when standard critical current density fabrication processes are used. The problem is alleviated when every Josephson junction is shunted by a resistor, but this reduces the output voltage considerably. Monte Carlo yield analyses [56] on a Suzuki stack, using the 1 kA/cm^2 Josephson junction model, showed that, even with shunt resistors across the Josephson junctions, the Suzuki stack was not a viable proposition for on-chip amplification at GHz frequencies, especially when a standard critical current density process was used.

The basic configuration of our first attempt to implement a COSL stack amplifier is shown in Figure 4.32 [62]. Two stacked two-junction SQUIDs, each driven individually by a one-junction SQUID, are shown. Each two-junction SQUID is shunted by a resistor to ensure switch off during the negative portion of a clock cycle. The output voltage of each individual two-junction SQUID will thus be reduced to less than the gap voltage, but enhanced switching stability will theoretically be obtained. The stack amplifier is designed to switch into 50 Ω.

To test the concept, an amplifier using 6 stacked two-junction SQUIDs at the output was designed [62]. The simulated nominal output voltage was 5.2 mV. The amplifier was fabricated using the 1 kA/cm^2 *HYPRES* process. The unaveraged measured performance of the amplifier is shown in Figure 4.33(a) at a frequency of 5 GHz. The input was generated by a pseudo-random bit sequence generator and applied directly to the input of the amplifier. The measured eye diagram of the 6 SQUID stack amplifier is shown in Figure 4.33(b). The diagram was measured at 5 GHz. It is quite clear from the very clean eye diagram that the bit error rate was very low. It was estimated to be less than 10^{-6}.

Measurements at 10 GHz were subsequently taken. The output voltage was measured as 4 mV, which was acceptable considering the notable attenuation of the measurement probe at that frequency (see Figure 4.34). At 1 GHz the output voltage was measured as 5 mV,

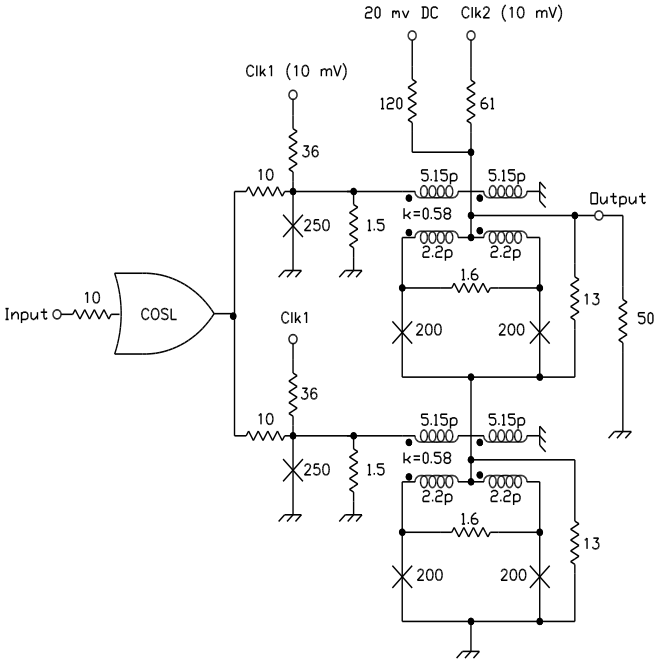
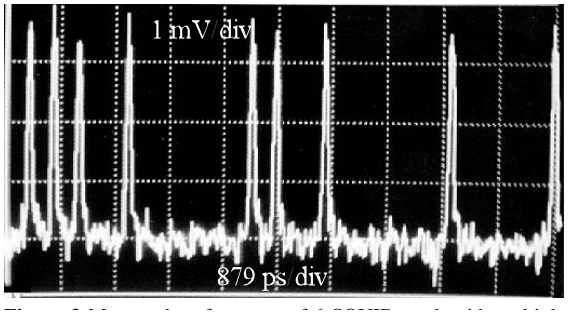
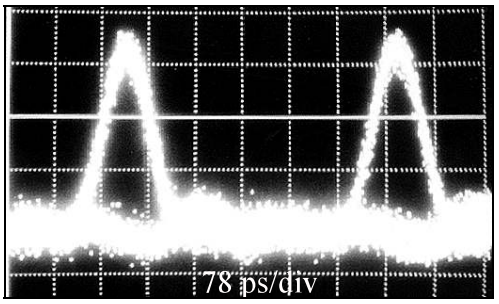


Figure 4.32: Circuit diagram of a 2 SQUID COSL stack amplifier. Each two-junction SQUID is driven by a separate one-junction SQUID. The OR gate feeding the one-junction SQUID drivers, is also shown. From [62].



(a)



(b)

Figure 4.33: Measured performance of 6 SQUID stack with multiple drivers at 5 GHz. (**a**) Unaveraged output voltage. (**b**) Eye diagram. From [62].

which corresponded well with the nominal value.

In order to eliminate the need for COSL OR gates to drive the one-junction SQUIDs of the mentioned amplifier configuration, an alternative input driver scheme was implemented, where only one driver was used to feed all two-junction SQUIDs in the stack. The circuit diagram of such a configuration is shown in Figure 4.35, where a stack of 4 two-junction SQUIDs was used. Monte Carlo yield analyses were done on the circuit, and the untrimmed yield was calculated as 86%, with the same global parameter deviations that were used for the optimization of the COSL gates, and with 10% local variations. With input trimming the yield improved to 96%.The nominal output voltage at 10 GHz was determined by simula-

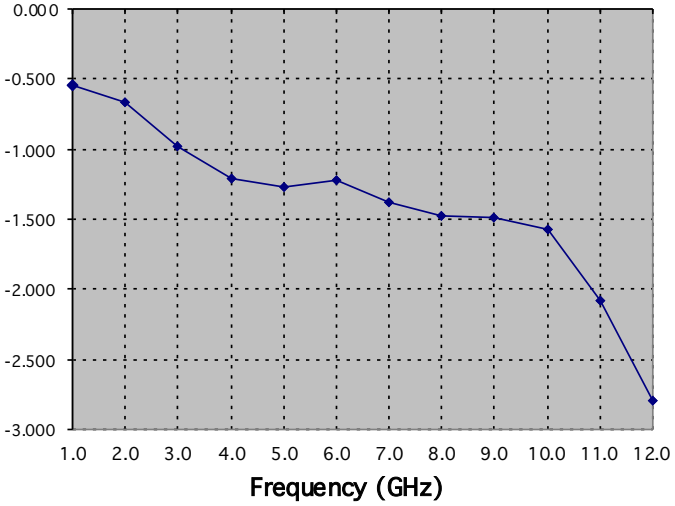


Figure 4.34: Measured probe attenuation as a function of data frequency. From [62].

tions as 4.7 mV.

In order to optimize the frequency performance of the amplifier, the 2.5 kA/cm^2 *HYPRES* process was used to fabricate the circuit. The one-junction SQUID driver was layed out to ensure that each inductance branch, feeding the two-junction SQUIDs in the stack, had the same inductance, including parasitic inductances, as shown in Figure 4.36(a).

The measured performance of this design was very unsatisfactory. It was suspected that the parasitic inductance in the inductance branches of the one-junction SQUID driver was the reason for the non-functionality of the amplifiers.

In a subsequent design, also using the 2.5 kA/cm^2 *HYPRES* process, the layout was changed to minimize the parasitic inductances, as is shown in Figure 4.36(b). The averaged measured performance of the stack amplifier is shown in Figure 4.37, at a clock frequency of 5 GHz. The input voltage was generated by a pseudo-random bit sequence generator. The relatively large input voltage was sent through a resistive 50 Ω to 5 Ω matching network. The output voltage, with the probe attenuation taken into account, was more than 4 mV. It was observed that the amplifier did misfire occasionally.

It was evident from the measurements that parasitic inductances inherent to the layout had a marked influence on the performance of the amplifier circuits, and that knowledge of these parasitic components, and incorporation of the parasitics into the yield prediction computer models, were crucial in the realistic prediction of circuit performance, especially at high frequencies.

To further explore the effect of parasitic components due to non-optimum circuit layout practices, it was decided to optimize the layout of the 4 SQUID stack with a single driver, by paying special attention to the elimination of parasitic inductance and the minimization of electromagnetic field concentrations. The parasitic inductances were minimized by folding the stacked two-junction SQUIDs in a horseshoe pattern [63]. This ensured equal parasitic inductance in each of the four inductive branches. The parasitic inductance in each branch was calculated by SLINE [64] as approximately 0.7 pF, which gave a noticeable improvement

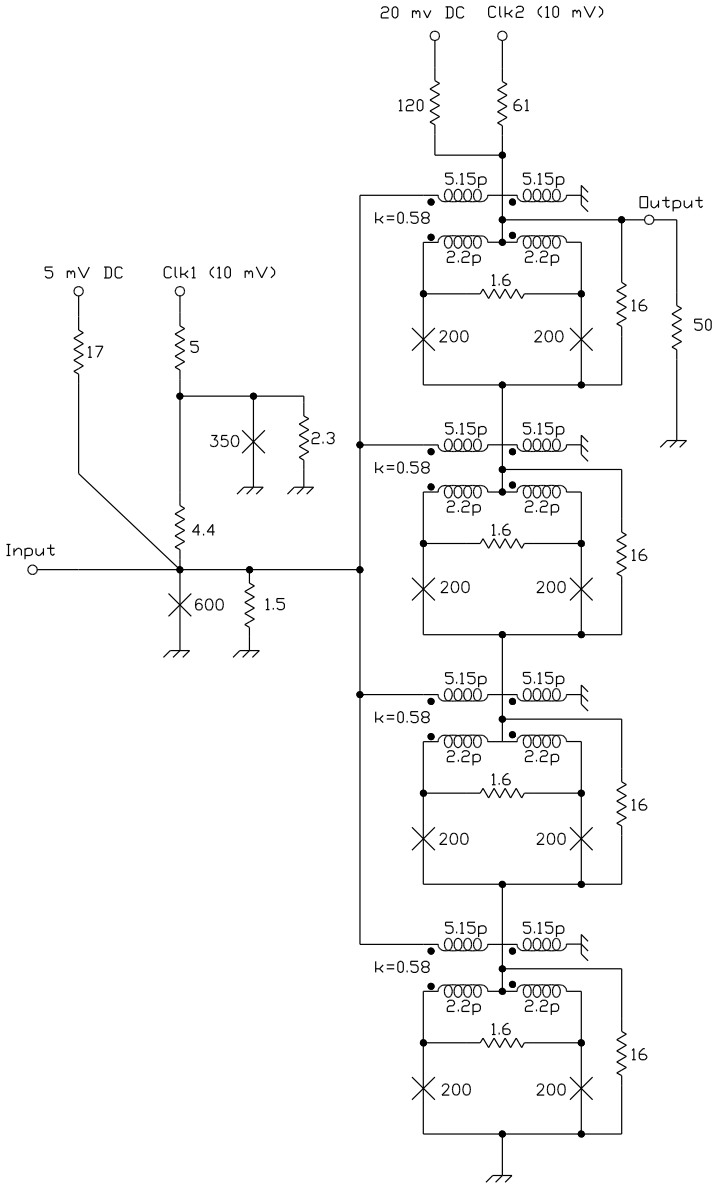
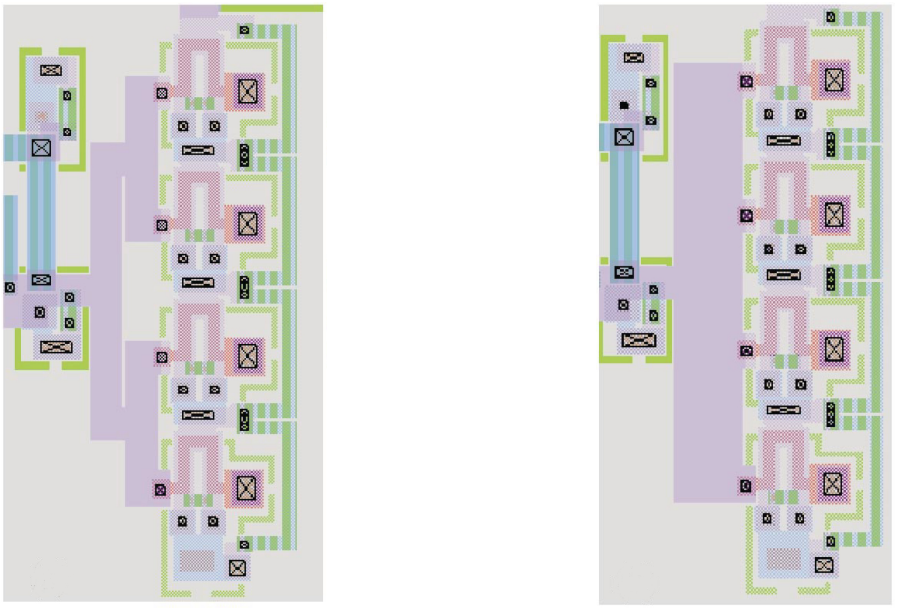


Figure 4.35: Circuit diagram of a 4 SQUID COSL stack amplifier with a single one-junction SQUID driver. From [62].

when compared to the values for the previous layouts. Electromagnetic field concentrations were minimized by making all structures with rounded corners. A portion of the layout is shown in Figure 4.38. The rounded Josephson junctions and resistor structures are noticeable.

The untrimmed yield of the new layout, including the parasitic inductances, was calculated as 92% for 50 Monte Carlo cycles. The yield increased to 98% with input trim. This was a vast improvement in yield when compared to the other layouts.

The 1 kA/cm^2 *HYPRES* process was used to implement the stack amplifier. The performance of the amplifier was tested at 2 GHz, 5 GHz and 10 GHz. The input voltage was generated by a pseudo-random bit sequence generator. The measured non-averaged out-



(a) (b)

Figure 4.36: Two different layout approaches for the inductive portion of the driver circuit, where (**a**) the inductances are made equal, and (**b**) attempts were made to minimize the total parasitic inductances. Only portions of the respective layouts are shown. From [62].

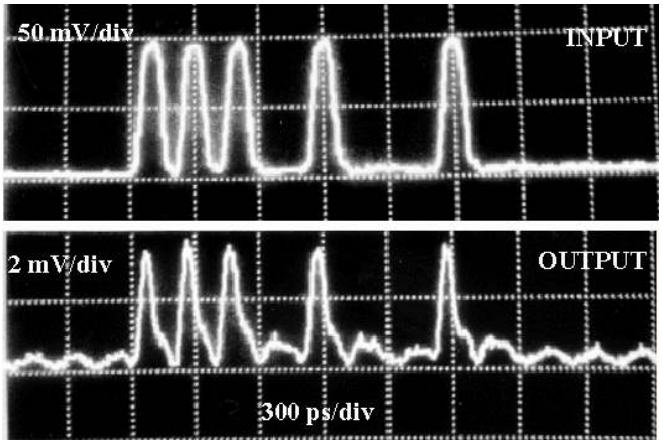


Figure 4.37: Measured response of 4 SQUID COSL stack amplifier with a single input driver, optimized to minimize parasitic inductances, at a clock frequency of 5 GHz. The measured data was averaged. From [62].

put data and the eye-pattern are shown in Figure 4.39, for a clock frequency of 2 GHz. The output voltage was measured as 3.2 mV, with a bit-error rate (BER) much less than 5×10^{-11}.

In Figure 4.40 the measured non-averaged output data and the eye-pattern are shown at a clock frequency of 5 GHz. The measured BER was 2×10^{-9}.

In Figure 4.41 the measured averaged output data is shown at 10 GHz. The output voltage was significantly attenuated by the measurement probe.

The measured results [62, 63] clearly suggested that parasitic components due to non-

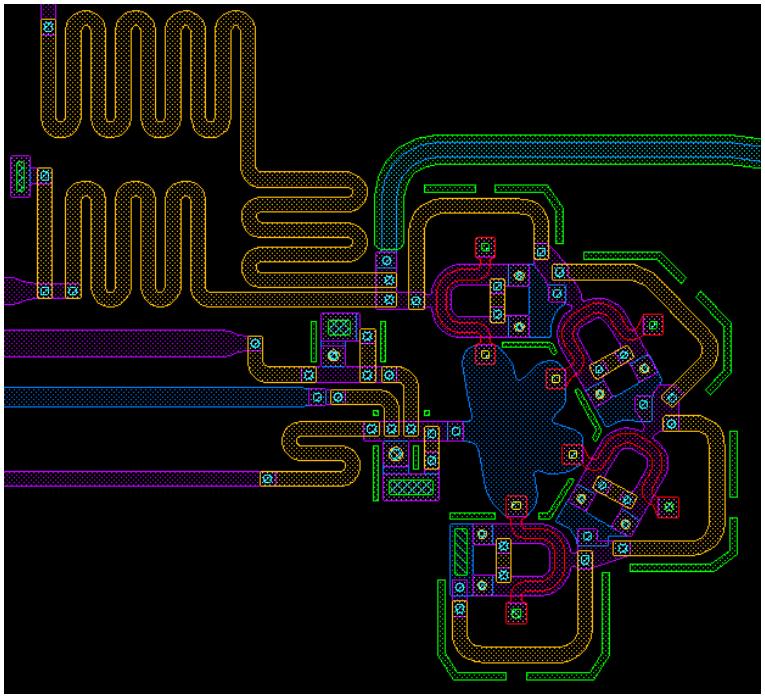
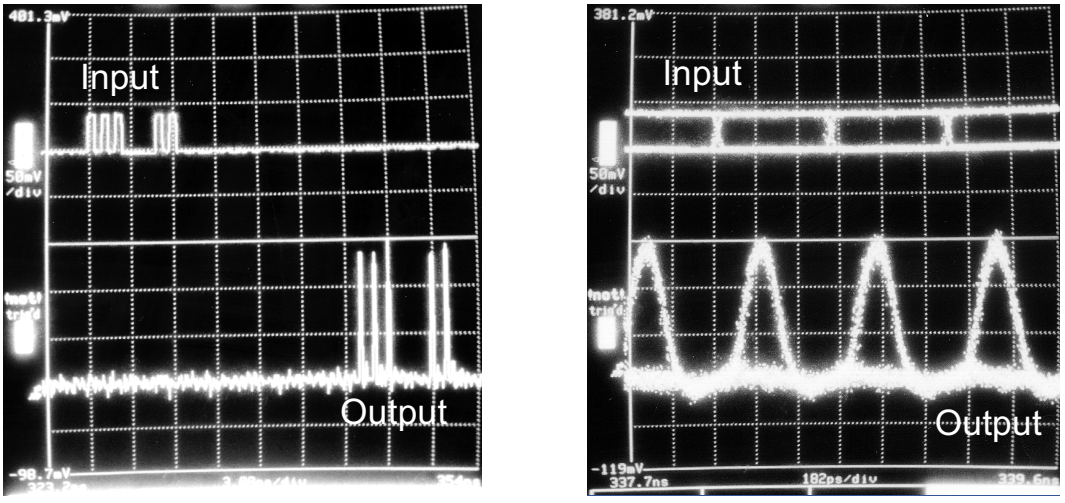


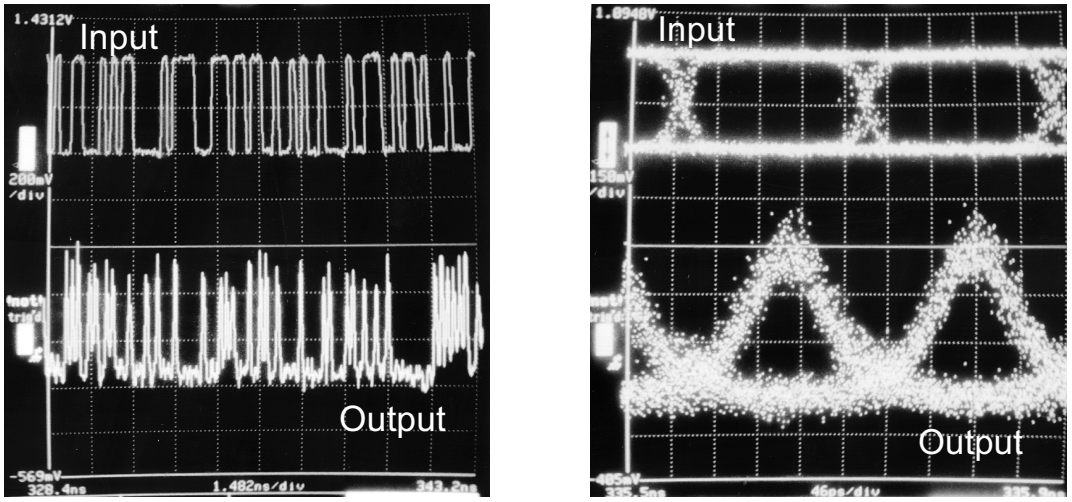
Figure 4.38: Optimized horseshoe architecture of 4 SQUID COSL stack amplifier. Rounded structures are used to minimize local electromagnetic field concentrations. From [63].

optimum layouts and process deviations had to be incorporated into the circuit models for accurate performance predictions, especially at frequencies higher than 5 GHz. The measurements also showed that the upper frequency limit for COSL circuits was around 10 GHz. Some of the insights only dawned on us after long and extended discussions with collaborators and friends, as shown in Figure 4.42.



(a) **(b)**

Figure 4.39: Measured response of 4 SQUID COSL stack amplifier with an optimized horseshoe architecture at a 2 GHz clock frequency. (**a**) Non-averaged output voltage versus input voltage. (**b**) Eye-pattern. From [63].



(a) (b)

Figure 4.40: Measured response of 4 SQUID COSL stack amplifier with an optimized horseshoe architecture at a 5 GHz clock frequency. (**a**) Non-averaged output voltage versus input voltage. (**b**) Eye-pattern. From [63].

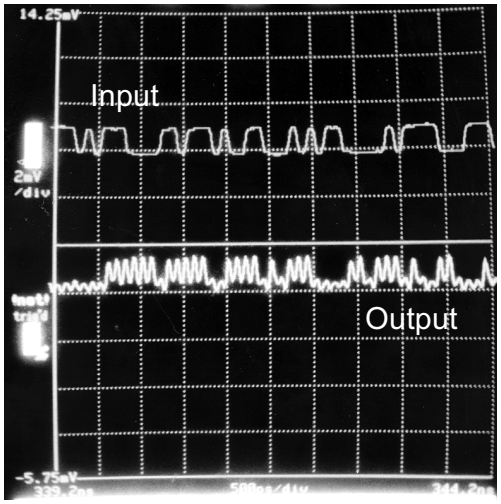


Figure 4.41: Measured averaged response of 4 SQUID COSL stack amplifier with an optimized horseshoe architecture at a 10 GHz clock frequency. From [63].

4.2 Summary

In this chapter my sabbatical year at UC Berkeley was described and also the subsequent collaboration with Prof Van Duzer's group, which actively continued until 1999.

During this period the new COSL voltage-state logic family was proposed [50, 52], and then the (for us very exciting) progress with regard to switching speed was reported [53, 54, 55]. A new approach to predict circuit yield was used to optimize the COSL family and also more complex circuit implementations [56]. The COSL family was successfully demonstrated at GHz frequencies for more complex circuits, such as a 2-bit encoder circuit for a flash analog-to-digital convereter [56] and a 4-bit pseudo-random bit sequence generator

(a) **(b)**

Figure 4.42: Technical discussions in Berkeley with (**a**) Mark Jeffery, and (**b**) Kazuo Saito of Hitachi, Japan.

(PRBSG) [59]. The last collaborative research was focused on the design and implementation of on-chip amplifiers to interface with 50 Ω room temperature instrumentation at GHz frequencies [62, 63].

Our work on on-chip interface amplifiers was important in the sense that it made us acutely aware of the pitfalls of non-optimum layout practices and the requirement that a knowledge of the parasitic components due to layout was very important for the accurate prediction of circuit performance. Back at Stellenbosch University, this influenced my research focus to quite a degree.

The Berkeley relationship had a marked influence on my career and I was indeed privileged to rub shoulders with Prof Ted Van Duzer, one of the all-time greats in superconductivity research – a remarkable and humble man indeed. The very close collaboration with Mark Jeffery was also very stimulating and productive, and proof that a physicist and engineer could actually be a good combination.

Chapter 5

Low-temperature superconductor circuit research at Stellenbosch

When I left Berkeley at the end of 1995 there were a number of research activities that were still in process, such as the high-frequency measurements on COSL gates. We also planned for continued collaboration on COSL circuit applications, such as encoding circuits and interface amplifiers. The collaboration continued until 1999, when Mark Jeffery left the research group at UC Berkeley to take up a position at the Kellogg School of Management in Evanston, Illinois. The contributions of the five year collaborative effort were discussed in Chapter 4.

Back at Stellenbosch research continued on the application of COSL circuits, but in combination with Rapid Single Flux Quantum (RSFQ) circuits. Circuit applications included analog-to-digital converter building blocks and also programmable logic circuits. It was also decided to explore the possibilities of high-T_c circuit fabrication.

Our planned research, to a large extent, was informed by the lessons that we have learnt with regard to the pitfalls of non-optimum layout practices and the resulting influence of parasitics on the performance of circuits.

5.1 Yield prediction based on circuit layout

The measured results of the COSL stack amplifiers [62, 63] clearly emphasized that the performance of a circuit could only be accurately predicted when the effect of parasitics was included in the yield prediction model.

In order to quantify the effect of the fabrication process on the performance of a device, a procedure was implemented in SPICE to calculate circuit yield using Monte Carlo analyses [65]. The global and local parameter variations of lumped components were extracted from the tolerances of the fabrication process.

To calculate inductance values based on circuit layout, the precomputed transmission line model of *HSPICE* [66] was used. The global (chip-to-chip) variations were incorporated by the layer thickness variations of the *HYPRES* fabrication process as specified in the de-

sign rules [67]. The local (on-chip) variations were taken as the inaccuracies in the mask dimensions. The mask offset values were also incorporated into the model. The parameter variations were thus included in the transmission line model as

$$h \Rightarrow h \pm \delta h_{global}, \tag{5.1.1}$$

$$t_{layer} \Rightarrow t_{layer} \pm \delta t_{layer(global)}, \tag{5.1.2}$$

$$w \Rightarrow w - w_{bias} \pm \delta w_{local}, \tag{5.1.3}$$

where h is the insulator thickness, t_{layer} is the layer thickness and w the width of the transmission line, as defined by the mask, and w_{bias} the mask offset value. The accuracy of the model was determined by comparing the inductance per unit length values for the M_1, M_2 and M_3 layers of the *HYPRES* process with values that were obtained by SLINE [64]. The maximum error values for the M_1, M_2 and M_3 layers were 1.3%, 2.1% and 3.2%, respectively.

The resistor structure shown in Figure 5.1 defines the length (ℓ), width (w) and thickness (h) of the resistor.

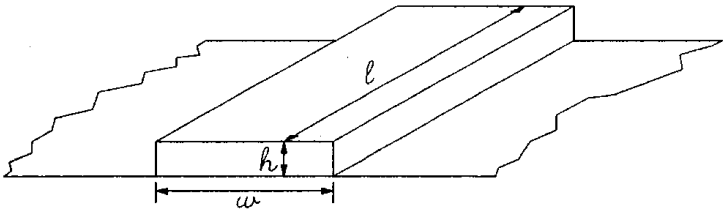


Figure 5.1: Cross-section of a resistor. From [65]

The resistance is expressed as

$$R = \rho\frac{\ell}{A} = \frac{\rho}{h}.\frac{\ell}{w} = R_{sheet}\frac{\ell}{w} \tag{5.1.4}$$

where ρ is the resistivity and R_{sheet} the sheet resistance ($\Omega/\square$) of the material.

Changes in the sheet resistance can be attributed to variations is layer thickness (global variations) and local variations to changes in the length and width of the resistor, due to variations in mask dimensions. The *HSPICE* resistor model could thus be described as

$$R = [R_{sheet} \pm \delta R_{sheet(global)}]\frac{\ell \pm \delta\ell_{local}}{w \pm w_{local}} + 2R_{contact} \tag{5.1.5}$$

where $R_{contact}$ is the contact resistance, and depends on the size of the via. The global variations in R_{sheet} was defined in the *HYPRES* design rules as $\pm$20%, while the uncertainty in the masks dimensions was specified as $\pm$ 0.5 μm.

In the *HSPICE* model of the Josephson junction the critical current density (J_c) and the area of the junction are defined. Changes in J_c can be attributed to changes in the thickness of the insulation layer and is thus defined as a global variation. Changes in the area, on the other hand, are attributed to inaccuracies in mask dimensions, and are thus seen as local

variations. These variations were incorporated into the expression of the Josephson current as

$$i_J = J_c A \sin(\varphi) = [J_c \pm \delta J_{c(global)}](\ell \pm \delta \ell_{local})(w \pm w_{local}) \sin(\varphi) \tag{5.1.6}$$

where A is the area of the Josephson junction, ℓ the length and w the width of the junction, and φ the gauge invariant phase difference.

HYPRES specified a changing mask-to-wafer offset bias between 3 μm and 6 μm, with zero offset for dimensions larger than 6 μm. The offset bias was approximated as a linear data fit by

$$\ell_{wafer} = 1.12\ell_{mask} - 0.72 \tag{5.1.7}$$

where ℓ represented either a length or width dimension.

The global variation in J_c was specified in the *HYPRES* design rules as $\pm$15%, while the local deviations on the mask were specified as $\pm$0.25 μm.

In order to test the usefulness of the layout based models, two layouts of a COSL stack amplifier [62] were analyzed, and compared to the yield of the ideal lumped element circuit.

For the ideal lumped element stack amplifier, the 3σ global variations of the critical current, resistance and inductance were taken as 10%, 15% and 15% respectively. The 3σ local variations of the Josephson junction area, resistance and inductance were all taken as 10%. The untrimmed yield of the stack amplifier at 10 GHz was then calculated as 94%, and the trimmed yield as 100%. In order to compare apples with apples, a circuit layout was done with the 2.5 kA/cm^2 *HYPRES* process, with all the global and local variations set to zero. All the nominal parameter values were thus defined by the fabrication process. The untrimmed yield was calculated as 88% and the trimmed yield as 90%.

The circuit yield of two layouts of the stack amplifier (Figure 4.36) [62] were then analyzed with the layout based approach. For the first layout the untrimmed and trimmed yield were calculated as 4%, while for the second layout the respective yield values were calculated as 84% and 76%. These values were thus in line with actual measurements, where the amplifier with the first layout did not function at all, and the amplifier with the second layout did function at 5 GHz, but with occasional misfires.

5.2 Circuit optimization utilizing genetic algorithms

In the period from 1999 to 2002 I supervised two students on research topics that did influence the direction of our research effort quite significantly. Coenrad Fourie looked at the implementation of a Sigma-Delta analog-to-digital converter using hybrid (RSFQ and COSL) digital logic [68] and Peter Gross investigated the implementation of superconducting FPGAs [69, 70]. The level of integration of the circuits, as well as the non-standard implementation of some logic functions, suddenly made cell optimization and circuit extraction tools important aspects of circuit design.

The COSL gate family was optimized manually by tweaking component values by hand until the Monte Carlo analysis peaked at certain yield value [50, 56]. This was a very tedious process and also did not guarantee that the circuit parameters were indeed optimum. In order to alleviate the problem, a procedure was proposed where the yield of superconducting circuits can be optimized by using genetic algorithms [71, 72].

The parent generation was defined as the initial nominal circuit parameters, and the first generation by random variations of the nominal circuit. This generation was then evaluated for fitness to reproduce. A fitness value was assigned to every component, and depending on the fitness value the components were allowed to reproduce. The fitness value was the circuit yield, as obtained from a Monte Carlo analysis. This process was allowed to go on until a required fitness value (yield) was obtained. A custom code was written to execute the genetic algorithm and interface with *WRSPICE* [64], which was used to generate the fitness values (circuit yield).

The optimization process was applied to two circuits, a novel RSFQ DC-resettable latch and a COSL set-reset flip-flop, as shown in Figure 5.2.

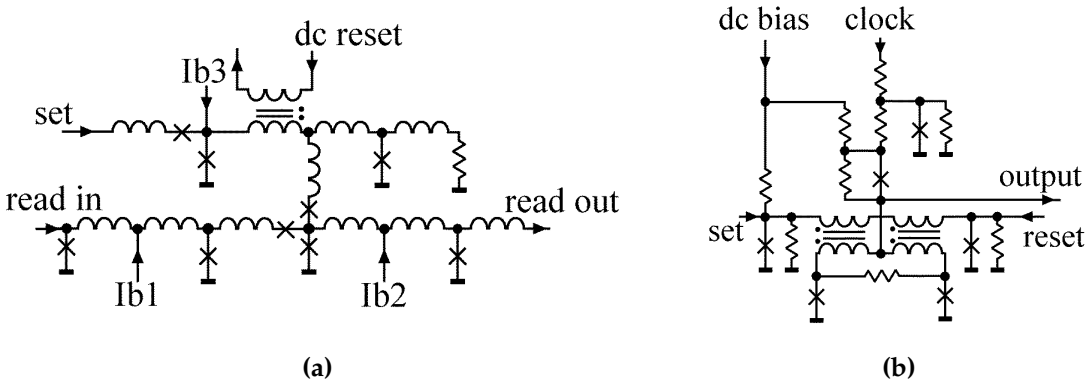


Figure 5.2: Simplified schematic circuit diagram for (**a**) a novel RSFQ DC-resettable latch, and (**b**) COSL set-reset flip-flop. Parasitics, damping resistors and input-output matching elements were omitted. From [71].

For the novel RSFQ DC-resettable latch the first functional circuit had a yield of 22.3%. The genetic algorithm eventually reached a yield of 97.7%. The original yield of the COSL set-reset flip-flop was calculated as 33.1%, which increased to 86.2% after optimization with the genetic algorithm.

5.3 Advanced circuit component extraction and yield analysis

Even though some progress was reported with regard to the extraction of circuit components from the actual circuit layout [65], the implementation was far from optimal. One of the restrictions was that the implementation was done in *HSPICE*, which did not have a unique model for the Josephson junction. Another complication was that the model could

not extract three-dimensional parasitics, such as the contribution of vias to inductance and resistance.

Due to the important role that inductance plays in the operation and reliability of COSL and RSFQ circuits, an important part of Coenrad Fourie's PhD research was directed at reliable three-dimensional extraction of inductance from circuit layouts [73]. In large circuits, inductance values were normally estimated by two-dimensional tools, such as *SLINE* [64], which rendered a per length inductance value. For corner segments, the inductance values were approximated by calculation of an effective length, as is shown in Figure 5.3, and then multiplying that with the per length inductance. This technique gives acceptable results for conductors on the same layers, but fail to predict the inductance of common structures such as vias, tees and Josephson junctions.

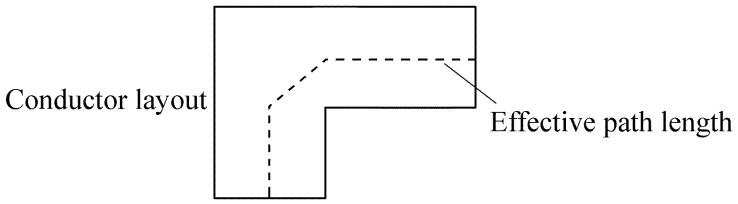
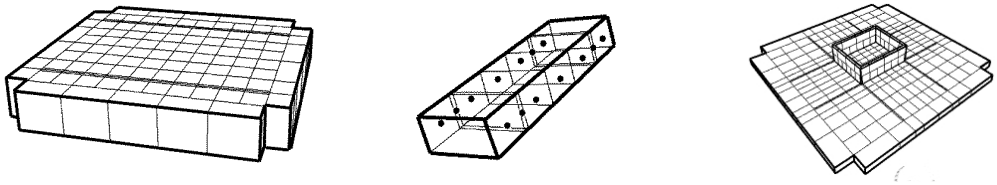


Figure 5.3: Effective path length for the two-dimensional approximation of the effect of a corner on the inductance of a thin film conductor. From [74].

To obtain accurate extracted inductance values of complex three-dimensional structures, a technique was developed to generate finely meshed three-dimensional models of complex structures [74] for input into a version of *FastHenry* that was adapted for superconductors [75]. *FastHenry* is an open source software package [64], and has the capability to calculate inductance from the actual layout of a structure.

Routines were developed that constructed segmented structures for common rectangular objects, such as lines, vias, uniform corner or tee-in pads, pads with nodes arranged for connection to vias, and connection strips. Examples of the most commonly used structures are shown in Figure 5.4.



(a) **(b)** **(c)**

Figure 5.4: Basic structures used to construct complex three-dimensional models are (**a**) the transmission line, (**b**) a connection strip, and (**c**) a via mounted on a pad. Dots on the connection strip show the location of nodes. From [74].

All the dimensional parameters of the basic building blocks were made variable, and any combination of the basic structures could be connected to form complex three-dimensional structures, with arbitrary dimensions. A library of more complex configurations was created and included a Josephson transmission line (JTL), an RFSQ pulse splitter, and several connected junctions with line crossings, layer changes, corners and tee-ins. The dimensions of a specific library component could be specified during the layout process, and tweaked if the extracted inductance values were not within the designed range.

Superconducting circuits are normally constructed above a ground plane. To preserve accuracy the ground plane segmentation need to be similar in size to the most critical conductors, which means that large parts of the ground plane, far from the conducting structures, waste segments and computing resources. In order to eliminate the computational inefficiency, the method of images was used to eliminate the ground plane [74]. It was also shown that the placement of the reflection plane had a significant influence on the accuracy of the extracted inductance values, especially for layers that were close to the ground plane [76]. The best results were obtained by placing the reflection plane at the effective penetration depth [77], given by

$$\lambda_{eff} = \lambda \coth\left(\frac{d}{\lambda}\right), \tag{5.3.1}$$

where λ is the London penetration depth of the superconducting film and d the thickness.

Although the method of images were used by default, the models could also be implemented with a ground plane when the effects of moats or large holes in the ground plane had to be considered.

All the models were developed for the 1 kA/cm^2 *HYPRES* process. As an example, the composition of a Josephson junction is shown in Figure 5.5.

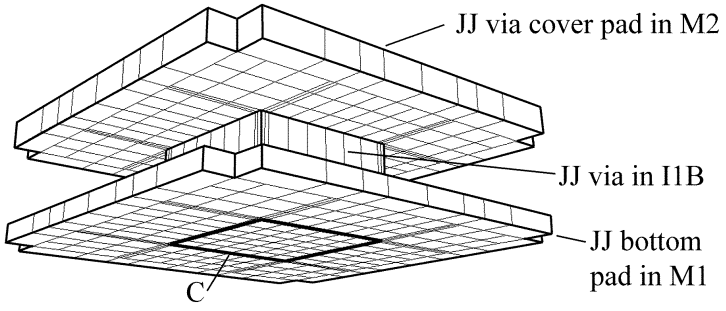


Figure 5.5: Composition of a Josephson junction. From [74].

A more problematic circuit, the RSFQ pulse splitter, was also analyzed. The circuit diagram and the segmented inductance calculation model are shown in Figure 5.6.

The design values for the inductors were L_1=1.16 pH and L_2=L_3=1.64 pH. The extracted inductance values were L_1=1.275 pH, L_2=1.667 pH and L_3=1.666 pH. It was thus clear that L_1 was actually 10% larger than the designed value, and that the inductor should be shortened

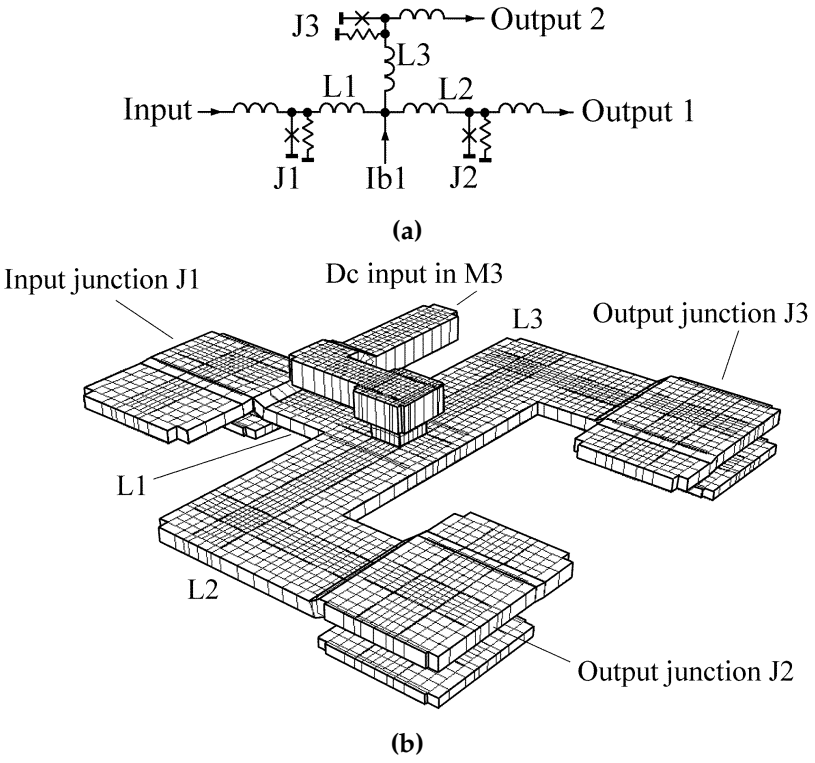


Figure 5.6: (**a**) RSFQ pulse splitter circuit diagram, and (**b**) the three-dimensional inductance calculation model. For clarity, vertical dimensions were doubled and the image was omitted. From [74].

in the layout. Another interesting observation was that, in the absence of the DC input, and L_2 and L_3, the extracted inductance L_1 was 1.361 pH, 6.8% higher than the value obtained with the full model.

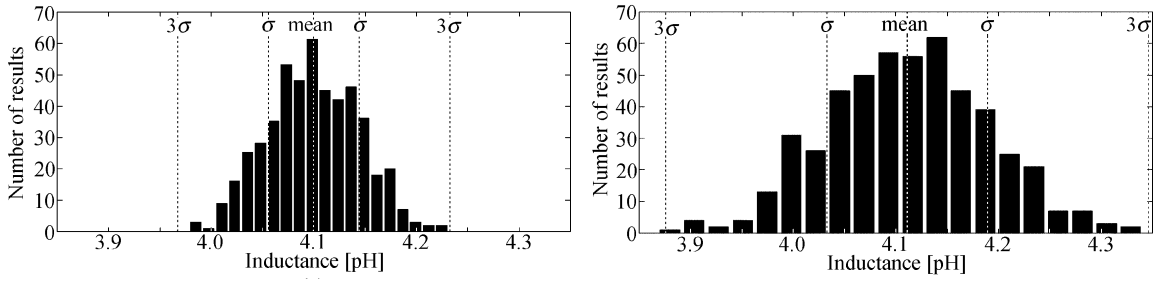
The development of the segmentation software [73, 74] was the first steps towards the birth of a powerful console application for the extraction of inductance from integrated circuits, which Coenrad Fourie appropriately named *InductEx*.

As was touched on previously, *InductEx* was designed to receive a layout of an integrated circuit from a standard GDSII file format, which was then segmentized and prepared for inductance extraction by *FastHenry*. The software package was later described in more detail [78].

The implementation of a layer information file feature in *InductEx* made it possible to define layer sequence, mask-to-wafer bias and process tolerances. A specific niobium integrated circuit process, such as the *HYPRES* 1 kA/cm^2 fabrication process, could thus be defined. This feature was based on previous work [65], but offered much more in terms of accuracy due to its inherent three-dimensional capabilities, and the elegant incorporation of mutual coupling between structures.

In Section 5.1 the two-dimensional inductance values were extracted by using the transmission line model of *HSPICE*, based on the published design rules of the *HYPRES* 1 kA/cm^2

fabrication process. The same procedure was implemented with *InductEx* for a conductor with a 4 μm width on the $M2$ layer, connected between two 250 μA Josephson junctions. The nominal inductance between the junctions was calculated as 4.1 pH. A histogram of the inductance distribution of 500 structures with only global variations (layer thickness and penetration depth) is shown in Figure 5.7(a). For this exercise the local variations (i.e. the width tolerances) were set to zero in the layer information file. In Figure 5.7(b) the inductance distribution is shown when all process tolerances were taken into account (global and local variations).



(a) **(b)**

Figure 5.7: Histogram of the inductance distribution of a line in $M2$ between two Josephson junctions, with (**a**) only global variations (layer thickness and penetration depth), and (**b**) when all process tolerances were taken into account (global and local variations). From [78].

From Figure 5.7 it is clear that the inductance variations due to process tolerances follow a Gaussian distribution. The 3σ limits are also indicated in the graphs.

Extensive analyses were also done for different line widths in the $M1$ and $M3$ layers. All lines were connected between two 250 μA Josephson junctions to create a realistic circuit structure. The global variations for every layer were calculated as the average over hundreds of randomly varied structures, and is shown in Table 5.1.

Table 5.1: Extracted global inductance variations for the 1 kA/cm^2 *HYPRES* process

Layer	Nominal inductance	σ_{global}
$M1$	3 pH	1.58%
$M2$	4 pH	1.2%
$M3$	5.5 pH	1.01%

The standard deviation of inductance was also calculated for all layers when all the process tolerances (σ_{all}) were incorporated. The local (on-chip) deviation (σ_{local}) was then calculated [79] as

$$\sigma_{local} = \sqrt{\sigma_{all}^2 - \sigma_{global}^2}. \tag{5.3.2}$$

The total and local inductance variations are shown in Table 5.2 for different line widths.

Table 5.2: Extracted total and local inductance variations for the 1 kA/cm^2 *HYPRES* process

Layer	Line width	σ_{all}	σ_{local}
*M*1	4 μm	2.26%	1.62%
*M*1	6 μm	1.93%	1.11%
*M*1	8 μm	1.69%	0.60%
*M*2	4 μm	1.91%	1.49%
*M*2	6 μm	1.63%	1.10%
*M*2	8 μm	1.38%	0.68%
*M*3	4 μm	1.52%	1.14%
*M*3	6 μm	1.41%	0.98%
*M*3	8 μm	1.34%	0.88%

It was shown by Jeffery *et al* [46] that moats in the ground plane was an effective method to reduce flux trapping in superconducting circuits. To determine whether moats in the ground plane would have a significant influence on inductance, a Josephson transmission line (JTL) between two 250 μA Josephson junctions was investigated for two cases, with and without moats in the ground plane [78]. For this the method of images could not be used. The ground plane was thus meshed to accommodate the moats as is shown in Figure 5.8.

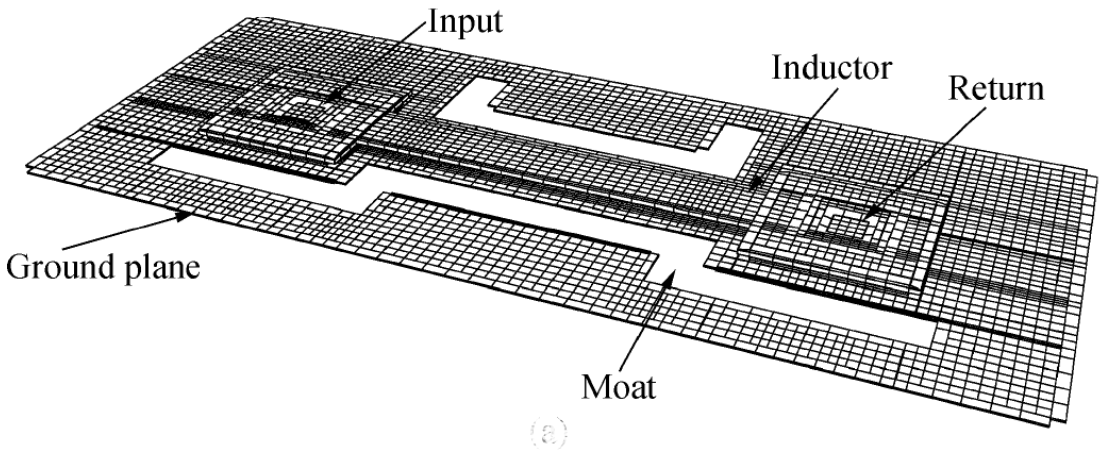


Figure 5.8: JTL with moats in ground plane. From [78].

The extracted value of the inductance with the moats in the ground plane was only 1.1% higher than the nominal value, proving that moat structures would, in general, not have a significant influence on the designed values of inductance. However, it was found that careless layout practices, such as letting a moat pass underneath a transmission line, could dramatically influence the inductance. In our case the inductance was increased by 160%.

A comprehensive procedure for Monte Carlo based yield prediction, based on the tolerances of a specific fabrication process, was developed [79]. The procedure was based on previous research by the group [65, 78].

In order to test the proposed procedure, the calculated Monte Carlo yield for a new Non-Destructive Readout Register (NDRO) [80] was compared to margin analyses [60] for the same structure. The margin and yield analyses curves are shown in Figure 5.9.

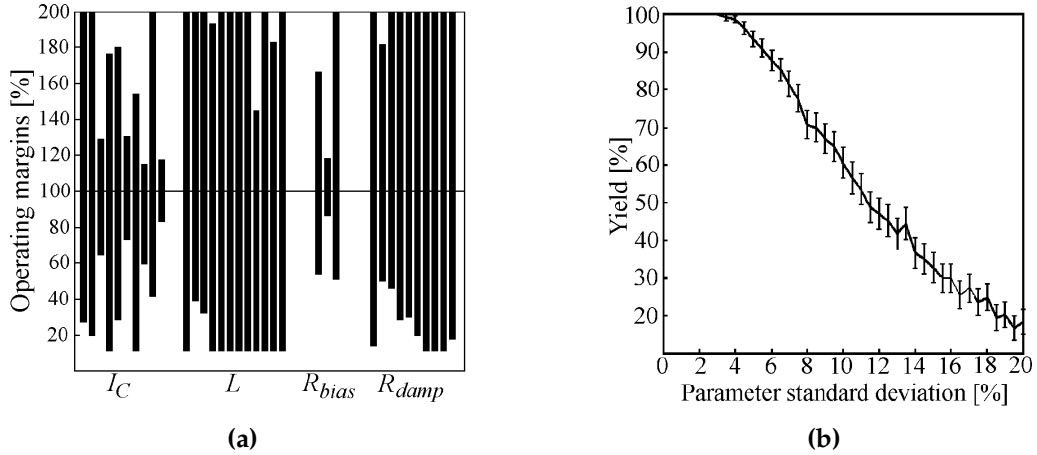


Figure 5.9: (**a**) Operating margins of NDRO for critical current (I_c), inductance (L), bias resistance (R_{bias}) and damping resistance (R_{damp}), and (**b**) yield curve for the same NDRO. From [79].

The critical margins were calculated as +15% and -17.5% for critical current, +50% and -60% for inductance, and +16.8% and -15.5% for bias current, which suggested reasonable operating limits, although it did not give a quantitative indication whether the circuit would work for random variations of the circuit parameters. On the other hand, looking at the yield curve (Figure 5.9(b)) it is clear that the yield started dropping significantly for generic tolerances (σ) larger than 3.5%.

The yield was also calculated with layout extracted parameter values and a value of $99.97^{+0.03}_{-0.07}$ % was achieved, which indicated that one circuit in every 3500 was likely to fail.

5.4 Building blocks for superconducting circuits

5.4.1 COSL Set-Reset Flip-Flop and SFQ-to-Voltage State Interface

One of the drawbacks of the COSL family was the absence of a storage element. A proposed storage element, a Set-Reset (SR) Flip-Flop, is shown in Figure 5.10 [81]. The circuit was optimized with genetic algorithms [71, 72] and the inductance values and coupling factors were extracted using *InductEx* [74].

The element was based on the basic COSL OR-gate, but the input clock was removed, thus preventing the input circuit (a one-junction SQUID in the basic OR-gate) from resetting

during the negative portion of the clock cycle. Instead, a DC offset was used as input bias. The one-junction SQUID of the basic OR-gate was also replaced by a two-junction SQUID, which allowed for a Set and a Reset input. With the DC bias, an input pulse at the Set or Reset terminal could thus switch the output two-junction SQUID.

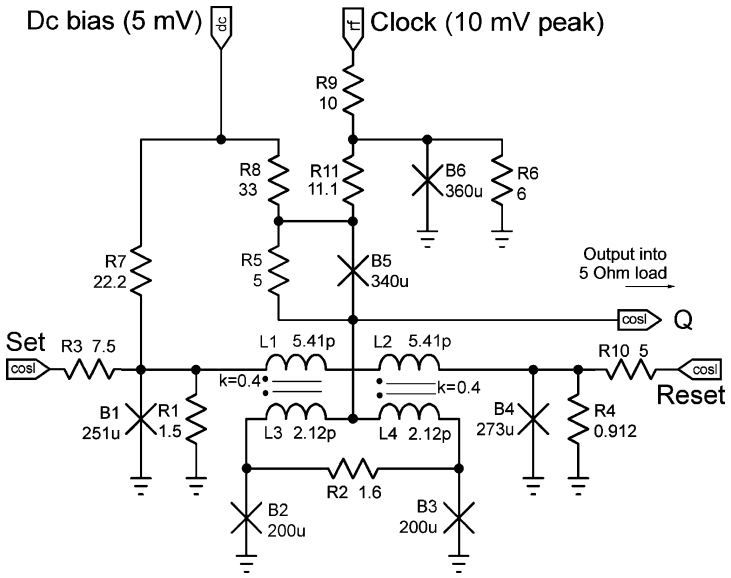


Figure 5.10: Circuit diagram of proposed COSL SR Flip-Flop. From [81].

The simulation results of the COSL SR Flip-Flop is shown in Figure 5.11, confirming the correct operation of the circuit at a clock frequency of 10 GHz.

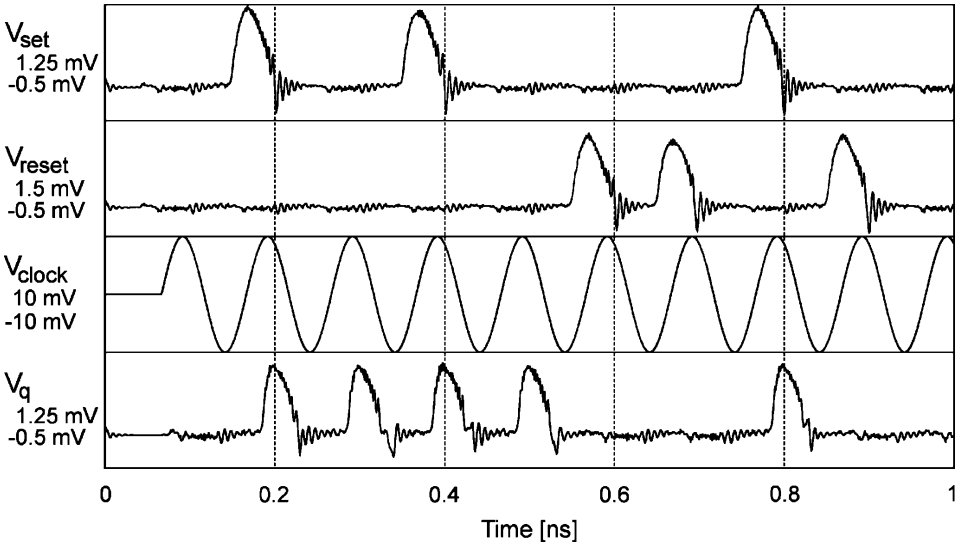


Figure 5.11: Simulation results of the COSL SR Flip-Flop at a clock frequency of 10 GHz. From [81].

Due to the absence of an input clock, the SR Flip-Flop is in essence asynchronous. This means that neither Set or Reset need to be in phase with the clock of the circuit.

An additional bonus is that, when Set and Reset are simultaneously high, the circuit will operate as a Toggle (T) Flip-Flop. The simulated results of the T Flip-Flop is shown in Figure 5.12 at a clock frequency of 10 GHz, confirming the correct operation of the circuit.

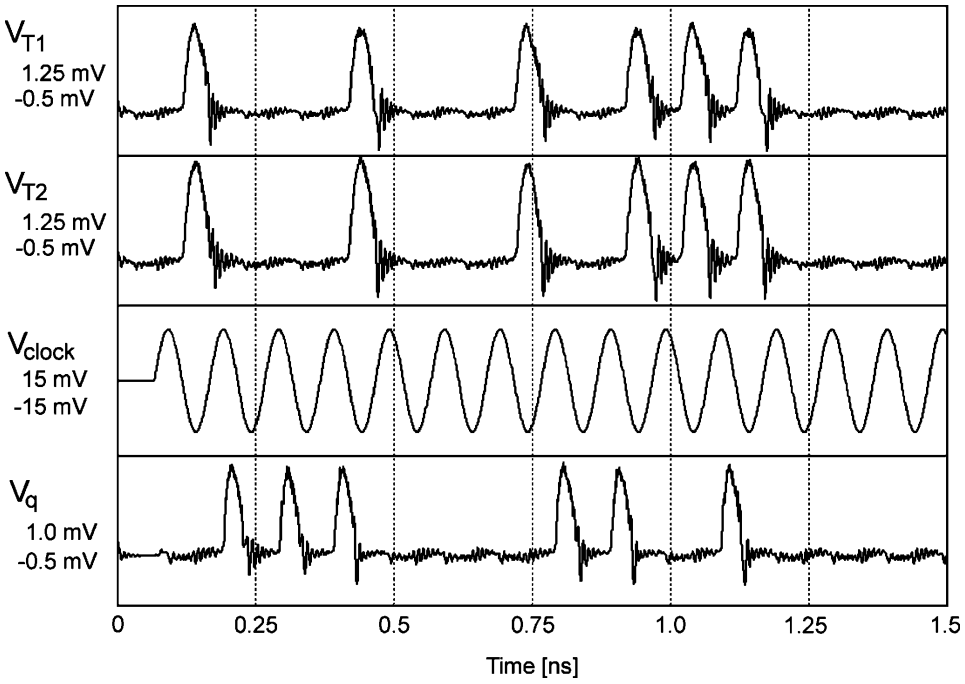


Figure 5.12: Simulation results of the COSL T Flip-Flop at a clock frequency of 10 GHz. From [81].

The asynchronous nature of the COSL SR Flip-Flop also opened up another possibility, to serve as a simple RSFQ to room temperature interface. Such a circuit would be able to capture an asynchronous RSFQ pulse, and convert it to a synchronized voltage-state pulse for off-chip room temperature applications.

The circuit diagram of the proposed RSFQ-to-COSL converter is shown in Figure 5.13 [81]. It can be seen that the input two-junction SQUID of the COSL SR Flip-Flop was replaced by a standard Destructive Readout (DRO), thus integrating the DRO into a COSL gate.

The simulated response of the RSFQ-to-COSL converter is shown in Figure 5.14. The Set input was driven by a Josephson transmission line and the SFQ pulses were staggered to demonstrate the asynchronous capabilities of the circuit. The output at Q was connected to the standard 5 Ω load of a COSL gate.

From Figure 5.14 it can be seen how the asynchronous SFQ pulse sets the current in the DRO (I_{L3}), which switches the output two-junction SQUID at the ensuing clock cycle.

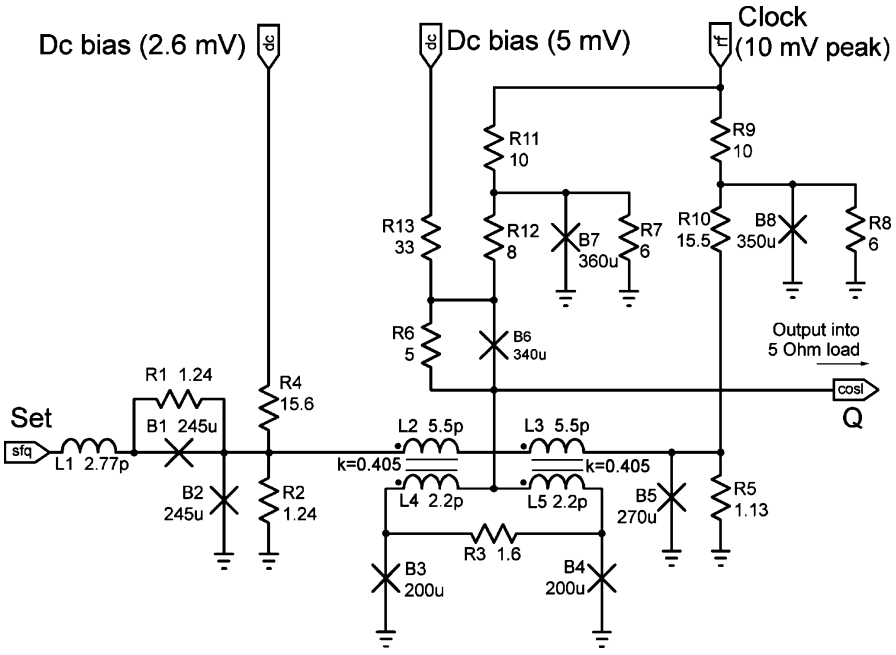


Figure 5.13: Circuit diagram of RSFQ-to-COSL converter at a clock frequency of 10 GHz. From [81].

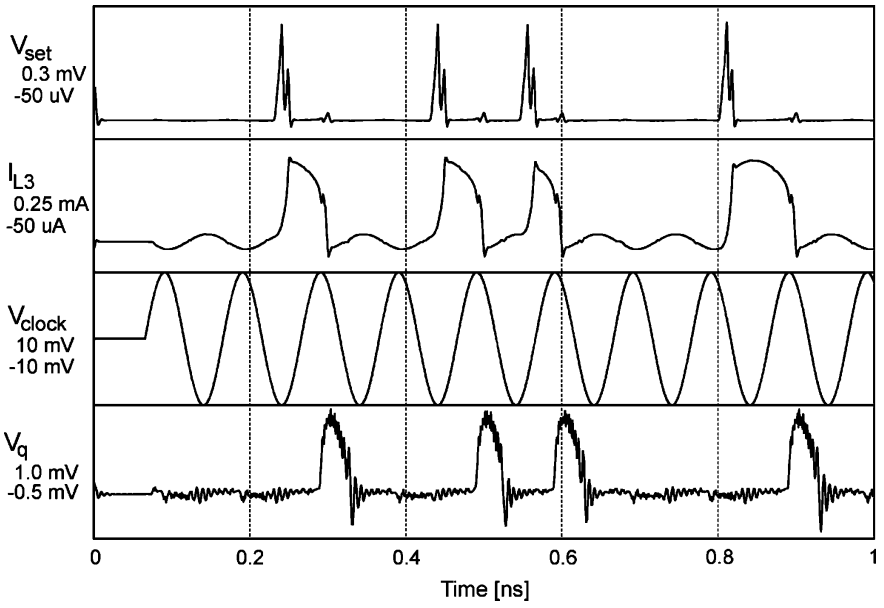


Figure 5.14: Simulation results of the RSFQ-to-COSL converter at a clock frequency of 10 GHz. From [81].

5.4.2 An RSFQ DC Resettable Latch for memory and reprogrammable circuits

In reprogrammable logic circuits it is a requirement that every latch should be addressed individually. However, circuit overhead would be reduced significantly if all latches could be reset with a single reset action.

Such a circuit, an RSFQ DC Resettable Latch (DCRL), was proposed [80], where a single

DC current could be used to reset all latches simultaneously. The circuit diagram of the DCRL is shown in Figure 5.15. The circuit was optimized by a genetic algorithm [71, 72], except for L_{13} and the coupling factor between L_{13} and L_2, which were extracted from the final *HYPRES* 1 kA/cm^2 process circuit layout, using *InductEx* [74]. The circuit yield was calculated as 100% when layout extracted parameter tolerances were used.

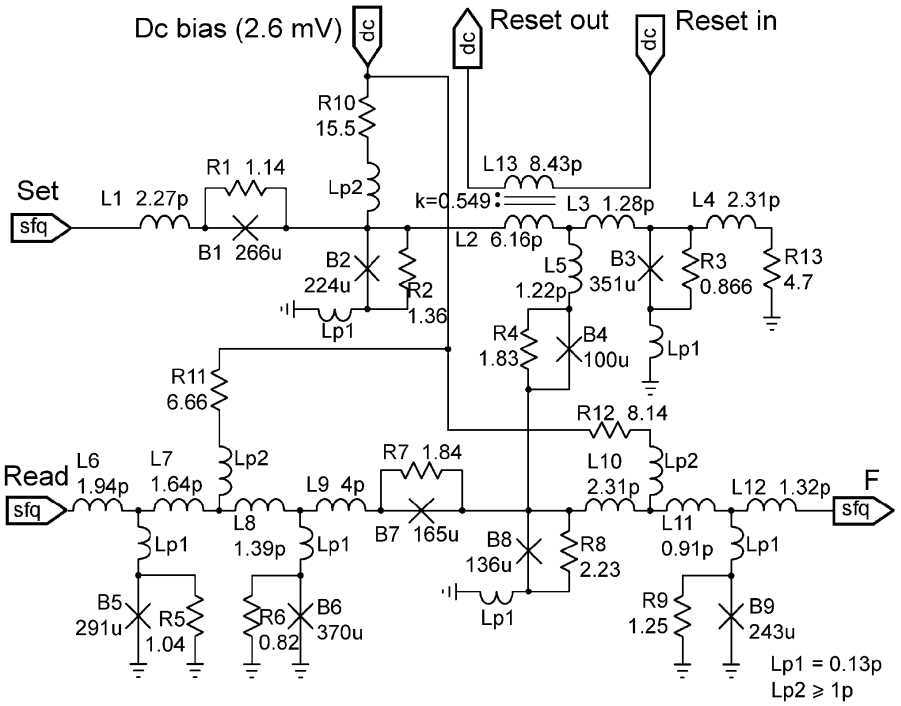


Figure 5.15: Circuit diagram of proposed DC Resettable Latch. From [80].

The correct operation of the DCRL was verified by the simulation results shown in Figure 5.16. In the absence of a *Set* pulse, a *Read* pulse did not generate an output pulse at *F*. However, when a *Set* pulse was present, a *Read* pulse did indeed generate an output pulse at *F*. A DC current of 720 μA, with the right polarity, was used to reset the DCRL to its original state, as can be seen from the state of the currents through L_2 and L_5.

It was also shown that the DCRL could be turned into an SFQ Resettable Non-Destructive Read-Out register (NDRO) when the DC reset line was removed, and the set-reset stage altered so that B_3 (in Figure 5.15) can accept SFQ reset pulses [80]. A simplified circuit diagram of the NDRO is shown in Figure 5.17. The theoretical circuit yield of the NDRO approached 100% when layout extracted parameter tolerances were used.

The functionality of the NDRO was confirmed by simulation and the results are shown in Figure 5.18. It was evident that, for the *Set* condition, a logical one was observed at the output for every *Read* pulse, and *vice versa* for the *Reset* condition.

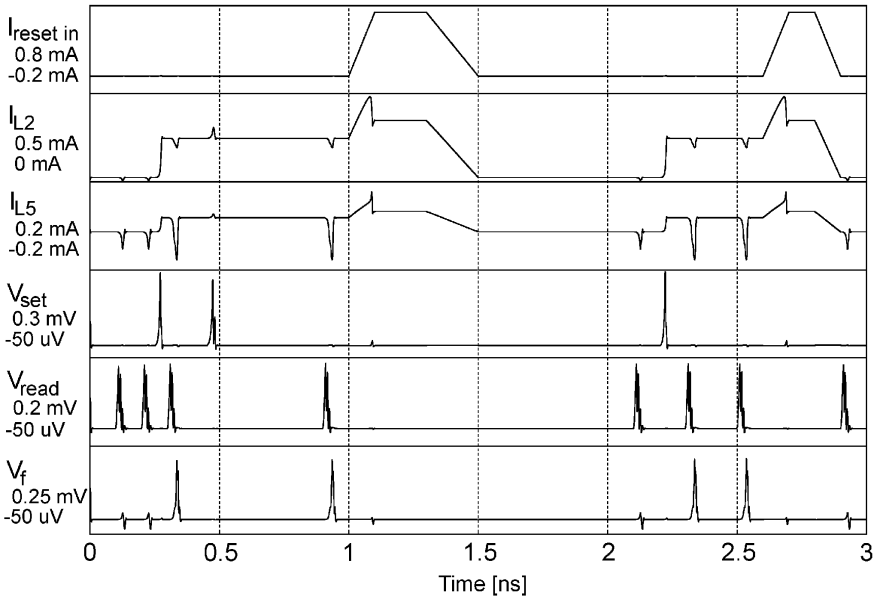


Figure 5.16: Simulation results of the DCRL. Various set, reset and read signals are applied, and the correct response of the latch is evident from the currents through L_2 and L_5, and the output signal at F. From [80].

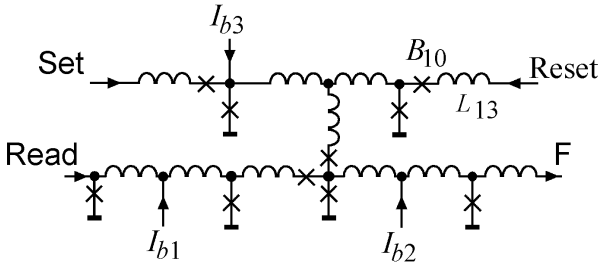


Figure 5.17: Simplified circuit diagram of the NDRO. From [80].

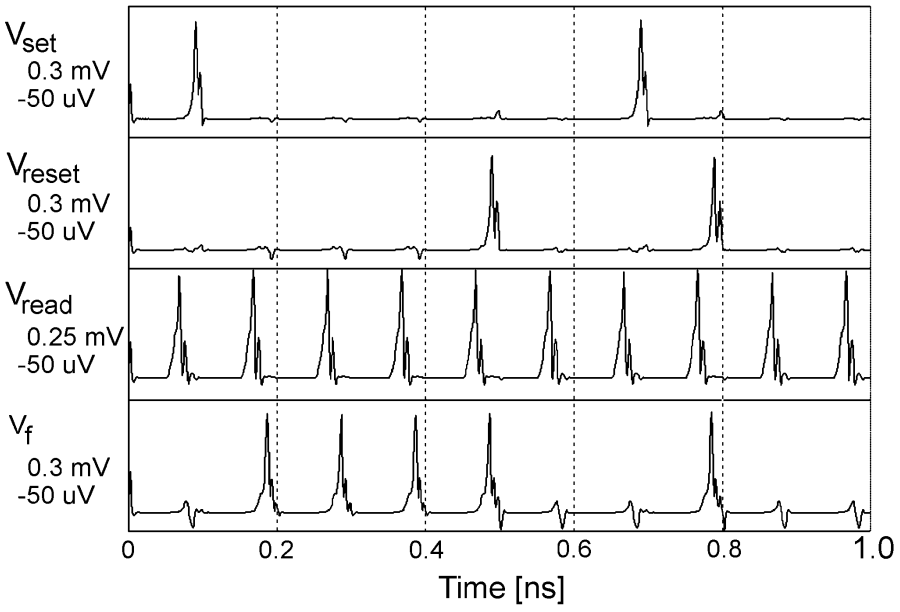


Figure 5.18: Simulation results of the NDRO, confirming correct operation. From [80].

5.4.3 Superconducting Programmable Gate Array elements

A generic Field Programmable Gate Array (FPGA), as is shown in Figure 5.19, consists of logic blocks that are surrounded by routing channels. The programmable elements in the routing channels control crosspoint switches, that can connect different routing channels, and inline switches, that can open or close paths in a routing channel.

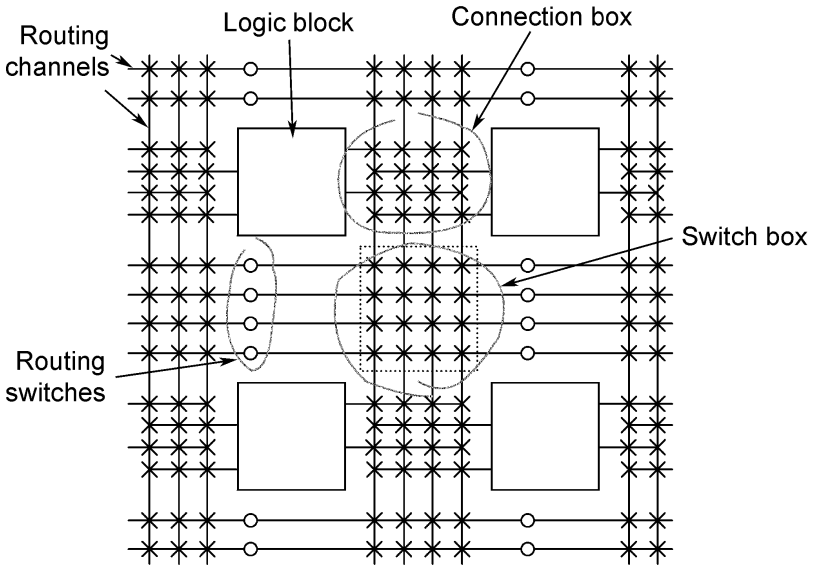


Figure 5.19: Schematic of a generic FPGA showing logic blocks surrounded by routing channels. The circles (○) represent inline switches and the crosses (×) crosspoint switches. From [80].

The DCRL was designed as the basic building block for a Superconducting Programmable Gate Array (SPGA) [73, 80].

An inline switch was implemented by a single DCRL that blocked the *Read* data when in the *Unset* condition and passed the *Read* data to the output in the *Set* condition. The crosspoint switch implementation is shown in Figure 5.20 and is more complex than the inline switch. A Hybrid Unlatching Flip-Flop Logic Element (HUFFLE) was used to generate the bipolar *Write select* current [82, 83]. The simulated circuit yield of the circuit approached 100% when layout extracted parameter tolerances were used.

The simulated results of the crosspoint switch is shown in Figure 5.21. As can be seen, data that enters on any track will always leave on the same track, but will only be switched to the other track when the crosspoint switch is set.

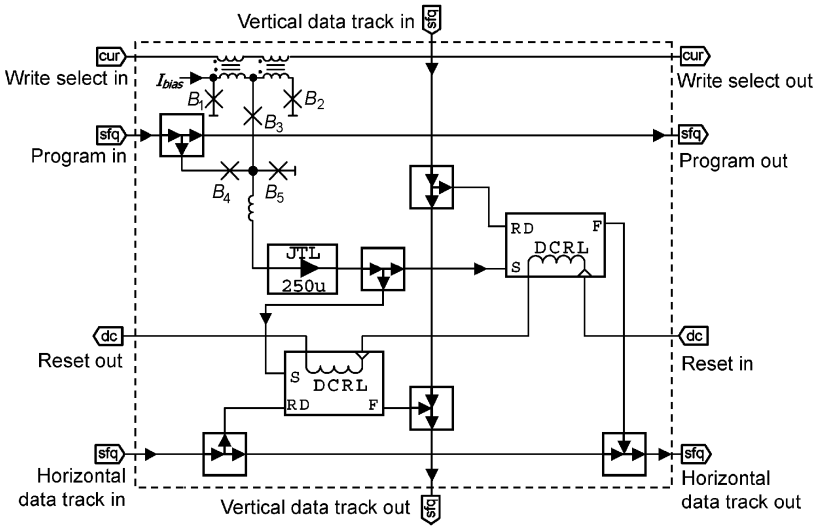


Figure 5.20: Schematic diagram of a crosspoint switch implemented with two DCRLs. The switch is addressed for programming by an SFQ as well as a bipolar current line. The symbols with three arrows represent SFQ pulse splitters and pulse mergers. From [80].

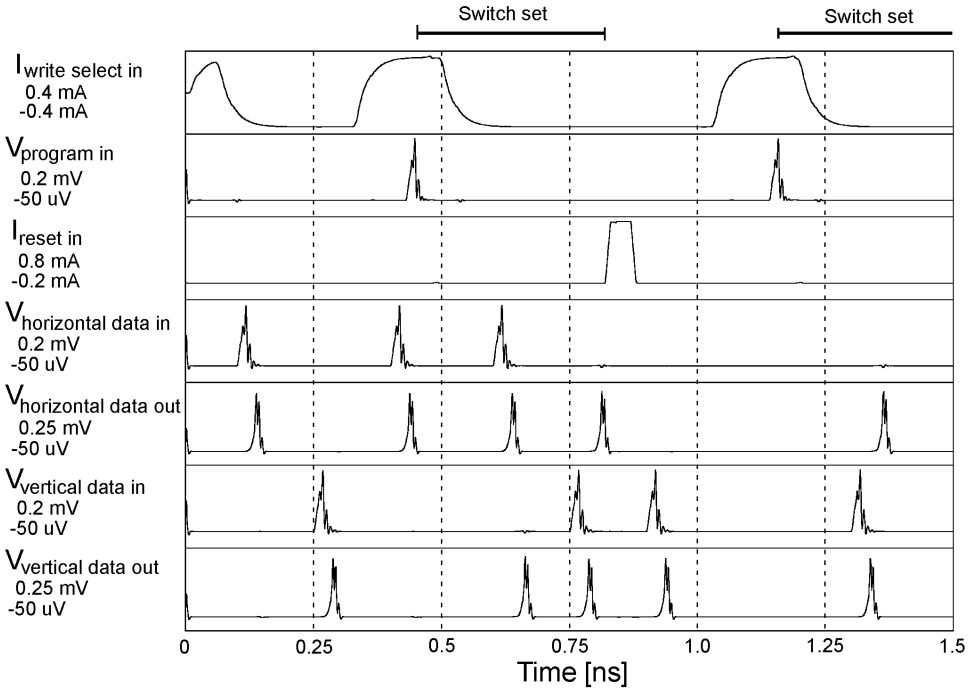


Figure 5.21: Simulation results of the crosspoint switch. Note that data entering on any track always leave on the same track, but only crosses to the other track when the crosspoint switch is set. From [80].

5.5 Computer Aided Design tools

5.5.1 A technology portable logic cell library for RSFQ

Fabrication processes are constantly being improved on. Although that is normally beneficial for circuit performance, it requires that all logic gates and circuits have to be ported to the new process, which normally entails circuit redesign, new layouts and component extraction. These processes are extremely time consuming, primarily due to the lack of automated tools. The availability of portable cell libraries would thus go a long way to streamline the porting process and also minimize human error. It would also enable designers to easily switch to different fabrication foundries with different design rules.

A procedure to define such a portable cell library was described [84]. In essence a portable cell is a generic logic cell that can be automatically adapted to a new fabrication technology.

In order to make the fabrication process generic, a standard format is required to specify the design rules. The use of a standard Extensible Markup Language (XML) file was proposed for this purpose. A portion of such a file is shown in Figure 5.22 for the 1 kA/cm^2 *HYPRES* fabrication process.

```
<PROCESS>
 <property name="hyp3000" />
 <property revision="19" />
 <property layercount="11" />
 <LAYER>
  <property name="M0" />
  <property description="Defines holes in ground plane" />
  <property polarity="dark" />
  <property level="0" />
  <property gdslayer"30" />
<property critcur="5mA/um" />
<property bias="0.25u" biasvar="0.25um" />
<property thickness="100nm" thickvar="10nm" />
 </LAYER>
 <LAYER>
  <property name="I0" />
 </LAYER>
<\PROCESS>
```

Figure 5.22: A portion of the XML description file for the 1kA/cm^2 *HYPRES* fabrication process. From [84].

A fully specified portable cell should contain the following information:

- Circuit – All circuit components specified in a technology independent format.
- Layout – The layout specified in a technology independent symbolic format.
- Symbol – The cell view that will be used for large designs.

- Functionality – Behavioral description of the cell.

An RSFQ Destructive Readout Register (DRO) [73] was used as an example to describe the portable cell specification procedure. The circuit is shown in Figure 5.23. A SPICE description of the circuit was the obvious technology independent way to capture the circuit.

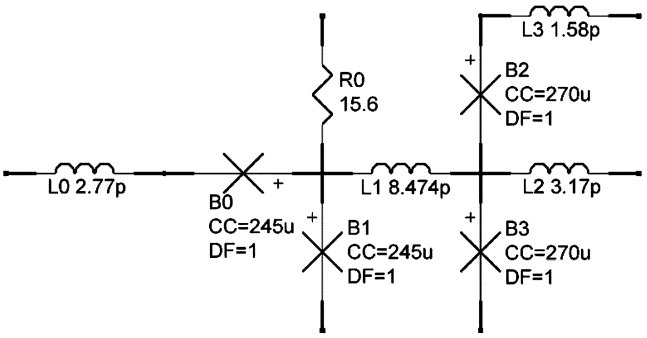
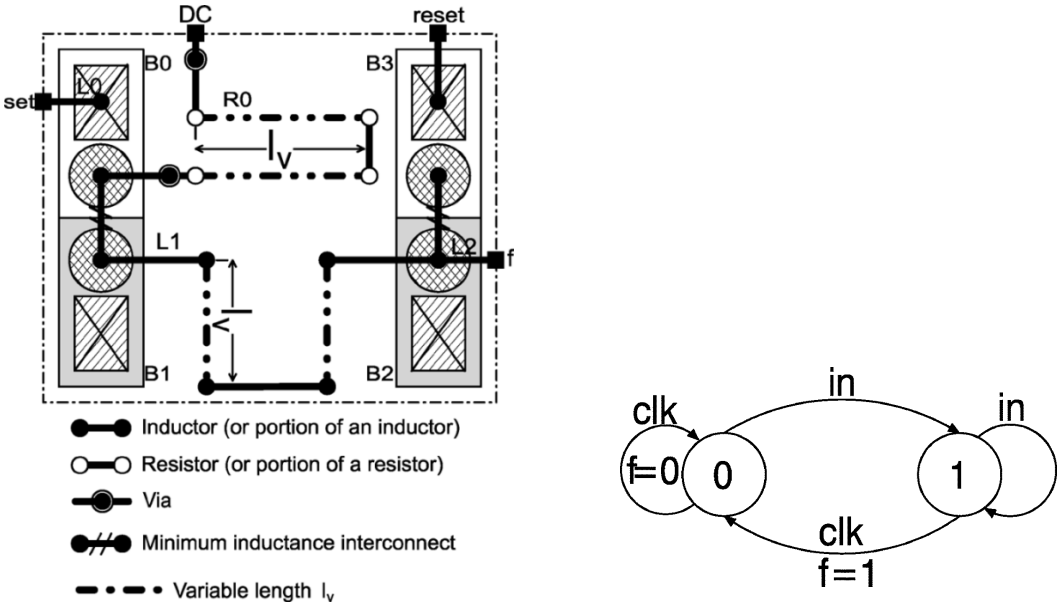


Figure 5.23: Circuit schematic of the RSFQ DRO. From [84].

A compilable layout of the portable cell was captured using an independent symbolic layout description, as is shown in Figure 5.24(a). For a specified fabrication technology the symbolic layout could then be converted into a real layout. The functionality of the portable cell could be described by using a Hardware Description Language (HDL) or a Moore diagram. The Moore diagram of the RSFQ DRO is shown in Figure 5.24(b).



(a) **(b)**

Figure 5.24: (**a**) Symbolic layout of the RSFQ DRO, and (**b**) the Moore diagram of the RSFQ DRO. From [84].

After compilation, a fully specified portable cell should contain the following information:

- Circuit – All circuit components, including parasitic components, their extracted values and junction models should be specified.
- Layout – The physical layout that complies with the design rules of the specific fabrication process.
- Symbol – The cell view that will be used for large designs.
- Functionality – The functional and timing characteristics of the cell.

The layout of circuit components, such as Josephson junctions, can be defined quite rigidly and it is thus relatively easy to convert a captured layout to a real layout. However, it is not always possible to convert a resistor or inductor with specified component values to fit into a predefined space on a layout. For this reason bendable structures were defined, where the designer could define bending points and bending directions. The symbolic versus real layouts of such bending structures are shown in Figure 5.25, for inductors and resistors, respectively.

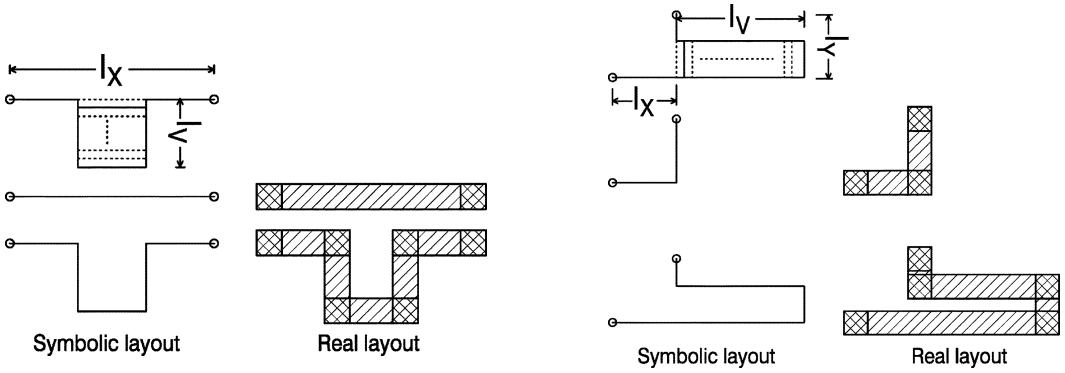


Figure 5.25: Symbolic versus real layout for (**a**) a bendable inductor, and (**b**) a bendable resistor. From [84].

A length in the bendable structure, denoted by l_v, can be changed to obtain a suitable effective length for the physical structure. The effective length (l_{eff}) was approximated [78, 79] as

$$l_{eff} \approx \begin{cases} l_x + 2l_v - 1.98w & \text{for } l_v \geq w \\ l_x & \text{for } l_v = 0 \end{cases} \tag{5.5.1}$$

for inductors, and as

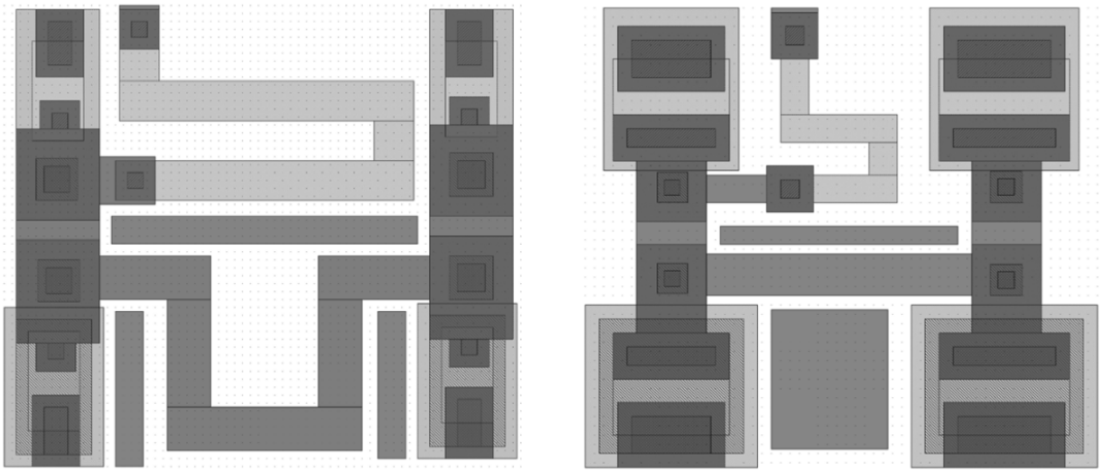
$$l_{eff} \approx \begin{cases} l_x + l_y + 2l_v - 0.879w & \text{for } l_v \geq w \\ l_x + l_y - 0.293w & \text{for } l_v = 0 \end{cases} \tag{5.5.2}$$

for resistors, where w is the width of the inductor or resistor, respectively.

Suitable values for w and l_v can be found from (5.5.1) and (5.5.2) that will satisfy the required component values. Once these values were found, exact and parasitic values could be extracted using *InductEx* [74].

The functional compilation comprised the iterative optimization of the cell for yield and also timing characteristics. This was done by iteratively changing the layout of the cell, re-extraction of the of the circuit structure, verification of the functional description and analysis of the yield and timing characteristics.

To illustrate the usefulness of the proposed procedure, the portable cell description of the RSFQ DRO was compiled for two different fabrication processes, the *HYPRES* 1 kA/cm^2 and the 4.5k A/cm^2 process, respectively. The real layouts for the two processes are shown in Figure 5.26.



(a) **(b)**

Figure 5.26: The real layout of the RSFQ DRO (**a**) for the 1 kA/cm^2 *HYPRES* process, and (**b**) the 4.5 kA/cm^2 *HYPRES* process. From [84].

5.5.2 The RSFQ-Asynchronous Timing design methodology

Asynchronous timing plays an important role in the design of superfast superconducting digital electronic circuits. However, the absence of design automation tools severely hampers progress made in this field. That can largely be attributed to the fact that super- and semiconductor technologies are substantially different in nature, making it difficult to make use of existing semiconductor CAD tools.

With that in mind, the RSFQ-Asynchronous Timing (RSFQ-AT) timing scheme was proposed [85]. Using the design methodology made it possible to make use of existing semiconductor based CAD tools.

In essence the RSFQ-AT scheme is a combination of the straight-line clock-follow-data and dual-rail (data driven) clocking schemes [86]. In this scheme the clock signals are propagated through the data path at maximum speed, triggering an event when the end of the data path was reached. In doing so, it is known that the circuit is ready to perform more work.

The basic implementation of an RSFQ-AT cell is shown in Figure 5.27. The pulse splitter provides the clock distribution, while the clocking logic is provided by the timing element.

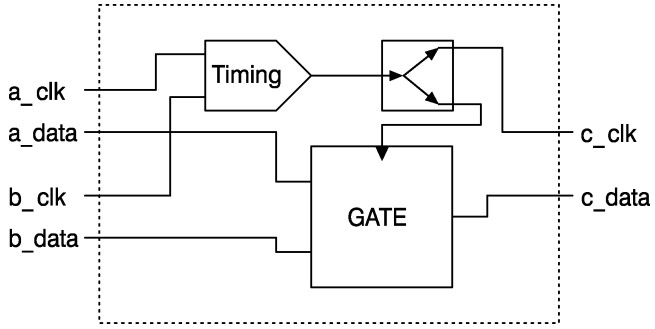


Figure 5.27: Basic implementation of an RSFQ-AT cell. From [85].

In order to test the viability of the RSFQ-AT clocking scheme, a 4-bit RSFQ-AT multiplier, amongst others, was implemented and compared to the results obtained by a different research group [87]. The results of the two implementations of the 4-bit multiplier are shown in Table 5.3 [85]. In the table t_c is the time required for the circuit to compute an answer, which is the time between the last input clock and the output clock ($t_c = t_{clko} - t_{clki}$), and f_{max} is the maximum simulated clock frequency.

Table 5.3: Comparison of 4-bit multiplier implementations

	RSFQ multiplier	RSFQ-AT multiplier
JJ count	±1100	±1300
t_c	>500 ps	±221 ps
f_{max}	<29 GHz	>29 GHz

The results showed that the RSFQ-AT 4-bit multiplier required less than 20% more junctions than the standard version, but that the more elegant clocking scheme led to a more than twofold increase in execution speed. In addition, the RSFQ-AT implementation was developed by using standard semiconductor design methodologies, which markedly reduced development time.

In order to verify the application of the RSFQ-AT design approach for more complex circuits, an asynchronous 4-bit RISC microprocessor with Harvard architecture was designed [88].

To provide basic functionality the microprocessor operation set included Load, Store, Add, Subtract, Jump, Conditional jump, AND, OR, XOR, Push, Pop and Stop. The system diagram of the final design for the microprocessor is shown in Figure 5.28.

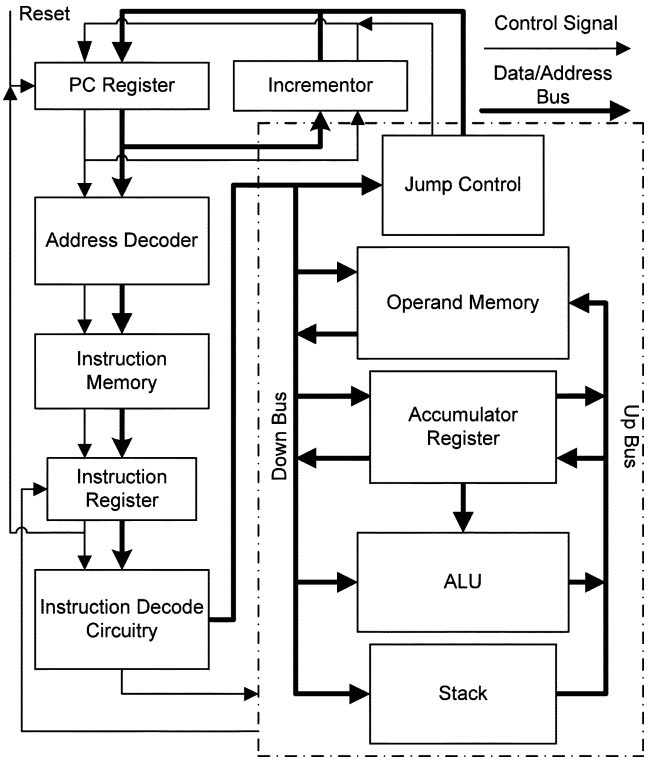


Figure 5.28: System diagram of the final microprocessor design. From [88].

The microprocessor implementation was not optimized for speed or Josephson junction count, and consisted of approximately 5300 junctions. The logic functioning of the circuit was verified by *Verilog* simulations. A summary of instruction operation times for selected instructions is listed in Table 5.4.

Table 5.4: Operation times of selected instructions

Instruction	Address mode	Operation time
LOAD	Immediate	370 ps
LOAD	Direct	605 ps
STORE	–	438 ps
ADD/SUB	Immediate	890 ps
OR	Direct	722 ps
OR	Immediate	808 ps
PUSH	–	476 ps
POP	–	419 ps

The logic implementation of the 4-bit microprocessor, using the RSFQ-AT design methodology, demonstrated that it was possible to utilize existing semiconductor architectures and tools to implement complex RSFQ circuits.

5.6 *NioCAD*

The research that was done on yield prediction, circuit optimization, layout-based circuit component extraction and building blocks for programmable circuits led to a realization that we may well be able to combine the diverse set of tools into a Computer Aided Design (CAD) suite of tools for superconducting circuit layout. The idea was based on the fact that, unlike the semiconductor industry, the layout of superconducting circuits was done by hand, with the help of a range of non-integrated software tools.

Myself, Coenrad Fourie (now a colleague) and a postgraduate student, Retief Gerber, shown in Figure 5.29(a), decided to try to raise industry funding for the development of a fully integrated professional CAD suite. We were fortunate to get a R8.1 million grant from the SA Government through the *Innovation Fund*, which gave us 2½ years to develop the tools. An initial team of 5 engineers and computer scientists, shown in Figure 5.29(b), started with the software development in February 2007.

(a)

(b)

Figure 5.29: (**a**)The founding members of *NioCAD*: Coenrad Fourie (left), myself (middle) and Retief Gerber (right). (**b**) The initial *NioCAD* development team: Craig Oliver (left), Dirk Bull, Jan Pool, Henk Marais and Tjaart van der Walt (right).

A further R12.5 million was obtained from the *Industrial Development Corporation*, making it possible to form an independent spinoff company, *NioCAD*, in September 2009, with the three founder members and Stellenbosch University as partial equity holders.

The basic concept was to develop a superconductor CAD package that would provide a complete and integrated solution for the development of superconducting circuits, including the following functionality:

- *Circuit capture* – Drawing circuit elements using a schematic editor and/or a text editor;
- *Circuit simulation* – A SPICE simulator to verify circuit operation;

- *Mask capture* – A graphics editor to define layout structures;
- *Component extraction* – The 3D extraction of components from the circuit layout, using tools such as *InductEx*;
- *Circuit optimization* – A process of constantly changing circuit component values, simulating and evaluating the circuit in order to, for example, obtain better yield;
- *Logic cell characterization* - The characterization of a subcircuit in order to create a logical model that can be used in larger scale designs and logic simulations.

A block diagram of the envisaged *NioCAD* system is shown in Figure 5.30 [89].

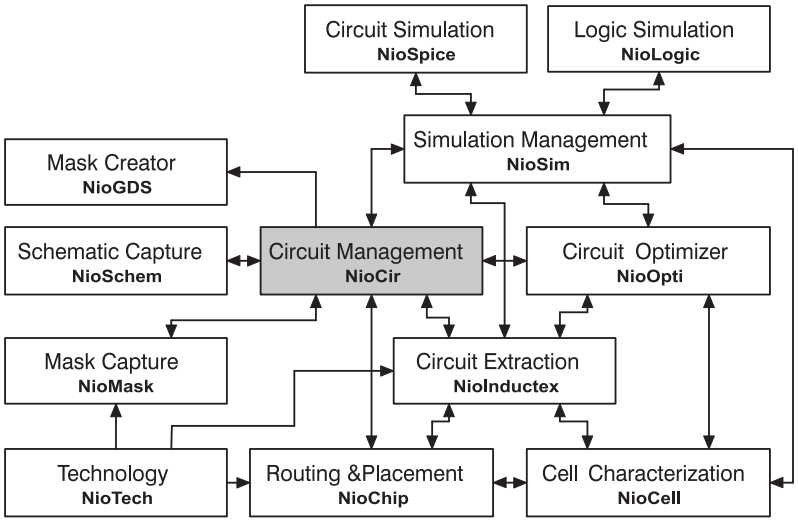


Figure 5.30: Block diagram of the *NioCAD* system. From [89].

The layout and physical models of components were tightly linked in the software, so that a change in the one would be carry over over the the other. As an example, the linkage between the physical and layout model of an inductor is shown in Figure 5.31.

The *NioCAD* system was launched as the *NioPulse* suite, and a screenshot of the Graphical User Interface (GUI) of the circuit capture component is shown in Figure 5.32 while the circuit parameters of a selected Josephson junction is being defined.

The software was developed in consultation with the major role players in Europe, Japan and the USA (specifically the fabrication company *HYPRES*), in order to incorporate the tools and the look-and-feel that designers are used to. Version 2 of the *NioPulse* software suite was released in 2012.

NioCAD closed its doors towards the end of 2012, mainly due to internal strife and mistrust between the funders. Fortunately the intellectual property reverted back to Stellenbosch University. Coenrad Fourie subsequently developed the 3D circuit extraction software *InductEx* up to the point where it is probably the benchmark in the superconducting research arena.

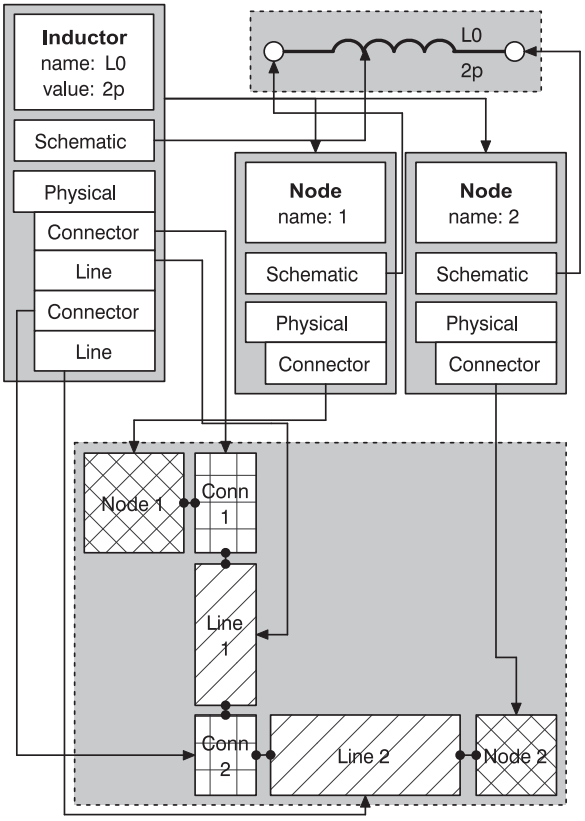


Figure 5.31: The linkage between the physical and layout model of an inductor as implemented in the *NioCAD* system. From [89].

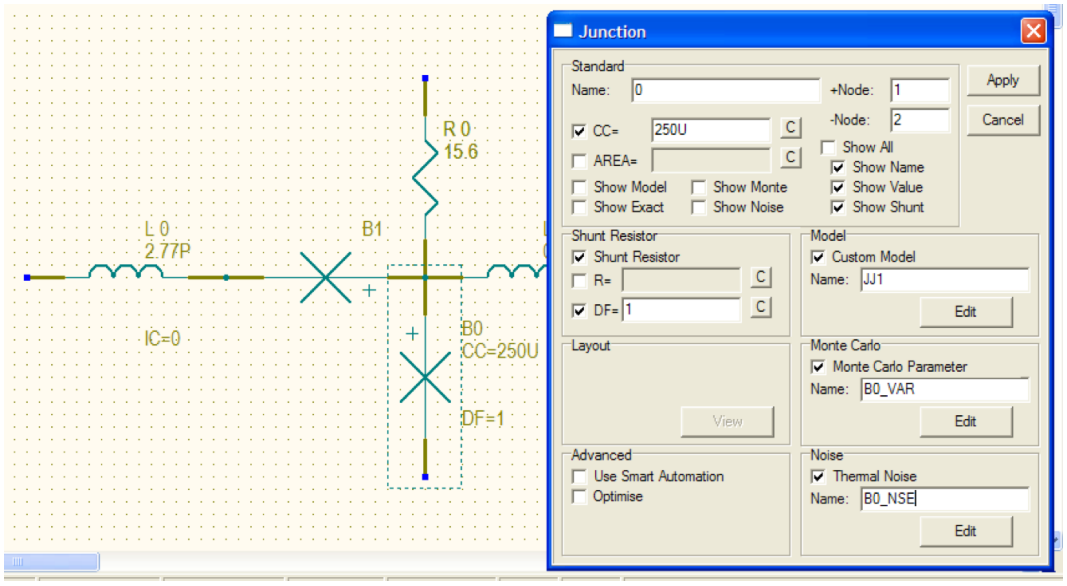


Figure 5.32: Screenshot of the GUI of the circuit capture component of the *NioPulse* suite while the circuit parameters of a selected Josephson junction is being defined.

5.7 Summary

In this chapter the post-Berkeley research activities in low-T_c superconducting circuits at Stellenbosch University was described.

The contributions included the work on yield prediction of circuits based on the layout of circuits [65], circuit optimization by using genetic algorithms [71], advanced techniques for accurate 3D circuit component extraction and yield prediction [73, 74, 78, 79], novel superconducting circuit building blocks [80, 81] and various CAD tools [84, 85, 88].

These contributions naturally led to the establishment of the spinoff company *NioCAD* and the development of the *NioPulse* software suite [89].

During this exciting period I was blessed to work with remarkable students, such as Coenrad Fourie and Retief Gerber. My journey with Coenrad started with the supervision of his undergraduate final year project, continued as supervisor for both his Master's and PhD studies, and is still continuing as a colleague. Retief opened my eyes with his intuitive gut feeling for software architecture.

Chapter 6

High-temperature superconductor device fabrication research at Stellenbosch

During the years we have been able to establish a reasonably well-equipped fabrication facility in the superconductivity laboratory, which included basic photolithography down to about 20 μm line-widths, thin film deposition capabilities (pulsed laser deposition, sputtering and thermal evaporation), wet- and dry etching capabilities, and also advanced inspection tools, such as a desktop SEM, an AFM and STM, and also optical microscopes.

Most of the existing fabrication equipment had to be modified to be able to do what was required, and some had to be designed and built from scratch, such as the argon ion-mill.

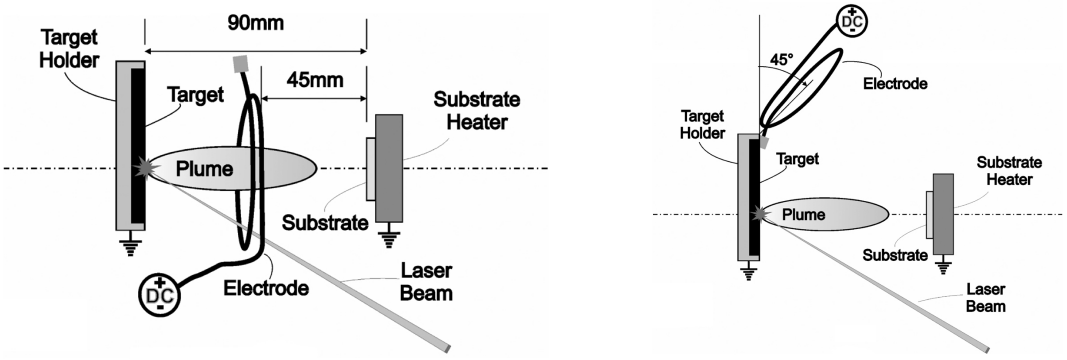
Although the main focus of our research was on low-T_c superconducting circuits, we also diverted some of our effort to the deposition of high-T_c materials and the fabrication of Josephson junctions/weak links.

6.1 Electric field enhanced pulsed-laser deposition of YBCO

Due to limited resources most of our fabrication equipment were either modified to fit our needs, or designed and built in our laboratory. The pulsed-laser deposition system was such a system. It was initially modified for the deposition of high-T_c superconductors and then continually adapted to try to optimize the quality of the films.

In order to investigate whether the *in situ* application of electric fields could possibly improve the crystallinity of YBCO thin films, the laser deposition system was modified to allow for the application of electrical fields during depositions [90]. The electric field was created in the vacuum chamber of the deposition system by application of a high voltage to an electrode that could be mounted in an in-line and a 45° off-axis configuration, as is shown in Figure 6.1.

YBCO films were deposited on MgO single crystalline substrates by pulsed laser deposition. The laser beam was focused onto an area of approximately 2 mm$\times$5 mm of a rotating

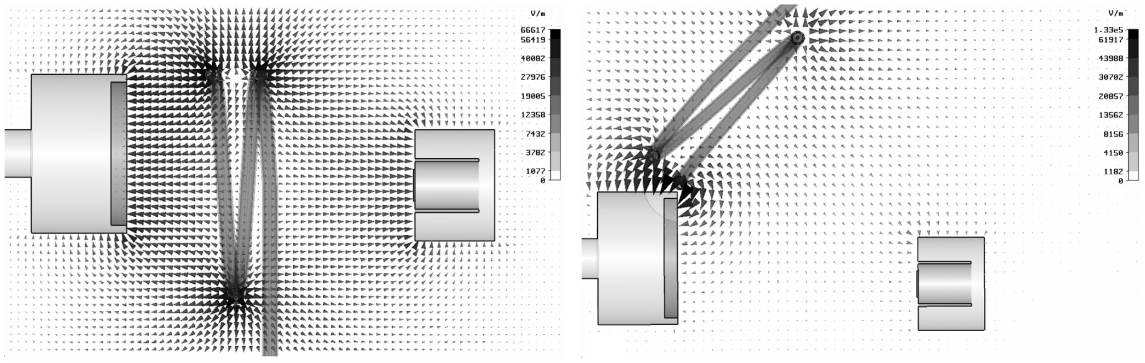


(a) **(b)**

Figure 6.1: Schematic of the experimental setup of the high voltage electrode inside the vacuum chamber of the pulsed laser deposition system. (**a**) In-line configuration. (**b**) 45° off-axis configuration. From [90].

stoichiometric YBCO target with a diameter of 50 mm. The separation between the target and substrate was fixed at 90 mm. The films were deposited at a substrate temperature of 726° C in an oxygen pressure of 7×10^{-2} mbar for 30 minutes. The thickness of the deposited YBCO films were approximately 190 nm. After deposition the films were annealed *in situ* at 500° C for 30 minutes at 1 bar.

Deposited thin films were tested at applied high voltage values ranging from -1 kV to +5 kV. Electrostatic simulations [91] were done to observe the electric field patterns for the in-line and 45° off-axis configurations at an applied voltage of +1 kV. The observed patterns are shown in Figure 6.2.



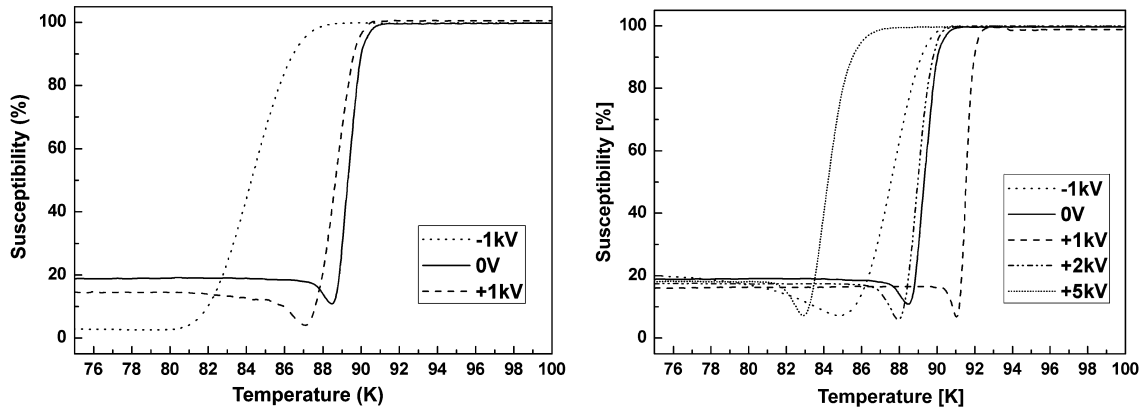
(a) **(b)**

Figure 6.2: Simulations of the static field inside the vacuum chamber of the pulsed laser deposition system at an applied voltage of +1 kV. (**a**) In-line configuration. (**b**) 45° off-axis configuration. The arrowheads indicate the direction of the electric field. Darker, larger arrowheads indicate higher fields. From [90].

As can be seen in Figure 6.2(a), the in-line configuration created a relatively uniform perpendicular electric field in the region of the substrate and target. On the other hand,

with the off-axis configuration, all the electrical field lines were concentrated to the side of the target closest to the electrode, producing practically no field at the substrate, as is shown in Figure 6.2(b).

Susceptibility measurements were done for YBCO thin films that were deposited at different voltage values, for both the in-line and 45° off-axis configurations. These are important measurements, as the measured value of the critical temperature (T_c) and the width of the transition from the superconducting to the normal state (ΔT_c) gives a good indication of the quality of the deposited YBCO thin film. Plots of the measured susceptibility values are shown in Figure 6.3 and the measured superconducting properties are summarized in Table 6.1.



(a) **(b)**

Figure 6.3: Measured susceptibility results of YBCO thin films deposited with the (**a**) in-line configuration, and (**b**) the 45° off-axis configuration. From [90].

Table 6.1: Summary of YBCO film properties

Setup	Voltage (kV)	T_c (K)	ΔT_c (K)
In-line	-1	80.5	7.6
In-line	+1	87.1	3.3
Off-axis	-1	84.8	5.4
Off-axis	0	88.5	2.4
Off-axis	+1	91.1	1.4
Off-axis	+2	88.0	2.6
Off-axis	+5	82.9	4.3

From measured data it was evident that the application of a +1 kV voltage in the off-axis configuration resulted in the best YBCO film quality. The application of a negative voltage deteriorated the properties of the thin films, irrespective of the configuration.

6.2 A novel buffered step-edge Josephson junction

Numerous topologies for the fabrication of high-T_c Josephson junctions have been proposed, including bi-crystal and bi-epitaxial junctions, constriction junctions, ramp type and step-edge junctions.

Due to the freedom that is offered with step-edge junctions, it was decided to investigate the fabrication of such a junction in our laboratory [92].

A well defined step-edge is of prime importance. Normally oxides such as CeO_2 on Yttria-stabilized zirconia (YSZ) substrates and $SrTiO_3$ on MgO substrates are used as buffer layers, as they offer good lattice matching properties with the high-T_c superconducting material, YBCO. However, these materials exhibit very slow etch rates that have a significant influence on the step-angles. It was shown [92] that an ideal buffer layer was found in $PrBa_2Cu_3O_{7-\delta}$ (PBCO), not only with regard to a faster etch rate, but also excellent lattice matching.

In order to predict the step-angle, a model proposed by Wu *et al.* [93] was adapted for our system requirements. The two main variables, as shown in Figure 6.4(a) and Figure 6.4(b) respectively, are:

- α: The incident etching ion-beam angle measured relative to the substrate normal;
- β: The substrate rotational angle.

These two angles were used to define the shading angle (ϕ), as shown in Figure 6.4(c), which should be smaller than the sidewall angle of the photoresist step (θ), as shown in Figure 6.4(d). From simple geometry it can be written that

$$\tan\phi = \frac{h}{s} = \frac{h}{r}.\frac{r}{s} = \frac{1}{\tan\alpha \sin\beta} \tag{6.2.1}$$

where h is the photoresist thickness, r the projection of the etching ion-beam on the substrate surface and s the projection of r on the y'-axis. In order to complete the model, the etch rates of the substrate and photoresist mask needed to be taken into consideration, as illustrated in Figure 6.4(d). After some geometric manipulations the step-angle (ω) was obtained as

$$\omega = \arctan\left(\frac{1}{1+x}\right)\tan\phi \tag{6.2.2}$$

where x is the relative etch rate given by

$$x = \frac{\text{mask etch rate}}{\text{substrate etch rate}}. \tag{6.2.3}$$

Pulsed laser deposition was used to deposit the PBCO buffer layer on the MgO substrate. Using an AFM, the thickness and roughness of the PBCO layer were measured as 250 nm and 788 nm, respectively. Etch rates and relative etch rates were determined during several etch runs, for different incident beam angles.

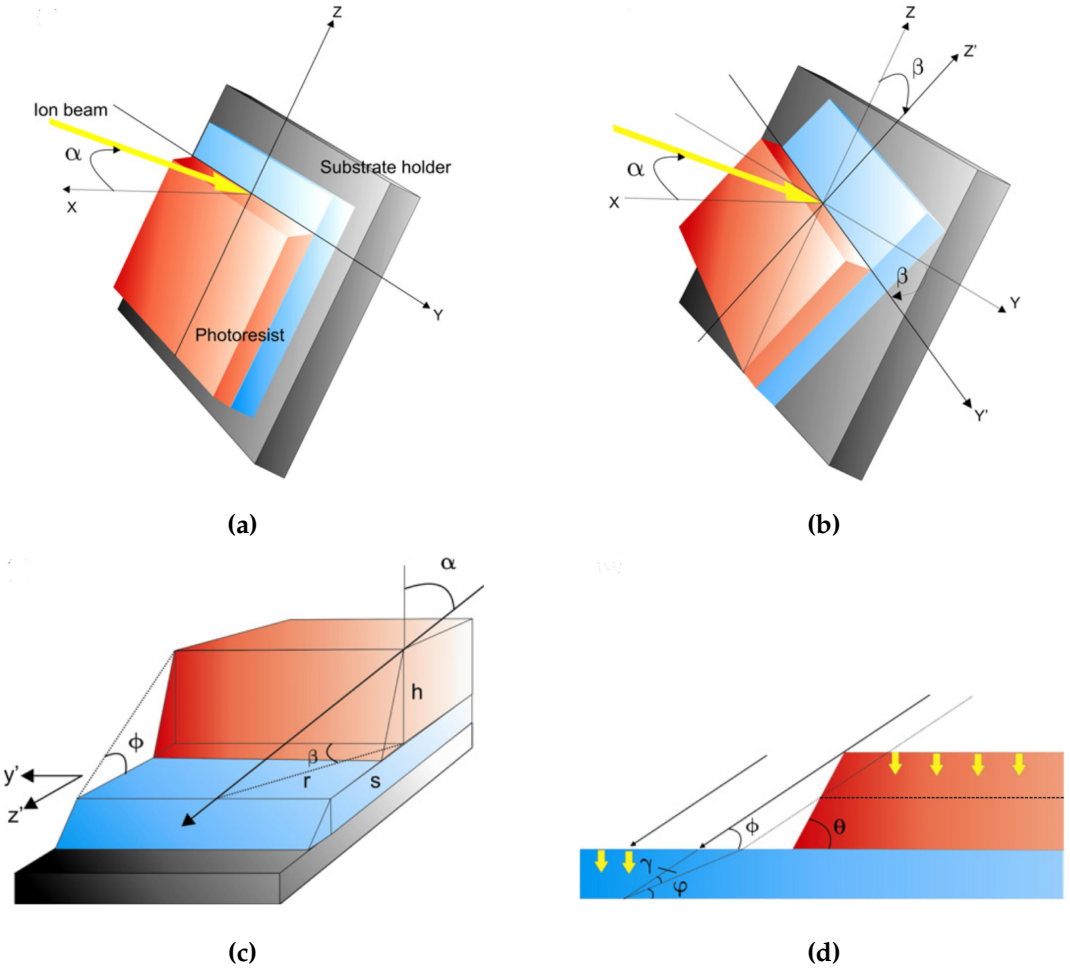


Figure 6.4: Model of step-edge process. (**a**) Definition of incident etching ion-beam angle (α). (**b**) Definition of substrate rotational angle (β). (**c**) Definition of shading angle (ϕ). (**d**) Illustration of general scenario. From [92].

To validate the prediction model, an incident etching ion-beam angle was chosen as $\alpha = 60^\circ$, and the step-angle (ω) was measured for different values of substrate rotation angle (β). The measured results are compared to the theoretical values in Figure 6.5. The ion-beam etching was done by an argon ion-mill that was designed and constructed in our laboratory.

As can be seen, the correlation between the measured and predicted values is quite good for $\beta \geq 10^\circ$.

An AFM image of the PBCO step-edge is given in Figure 6.6 for $\alpha = 60^\circ$, $\beta = 15^\circ$ and $\omega = 25^\circ$.

After the step-edge formation, the substrate was annealed in oxygen at 500° C for 30 minutes to allow for recrystallization of the bombarded material.

A superconducting YBCO layer was then deposited by pulsed reactive crossed-beam laser ablation. The film thickness was limited to about 70% of the step height to ensure that the grain boundary close to the step-edge did not shunt the junction. The substrate

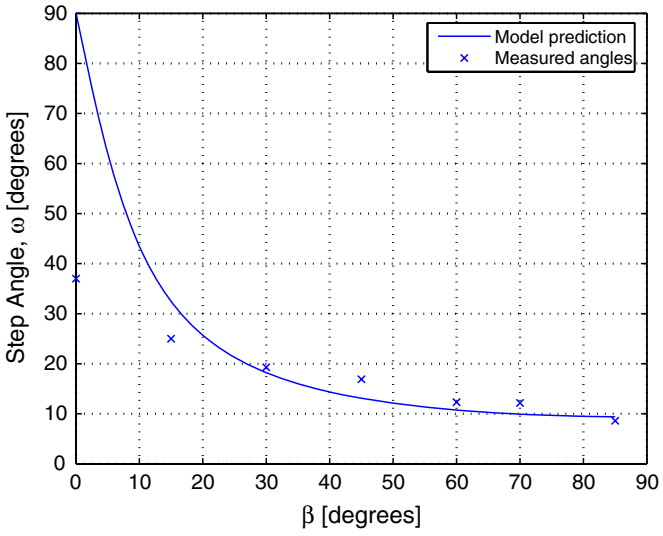


Figure 6.5: Predicted and measured PBCO step-angles (ω) for different values of substrate rotation angle (β). From [92].

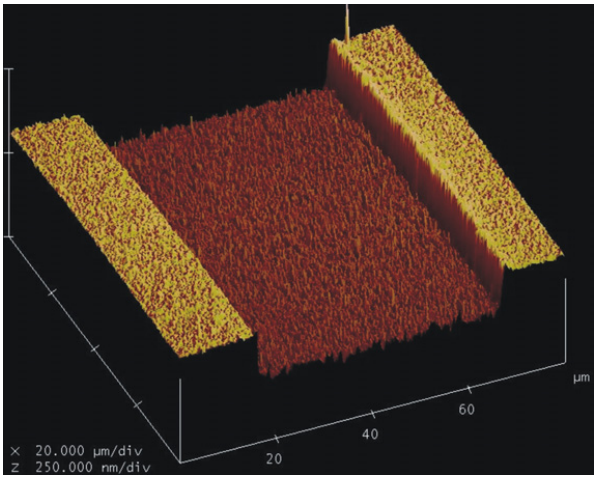


Figure 6.6: AFM image of PBCO step-edge for $\alpha = 60°$, $\beta = 15°$ and $\omega = 25°$. From [92].

was then patterned into 10 μm wide strips traversing the step-edge in order to form the Josephson junctions.

The test setup is shown in Figure 6.7. The magnetic field was applied by a Helmholtz two-coil system over the cold finger. A Hall probe was used to calibrate the magnetic field before measurements were taken.

The measured IV curve at a temperature of 70 K is shown in Figure 6.8(a) and exhibited well-defined Josephson behavior. In order to verify true Josephson behavior of the step-edge junction, the junction was exposed to RF power to check whether Shapiro steps could be observed. The measured response of the junction is shown in Figure 6.8(b) at an RF frequency of 8.891 GHz and at a temperature of 40 K. The clear Shapiro steps confirmed that true Josephson behavior was indeed obtained from the step-edge junction.

The magnitude of the Shapiro voltage steps (V_o) are related to the RF frequency (f_s) by

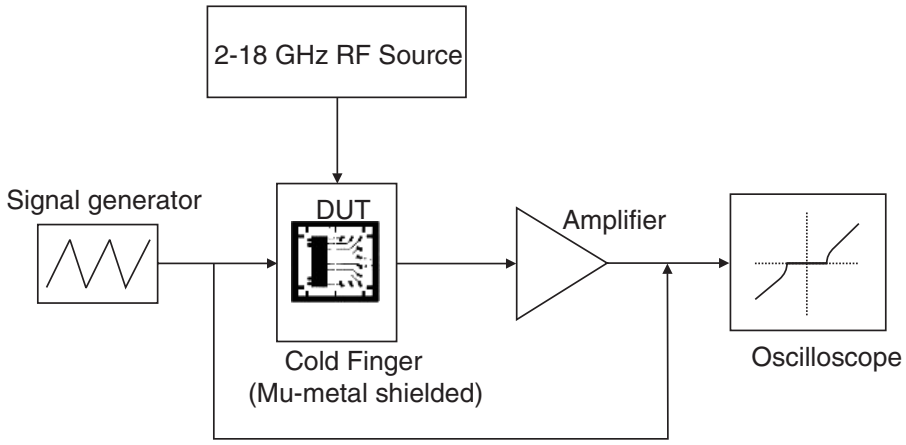
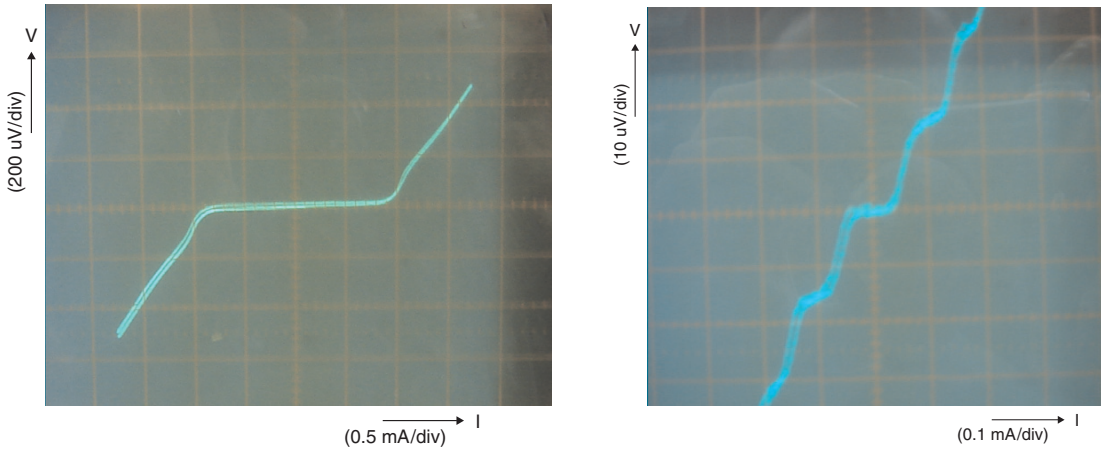


Figure 6.7: Schematic of basic test setup. From [92].



(a) **(b)**

Figure 6.8: (**a**) Measured IV characteristics at 70 K. (**b**) Shapiro steps measured at 40 K with f_s=8.891 GHz. From [92].

the expression

$$V_o = n\left(\frac{\Phi_o}{2\pi}\right)\omega_s = n\Phi_o f_s \tag{6.2.4}$$

where Φ_o ($= 2.0678 \times 10^{-15}$ Wb) is defined as a flux quantum or fluxon.

From Figure 6.8(b) the magnitude of the Shapiro voltage step was approximated as V_o=18 μV, and with an RF frequency of f_s=8.891 GHz, the value of an fluxon was calculated from (6.2.4) as

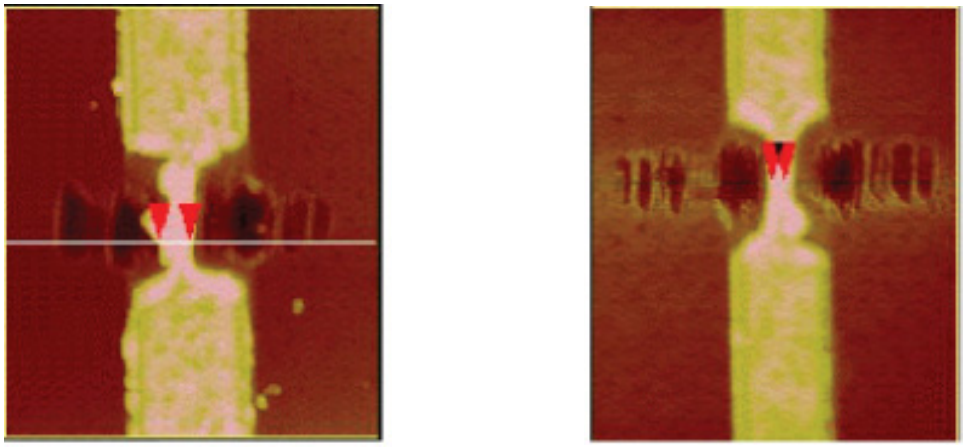
$$\Phi_{o(meas)} = \frac{V_o}{f_s} = 2.0245 \times 10^{-15}\ \text{Wb}, \tag{6.2.5}$$

which confirmed the quantum behavior of the junction.

6.3 Laser-etched submicron YBCO Josephson junctions

Numerous fabrication techniques for high-T_c Josephson junctions are available in the literature. However, most of them involve tedious multi-step processing.

In order to minimize the number of processing steps, a 213 nm laser system, attached to a sample mosaic navigation system, was used to etch constrictions in YBCO lines to form Josephson junctions [94]. Inverse cylindrical magnetron (ICM) sputtering was used to deposit 150 nm thick YBCO films on MgO substrates. Surface roughnesses of about 9 nm were measured by AFM. The films were then patterned by argon ion-milling into strips that varied from 4 μm to 10 μm in width. The laser system was then used to etch micron- and submicron-sized constrictions in the YBCO strips, etching from both edges of the strips. Two AFM images of laser-etched constrictions are shown in Figure 6.9.



(a) **(b)**

Figure 6.9: (**a**) AFM image of a laser-etched constriction with a 1.64 μm width, and (**b**) a submicron constriction with a 703 nm width. From [94].

The measured IV curves of the laser-etched constriction that is shown in Figure 6.9(b) are shown in Figure 6.10(a) for a range of temperatures. The decrease in critical current (I_c) with increasing temperature is clearly observed. The measured Shapiro steps are shown in Figure 6.10(b) at an RF frequency of 9.073 GHz and at a temperature of 57.1 K.

From Figure 6.10(b) the magnitude of the Shapiro voltage step was approximated as V_o=20 μV, and with an RF frequency of f_s=9.073 GHz, the value of an fluxon was calculated from (6.2.4) as

$$\Phi_{o(meas)} = \frac{V_o}{f_s} = 2.2043 \times 10^{-15}\ \text{Wb}, \tag{6.3.1}$$

which confirmed the quantum behavior of the junction.

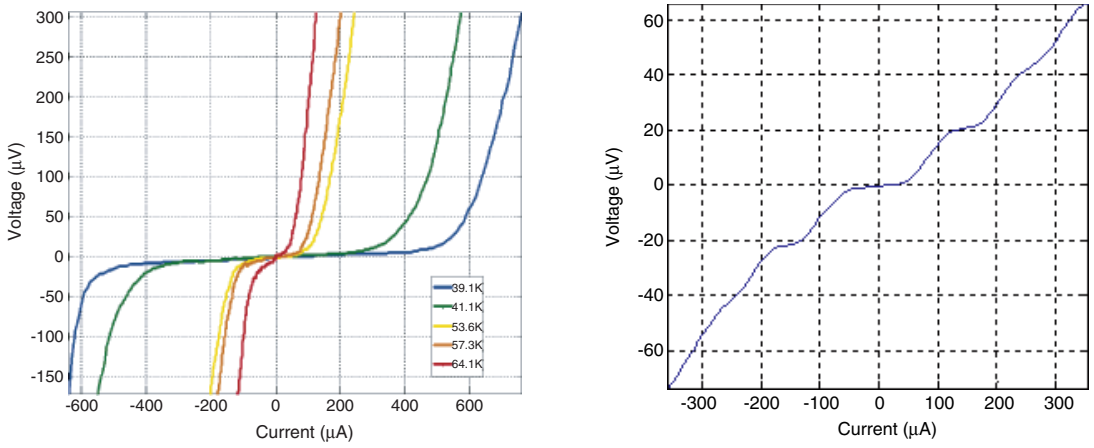


Figure 6.10: (**a**) Measured IV curves for the laser-etched Josephson junction shown in Figure 6.9(b) at different temperature values. (**b**) Measured Shapiro steps at T=57.1 K and a frequency of 9.073 GHz. From [94].

6.4 Nanoplough constrictions in thin YBCO films made with Atomic Force Microscopy

Another option that was explored for the production of Josephson junctions, was to use the AFM in contact mode to test the viability of scratching/ploughing constrictions in thin YBCO films [95].

For the experiment YBCO films were deposited on a MgO substrate by pulsed laser deposition. AFM images of the film surface showed average roughness values of 20 nm. A number of micron-sized YBCO strips were then defined by wet-etching. The AFM, with a diamond-coated tip, in contact mode, was then used to plough into a line from both sides to produce a very narrow constriction. The principle is shown in Figure 6.11.

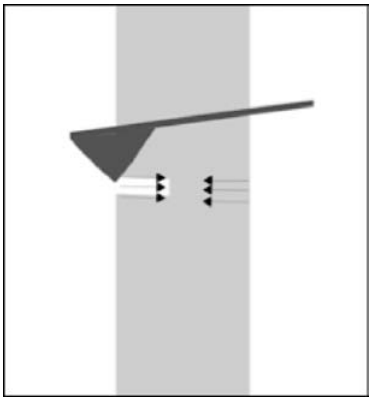
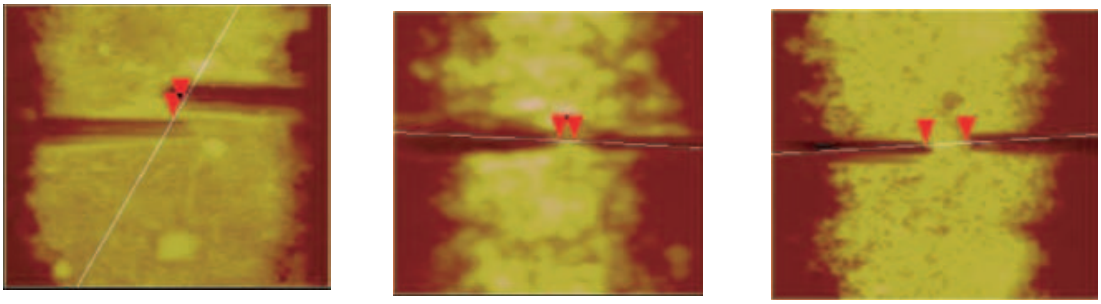


Figure 6.11: Schematic principle of nano-lithography with the AFM. From [95].

In Figure 6.12 a selection of the results of the proposed ploughing technique is shown.



(a) **(b)** **(c)**

Figure 6.12: Nano-constrictions on YBCO thin films ploughed by AFM. The separation of the arrow marks shows the width. (**a**) A new type of *S*-shaped constriction with a width of 377.9 nm. (**b**) A Dayem type constriction with a width of 269.9 nm. (**c**) A Dayem type constriction with a width of 939.9 nm. From [95].

Although it was demonstrated that it was possible to scratch sub-micron constrictions in thin YBCO films, Josephson behavior could not be observed in these junctions.

Another batch of samples were subsequently prepared. The same deposition processes were followed, but this time the YBCO strips were patterned by argon ion-milling, instead of the wet-etching process that was followed previously [96]. To minimize the loss of oxygen in the YBCO layers during the milling process, the film was attached to a water-cooled copper sample holder with thermal paste. The normal AFM ploughing procedure was then followed to create the constrictions.

Prior to the milling process, the quality of the deposited YBCO films was determined by measuring the resistance versus temperature characteristics. The measure characteristics of a 100 nm thick YBCO film is shown in Figure 6.13.

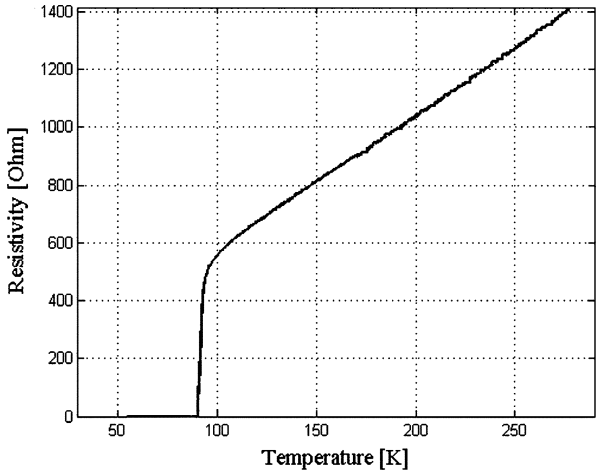
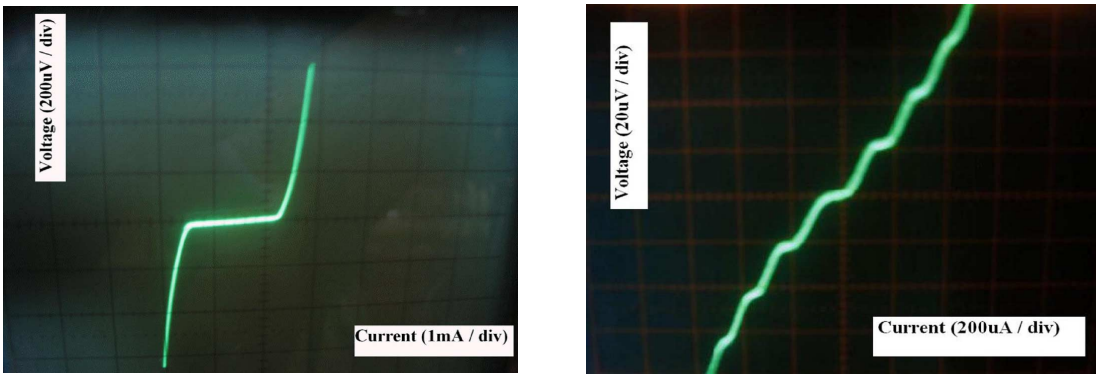


Figure 6.13: Measured resistance versus temperature characteristics of a 100 nm thick YBCO film. From [96].

From the graph it is evident that the quality of the YBCO film was very good, with

T_c=90.2 K and the transition width (ΔT_c) only about 1 K.

The same measurement setup that was shown in Figure 6.7 was used to measure the characteristics of the junctions. The measured IV curve of a 3.6 μm wide micro-plough constriction, at a temperature of 57 K, is shown in Figure 6.14(a). The IV curve exhibited a sharp knee, which meant that true Josephson behavior was a strong possibility. The micro-plough constriction was then exposed to RF power to check whether Shapiro steps could be observed. The measured response of the junction is shown in Figure 6.14(b) at an RF frequency of 10.225 GHz and at a temperature of 54 K. The clear Shapiro steps confirmed that true Josephson behavior was indeed obtained from the micro-plough constriction.



(a) **(b)**

Figure 6.14: (**a**) Measured IV characteristics at 57 K. (**b**) Shapiro steps measured at 54 K with f_s=10.225 GHz. From [96].

From Figure 6.14(b) the magnitude of the Shapiro voltage step was approximated as V_o=21 μV, and with an RF frequency of f_s=10.225 GHz, the value of a fluxon was calculated from (6.2.4) as

$$\Phi_{o(meas)} = \frac{V_o}{f_s} = 2.0538 \times 10^{-15} \text{ Wb}, \tag{6.4.1}$$

which confirmed the quantum behavior of the junction.

Additional studies were done to characterize the dependence of the critical current (I_c) on temperature, constriction width and applied magnetic flux density (B) [97]. Samples with constriction widths of 1.9 μm, 3.1 μm and 4.1 μm were prepared, using the same deposition and milling parameters and procedures as before.

The measured temperature dependence of the critical current is shown in Figure 6.15 for the three different constriction widths. As can be seen from the graph, the temperature dependence of the critical current can be approximated by a straight line for all constriction widths. This is typical for constriction type junctions.

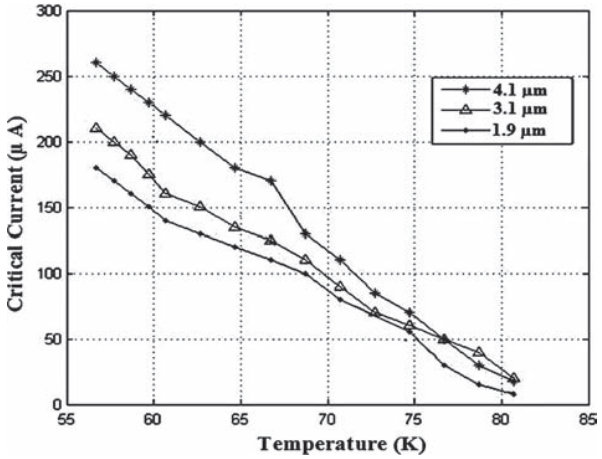
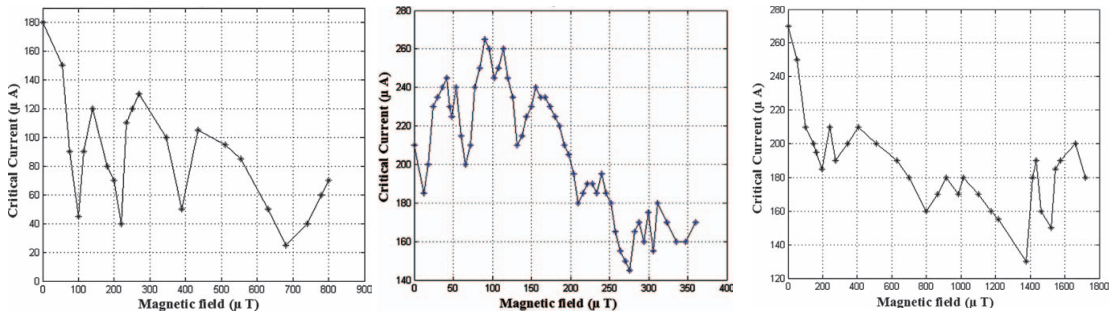


Figure 6.15: Measured temperature dependence of the critical current for constriction widths of 1.9 μm, 3.1 μm, and 4.1 μm. From [97].

A pair of Helmholtz coils was used to to apply a DC magnetic field perpendicular to the surface of the structure. The measured response of the critical current as a function of the applied magnetic flux density is shown in Figure 6.16 for the different constriction widths.



(a) **(b)** **(c)**

Figure 6.16: Measured critical current versus magnetic flux density for constriction widths of (**a**) 1.9 μm, (**b**) 3.1 μm, and (**c**) 4.1 μm. From [97].

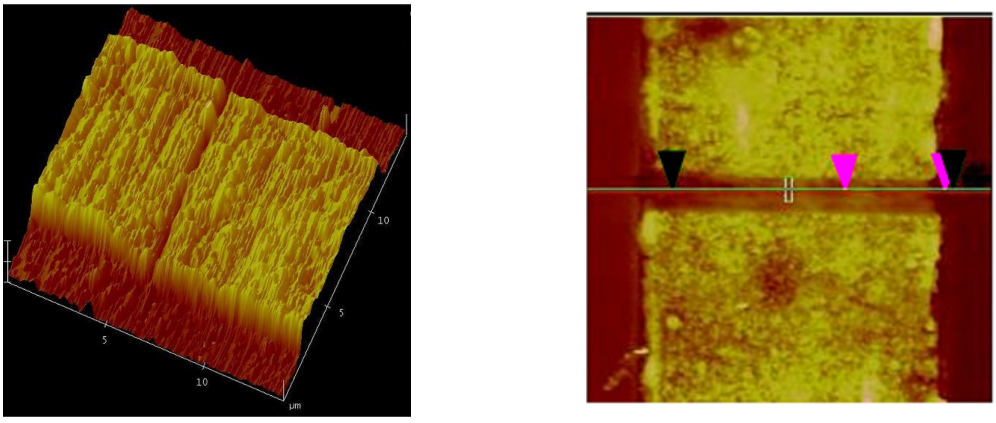
In theory, when magnetic flux threads a junction, the critical current will be modulated by the amount of flux threading the junction. In an ideal Josephson junction the value of the critical current can be expressed as

$$i_c(\Phi_J) = I_c \left| \frac{\sin(\pi\Phi_J/\Phi_o)}{\pi\Phi_J/\Phi_o} \right| \tag{6.4.2}$$

where Φ_J is the flux threading the junction [98]. This leads to a typical Fraunhofer diffraction pattern. As can be seen in Figure 6.16, Fraunhofer-like patterns were observed, but with substantial deviation from the ideal pattern expressed by (6.4.2).

In further experiments the characteristics of a sample with a constriction width of 492 nm were compared to the characteristics of a so-called variable thickness bridge (VTB) junction

[99]. In the VTB junction the AFM was used to scratch the junction from left to right, but in the process changing the force on the tip of the AFM. This led to a constriction that varied in thickness from 25 nm to 50 nm from edge to edge. A 3D AFM image of the constriction with a width of 492 nm is shown in Figure 6.17(a) and the VTB junction in Figure 6.17(b). Both junctions exhibited Shapiro steps and also Fraunhofer-like dependence of the critical current on magnetic flux density.



(a) **(b)**

Figure 6.17: (**a**) 3D AFM image of the top view of the junction with a constriction width of 492 nm. (**b**) AFM view of the VTB junction. The variable thickness can be seen in the constriction area. From [99].

The research confirmed that it was indeed possible to use AFM ploughing to manufacture junctions with constant thickness (Dayem-type) and also variable thickness (VTB) junctions. All junctions showed Josephson behavior, as was confirmed by the measured Shapiro steps in the IV curves when exposed to RF magnetic fields, and also the Fraunhofer-like dependence of the critical current on applied magnetic field.

6.5 Summary

In this chapter the work that was done on high-temperature superconductors was described.

Due to financial constraints we were compelled to either modify existing equipment or design and build our own. Here mention must be made of Ulrich Büttner, one of the best engineering technicians I have ever come across. He was instrumental in the modifications to the pulsed laser deposition system [90] and the design and fabrication of the argon ion-mill. Based on the work that he did to build out our fabrication capabilities he received his Master's degree in 2011 [100].

A number of my postgraduate students also did some stellar work on the fabrication of high-T_c Josephson junctions. The work of Hennie de Villiers [101] on bi-epitaxial Josephson junctions and Wynand van Staden [92, 102] on PBCO buffered step-edge junctions are worth

mentioning. Akram Elkaseh was able to extend the use of our AFM and showed that it can be used to fabricate junctions by scratching constrictions into YBCO [103, 95, 96, 97, 99, 104].

During this time we were also very fortunate to have Srinivasu Vallabhapurapu as a Postdoctoral Fellow in the laboratory. He was a true inspiration for the students and for myself.

Chapter 7

Nano-devices and sensors

Over the years we have been able to build up a reasonably well-equipped laboratory for the fabrication of thin film devices. Although we have primarily used the laboratory for the fabrication of high-T_c devices, specifically YBCO Josephson junctions, the equipment was obviously also suitable for the fabrication of non-superconducting devices.

Although we have been successful in the fabrication of the basic building block of superconducting circuits, the Josephson junction, we realized that we did not have the capabilities and finances to fabricate more complex high-T_c circuits. We were also convinced that high-T_c integrated circuits were probably not viable in the short term, or even in the long term.

We thus started to explore other research areas, such as nano-devices and sensors.

7.1 Zinc oxide nanogenerators

7.1.1 Pressure sensors

One of the first non-superconducting projects was an investigation to determine whether a zinc oxide (ZnO) nanogenerator could be used as a pressure sensor [105, 106].

Two 10 mm $\times$ 10 mm silicon substrates were used as base material. Thin layers of gold (10–20 nm thick) were then sputtered on the substrates to act as a catalyst for the ZnO nanowire growth. The Vapor-Liquid-Solid (VLS) method was used to grow the ZnO nanowires from a mixture of graphite and ZnO powder at 920° C for 20 minutes [107]. A SEM photograph of the ZnO nanowires is shown in Figure 7.1. The average height of the nanowires were 200 nm.

A thin layer of gold was then sputtered on top of the nanowires of one substrate. This was done to form a Schottky contact, which was a crucial step to make the device piezoelectric. The two samples were then glued together to form the complete sensor. A diagrammatic presentation of the fabrication process is shown in Figure 7.2(a), and a photograph of the complete sensor in Figure 7.2(b).

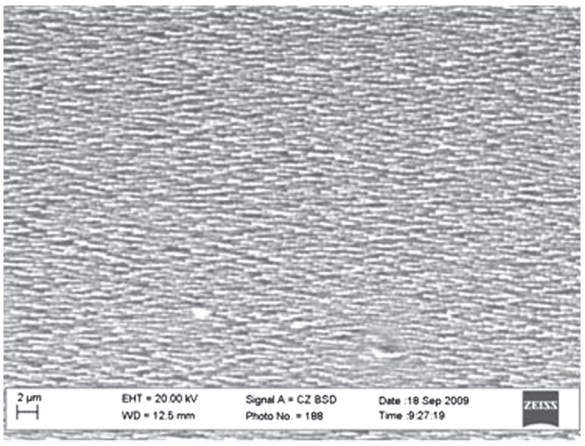


Figure 7.1: SEM photograph of the ZnO nanowires grown with the VLS method at 920° C for 20 minutes. From [106].

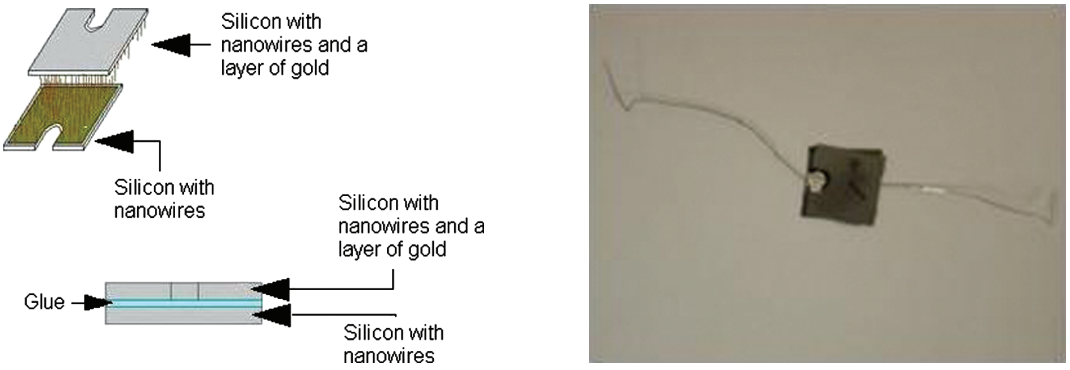


Figure 7.2: (**a**) Diagrammatic presentation of the fabrication process of the sensor. (**b**) Photograph of the fabricated ZnO nanowire pressure sensor. From [106].

Comsol Multiphysics [108] simulations were performed on a single ZnO nanowire with a length of 600 nm and a diameter of 30 nm, to verify that the concept was viable. As can be seen from Figure 7.3(a), a potential of 0.358 V was generated when a force of 40 MN was applied to the top of the nanowire in the x-direction.

The response of five fabricated sensors were tested by measuring the output voltage when different weights were put on the sensors. The weights were placed on a 25 mm^2 block to ensure that the pressure point remained the same. The output voltage was amplified with a gain of 1000. The measured responses of the five sensors are shown in Figure 7.3(b).

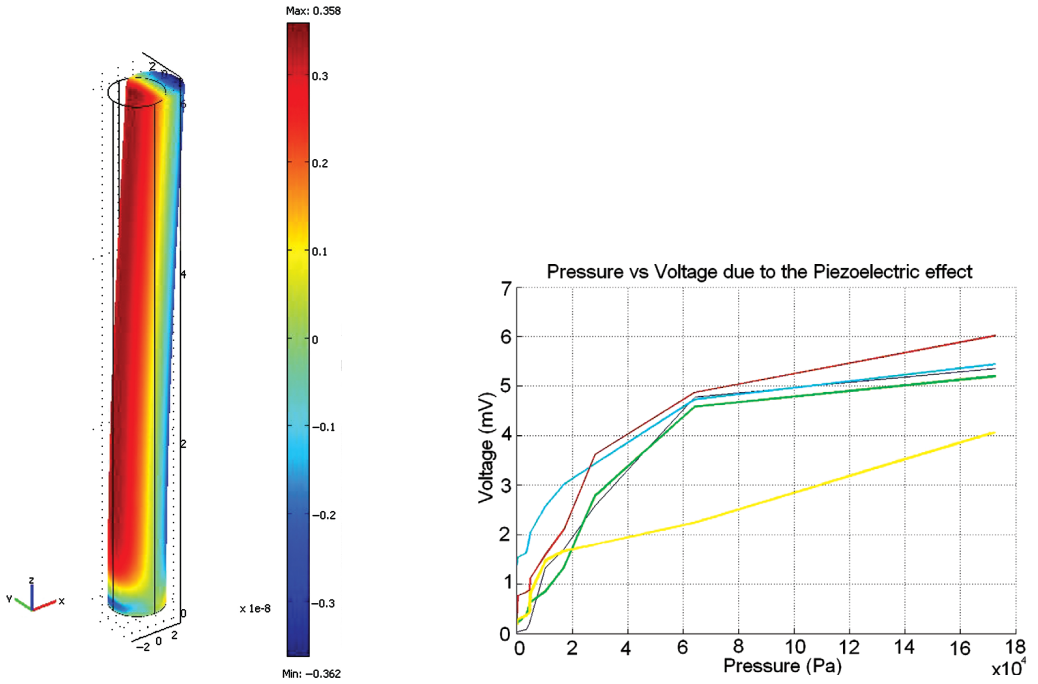


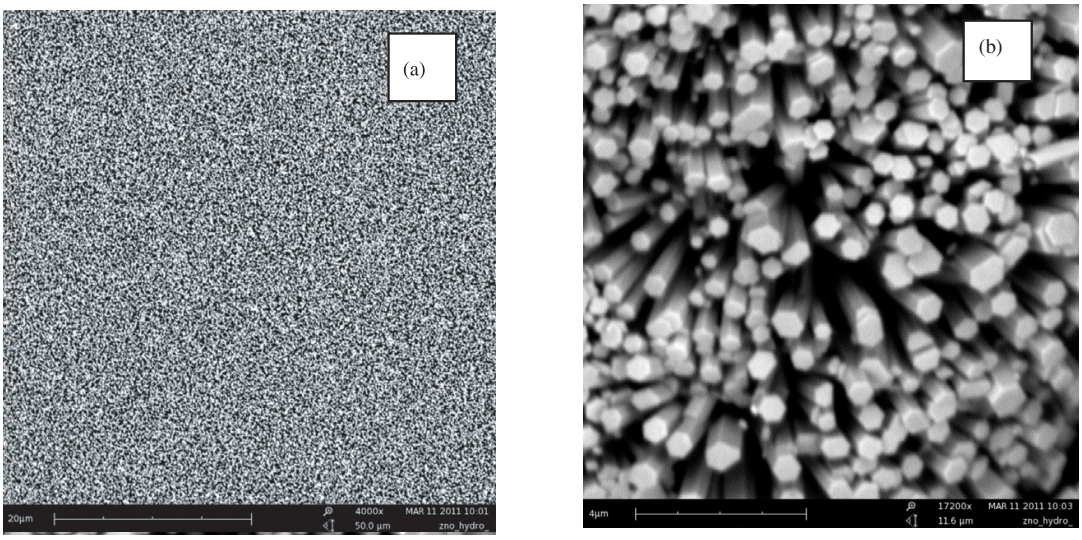
Figure 7.3: (**a**) Electric potential of a simulated ZnO nanowire when a force of 40 MN is applied in the x-direction. (**b**) Measured relationship between the output voltage and applied pressure, for 5 different sensors. From [106].

It was clear from the graphs that most sensors exhibited almost linear behavior up to about a pressure of 60 kPa, after which the voltages flattened out. One sensor (yellow line) showed a substantially different characteristic.

It was also observed that the measured output voltages of the sensors were much lower than the simulated values. That was due to the fact that loss factors, such as the internal resistance of the nanowires, the contact resistance of the contact pads and the resistance of the Si/Au substrate were not taken into account.

Due to the high temperature required for the growth of the ZnO nanowires in previous experiments, a different technique was used to further explore the characteristics of the piezoelectric pressure sensor. The nanowires were grown by the aqueous solution method [109], which is a low temperature process. Thin layers of ZnO (15–20 nm thick) were deposited on 10 mm $\times$ 10 mm silicon substrates by RF magnetron sputtering. The coated substrates were then placed face down in an equal molar aqueous solution of hexahydrate and hexamethylenetetramine. The solution was then placed in an oven at 85° C for 20 hours. The density and morphology of the grown ZnO nanowires are shown in Figure 7.4 [110].

A top electrode was manufactured by evaporating a 100 nm layer of gold (Au) on a silicon substrate to form a Schottky contact. The final assembly is shown in Figure 7.5, where the gold side of the top electrode is resting on top of the nanowires. In order to verify that a



(a) **(b)**

Figure 7.4: (**a**) The density and (**b**) morphology of the grown ZnO nanowires grown by the aqueous method. The growth was done at 85° C for 20 hours. From [110].

Schottky contact had been formed, the IV curve of the assembled sensor was measured. The measured result is shown in Figure 7.6. The diode-like characteristic confirmed the existence of a Schottky contact.

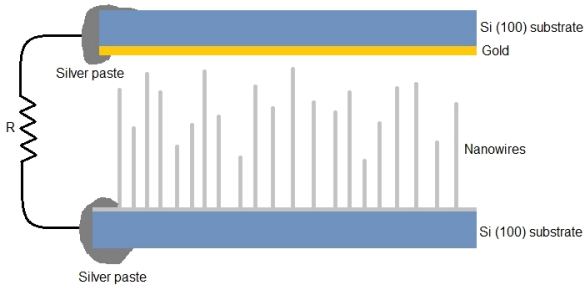


Figure 7.5: Schematic of the assembled nanogenerator. From [110].

An in-phase operational amplifier circuit, with a voltage gain of 100, was used to measure the output voltage of the nanogenerator across the load resistor shown in Figure 7.5. The measurements were taken by moving the top electrode around, with the gold side of the top electrode resting on top of the nanowires, thus bending the nanowires. The measured output voltage of the nanogenerator is shown in Figure 7.7, with a load resistor of 10 MΩ. It can clearly be seen that an output, significantly above the noise level, was only generated when the nanowires were disturbed.

To establish whether the generated voltages were not due to mechanical noise, but due to the friction of the top electrode on the nanowires, the gold layer of the top electrode was replaced by silver (Ag), which would inhibit the formation of a Schottky contact. The measurements confirmed that the observed output voltage in contact mode was similar to

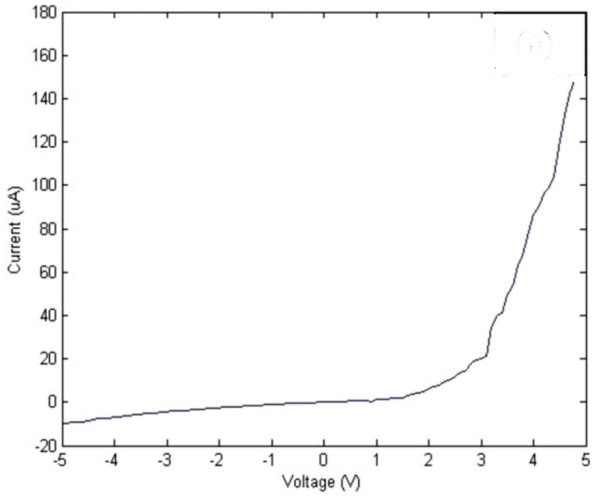


Figure 7.6: Measured IV curve of the nanogenerator. From [110].

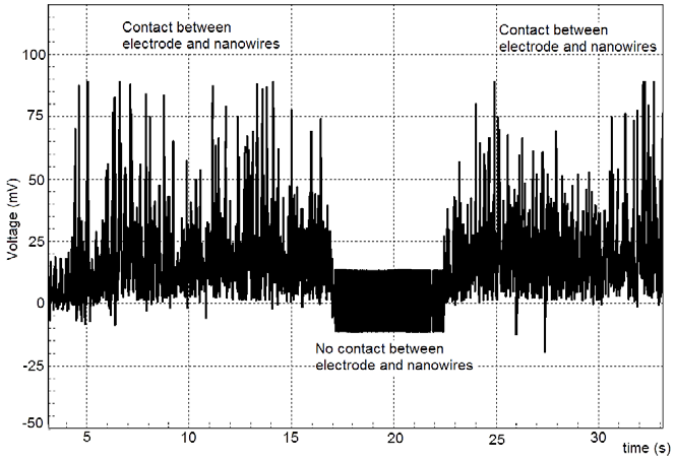


Figure 7.7: Measured output voltage of the nanogenerator with a load resistance of 10 MΩ. From [110].

the noise observed in non-contact mode. This was a clear indication that the measured voltages in contact mode were indeed a result of the presence of the Schottky contact, and thus due to piezoelectricity.

The existing nanogenerators were still some way off from being practical, mainly due to the fact that the friction between the nanowires and the gold electrodes damaged both the nanowires and the gold electrodes.

7.1.2 Optimization of the output voltage of a rigid ZnO nanogenerator

Two different methods to synthesize ZnO nanowires were used previously [106, 110]. Each method had a set of parameters which, if varied, would change the output voltage of the nanogenerator.

The influence of the changes in these parameters were investigated for both growth methods to determine whether optimum conditions for resistance and carrier concentra-

tion could be found with respect to the generated output voltages of the nanogenerators [111, 112]. The standard procedures for the Vapor-Liquid-Solid (VLS) and aqueous solution methods were followed, as described in Section 7.1.1 (p. 118 and p. 120, respectively).

Certain parameters were changed between specified levels, one at a time, during the growth process of the nanowires. The parameter values that were changed, with their minimum and maximum values, are shown in Table 7.1 for the VLS method, and in Table 7.2 for the aqueous solution method. The influence of the change of the parameters was then visually observed with a SEM for each sample, and the resistance, carrier concentrations and the generated output voltages were also determined.

Table 7.1: Different high and low levels of growth parameters that were used during the VLS growth of ZnO nanowires

Parameter	Low level	High level
Growth time (minutes)	5	30
Growth temperature (°C)	500	1200
Initial pressure (mTorr)	200	2000
Growth pressure (mTorr)	500	1500
Source powder (grams)	1	3
Argon flow rate (sccm)	20	120

Table 7.2: Different high and low levels of growth parameters that were used during the aqueous solution growth of ZnO nanowires

Parameter	Low level	High level
Growth time (hours)	1	24
Growth temperature (°C)	60	120
Concentration (mM)	10	100
Covered	No	Yes
Ratio (Zinc salt:HMTA)	1:0.75	1:1.125

The substrate with the grown nanowires was fixed to a test board, as shown in Figure 7.8. Conducting wires were attached to the four corners of the substrate, using silver paste. The Van der Pauw method was used to measure the resistivity of the nanowires. A total of eight resistance values were measured by application of a current between two terminals, and then measuring the voltage across the other two terminals. The resistance values $R_{12,34}$, $R_{34,12}$, $R_{21,43}$, $R_{43,21}$, $R_{23,41}$, $R_{41,23}$, $R_{32,14}$ and $R_{14,32}$ were measured. The subscript convention is explained in Figure 7.8. The average of the first four values was defined as R_v and the average of the last four values as R_h. The resistance of the nanowire substrate (R_s) could then be calculated by solving the Van der Pauw equation [113]

$$e^{-\pi R_v/R_s} + e^{-\pi R_h/R_s} = 1. \tag{7.1.1}$$

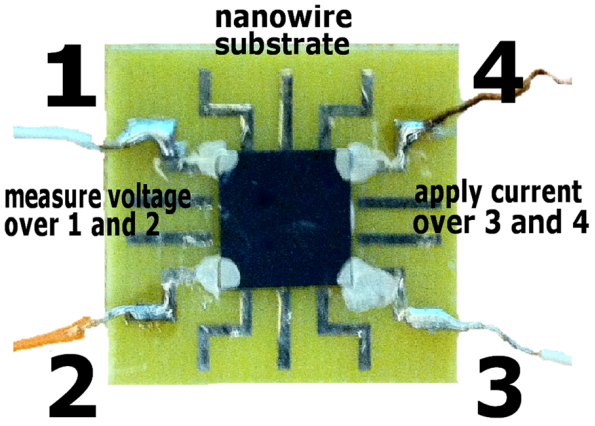


Figure 7.8: Photograph of a nanowire sample attached to the test board for Van der Pauw and Hall measurements. The measurement setup for $R_{12,34}$ is shown. From [112].

The carrier concentration was measured by applying a constant magnetic field perpendicular to the nanowire substrate. Constant currents I_{13}, I_{31}, I_{24} and I_{42} were then applied consecutively and the resultant Hall voltages V_{42}, V_{24}, V_{13} and V_{31} were measured. The respective carrier concentrations were then calculated from a modified version of the Hall equation [110] as

$$n_s = \frac{8 \times 10^{-8} IB}{qd(V_{24} + V_{42} + V_{13} + V_{31})} \tag{7.1.2}$$

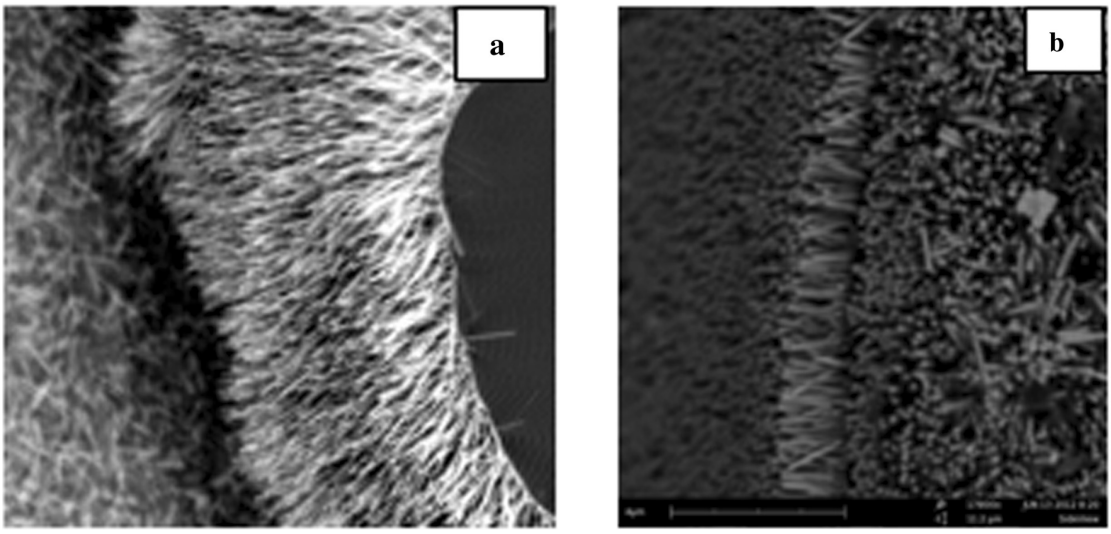
where I is the applied constant current, B the applied magnetic field (in Gauss), q electron charge and d the thickness of the material.

More than 120 samples were grown, of which more than 30 were grown with the VLS method and 90 using the aqueous solution method. Every sample was examined with a SEM at different magnification values in order to compare nanowire morphology, growth direction and density. Images of typical nanowire growth is shown in Figure 7.9 for the two growth methods. Typically the VLS method produced nanowires with lengths ranging from 3 to 4 μm and diameters from 60 to 100 nm. For the aqueous solution method the lengths ranged from 1.5 to 2 μm and diameters from 100 to 150 nm. On average the growth characteristics of the two methods looked very similar, but occasionally random growth directions were obtained by the VLS method.

The measured relationships between resistance and output voltage, and carrier concentration and output voltage, are shown in Figure 7.10 for both growth methods.

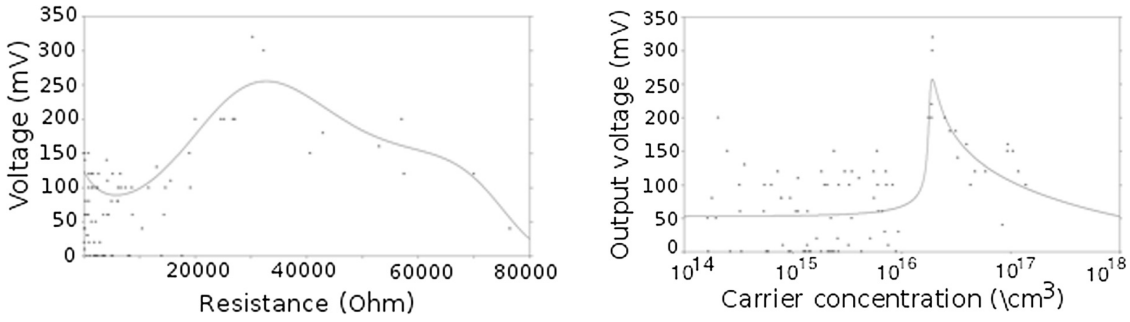
From Figure 7.10(a) it is clear that an optimum output voltage is observed within a certain resistance range. The observations made intuitive sense, because, at low resistance values the carrier concentration is high, which has a screening effect of the piezoelectric potential, thus suppressing the generated output voltage. At high resistance values, on the other hand, the lower output voltages were due to internal losses.

Figure 7.10(b) shows a distinct peak at a certain carrier carrier concentration. At low carrier concentrations piezoelectric charges are not free to move and a lot of losses occur



(a) (b)

Figure 7.9: Typical nanowire growth obtained by the (**a**) VLS method, and (**b**) the aqueous solution growth method. From [112].



(a) (b)

Figure 7.10: (**a**) Measured relationship between the resistance and output voltage of grown ZnO nanowire samples as obtained from both VLS and aqueous solution growth methods. (**b**) Measured relationship between the carrier concentration and output voltage of grown ZnO nanowire samples as obtained from both VLS and aqueous solution growth methods. From [112].

internally, resulting in low output voltages. As was discussed previously, at high carrier concentrations (low resistance values) piezoelectric charges are screened, leading to low output voltages as well.

It was thus experimentally confirmed that both carrier concentration and resistance needed to be optimized for maximum output voltage generation of ZnO nanogenerators.

7.1.3 Nanogenerators fabricated on rigid and flexible substrates

Contact resistance can drastically influence the magnitude of the generated output voltage of a nanogenerator. At nanoscale contact areas become so small that conventional equations

for resistance calculations do not hold true.

In order to try to minimize contact resistance a different nanogenerator structure was proposed [114]. The structure was implemented on both rigid and flexible substrates.

The basic nanogenerator structure that was previously used is shown in Figure 7.11. A gold electrode rests on the tips of the longest nanowires to form Schottky contacts and with downward pressure the nanowires will bend. Those wires in contact with the gold will thus generate a voltage.

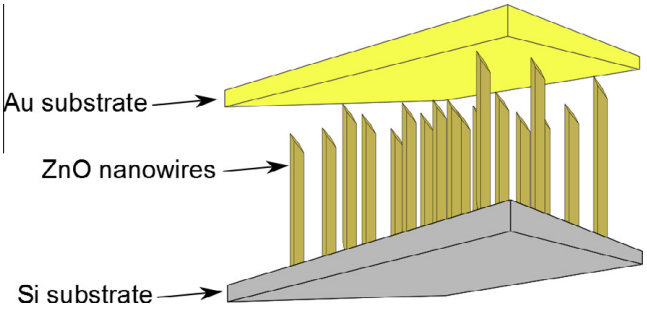


Figure 7.11: Graphical representation of a nanogenerator manufactured on a silicon substrate. From [114].

Due to the very small contact area of the tips of the nanowires in contact with the gold, the contact resistance equations of Holm [115] are not valid anymore. Ideally, when two materials are in contact, the contact resistance is described by the Holm resistance

$$R_H = \frac{\rho_1 + \rho_2}{4a}, \tag{7.1.3}$$

where ρ_1 and ρ_2 are the resistivities of material 1 and 2, respectively, and a is the contact radius. For small values of contact area the Holm resistance becomes inaccurate and the Sharvin resistance [115], given by

$$R_S = \frac{\rho_F}{N\pi q^2 a^2}, \tag{7.1.4}$$

where ρ_F is the Fermi momentum of electrons, N the electron density and q electron charge.

The two equations (7.1.3) and (7.1.4) can be combined to give

$$R = \frac{4(\rho_1 + \rho_2)\lambda}{9\pi a^2} + \frac{\rho_1 + \rho_2}{2a\pi^2} \arctan\left(\frac{\pi a}{\lambda}\right), \tag{7.1.5}$$

where λ is the mean free path of the charge carriers. This expression can be used to calculate the contact resistance for all values of contact area, a [115].

The contact area of the nanogenerator configuration shown in Figure 7.11 is inherently small, which results in a large contact resistance and thus a low output voltage.

A configuration with an improved contact between the nanowires and the gold electrode is shown in Figure 7.12. In this configuration the space between the nanowires were

filled with Poly(methyl methacrylate) (PMMA), with only the tips of the nanowires sticking out. Gold was then deposited over the nanowire tips, thus making contact with all the nanowires. This ensured a marked increase in contact area, when compared with the previous configuration, and thus an expected increase in the generated output voltage. For the bottom electrode a flexible Kapton film was used.

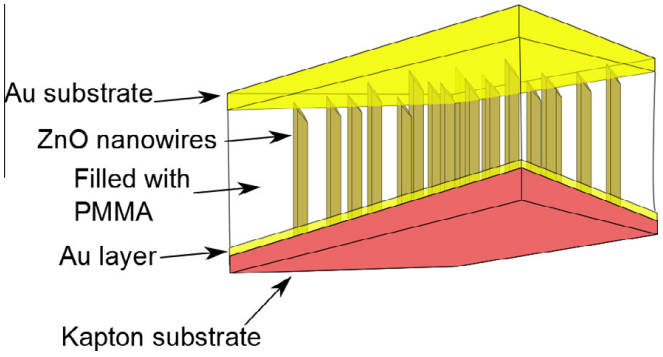


Figure 7.12: Graphical representation of a nanogenerator manufactured on a flexible Kapton film. From [114].

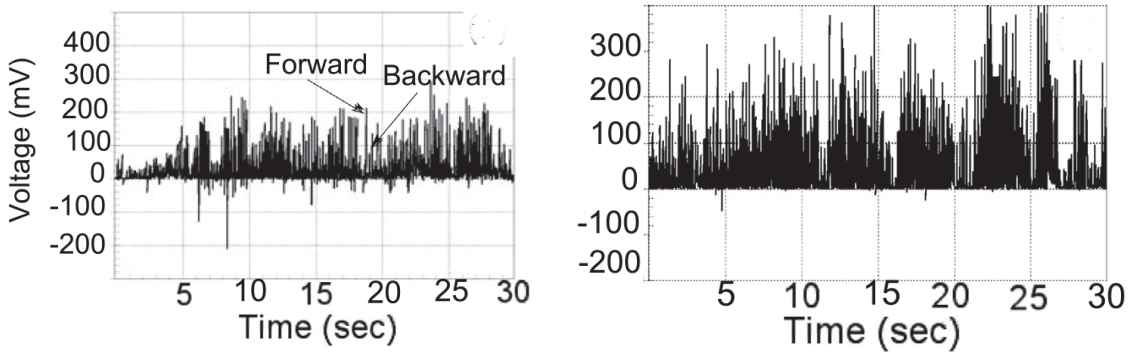
To test the performance of the optimized nanogenerators, samples were prepared on rigid and flexible substrates [114]. For the nanogenerator on a rigid silicon substrate, the configuration shown in Figure 7.11 was used, but with PMMA between the nanowires. A separate gold coated silicon electrode was manufactured, which was placed on top of the nanowires tips, with the gold side resting on the nanowire tips. An output voltage was generated by moving the top electrode over the nanowires tips.

The structure of the nanogenerator on the flexible Kapton film was identical to the configuration shown in Figure 7.12. In this case an output voltage was generated by bending the flexible structure to and fro.

The aqueous solution nanowire growth method was used for both substrates, because it is a low temperature method and Kapton has a relatively low melting point.

The measured output voltage of the rigid silicon nanogenerator is shown in Figure 7.13 for two different magnitude forces. The gold electrode was moved backwards and forwards on top of the nanowires, twice a second, to generate the voltage output. A voltage peak was observed for every movement, thus generating four pulses every second. As expected, larger applied force generated higher output pulses. Also evident was that the pulses were all rectified by the Schottky contact. The average generated voltage for the higher applied forces was about 200 mV, with some peaks over 400 mV. For the smaller forces the average generated voltage was around 150 mV with a few peaks at 300 mV. These results compared very favorably with reported results of 243 mV that were obtained with the same technique [116].

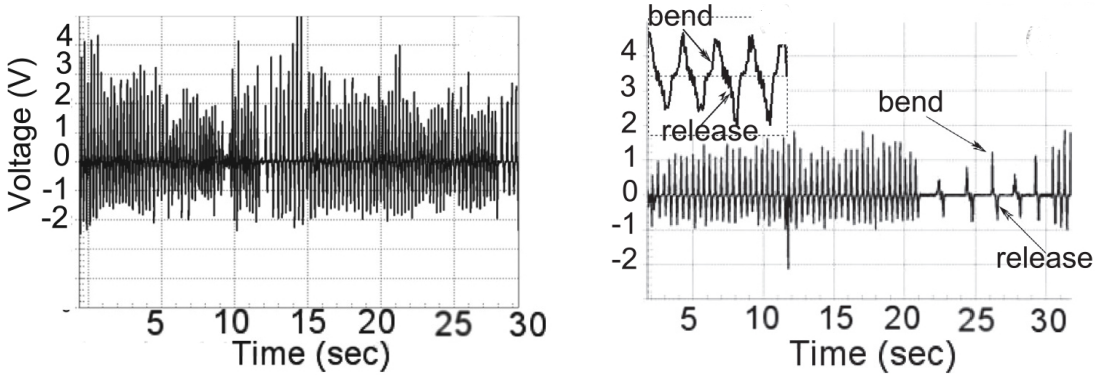
The measured output voltage of the flexible Kapton film nanogenerator is shown in Figure 7.14, for different bending frequencies. In Figure 7.14(a) the flexible film nanogenerator



(a) **(b)**

Figure 7.13: Measured output voltage of the rigid nanogenerator when the gold electrode is moved backwards and forwards, at 2 cycles per second, on top of the nanowires. (**a**) Generated output voltage when a standard force is applied. (**b**) Generated output voltage when double the standard force is applied. From [114].

was bent over 90° at a rate of 2 cycles per second, and in Figure 7.14(b) the film was bent to a maximum of 90° at 1 cycle per second, and then at 1 cycle every 3 seconds.



(a) **(b)**

Figure 7.14: Measured output voltage of the flexible Kapton film nanogenerator when (**a**) the film is bent over 90° at a rate of 2 cycles per second, and (**b**) when the film is bent to a maximum angle of 90° at 1 cycle per second, and then at 1 cycle every 3 seconds. From [114].

The first interesting observation was that the bending and releasing action generated voltage pulses with different polarities, as can be clearly observed in the magnified inset in Figure 7.14(b). This can be ascribed to the fact that gold layers were deposited on both electrodes, thus forming rectifying Schottky contacts at both electrodes. As expected, the flexible film nanogenerator was superior and generated much higher voltage peaks than the rigid nanogenerator. The observed average output voltage in Figure 7.14(a), where a larger bending angle was used, was over 2 V, with some peaks as high as 4 V. From Figure 7.14(b), where a smaller bending angle was used, the average voltage was about 1 V, with some peaks at 1.8 V.

The performance of the flexible Kapton film nanogenerator illustrated clearly that a bigger force would always result in higher output voltages, and that the smaller contact resistance of the configuration shown in Figure 7.12 would also result in higher output voltages.

7.1.4 Optimization of flexible film nanogenerators

In order to maximize the generated output voltage of the flexible film nanogenerator, the influence of different fabrication parameters were investigated [117].

The standard fabrication process, as was used to fabricate the flexible Kapton film nanogenerator shown in Figure 7.12, was used to manufacture the non-optimized nanogenerator. A schematic of the basic structure, with an inset showing the actual finished device, is shown in Figure 7.15. The measured voltage peaks of the non-optimized nanogenerator were very small, with an average of about 200 mV, and the highest peaks almost reaching 400 mV.

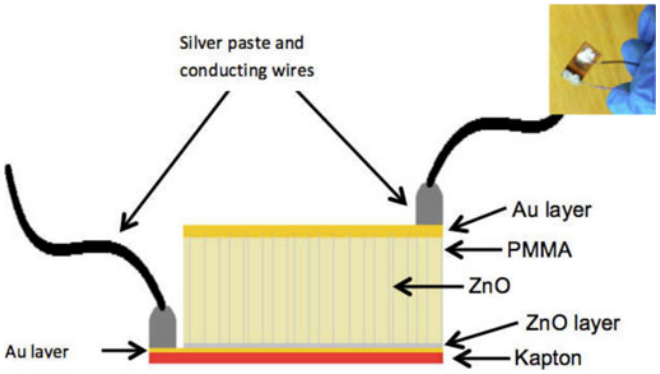


Figure 7.15: Schematic presentation of the flexible Kapton film nanogenerator. The inset is a picture of the actual finished device. From [117].

As a first optimization step the grown ZnO nanowires were annealed at 350° C for 30 minutes in different gas environments. The measured output voltages for the different gas environments are shown in Table 7.3.

Table 7.3: Measured output voltages of nanogenerators for different gas environments

Gas used	Voltage (mV)
None (non-optimized device)	400
Air	1200
Nitrogen	500
Oxygen	600
Argon	400

From the measured results it was clear that an annealing step in air had a marked effect on the output voltage, increasing the 400 mV output of the non-optimized nanogenerator to 1.2 V.

As a second investigation, various materials were added to the PMMA before it was spun onto the substrate to fill the space between the nanowires. The materials were gold nanoparticles (10 nm in diameter), single-walled carbon nanotubes (SWCNTs), multi-walled carbon nanotubes (MWCNTs), graphene (12 nm flakes) and ZnO nanowires. The measured output voltages of the nanogenerators, for the different materials that were added to the PMMA, are shown in Table 7.4.

Table 7.4: Measured output voltages of nanogenerators for various materials that were added to the PMMA

Material	Voltage (mV)
Gold nanoparticles	800
SWCNTs	1000
MWCNTs	600
Graphene	800
ZnO nanowires	1200

All the additions to the PMMA had a beneficial effect on the measured output voltages of the nanogenerators, with ZnO nanowires performing the best, with a threefold increase in output voltage, when compared to the non-optimized nanogenerator.

Finally, a combination of the optimization steps were used to fabricate a nanogenerator. The grown nanowires were annealed in air at 350° C for 30 minutes. As both ZnO nanowires and SWCNTs individually had a marked influence on the output voltage, a combination of the two materials was added to the PMMA and then spun onto the substrate. The measured output voltage of the optimized nanogenerator is shown in Figure 7.16.

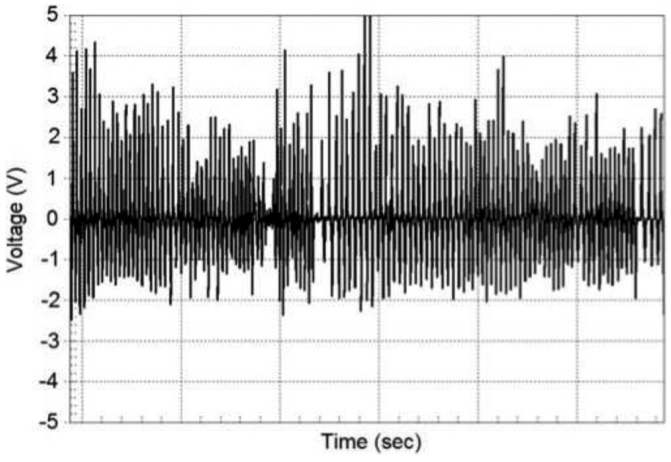


Figure 7.16: Measured output voltage of the optimized nanogenerator. From [117].

The measured output voltage showed peaks as high as 5 V, with an average voltage of about 2 V. This was a tenfold increase in output voltage, when compared to the original non-optimized nanogenerator.

7.1.5 Energy harvesting circuits for ZnO nanogenerators

For nanogenerators to be useful, the generated energy needs to be stored. To explore the energy storage problem, three different energy harvesting circuits were investigated [118].

A nanogenerator was fabricated on a flexible Kapton film. The grown nanowires were annealed in air at 350° C for 1 hour, but no additional materials were added to the PMMA before it was spun onto the substrate. This nanogenerator was used for the practical tests, and was able to supply a maximum of 5 V at a load current of 1.25 μA.

A full-bridge rectifier, a synchronized switch harvesting on inductor (SSHI) circuit and the LTC3588 integrated circuit chip were tested as energy harvesting circuits. The nanogenerator was connected to the energy harvesting circuit and then bent by placing it between two fingers and then bending it to 90° and then back to flat. The bending rate was from flat to 90° and then back to flat in 1 second.

The full-bridge rectifier was implemented with four MBR0520L Schottky diodes to minimize the forward voltage drop over the diodes. A 10 mF supercapacitor was connected across the output and the nanogenerator was then bent for 5 minutes to charge the supercapacitor. A load resistor was then connected and the output voltage was measured. The measured output voltage is shown Figure 7.17. The output voltage remained constant at 5.75 V for 10 seconds, after which it decayed to zero. For the chosen load, the maximum output current achieved at that voltage was 20 μA, giving a load power of 115 μW.

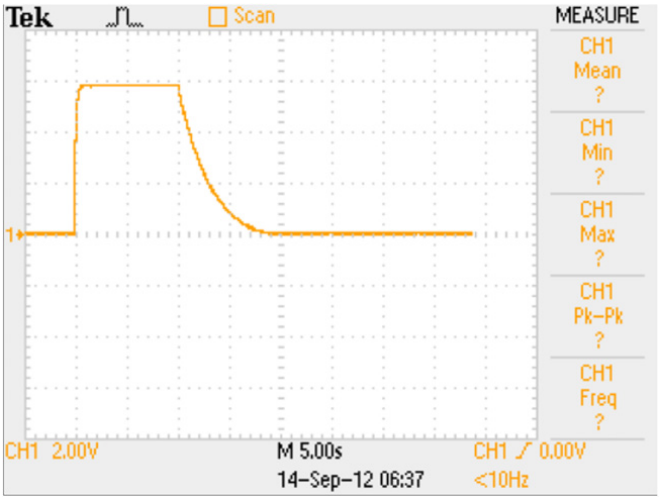


Figure 7.17: Measured output voltage of the full-bridge rectifier circuit. From [118].

Due to the fact that the full-bridge rectifying circuit is inherently lossy, an SSHI circuit implementation was tested, as it was claimed that it had up to a 900% better efficiency than that of a full-bridge rectifying circuit [119]. An SSHI circuit is designed to switch on maximum and minimum peaks, which is achieved by using an electronic breaker, consisting of an envelope detector, a comparator and a switch. The measured output generated by the SSHI circuit was rectified indeed, but so low that it had no practical use. The reason for that

was that the input current required to drive the circuit was about 60 μA, about five times more than what the nanogenerator could supply.

The last circuit that was investigated was the LTC3588 integrated circuit chip from *Linear Technologies*. The circuit was specifically designed as a piezoelectric energy harvesting power supply and thus required a very low input current from the nanogenerator. The measured output voltage of the LTC3588 circuit, with the supercapacitor as load, is shown in Figure 7.18. After 10 minutes of bending, the output voltage achieved was 1.8 V. With a 10 kΩ load, the output voltage stayed constant for 20 seconds before the output decayed to zero. The output current at 1.8 V was 0.17 mA, giving an output power of 306 μW, more than double the value that was achieved with the full-bridge rectifier.

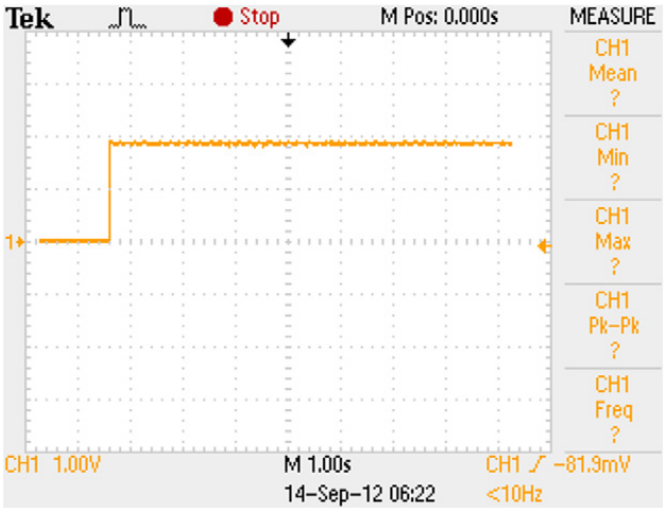


Figure 7.18: Measured output voltage of the LTC3588 circuit with the supercapacitor connected at the output. From [118].

7.2 A ZnO nanowire gas sensor with UV light to enhance sensitivity

A gas sensor was manufactured by growing ZnO nanowires on a patterned substrate. The sensor was placed inside a testing chamber to investigate the response when different gases were introduced into the chamber. A commercial laser pointer was used to modify the sensitivity of the sensor to differentiate between different gasses [120].

ZnO nanowires were grown on a substrate with copper tracks, as shown in Figure 7.19, using the aqueous solution method, as was described previously. The nanowire growth was then removed in two areas to solder conducting wires to the substrate.

The substrate was then placed in an aluminum testing chamber, as is shown in Figure 7.20. The chamber consisted of a single gas inlet and outlet, a glass window at the top to attach the laser pointer, and insulated connectors for connecting the sensor inside the chamber to the external test equipment.

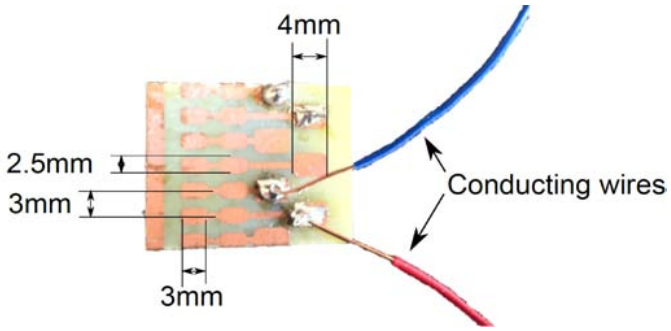


Figure 7.19: Picture of the patterned substrate used for nanowire growth. From [120].

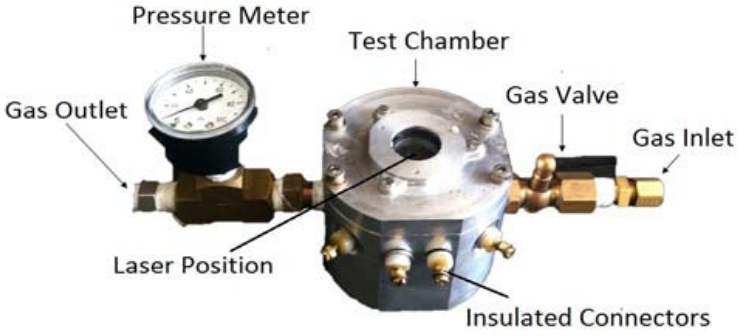


Figure 7.20: Picture of the testing chamber used for testing the sensor. From [120].

The resistance of the sensor was measured over time when different gasses were introduced into the testing chamber. The sensor showed a negligible response for all cases.

It is known that the resistance of ZnO nanowires decreases by four to six orders of magnitude when exposed to UV light in the 380 nm wavelength range [121]. Therefore a commercially available laser pointer with a wavelength of 400 nm was chosen as UV light source to shine into the testing chamber when filled with different gasses, to investigate whether that would have an influence on the measured resistance of the sensor.

Different gasses were added to the system while the laser was being pulsed. The measured response of the sensor is shown in Figure 7.21 for argon, oxygen, nitrogen, carbon dioxide, and also for no gas.

It was quite clear from the measurements that all four gasses showed different responses and that all responses differed from the no-gas case. The measurement response time was slow and the measurements reached a steady state only after about 300 seconds.

The recovery time of the sensor, i.e. the time it took for the sensor to reach its maximum value in ambient conditions again, was also measured. The recovery time was disappointingly slow, as it took about 4000 seconds for the sensor to recover to its initial resistance condition.

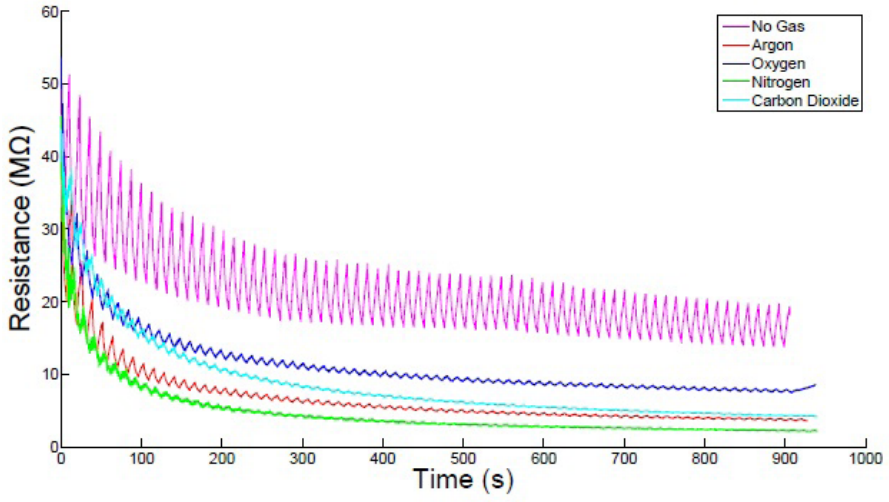


Figure 7.21: Measured response of the ZnO nanowire sensor when different gasses were added to the chamber while pulsing the laser. From [120].

7.3 Biosensors

7.3.1 Piezoelectric biosensors

During my career at Stellenbosch University, I served on numerous university committees. One of the committees is called Subcommittee B. The committee members are selected from the science faculties and the function of the committee is to promote research by the allocation of funding for postdoctoral fellows and newly appointed academics, amongst others.

It was during a tea break at one of those meetings, about five years ago, that one of the members of Subcommittee B from the Department of Microbiology, Prof Leon Dicks, told me about their research on tuberculosis (TB). He mentioned that they encapsulated TB antibodies in a capsule, tied a piece of string to it and let people swallow the capsule. After a few hours the capsule would be retrieved through the mouth again. The capsule was then sent to a laboratory to be tested. In an infected person TB pathogens would bind to the antibodies, thus making a positive TB diagnosis possible. Leon jokingly asked whether "you engineering guys could not come up with something that would enable us to remove the string, detect infection remotely and let the capsule take its natural course"?. I told him about Stanley van den Heever's PhD research on nanogenerators [111] and speculated that, if we could attach the antibodies to the nanogenerator, it would theoretically be possible that the antigen/antibody binding process could generate a piezoelectric voltage detectable by an antenna. Although we both agreed that it was possibly a silly idea, we decided that we would explore the concept. Fortunately there was a Master's student, Deon Neveling, available to take up the challenge and that was the start of a very interesting multidisciplinary research journey.

As a first step, the ZnO nanowire growth process was revisited [122]. In the study ZnO nanowires were grown by the hydrothermal growth (aqueous solution) approach [109]. Si-

licon substrates were coated with a gold layer and then a ZnO seed layer. Two seed layer deposition techniques, sol-gel spin coating and RF cylindrical magnetron sputtering, were compared to identify the most suitable technique. The effect of the gold layer beneath the ZnO seed layer, with respect to the thickness and crystal orientation, on the morphology and alignment of the grown ZnO nanowires was also studied. The ZnO seed layers were characterized by AFM and ellipsometry, while the ZnO nanowires were characterized by scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDS), transmission electron microscopy (TEM) and X-ray diffraction (XRD).

AFM images of the surface topology of ZnO seed layers deposited by RF cylindrical magnetron sputtering and the sol-gel spin coating technique, respectively, are shown in Figure 7.22.

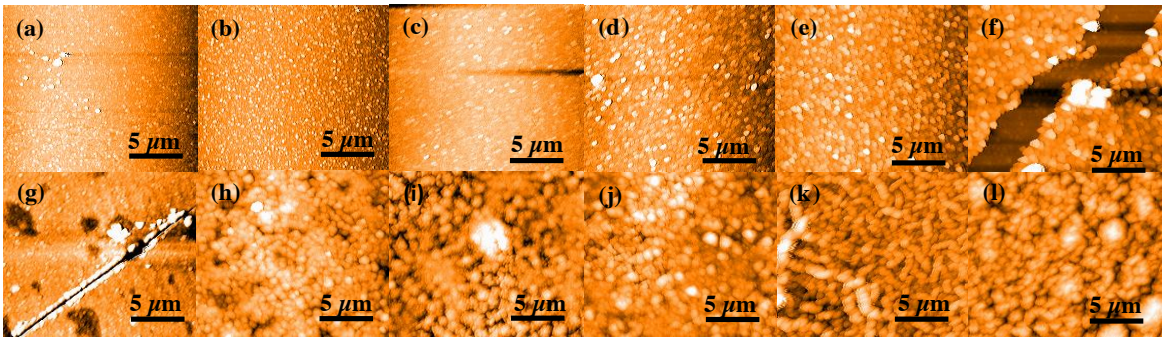
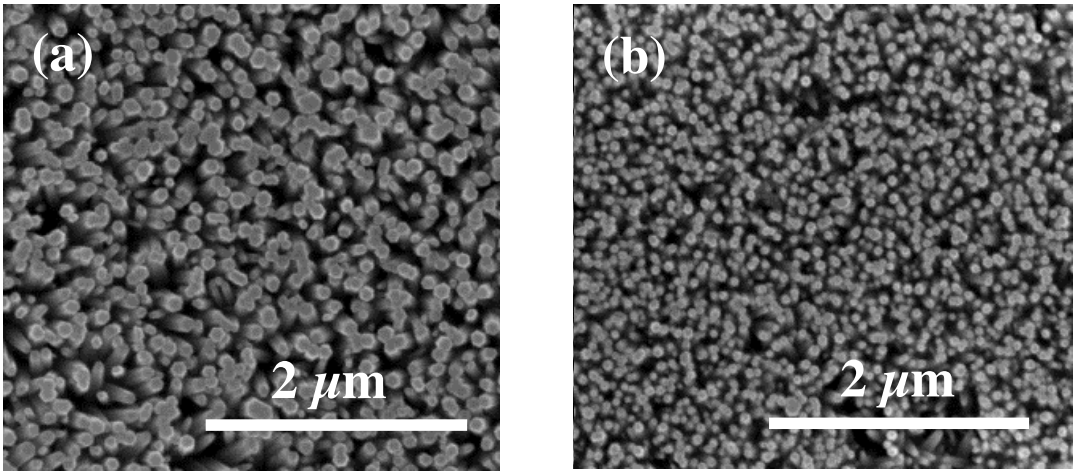


Figure 7.22: AFM images of the surface topology of ZnO seed layer films deposited by the RF cylindrical magnetron sputtering technique for 1–6 min deposition (**a-f**, respectively) and the sol-gel spin coating technique for 1-6 spin coats (**g-l**, respectively). From [122].

In general it was found that an increase in the ZnO seed layer thickness increased the mean diameter of the synthesized ZnO nanowires. When the RF cylindrical magnetron sputtering technique was used, an increase in the ZnO seed layer thickness led to better *c*-axis alignment of the ZnO nanowires. For the sol-gel spin coating technique the opposite was observed. The RF cylindrical magnetron sputtering technique also resulted in more ZnO nanowires having the mean diameter value, something that was not true for the sol-gel spin coating technique. These results confirmed the superiority of the RF cylindrical magnetron sputtering technique for the deposition of ZnO seed layers.

The effect of the gold layer beneath the ZnO seed layer was studied by using a range of techniques to look at the morphology and alignment of the synthesized ZnO nanowires. As an example, high magnification top SEM images are shown in Figure 7.23 for gold layers with different characteristics.

From the images it was clear that hexagonally shaped ZnO nanowires were synthesized on both types of gold layers. However, thicker ZnO nanowires (mean diameter of 57 nm) were produced on the polycrystalline gold layer than on the Au (111) layer (mean diameter of 35 nm).



(a) **(b)**

Figure 7.23: High magnification top SEM images of vertically aligned ZnO nanowires on substrates covered with 40 nm of either **(a)** polycrystalline Au, or **(b)** Au (111). The layers were covered by a ZnO seed layer film deposited by the RF cylindrical magnetron sputtering technique for 3 minutes. From [122].

The optimal ZnO nanowire structure in a transducer is one with the smallest diameter and which is perfectly orientated. With this in mind, the measured results indicated that RF cylindrical magnetron sputtering was the preferred technique to deposit thin ZnO seed layers, because of the superior *c*-axis alignment of the produced ZnO nanowires. The choice of deposited Au (111) layers was also confirmed, as it also resulted in thinner nanowires.

After the optimization studies on the ZnO nanowire synthesis processing steps were completed, a ZnO nanowire-array biosensor for the detection of immunoglobulins was designed and fabricated [123].

The sensor was fabricated on silicon (100) wafers that were cut into 1 cm $\times$ 1 cm pieces. A 20 nm layer of titanium was sputter coated onto the silicon substrate, followed by a 40 nm layer of sputtered gold (111). The ZnO seed layer was then deposited using the sol-gel spin coating technique. The ZnO nanowires were grown by the aqueous solution method, after which PMMA was spun on the substrate to fill the gaps between the nanowires. This was followed by the deposition of a 10 nm layer of gold to form the Schottky contact. That completed the ZnO nanowire nanogenerator.

In order to attach proteins to the fabricated nanogenerator, self-assembled monolayers (SAM) were required to act as molecular scaffolds to immobilize proteins. That was done by dissolving alkanethiol, 3-mercaptopropanoic acid (1mM) in absolute ethanol by sonication. The ZnO nanogenerator was immersed in the self-assembled monolayer (SAM) solution for 24 hours at 25° C in a Schlenk reaction vessel filled with nitrogen gas. The formation of the self-assembled monolayers was terminated by rinsing the nanogenerator with absolute ethanol.

The nanogenerator bound with the self-assembled monolayers was then exposed to

5mM ethyl (dimethylaminopropyl) carbodiimide (EDC) and 5mM N-hydroxysuccinimide (NHS) in absolute ethanol. This was done to increase the coupling efficacy.

Finally the nanogenerator was rinsed with phosphate buffered saline (PBS) and immersed into PBS containing lysozyme (1 mg/ml) from hen egg white for 24 hours at 4° C. A schematic presentation of the finished biosensor is shown in Figure 7.24.

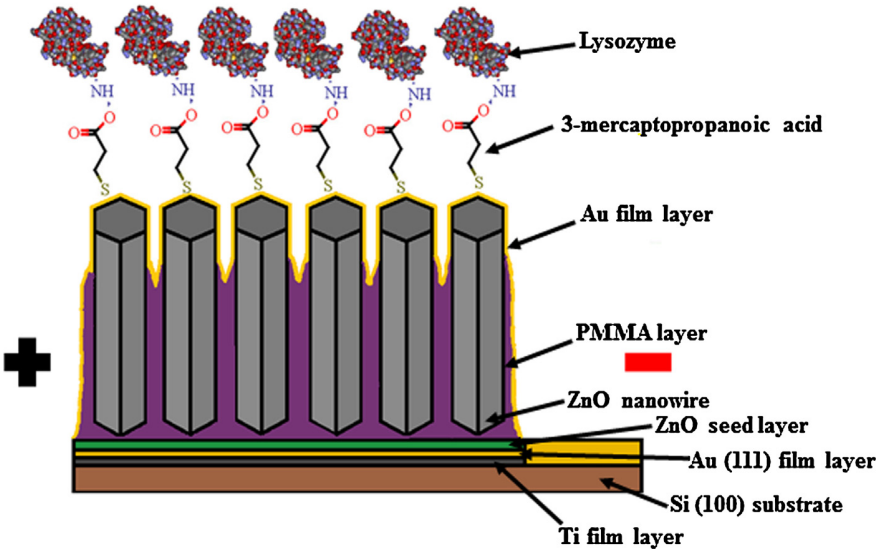
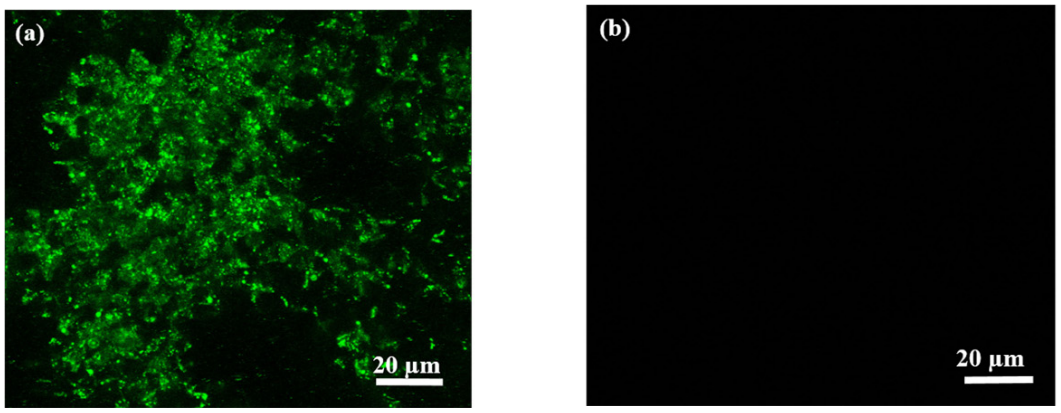


Figure 7.24: Schematic presentation of the finished ZnO nanowire-array biosensor. From [123].

Fluorescence microscopy was used to test whether the lysozyme was successfully bound to the biosensor surface. To do that, the biosensor was incubated with primary lysozyme antibodies and secondary lysozyme fluorescent antibody conjugates. Non-specific binding of the secondary antibody conjugate and lysozyme to the biosensor surface was then assessed. Fluorescence microscopy images of the biosensor surface is shown in Figure 7.25. The relative fluorescence intensity of the immobilized lysozyme biosensor surface, shown in Figure 7.25(a), was measured as 287 RFU. On the other hand, the relative fluorescence intensity of the non-specific binding of the secondary antibody conjugates, as shown in Figure 7.25(b), was measured as only 8 RFU. From these results it was clear that lysozyme was indeed immobilized to the SAMs, as the fluorescence intensity could definitely not be attributed to non-specific binding of the secondary antibody conjugate to the biosensor surface.

To test for the correct functioning of the biosensor, *in vitro* tests were done by using monospecific antibody serum specific for lysozyme. Different concentrations were placed on the biosensor surface and incubated for 1 hour to allow for biorecognition to take place.

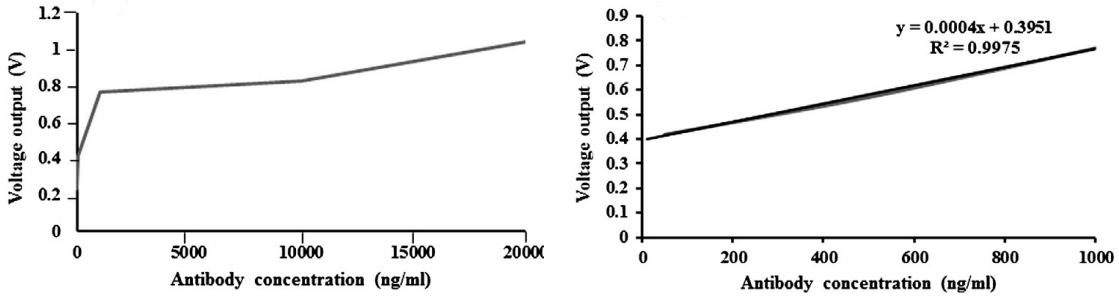
The sensitivity of the biosensor was tested with antibody levels ranging from 10 ng/ml to 20 μg/ml. The measured response of the biosensor is shown in Figure 7.26(a). As can be seen, the measured output voltage increased linearly with antibody levels in the range from 50 ng/ml to 1 μg/ml, followed by a non-linear increase in output voltage as antibody



(a) (b)

Figure 7.25: Fluorescence microscopy images of the biosensor surface immobilized with **(a)** lysozyme, and **(b)** non-specific binding of the secondary antibody conjugate to the biosensor surface. Green fluorescence is indicative of lysozyme molecules immobilized onto the biosensor surface. From [123].

levels increased to 20 μg/ml. This indicated that the biosensor became saturated at antibody concentrations above 1 μg/ml. An enlarged view of the measured linear response for antibody concentrations ranging from 50 ng/ml to 1 μg/ml is shown in Figure 7.26(b). The limit of detection (LOD) was calculated as 102.76 ng/ml, using the linear equation in Figure 7.26(b) [124].



(a) (b)

Figure 7.26: **(a)** Measured output sensitivity of the biosensor for antibody levels ranging from 10 ng/ml to 20 μg/ml. **(b)** Enlarged view of the measured linear response for antibody concentrations ranging from 50 ng/ml to 1 μg/ml. From [123].

The reproducibility of the sensor was tested by using three biosensors incubated with 1 g/ml lysozyme antibodies. The average measured output readings were 0.722 V, 0.770 V and 0.691 V, respectively.

An attractive characteristic of the ZnO nanowire-array biosensor is that it is self-powering. It thus has the potential to be used as an implant for the detection of early post-operative

infection. A patent application describing the invention was filed by Stellenbosch University [125].

The piezoelectric biosensor did catch the attention of the general public after publication of the invention in *Popular Mechanics*[1], the subsequent *Popular Mechanics Breakthrough Award – 2014* (see Figure 7.27), a TV interview on *KykNet*[2], and an article titled "Bacteria may have had their nanochips" in *The Times*[3].

Figure 7.27: At the *Popular Mechanics Breakthrough Award* ceremony (December 2014).

7.3.2 Fiber-optic biosensors

An interesting alternative to the ZnO piezoelectric biosensor was investigated by a Master's student, Michael Maas. He coated a fiber-optic fiber with *Escherichia coli* (*E. coli*) antibodies and investigated whether the transmission of light would be impeded by the attachment of *E. coli* bacteria to the antibodies [126].

Optical fibers were manufactured from borosilicate glass. A borosilicate glass rod was heated with a buthane flame and thin fibers were then extruded from the melted glass. *E. coli* antibodies were then immobilized on the borosilicate glass fibers by using (3-glycidyloxypropyl) 4 trimethoxysilane (GPS) to bind antibodies onto the glass fiber surfaces.

A schematic presentation of the fiber-optic biosensor is shown in Figure 7.28. The theoretical operational principles of the biosensor are shown in Figure 7.29. A light launched by the LED and traveling through the optical fibre is an evanescent wave and will not be entirely contained by the fiber. If a bacterium-antibody binding has taken place, the evanescent

[1] "Big bug hunt: Thinking small", *Popular Mechanics*, October 2014, pp. 92-93.
[2] Dagbreker, *KykNet*, 24 September 2014. (https://www.youtube.com/watch?v=6qwJtC9Fpg8)
[3] "Bacteria may have had their nanochips", *The Times*, 21 October 2015. (http://www.timeslive.co.za/thetimes/2015/10/21/Bacteria-may-have-had-their-nanochips)

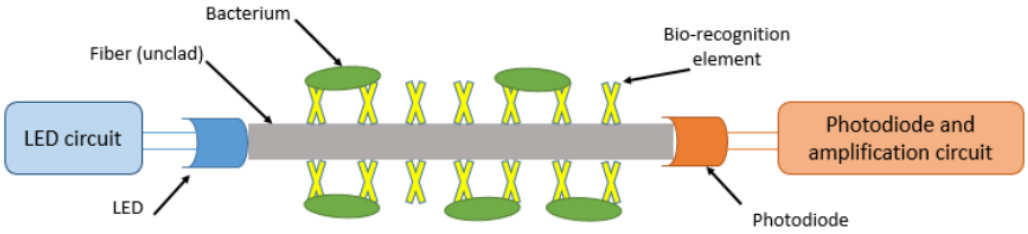


Figure 7.28: Schematic presentation of the fiber-optic biosensor. From [126].

wave will theoretically interact with the attached bacteria and thus impede the transmission of the light through the fiber.

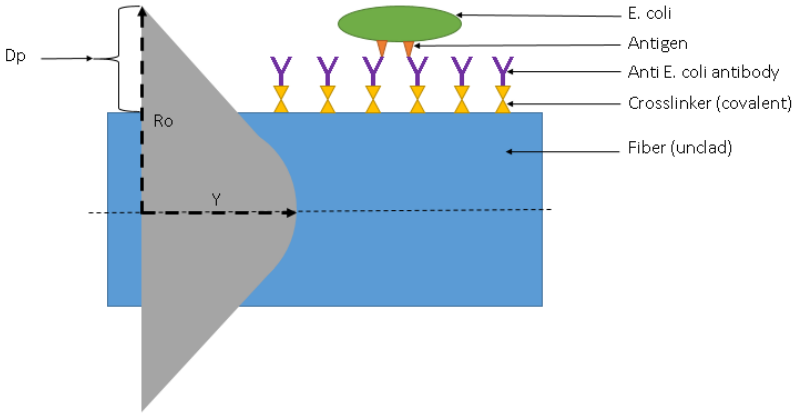


Figure 7.29: Theoretical operational principles of the optical-fiber biosensor. From [126].

The sensor was exposed to *Escherichia coli* DH5α to test the functionality. The voltage response of the sensor was recorded for concentrations of 2.77×10^9 CFU/ml[4] and 3×10^7 CFU/ml, respectively. The measured voltages are the average of three readings, and are shown In Figure 7.30.

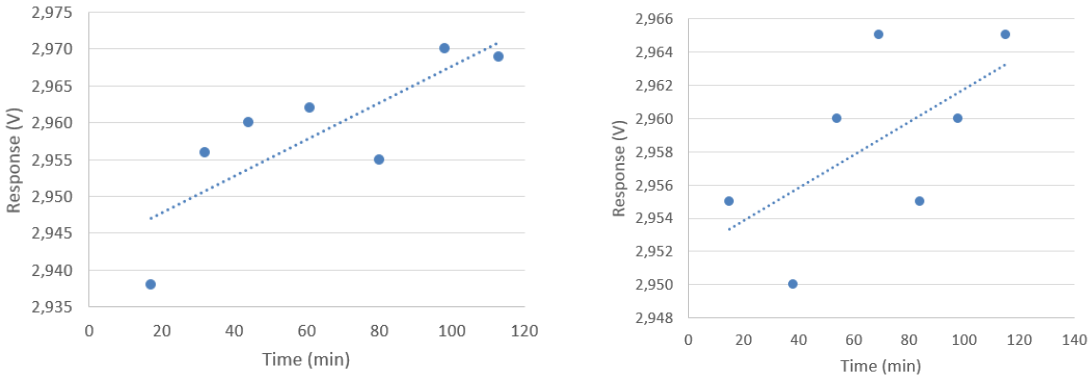
From the measured results it was apparent that the sensor in its current form was not a viable biosensor implementation, although it was suitable to follow the progression of a bacterial infection.

7.3.3 Resistive biosensors

In the South African context, where diseases such as TB and HIV infection have reached endemic proportions, there is a need for inexpensive, handheld point-of-care diagnostic devices that are able to detect specific infections rapidly and with high accuracy, and without the need for trained medical personnel.

Although we have demonstrated that ZnO piezoelectric biosensors have some unique characteristics, the manufacturing process is quite involved. That specific biosensor imple-

[4]Colony-forming Units/ml



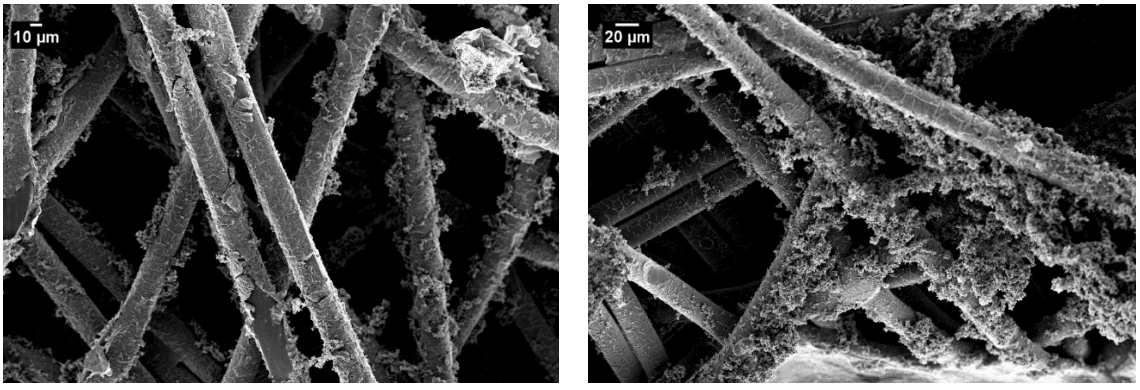
(a) **(b)**

Figure 7.30: Measured voltage response of the fiber-optic biosensor for an *E. coli* concentration of **(a)** 2.77×10^9 CFU/ml, and **(b)** 3×10^7 CFU/ml. From [126].

mentation thus was not necessarily the answer for our envisaged point-of-care diagnostic biosensor.

For his final year undergraduate project, Christiaan Viviers was asked to look at options to replace the piezoelectric transducer with a resistive element. He suggested that electrospun microfibers be considered as a resistive element, as it inherently exhibited a large surface area and thus possibly a high sensitivity.

The polypropylene microfibers that were available were not conductive and therefore had to be coated with polypyrrole, co-polymerized with 3-thiophene acetic acid (3TAA), and treated with Fe(III)chloride ($FeCl_3$) and 5-sulfosalicylic acid (5SSA), to make it conductive. Lysozyme was then cross-linked to the microfibers by using glutaraldehyde [127]. A high magnification SEM image of the conductive microfiber is shown in Figure 7.31(a) and of the conductive fiber coated with glutaraldehyde in Figure 7.31(b).



(a) **(b)**

Figure 7.31: A 272× magnification SEM image of the **(a)** conductive microfiber, and **(b)** the conductive fiber coated with glutaraldehyde. From [127].

A mounting block was designed and 3D printed for the 3×3 cm electrotextile biosensor. A schematic of the mounting block and resistance measurement setup is shown in Figure 7.32.

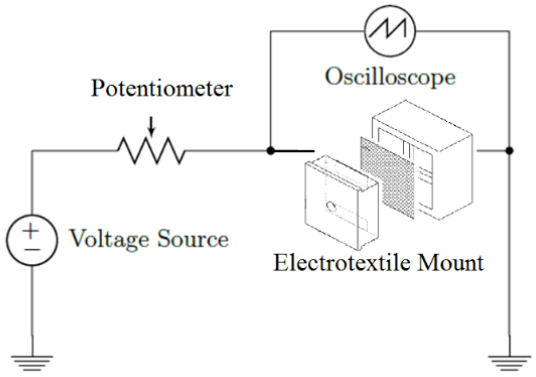


Figure 7.32: Schematic presentation of the mounting block and resistance measurement setup. From [127].

To verify the functionality of the biosensor, resistance measurements were made for lysozyme-coated microfiber preparations, exposed to various concentrations of antibodies. The measured results are shown in Figure 7.33.

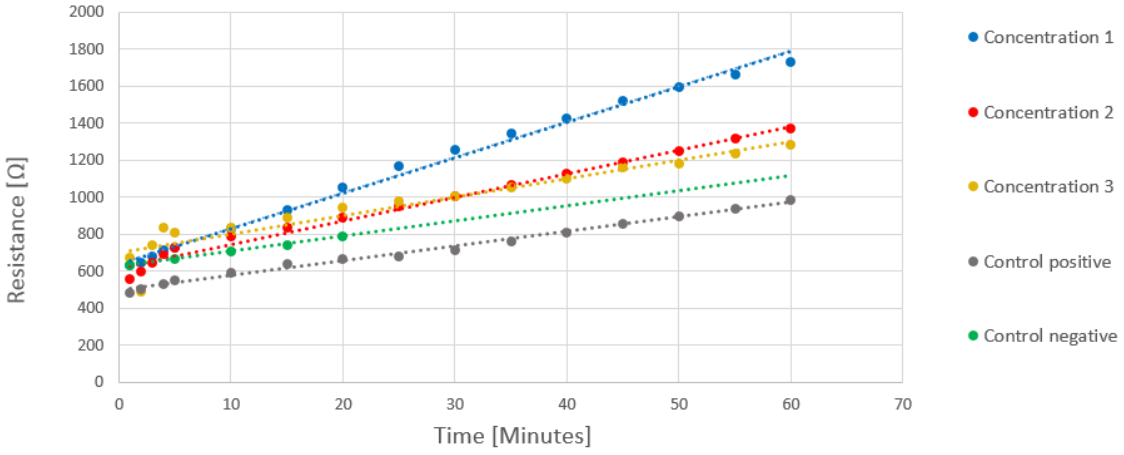


Figure 7.33: Measured resistance of electrotextile biosensensor against time for different antibody concentrations. From [127].

Concentration 1 (62.72 μg; 1:100 antibody dilution) resulted in an average trendline of $y = 19.203x638.25$, Concentration 2 (3.16 μg; 1:10 000 antibody dilution) showed an average trendline of $y = 12.775x + 617.39$ and Concentration 3 (0.16 μg; 1:100 000 diluted antibody) a trendline of $y = 10.046x + 698.71$.

These results were compared with measurements of an electrotextile that was not treated with any antibody (negative control test) and an electrotextile treated with a non-specific

antibody (positive control). The trendlines for the positive and negative control tests were $y = 7.9448x + 495.41$ and $y = 8.2199x + 623.19$, respectively.

An initial increase in resistance was recorded for each of the prepared fiber sets immediately after the antibody had been added. This clearly indicates that the positive detection of antibodies can be achieved. A marked difference between adding a concentration of as low as 1:100 000 (0.8 μg/ml) and the negative control test confirmed that the electrotextile biosensors were exceptionally sensitive to even small amounts of antibody.

The fact that there was a clear distinction between the trendline of the positive control test (non-specific antibodies) and the specific antibody concentrations, confirmed that only specific binding between the lysozyme and the antibodies resulted in a positive indication of the presence of antibodies, thus verifying the specificity of the biosensor.

During the latter part of 2015 we were able to attract some funding (∼R420 000) from the *Technology Innovation Agency* (TIA) to develop a prototype handheld point-of-care device based on our developed transducer technology. It was decided to use the resistive electrotextile biosensor technology and develop the prototype for the specific detection of *Escherichia coli* (*E. coli*) bacteria. The sensor was extensively tested for sensitivity, repeatability and specificity and very good results were obtained. The results have not been published yet, but a journal article is in process.

We have also made significant progress in using paper as the resistive transducer, instead of electrospun microfiber. Preliminary results, also using lysozyme, are shown in Figure 7.34. The change in resistance, relative to the baseline resistance, was measured for different antibody dilutions. Positive and negative control tests were also done, by using non-specific antibodies and PBS, respectively.

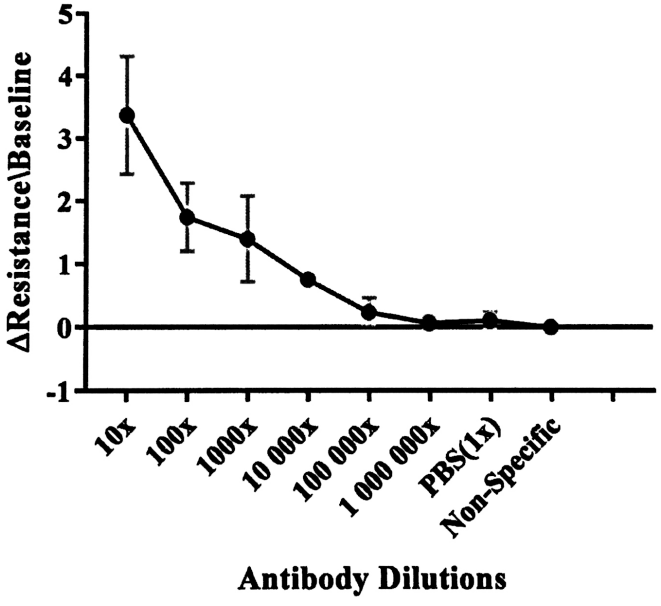


Figure 7.34: Measured resistance of paper based biosensor for different antibody dilutions and controls. From [128].

As can be seen from the results, a notable increase in resistance was observed for dilutions down to 100 000×. A limit of detection (LOD) was calculated as 100 ng/ml. It was also clear that negligible responses were observed for both the negative and positive control tests. This confirmed that the sensor only reacted to, in this case, a lysozyme-specific antibody, thus verifying the specificity of the sensor.

A patent has been filed by Stellenbosch University, which describes the use of either electrospun microfiber or paper as transducer for a handheld biosensor [129].

We have started collaboration with researchers at the Faculty of Health Sciences at Stellenbosch University with regard to the development of biosensors for the detection of viral infections (HIV) and also TB. Apart from our continuing collaboration with the Department of Microbiology in the Faculty of Science, we are also part of a team that is looking at the measurement of autophagy flux, a topic that has suddenly attracted a lot of attention due to the Nobel Prize for Medicine for 2016 being awarded to Yoshinori Ohsumi for his discoveries of mechanisms for autophagy.

7.4 Summary

In this chapter the research transition from superconducting technology to nano-devices and sensors was described.

The work by postgraduate student, Stanley van den Heever [105, 111, 106, 110, 112, 114, 117, 118, 120], was influential in the direction that the research effort evolved towards. It was this serendipitous stimulus that steered the work in the direction of biosensors.

Our research on biosensors is strongly reliant on multidisciplinary collaboration and here Prof Leon Dicks was instrumental in opening the new and exciting world of bacteria and viruses, and the multitude of possibilities with regard to new applications. I was blessed to be involved with a new breed of multidisciplinary research students, such as Deon Neveling [122, 123, 125], Michael Maas [126], Christiaan Viviers [127], Nick Lawrenson and Giles Maybery [128].

This journey is still in progress.

Chapter 8

Final Conclusion

My research career started in 1982, when I joined the Department of Electrical and Electronic Engineering at Stellenbosch University.

In a sense the choice of a research direction was influenced by a serendipitous opportunity to do postgraduate work in microelectronics, thanks to Professor Christo Viljoen. This led to a microelectronics research path that included my PhD on high-voltage diodes and the work on Monte Carlo particle analysis and high-frequency diode design.

The next chapter in my career can also be attributed to a serendipitous conversation in our microelectronics laboratory with Dr Karl Gehring in 1987, planting the seed of a sabbatical at *GEC Hirst Research Centre* in London. This is where superconducting devices became part of my life.

The superconductivity journey has been a most fulfilling experience. I was blessed to meet some extraordinary people that had a marked influence on my life, such as Professor Theodore Van Duzer, Mark Jeffery, Oleg Mukhanov, Steve Kaplan, John Przybysz, Nobuyuki Yoshikawa and Kazuo Saitoh, to name just a few. I was also privileged to meet some of them on home turf in South Africa. This included a typical South African braai with Yoshi at my home in Somerset West, and a braai with Oleg and Steve at Keurboomstrand, after Oleg swam the Indian Ocean in the middle of winter, and Steve shared his wonderful Woodstock (the real one) stories.

Our limit resources was influential in the decision to also start looking at non-superconducting devices. Here the focus of our current research was noticeably influenced by another serendipitous conversation with Leon Dicks, which put us on our current biosensor research path.

Rugby legend, Danie Craven, was once asked what he believed the most important aspect of good scrummaging was. He stated that three things were very important and that it was "push, push and push". If that question is rephrased to "good research" instead of "good scrummaging", my answer would definitely be "students, students and students". I was privileged to supervise some exceptional students, as was mentioned in this dissertation. I have learnt, and is still learning, so much from them.

Throughout my research journey the golden thread was always microelectronic devices –

semiconductor, superconductor, biological, or a combination. This dissertation is an attempt to contextualize that microelectronic device journey.

Bibliography

[1] "Development of the HP-35, the First Handheld Scientific Calculator, 1972." [Online]. Available: http://ethw.org/Milestones:Development_of_the_HP-35,_the_First_Handheld_Scientific_Calculator,_1972

[2] Perold, W.J., "The Design of Semiconductor High-Voltage Diodes," Ph.D. dissertation, Stellenbosch University, 1986.

[3] Kokosa, R.A. and Davies, R.L., "Avalanche Breakdown of Diffused Silicon p-n Junctions," *IEEE Trans. Electron Devices*, vol. 13, no. 12, pp. 874–881, 1966.

[4] Perold, W.J., "Novel method for calculating maximum bulk electric field in high-voltage diodes with large negative bevel angles," *Electron. Lett.*, vol. 21, no. 13, pp. 576–577, 1985.

[5] Perold, W.J., "Calculation of maximum bulk electric field in high-voltage diodes with small and intermediate negative bevel angles," *Electron. Lett.*, vol. 21, no. 25, pp. 1191–1192, 1985.

[6] Ghandi, S.K., *Semiconductor Power Devices: Physics of Operation and Fabrication Technology*, 1st ed. John Wiley & Sons, 1977.

[7] Keppke, K.D., Perold, W.J. and van der Walt, P.W., "A high performance four port PIN diode switch for television broadcasting applications," *IEEE Trans. Broadcast.*, vol. 34, no. 3, pp. 331–335, 1988.

[8] Mumford, W.W., "Tables of Stub Admittances for Maximally Flat Filters Using Shorted Quarter-Wave Stubs," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-13, pp. 695–696, 1965.

[9] Conradie, G. and Perold, W.J., "A comparison of various one-dimensional algorithms for the accurate simulation of IMPATT diodes," *SA J. Phys.*, vol. 16, no. 1/2, pp. 115–117, 1993.

[10] Kurosawa, T., "Monte Carlo calculation of hot-electron problems," *J. Phys. Soc. Jpn.*, vol. 21, p. 424, 1966.

[11] Van Zyl, R.R. , Perold, W.J. and Grobler, H., "An efficient parallel implementation of the Monte Carlo particle simulation technique on a network of personal computers," *Int. J. Numer. Model. Electron. Networks, Devices Fields*, vol. 13, pp. 369–380, 2000.

[12] Van Zyl, R.R., "The optimisation of mm-wave GaAs Gunn diodes using a parallel implementation of the Monte Carlo particle simulation technique," Ph.D. dissertation, Stellenbosch University, 2006.

[13] Tomizawa, K., *Numerical Simulation of Submicron Semiconductor Devices*. London: Artech House, 1993.

[14] Van Zyl, R.R., Perold, W.J. and Botha, R., "The Gunn-diode: Fundamentals and fabrication," in *Proc. 1998 South African Symp. Commun. Signal Process.*, Cape Town, South Africa, 1998, pp. 407–412.

[15] Tully, J.W., "Monte Carlo simulation of a millimeter-wave Gunn-effect relaxation oscillator," *IEEE Trans. Electron Devices*, vol. 30, no. 6, pp. 566–571, 1983.

[16] Francis, S., van Zyl, R. R. and Perold, W. J., "An empirical determination of upper operational frequency limits of transferred electron mechanism in bulk GaAs and GaN through ensemble Monte Carlo particle simulations," *Indian J. Phys.*, vol. 89, no. 8, pp. 825–828, 2015.

[17] Keppke, K.D., "The analysis and design of a microwave avalanche diode," Master's thesis, Stellenbosch University, 1988.

[18] Conradie, G., "Efficient computer algorithms for the simulation of IMPATT diode," Master's thesis, Stellenbosch University, 1991.

[19] Van Zyl, R.R., "The Monte Carlo particle simulation technique," Master's thesis, Stellenbosch University, 1994.

[20] Bednorz, J.G. and Müller, K.A., "Possible high T_c superconductivity in the Ba-La-Cu-O system," *Z. Phys. B*, vol. 64, no. 1, pp. 189–193, 1986.

[21] Taylor, B.N., "A study of some electron tunnelling phenomena in superconductors and magnetotunnelling in InAs Esaki diodes," Ph.D. dissertation, University of Pennsylvania, 1963.

[22] Blonder, G. E. and Tinkham, M., "Metallic to tunneling transition in Cu-Nb point contacts," *Phys. Rev. B*, vol. 27, pp. 112–118, 1983.

[23] Octavio, M., Tinkham, M., Blonder, G. E. and Klapwijk, T. M., "Subharmonic energy-gap structure in superconducting constrictions," *Phys. Rev. B*, vol. 27, pp. 6739–6746, 1983.

[24] Tinkham, M. and Clarke, J., "Theory of Pair-Quasiparticle Potential Difference in Nonequilibrium Superconductors," *Phys. Rev. Lett.*, vol. 28, pp. 1366–1369, 1972.

[25] Perold, W.J., "A Laplace solution of the Bogoliubov equations applied to a normal metal/superconductor interface," *Supercond. Sci. Technol.*, vol. 1, no. 3, pp. 128–131, 1988.

[26] Bardeen, J., Cooper, L. N. and Schrieffer, J. R., "Microscopic Theory of Superconductivity," *Phys. Rev.*, vol. 106, pp. 162–164, 1957.

[27] Blonder, G. E., Tinkham, M. and Klapwijk, T. M., "Transition from metallic to tunneling regimes in superconducting microconstrictions: Excess current, charge imbalance, and supercurrent conversion," *Phys. Rev. B*, vol. 25, pp. 4515–4532, 1982.

[28] Perold, W.J., "A computer model for the simulation of quasiparticle injection and detection in superconducting double-junction geometries," *Supercond. Sci. Technol.*, vol. 1, no. 5, pp. 232–238, 1989.

[29] Shapiro, S., Smith, P.H., Nicol, J., Miles, J.L. and Strong, P.F., "Superconductivity and Electron Tunneling," *IBM J. Res. Dev.*, vol. 6, no. 1, pp. 34–43, 1962.

[30] Rothwarf, A. and Taylor, B.N., "Measurement of Recombination Lifetimes in Superconductors," *Phys. Rev. Lett.*, vol. 19, pp. 27–30, 1967.

[31] Wong, T., Yeh, J.T.C. and Langenberg, D.N., "Controllable superconducting weak links," *IEEE Trans. Magn.*, vol. MAG-13, no. 1, pp. 743–746, 1977.

[32] Owen, C. S. and Scalapino, D. J., "Superconducting State under the Influence of External Dynamic Pair Breaking," *Phys. Rev. Lett.*, vol. 28, pp. 1559–1561, 1972.

[33] Perold, W.J., "Non-equilibrium quasiparticle processes in superconductor tunnelling structures," *Trans. SAIEE*, vol. 81, no. 2, pp. 53–58, 1990.

[34] Gray, K.E., "A Superconducting Transistor," *Appl. Phys. Lett.*, vol. 32, pp. 392–395, 1978.

[35] Perold, W.J., "Computer simulation of the superconducting Gray transistor," *Supercond. Sci. Technol.*, vol. 2, no. 3, pp. 202–205, 1989.

[36] Iguchi, I., "Study of the nonequilibrium state of superconductors by large quasiparticle injection from an external current source," *Phys. Rev. B*, vol. 16, pp. 1954–1968, 1977.

[37] Kaplan, S.B., Chi, C.C., Langenberg, D.N., Chang, J.J., Jafarey, S. and Scalapino, D.J., "Quasiparticle and phonon lifetimes in superconductors," *Phys. Rev. B*, vol. 14, pp. 4854–4873, 1976.

[38] Smith, L.N. and Mochel, J.M., "Phonon and Quasiparticle Dynamics in Superconducting Aluminum Tunnel Junctions," *Phys. Rev. Lett.*, vol. 35, pp. 1597–1600, 1975.

[39] Perold, W.J., "Superconducting Gray transistor with temperature-insensitive current gain," *Electron. Lett.*, vol. 25, no. 2, pp. 146–148, 1989.

[40] Perold, W.J., "Superconductive three-terminal devices utilizing quasiparticle tunnelling'," *Trans. SAIEE*, vol. 81, no. 2, pp. 43–47, 1990.

[41] De Kock, P.D., "Electronic simulation of Josephson junction," Master's thesis, Stellenbosch University, 1990.

[42] Powell, I.A., "The simulation and design of a superconducting DC SQUID linear magnetic flux detector system," Master's thesis, Stellenbosch University, 1993.

[43] Maritz, E.J., "Superconducting three-terminal devices," Master's thesis, Stellenbosch University, 1994.

[44] Van der Merwe, E.F., "The use of SQUIDs for the measurement of brain and muscular activity," Master's thesis, Stellenbosch University, 1995.

[45] Perold, W.J., "Superconducting Quantum Interference Devices," *Trans. SAIEE*, vol. 83, no. 1, pp. 24–31, 1992.

[46] Jeffery, M., Van Duzer, T., Kirtley, J.R. and Ketchen, M.B., "Magnetic imaging of moat-guarded superconducting electronic circuits," *Appl. Phys. Lett.*, vol. 67, no. 12, pp. 1769–1771, 1995.

[47] Fujimaki, N., Kotani, S., Imamura, T. and Hasuo, S, "Josephson Modified Variable Threshold Logic Gates for Use in Ultra-High-Speed LSI," *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 433–446, 1989.

[48] Fang, E.S., Hebert, D. and Van Duzer, T., "A multigigahertz Josephson flash A/D converter with a pipelined encoder using large-dynamic-range current-latch comparators," *IEEE Trans. Magn.*, vol. 27, pp. 2891–2894, 1991.

[49] Luong, H., Hebert, D. and Van Duzer, T., "Fully parallel superconducting analog-to-digital converter," *IEEE Trans. Appl. Supercond.*, vol. 3, pp. 2633–2636, 1993.

[50] Perold, W.J., Jeffery, M., Wang, Z. and Van Duzer, T., "Complementary Output Switching Logic – A New Supercoducting Voltage-State Logic Family," *IEEE Trans. Appl. Supercond.*, vol. 6, no. 3, pp. 125–131, 1996.

[51] Spence, R. and Soin, R.S., *Tolerance Design of Electronic Circuits*. New York: Addison-Wesley, 1988, pp. 56–87.

[52] Perold, W.J., Jeffery, M., Wang, Z. and Van Duzer, T., "Complementary Output Switching Logic - A new superconducting ultra high speed voltage state logic family," in *Biannual American Workshop on Superconducting Electronics*, Farmington, Pennsylvania, 1995.

[53] Jeffery, M., Perold, W. J. and Van Duzer, T., "Superconducting complementary output switching logic operating at 5-10 Gb/s," *Appl. Phys. Lett.*, vol. 69, no. 18, pp. 2746–2748, 1996.

[54] Jeffery, M., Perold, W.J. and Van Duzer, T., "Experimental demonstration of complementary output switching logic approaching 10 Gb/s clock frequencies," *IEEE Trans. Appl. Supercond.*, vol. 7, no. 2, pp. 2665–2668, 1997.

[55] Jeffery, M., Van Duzer, T. and Perold, W. J., "Superconducting complementary output switching logic circuits operating at 10–18 GHz," in *The American Physical Society March Meeting*, Los Angeles, California, 1998.

[56] Jeffery, M., Perold, W.J. and Van Duzer, T., "Monte Carlo optimization of superconducting Complementary Output Switching Logic circuits," *IEEE Trans. Appl. Supercond.*, vol. 8, no. 3, pp. 104–119, 1998.

[57] Gaj, K., Herr, Q.P. and Feldman, M.J., *Applied Superconductivity*. U.K.: Inst. Physics, 1995, ch. Parameter variations and synchronization of RSFQ circuits, pp. 1733–1736.

[58] Polonsky, S., SUNY Stony Brook, private communication.

[59] Wang, Z., Jeffery, M., Perold, W.J. and Van Duzer, T., "High-speed demonstration of a super-conducting pseudo-random bit-sequence generator," *IEEE Trans. Appl. Supercond.*, vol. 10, no. 2, pp. 1593–1597, 2000.

[60] Likharev, K.K. and Semenov, V.K., "RSFQ Logic/Memory Family: A New Josephson Junction Technology for Sub-Terahertz Clock Frequency Digital Systems," *IEEE Trans. Appl. Supercond.*, vol. 1, pp. 3–27, 1991.

[61] Suzuki, H., Inoue, A., Imamura, T. and Hasuo, S., "A Josephson driver to interface Josephson junctions to semiconductor transistors," in *Technical Digest of the International Electron Device Meeting*, San Francisco, California, 1988.

[62] Perold, W.J., Jeffery, M. and Van Duzer, T., "Synchronous Superconducting Amplifier Circuits for 5 – 10 GHz Applications," in *IEEE Applied Superconductivity Conference*, Palm Desert, California, 1998.

[63] Perold, W.J. and Jeffery, M., "Synchronous 5-10 Gb/s digital superconducting amplifier circuits fabricated with a horseshoe architecture," in 7^{th} *International Superconductive Electronics Conference*, Berkekely, California, 1999.

[64] Whiteley Research Inc., 456 Flora Vista Avenue, Sunnyvale, CA 94086. [Online]. Available: http://www.srware.com/

[65] Perold, W.J. and Fourie, C.J., "Modeling superconducting components based on the fabrication process and layout dimensions," *IEEE Trans. Appl. Supercond.*, vol. 11, no. 1, pp. 345–348, 2001.

[66] Synopsys, Inc., 700 East Middlefield Road, Mountain View, CA 94043. [Online]. Available: http://www.synopsys.com/

[67] HYPRES, 175 Clearbrook Road, Elmsford, New York, 1052. [Online]. Available: http://www.hypres.com/

[68] Fourie, C.J., "A 10 GHz oversampling Delta modulating analogue-to-digital converter implemented with hybrid superconducting digital logic," Master's thesis, Stellenbosch University, 2001.

[69] Gross, P.A., "Rapid Single Flux Quantum Very Large Scale Integration," Master's thesis, Stellenbosch University, 2002.

[70] Gross, P.A. and Perold, W.J., "Rapid Single Flux Quantum (RSFQ) Programmable Gate Array," Patent number: 2002/7825.

[71] Fourie, C.J. and Perold, W.J., "Comparison of genetic algorithms to other optimization techniques for raising circuit yield in superconducting digital circuits," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 511–514, 2003.

[72] Fourie, C.J. and Perold, W.J., "Yield optimization of high frequency superconducting digital circuits with genetic algorithms," *Trans. SAIEE*, vol. 94, pp. 11–7, 2003.

[73] Fourie, C.J., "A Tool Kit for the Design of Superconducting Programmable Gate Arrays," Ph.D. dissertation, Stellenbosch University, 2003.

[74] Fourie, C.J. and Perold, W.J., "On using finite segment methods and images to establish the effect of gate structures on inter-junction inductances in RSFQ circuits," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 539–542, 2003.

[75] Kamon, M., Tsuk, M.J. and White, J.K., "FastHenry: A multipole-accelerated 3-D inductance extraction program," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 9, pp. 1750–1758, 1994.

[76] Fourie, C.J. and Perold, W.J., "Reflection plane placement in numerical inductance calculations using the method of images for thin-film superconducting structures," *Trans. SAIEE*, vol. 94, pp. 18–24, 1993.

[77] Teh, C.K., Kitagawa, M. and Okabe, Y., "Inductance calculation of 3D superconducting structures with ground plane," *Supercond. Sci. Technol.*, vol. 12, pp. 921–924, 1999.

[78] Fourie, C.J. and Perold, W.J., "Simulated inductance variations in RSFQ circuit structures," *IEEE Trans. Appl. Supercond.*, vol. 15, pp. 300–303, 2005.

[79] Fourie, C.J., Perold, W.J. and Gerber, H.R., "Complete Monte Carlo model description of lumped-element RSFQ logic circuits," *IEEE Trans. Appl. Supercond.*, vol. 15, pp. 384–387, 2005.

[80] Fourie, C.J. and Perold, W.J., "An RSFQ DC-resettable latch for building memory and reprogrammable circuits," *IEEE Trans. Appl. Supercond.*, vol. 15, pp. 348–351, 2005.

[81] Fourie, C.J. and Perold, W.J., "A single-clock asynchronous input COSL set-reset flip-flop and SFQ to voltage state interface," *IEEE Trans. Appl. Supercond.*, vol. 15, pp. 263–266, 2005.

[82] Hebard, A., Pei, S., Dunkleberger, L. and Fulton, T., "A DC-powered Josephson flip-flop," *IEEE Trans. Magn.*, vol. 15, no. 1, pp. 408–411, 1979.

[83] Schneider, D.F., Lin, J.C., Polonsky, S.V. and Semenov, V.K., "Broadband interfacing of superconducting digital systems to room tempera-ture electronics," *IEEE Trans. Appl. Supercond.*, vol. 5, no. 2, pp. 3152–3155, 1995.

[84] Gerber, H.R., Fourie, C.J. and Perold, W.J., "Specification of a technology portable logic cell library for RSFQ: An automated approach," *IEEE Trans. Appl. Supercond.*, vol. 15, pp. 368–371, 2005.

[85] Gerber, H.R., Fourie, C.J. and Perold, W.J., "RSFQ-Asynchronous Timing (RSFQ-AT): A new design methodology for implementation in CAD automation," *IEEE Trans. Appl. Supercond.*, vol. 15, pp. 272–275, 2005.

[86] Herr, Q.P. and Bunyk, P., "Implementation and application of first-in first-out buffers," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 563–566, 2003.

[87] Herr, Q.P., Vukovic, N., Mancini, C.A., Gaj, K., Ke, Q., Adler, V., Friedman, E.G., Krasniewski, A., Bocko, M.F. and Feldman, M.J., "Design and low speed testing of a four-bit RSFQ multiplier-accumulator," *IEEE Trans. Appl. Supercond.*, vol. 7, no. 2, pp. 3168–3171, 1997.

[88] Gerber, H.R., Fourie, C.J., Perold, W.J. and Müller, L.C., "Design of an asynchronous microprocessor using RSFQ-AT," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 490–493, 2007.

[89] Gerber, H.R., Fourie, C.J. and Perold, W.J., "Investigating the requirements on CAD tools for the development of VLSI RSFQ circuits," in *IEEE Applied Superconductivity Conference*, Jacksonville, Florida, 2004.

[90] Hardie, G.L., Büttner, U. and Perold, W.J., "The Enhancement of Superconducting $YBa_2Cu_3O_{7-x}$ Thin Films by Electric Field Application During Deposition," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 3387–3390, 2009.

[91] CST EM Studio 2006B, Darmstadt, Germany, CST Computer Simulation Technology. [Online]. Available: http://www.cst.com/

[92] Van Staden, W.F., Büttner, U., Srinivasu, V.V. and Perold, W.J., "A novel buffered high-T_c superconducting step-edge Josephson junction," *Supercond. Sci. Technol.*, vol. 20, no. 11, pp. S419–S425, 2007.

[93] Wu, C.H., Chen, M.J., Chen, J.C., Chen, K.L., Yang, H.C., Hsu, M.S., Lai, T.S., Tsai, Y.S., Horng, H.E., Chen, J.H. and Jeng, J.T., "High quality step-edge substrates for high-T_c superconducting devices," *Rev. Sci. Instrum.*, vol. 77, no. 3, p. 033901, 2006.

[94] Büttner, U., Hardie, G.L., Rossouw, R., Srinivasu, V.V. and Perold, W.J., "Fabrication of submicron YBCO Josephson junctions by a sample mosaic navigation assisted laser etching process," *Supercond. Sci. Technol.*, vol. 20, no. 11, pp. S426–S429, 2007.

[95] Elkaseh, A.A.O., Büttner, U., Meincken, M., Hardie, G.L., Srinivasu, V.V. and Perold, W.J., "Nanoplough–Constrictions on Thin YBCO Films Made with Atomic Force Microscopy," *J. Nanosci. Nanotechnol.*, vol. 7, no. 9, pp. 3348–3349, 2007.

[96] Elkaseh, A.A.O., Srinivasu, V.V. and Perold, W.J., "Observation of Shapiro-steps in AFM-plough micron-size YBCO planar constrictions," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 187–190, 2009.

[97] Elkaseh, A.A.O., Perold, W.J. and Srinivasu, V.V., "AFM Nano-Plough Planar YBCO Micro-Bridges: Critical Currents and Magnetic Field Effects," *J. Nanosci. Nanotechnol.*, vol. 10, no. 10, pp. 6510–6513, 2010.

[98] Orlando, T.P. and Delin, K.A., *Foundations of Applied Superconductivity*. Addison-Wesley, 1990, p. 423.

[99] Elkaseh, A.A.O., Perold, W.J. and Srinivasu, V.V., "Josephson nanoconstrictions made by AFM plowing of $YBa_2Cu_3O_{7-x}$ films," *J. Appl. Phys.*, vol. 108, no. 5, p. 053914, 2010.

[100] Büttner, U., "The Development of Equipment for the Fabrication of Thin Film Superconductor and Nano Structures," Master's thesis, Stellenbosch University, 2011.

[101] De Villiers, H.A.C., "A process for the manufacture of high temperature bi-epitaxial Josephson junctions," Master's thesis, Stellenbosch University, 2007.

[102] Van Staden, W.F., "The fabrication of PBCO buffered step-edge Josephson junctions," Master's thesis, Stellenbosch University, 2007.

[103] Elkaseh, A.A.O., "Fabrication of Superconducting Circuits using AFM," Master's thesis, Stellenbosch University, 2006.

[104] Elkaseh, A.A.O., "Fabrication of Josephson junctions using AFM Nanolithography," Ph.D. dissertation, Stellenbosch University, 2010.

[105] Van den Heever, T.S., "A Zinc Oxide Nanowire Pressure Sensor," Master's thesis, Stellenbosch University, 2010.

[106] Van den Heever, T. S., Perold, W.J. and Büttner, U., "A Zinc Oxide Nanowire Pressure Sensor," *Nanosci. Nanotechnol. Lett.*, vol. 2, pp. 203–207, 2010.

[107] Zhao, Q.X., Klason, P. and Willander, M., "Growth of ZnO nanostructures by vapor–liquid–solid method," *Appl. Phys. A*, vol. 88, no. 1, pp. 27–30, 2007.

[108] Comsol Multiphysics, Burlington, USA. [Online]. Available: http://www.comsol.com/

[109] Vayssieres, L., Keis, K., Lindquist, S-E. and Hagfeldt, A., "Purpose-Built Anisotropic Metal Oxide Material: 3D Highly Oriented Microrod Array of ZnO," *J. Phys. Chem. B*, vol. 105, no. 17, pp. 3350–3352, 2001.

[110] Van den Heever, T. S., Büttner, U. and Perold, W.J., "A novel method to measure the generated voltage of a ZnO nanogenerator." *Nanotechnology*, vol. 22, no. 39, p. 395204, 2011.

[111] Van den Heever, T.S., "Development and optimisation of a zinc oxide nanowire nanogenerator," Ph.D. dissertation, Stellenbosch University, 2013.

[112] Van den Heever, T. S. and Perold, W.J., "The influence of resistance and carrier concentration on the output voltage of a ZnO nanogenerator," *Micro Nano Syst. Lett.*, vol. 1, p. 4, 2013.

[113] Van der Pauw, L.J., "A method of measuring the resistivity and Hall coefficient on lamellae of arbitary shape," *Philips Tech. Rev.*, vol. 20, pp. 220–224, 1958.

[114] Van den Heever, T. S. and Perold, W.J., "The performance of nanogenerators fabricated on rigid and flexible substrates," *Microelectron. Eng.*, vol. 112, pp. 41–45, 2013.

[115] Baek, S.S. and Fearing, S.F., "Reducing Contact Resistance Using Compliant Nickel Nanowire Arrays," *IEEE Trans. Compon. Packag. Technol.*, vol. 31, no. 4, pp. 859–868, 2008.

[116] Xu, S., Qin, Y., Xu, C., Wei, Y., Yang, R. and Wang, Z.L., "Self-powered nanowire devices," *Nat. Nanotechnol.*, vol. 5, pp. 366–373, 2010.

[117] Van den Heever, T. S. and Perold, W.J., "Improving the output voltage of a ZnO nanogenerator by adding CNTs and lateral ZnO nanowires," *IEEE Trans. Nanotechnol.*, vol. 12, no. 6, pp. 1012–1017, 2013.

[118] Van den Heever, T. S. and Perold, W.J., "Comparing three different energy harvesting circuits for a ZnO nanowire based nanogenerator," *Smart Mater. Struct.*, vol. 22, no. 10, p. 105029, 2013.

[119] Lallart, M. and Guyomar, D., "An optimized self-powered switching circuit for nonlinear energy harvesting with low voltage output," *Smart Mater. Struct.*, vol. 17, no. 3, p. 035030, 2008.

[120] Van den Heever, T.S., Hardie, G.L. and Perold, W.J., "ZnO nanowire gas sensor with UV-light for improved sensitivity Research," *Int. J. Nano Stud. Technol.*, vol. II, no. 1, pp. 1–6, 2013.

[121] Kind, H., Yan, H., Messer, B., Law, M. and Yang, P., "Nanowire Ultraviolet Photodetectors and Optical Switches," *Adv. Mater.*, vol. 14, no. 2, pp. 158–160, 2002.

[122] Neveling, D.P., van den Heever, T.S., Bucher, R., Perold, W.J. and Dicks, L.M.T., "Effect of Seed Layer Deposition , Au Film Layer Thickness and Crystal Orientation on the Synthesis of Hydrothermally Grown ZnO Nanowires," *Curr. Nanosci.*, vol. 10, pp. 827–836, 2014.

[123] Neveling, D.P., van den Heever, T.S., Perold, W.J. and Dicks, L.M.T., "A nanoforce ZnO nanowire-array biosensor for the detection and quantification of immunoglobulins," *Sensors Actuators B Chem.*, vol. 203, pp. 102–110, 2014.

[124] Shrivastava, A. and Gupta, V.B., "Methods for the determination of limit of detection and limit of quantitation of the analytical methods," *Chron. Young Sci .*, vol. 2, no. 1, pp. 21–25, 2011.

[125] Dicks, L.M.T, Perold, W.J., Neveling, D. and van den Heever, T.S., "Nanowire-array biosensor," Patent application number: PCT/IB2014/065765.

[126] Maas, M.B., Perold, W.J., Dicks, L.M.T. and Neveling. D., "Immobilization of primary antibodies on borosilicate glass fibers for use in a fiber-optic biosensor," *Sensors Actuators B Chem.*, 2016 (Submitted for publication).

[127] Viviers, C.G.A., Perold, W.J., Maas, M.B., Neveling, D. and Dicks, L.M.T., "A conductive microfiber biosensor for the detection of antibodies," *Sensors*, 2016 (Submitted for publication).

[128] Maybery, H.C.M, "Design and fabrication of a paper-based biosensor," Stellenbosch University, Final year project report, 2016.

[129] Viviers, C.G.A., Perold, W.J., Dicks, L.M.T. and Maybery, G.H.C., "A device for the detection of biomolecules," Ref No: P3140ZA00.