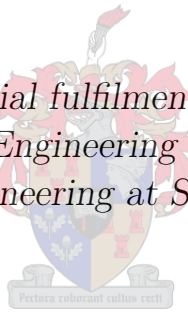
Adaptive Noise and Interference Cancellation for Mobile Communications.

by

Jason Bonarius



Thesis presented in partial fulfilment of the requirements for the degree of Master of Engineering (Electric and Electronic) in the Faculty of Engineering at Stellenbosch University

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December 2016

Declaration

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Acknowledgements

First and foremost, I would like to thank my study leader, Prof. J.B. de Swardt, for his great support and feedback through every step of the project.

To Dr. Cornell van Niekerk for his insight and support during my visit at GEW and throughout the entire project.

A thank you to Wessel Croukamp for all that I learned from him, as well as his help in the assembly of project components.

I would like to extend my gratitude to Anneke Stofberg for always being available to help.

I thank my mother Zenobia for her unwavering support throughout my entire career. Her guidance and care have made my achievements possible.

To Luzanne Labuschagne, for her everyday love, support and encouragement.

Abstract

In an arena of electronic warfare measures, to inhibit enemy operations as well as provide safety for allied forces from radio triggered explosive devices, interference and noise coupling degrade allied communications severely. In an attempt to allow for communications to occur uninterrupted while maintaining electronic warfare capabilities, a noise and interference cancellation system is to be investigated and developed, whereby wave superposition principles are to used to adaptively provide noise and interference cancellation.

Opsomming

In ’n arena van elektroniese oorlogvoering maatreëls, om die vyand bedrywighede te belemmer, asook veiligheid te verskaf vir geallieerde magte teen radio ploftoestelle, word die kommunikasie vermoëns sterk belemmer. In ’n poging om voorsiening te maak vir kommunikasie om plaas te vind ononderbroke saam met aktiewe elektroniese oorlogvoering vermoëns, word ’n geraas en inmenging kansellasie stelsel ondersoek en ontwikkel, waardeur golf superposisie beginsels gebruik word om geraas en inmenging kansellasie te voorsien.

Contents

Nomenclature

Symbols

G_P	Protection Circuit Gain
F_P	Protection Circuit Noise Figure
G_1	Coarse Coupler 1 through Gain
G_2	Cancel Error Coupler through Gain
G_3	Coarse Coupler 2 through Gain
G_A	Control Circuit Amplifier Gain
F_A	Control Circuit Amplifier Noise Figure
G_C	Summation Coupler Coupling Value
G_L	Coarse Attenuator Gain
F_L	Coarse Attenuator Noise Figure
G_Q	Quadrature Coupler Gain
F_Q	Quadrature Coupler Noise Figure
G_V	Vector Modulator Gain
F_V	Vector Modulator Noise Figure
G_{RX}	Receiver Gain
F_{RX}	Receiver Noise Figure
T_0	Noise Temperature
B_W	Bandwidth
k_B	Boltzmann Constant
G_{CAN}	Cascaded G_P, G_A, G_3, G_L, G_Q, and G_V Gain
F_{CAN}	Cascaded F_P, F_A, F_3, F_L, F_Q, and F_V Noise Figure
N_T	Total System Noise
$IP3_A$	Amplifier Third-Intercept Point
$IP3_L$	Attenuator Third-Intercept Point
$IP3_V$	Vector Modulator Third-Intercept Point
$IP3_{RX}$	Receiver Third-Intercept Point
$GINT$	Cascaded G_3, G_L and G_Q Gain

G_R	Cascaded G_3, G_L and G_Q Noise Figure
X_{IN}	Primary Input Noise Power
X_{REF}	Reference Input Noise Power
G_T	System Gain
G_e	Cancellation Block Gain
$OIP3_e$	Cancellation Block Output Third-Intercept Point
$IIP3_{RX}$	Receiver Input Third-Intercept Point
j	$j^2 = -1$
Z_0	Characteristic Impedance

Greek Symbols

θ	Theta in Degrees
$\sum$	Sum of Inputs
ω	Angular Frequency
t	Time
π	pi ≈ 3.14159
λ	wavelength
Ω	Unit of Resistance

Abbreviations

IED	Improvised Explosive Devices
SINAD	Signal to Interference, Noise and Distortion
RF	Radio Frequency
PA	Power Amplifier
SOI	Signal of Interest
FM	Frequency Modulated
UHF	Ultra High Frequency
SNR	Signal to Noise Ratio
NF	Noise Figure
DUT	Device Under Test
IMD	Inter-Modulation Distortion
FSPL	Free Space Propagation Loss
LNA	Low-Noise Amplifier
ADC	Analog to Digital Converter

DR	Dynamic Range
SFDR	Spurious Free Dynamic Range
LPF	Low-Pass Filter
HPF	High-Pass Filter
BPF	Band-Pass Filter
BSF	Band-Stop Filter
DC	Direct Current
ELS	Electronic Line Stretcher
VCO	Voltage Controlled Oscillator
I/Q	In-Phase/Quadrature
ESD	Electrostatic Discharge
ADS	Advanced Design Studio
IC	Integrated Circuit
RMS	Root Mean Square
LED	Light Emitting Diode
SPDT	Single-Pole Double-Throw
GPS	Ground Positioning System
IDE	Integrated Development Environment
CNC	Computer Numeric Code
VNA	Vector Network Analyser
PCB	Printed Circuit Board
DAC	Digital to Analog Converter
SINR	Signal to Interference and Noise
IP3	Third-order Intercept Point
IIP3	Input Third-order Intercept Point
OIP3	Output Third-order Intercept Point
P1dB	1 dB Gain Compression Point
SP4T	Single Pole 4-Throw
LO	Local Oscillator

Chapter 1

Introduction and Project Specification

1.1 Motivation and thesis topic

Active noise cancellation has a wide range of applications ranging from military applications to commercial telecommunications. Military operations include the ability to incapacitate enemy military communications and information relaying structures, as well as the detection and suppression of Improvised Explosive Device (IED) detonation [10].

In order to achieve these goals, large jamming signals are generated in the frequency band of the enemy signal of interest in order to saturate the receiver of the enemy communications or explosives, preventing communication or detonation. Sensitive, high speed receivers are incorporated into jamming systems allowing them to track these fast moving enemy communications and instantly jam the band in which the enemy forces are attempting to communicate. Generating sufficiently large jamming signals rely heavily on large power amplifiers. These power amplifiers generate large levels of noise and interference, in the band of operation, as well as out-of-band. Close proximity of the jamming systems to communications systems on a vehicle allows for large levels of noise coupling from the jamming system to the vehicle's own communications receiver. The coupling of high noise levels, jamming barrages, harmonics and spurious signals from the jamming systems greatly reduce the sensitivity of the vehicle's own communication receivers.

An adaptive cancellation system is required to actively cancel the noise levels from the jamming system in the on-board received communications channels. Anti-phase versions of the jamming system signals that are coupled to the receiver, will be generated and injected into the receiver. These anti-phase signals are to combine with the noise coupled from the jammer

antennae and result in cancellation. Constant adaption through the use of gain and phase control of the anti-phase cancellation signal will be performed in order to eliminate interference continuously in a dynamic environment [39; 40].

1.2 Objectives of this study

The objectives of the study are to research and evaluate adaptive cancellation systems and to construct a working, first iteration prototype model. The theory and basic concepts associated with cancellation are to be covered along with technology and topology choices available through current technologies, as well as novel approaches.

This first iteration proof of concept prototype is to be designed, constructed, and tested for its ability to cancel noise and interference. Mathematical analysis and physical testing will be performed in order to allow for optimised and improved system performance for a second iteration prototype.

1.3 Work overview

- Chapter 2 characterises the ideal phase and amplitude requirements for required transmission distances. It serves as a design performance guideline. Propagation and vector concepts are then mathematically combined and plotted in order to allow for the user to identify the maximum allowable phase and amplitude error tolerances of the cancellation signal in order to achieve a certain transmission distance in the presence of the jammer.
- Chapter 3 provides background knowledge to the reader by reviewing the basic theory concepts that are used throughout the text and associated with noise cancellation.
- Chapter 4 reviews numerous possible approaches for each of the main design sections required for a basic adaptive canceller system. The options are reviewed from where a first iteration build approach is chosen.
- Chapter 5 covers the design of each of the system main design blocks and all of the sub-circuits associated with each block. The simulated outputs as well as measured outputs of the sub-blocks components are displayed where possible. The complete build and the integration of all sub-design blocks are included.

- Chapter 6 assesses the implications of the canceller system on the noise figure and 3rd order inter-modulation interception points of the receiver. The noise of the canceller is assessed with optimisation of the component sequences and optimal coupling considered.
- Chapter 7 will be used to describe the different test setups and corresponding measurements and results.
- Chapter 8 discusses the results and draws conclusions on the design process and validity of the system. Future development approaches and considerations are also discussed.

1.4 Project Specifications

1.4.1 Section overview

The project specifications section presents the system as it currently performs and operates without a canceller system present. The current system setup, as well as the problem it faces, is described in further detail. Current system performance, for set hardware components, is provided and will be used as a reference for cancellation performance once the canceller has been implemented and tested.

1.4.2 Background

The project application regards mobile personnel carrier and strategic command vehicles for in-field military operations. These vehicles are designed with forward mounted communications antennas, while jamming antennas are mounted at the rear of the vehicle to allow for as much separation in order to minimise antenna coupling.

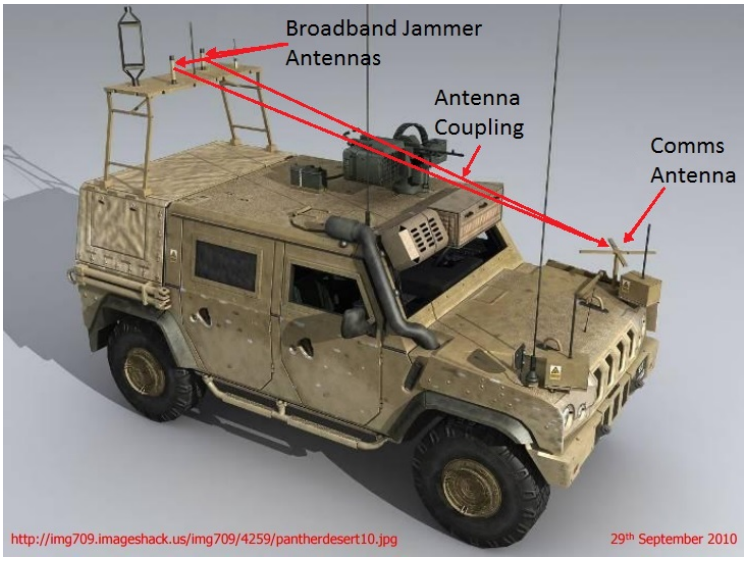

Figure 1.1: Vehicle antenna configuration demonstrating jammer coupling [3]

Signals received by the communications channels are inherently small due to the free space losses incurred through propagation from the distant sender to the forward mounted vehicle receiver antenna. (The jamming signals and noise signals generated by the rear mounted antennas are high power signals with little propagation loss over the distance from their source to the on-board communications receiver antennas, mere meters away.) Figure 1.1 illustrates the antenna proximity and the coupling between these antennas as a result of their proximity [3].

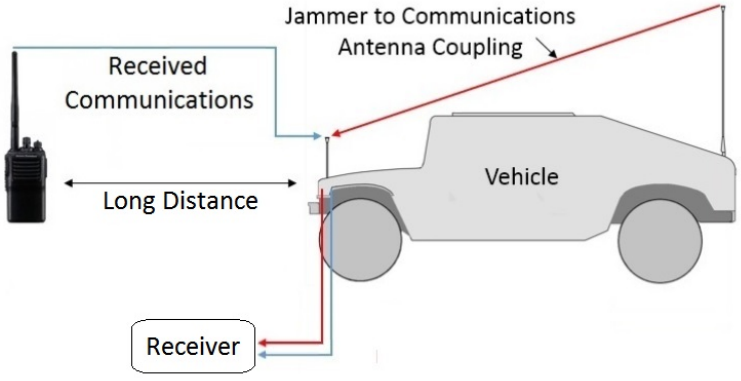

Figure 1.2: Description of internal signals as a result of wireless antenna coupling

The phenomenon in Figure 1.1 can be further described by the image in Figure 1.2. Here the signals from the jammer antennas, marked in red, are coupled over to the forward mounted antennas where they are received at the communications receiver alongside the low power communications signals, marked in blue. The interference signals overpower the communications signals, greatly limiting communication distance and reliability.

In order to alleviate the effects of interference in the communications channels, a canceller system is to be implemented as seen in Figure 1.3. The purpose of the canceller is to remove interference and allow for the communication signals to pass as would be the case if the jammer system was not present.

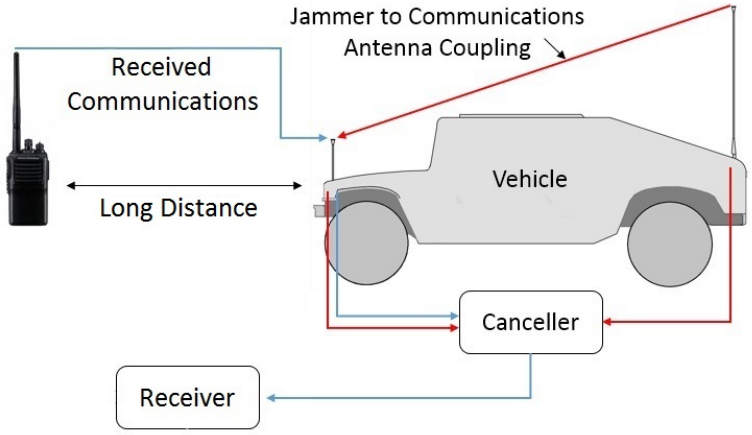

Figure 1.3: Cancellation concept implemented on a vehicle

1.4.3 Noise Spectral Density and Antenna Coupling

1.4.3.1 Receiver Noise Floor

The sensitivity of a receiver translates directly to the smallest signal the receiver can discriminate. Vibrations at atomic level; a temperature dependant factor, present in all the electronic components within a receiver, are responsible for the receiver noise floor. It is a noise threshold that any received signal must surpass in order to be successfully received. A Signal to Noise and Distortion (SINAD) measurement can be used to characterise a receiver by relating incoming signal power to noise and interference.

The internal components of a receiver are not the only source of noise that contribute to the receiver noise floor. A level of noise from a high noise figure device, such as a power amplifier, coupled via an antenna network, can be received and directly contribute the noise floor of a receiver. This phenomena

is present in the antenna coupling from the rear mounted jammer antenna to that of the forward receiving antenna as in Figure 1.2. Figure 1.4 demonstrates this concept by presenting a Frequency Modulated (FM) communication signal at 460 MHz in the presence of a noise floor as a result of the receiver internal components, plotted in blue. The red spectrum represents the new heightened level as a result of the jammer presence. The received communication signal at 460 MHz cannot be extracted from the new power amplifier induced noise floor as it falls well below the noise threshold.

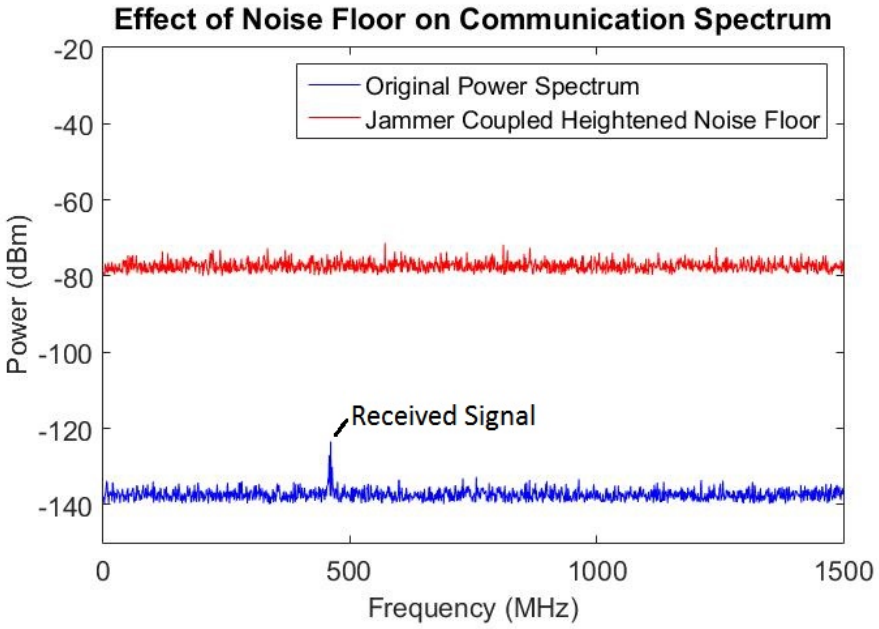

Figure 1.4: Demonstration of the effect of a heightened noise floor spectrum on received signals

1.4.3.2 Antenna Coupling

The noise levels are produced by the combined effects of the power amplifiers as well as the level of coupling between the forward and rear mounted antennas. A measurement of the antenna coupling is required over a broad frequency range in order to quantify the change to the receiver sensitivity by the power amplifier via the antenna coupling.

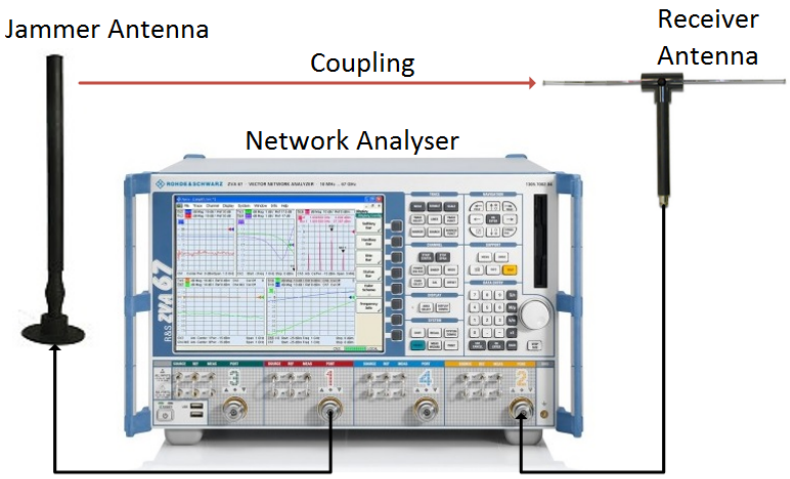

Figure 1.5: Antennae coupling factor test setup

The test setup as presented in Figure 1.5 will be used to characterise the coupling levels between the antennas for a wide frequency range. This measurement can be used to quantify the coupling between jammer and receiver antennas at various frequencies. The antenna pair that will be used to demonstrate coupling are a tri-band GSM OMNI-A0090 antenna, and a 460 MHz dipole antenna. The OMNi-A0090 antenna is connected to Port 1 on the Vector Network Analyser (VNA) and the 460 MHz antenna is connected to Port 2. S11, S22 and S21 values are plotted from 20 MHz to 3 GHz in Figure 1.6.

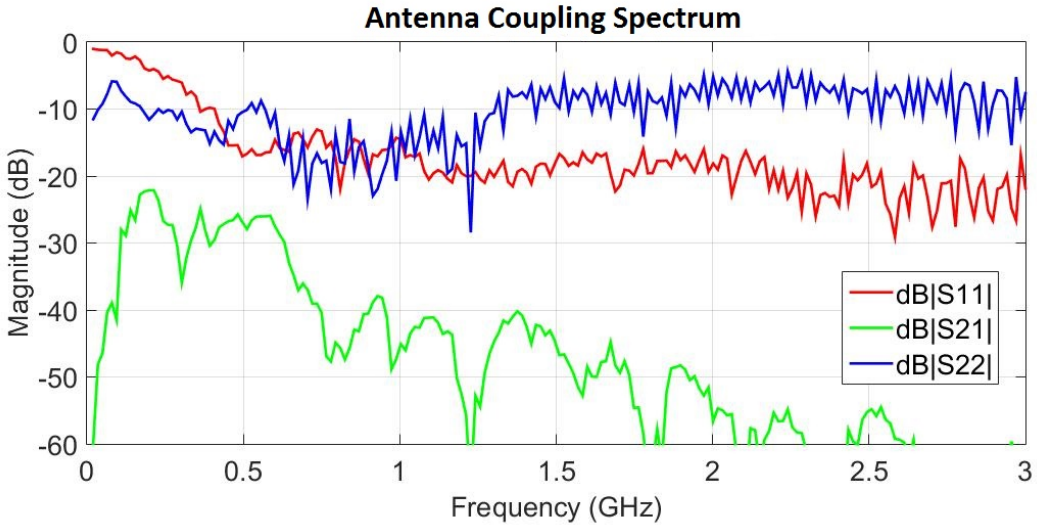

Figure 1.6: Coupling levels between 2 antennae

1.4.4 Hardware Specifications

The hardware that will be used to test the current system performance, as well as the performance of the system once the canceller has been implemented, is as follows:

1. Test Radio (Receiver) : Vertex Standard VX-160EU
2. Spectrum Analyser : Rhode and Swartz FSEK30
3. Noise Source : OP-AMP source - Appendix A.3
4. Noise Source LO (AF to RF) : Rhode and Swartz SML 03
5. Power Sensor LO Source : Rhode and Swartz SMIQ 04B
6. Test Signal (FM) Source : Hewlett Packard 8647A
7. SINAD Tester : Hewlett Packard 8920A
8. Vector Network Analyser : Rhode and Swartz FSEK30

1.4.4.1 Current Performance

The current performance is dependent on the level of noise coupled into the receiver. For a noise level of -80 dBm, a maximum achievable communication distance of 200 m is achievable. With the implementation of a canceller, every dB of cancellation will increase the maximum transmission distance.

Chapter 2

Calculating the Effect of Phase and Amplitude Error on Cancellation

2.1 Chapter Summary

Phase and magnitude error of a vector can be related to cancellation in dB through vector addition mathematics. Propagation loss equations can be used to determine ideal propagation distances for defined levels of cancellation. Chapter 2 provides a method of determining the maximum amplitude and phase error tolerances allowable for a predetermined transmission distance goal.

2.2 Phase and Magnitude Error Dependent Cancellation Performance

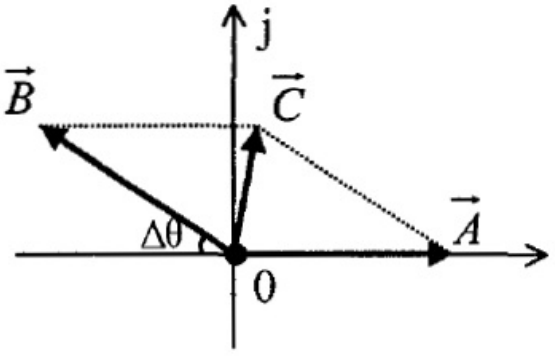

Figure 2.1: Diagram of vector addition cancellation [17]

Figure 2.1 is a visual representation of vector addition. Vector B is created in an effort to cancel the effects of vector A. The phase and amplitude of the corresponding anti-phase vector B is directly responsible for the cancellation performance. The resultant error vector C is the error of cancellation with minimisation of this vector as the main project goal. The effects of phase and amplitude error can be expressed through (2.1) [17; 20]. Cancellation ratio D is a logarithmic relationship between the reference signal and error signal, representative of cancellation performance.

$$D = 20\log\left(\frac{A}{C}\right) = -10\log\left[1 + \frac{B}{A}^2 - 2\frac{B}{A}cos\Delta\theta\right] \tag{2.1}$$

Using 2.1, cancellation performance versus phase and amplitude error between phasors A and B are plotted in Figure 2.2. This analysis will characterise the phase and amplitude performance requirements for successful cancellation. This graphic will be useful to determine the maximum error in amplitude and phase allowable for a certain cancellation goal.

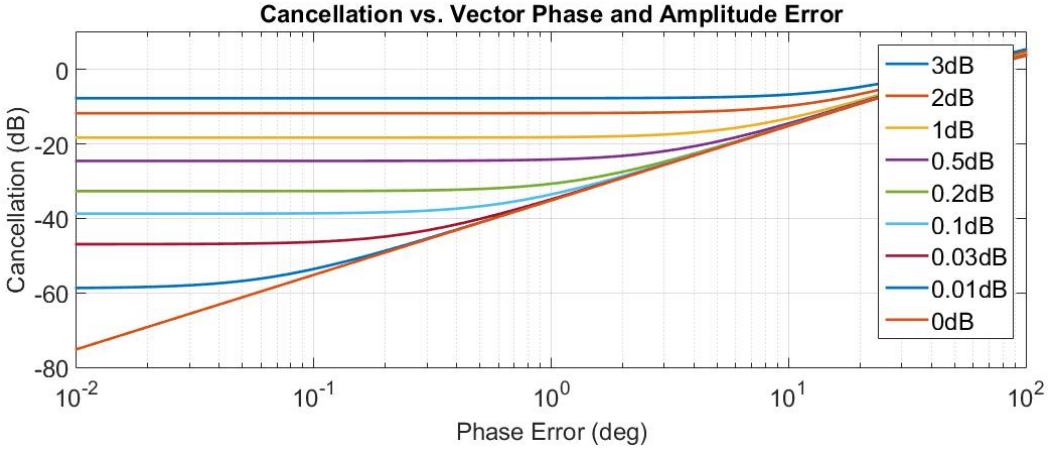

Figure 2.2: Cancellation Performance vs. Phase and Amplitude Error

2.3 Theoretical Ideal Maximum Transmit Distance

The derivation of the propagation loss equation allows for the calculation of maximum transmission distance [30; 31]. By use of the propagation equations, the transmission distance vs. cancellation will be plotted for a set of cancellation values, giving an idealised prediction for the increase in transmission distance for the level of cancellation performance the system will achieve once tested.

These calculations do not include an array of parameters that can affect the maximum propagation distance, such as physical obstacles or the curvature of the planet's surface. They will however prove useful to compare propagation distances between the two system states (relative) under ideal conditions.

The transmitted distances vs. cancellation for a variety of power levels as transmitted by the in-field transmitting radio, are plotted in Figure 2.3. The graph relates cancellation level and transmitted signal power to maximum transmit distance for a receiver with a heightened noise floor of -80 dBm.

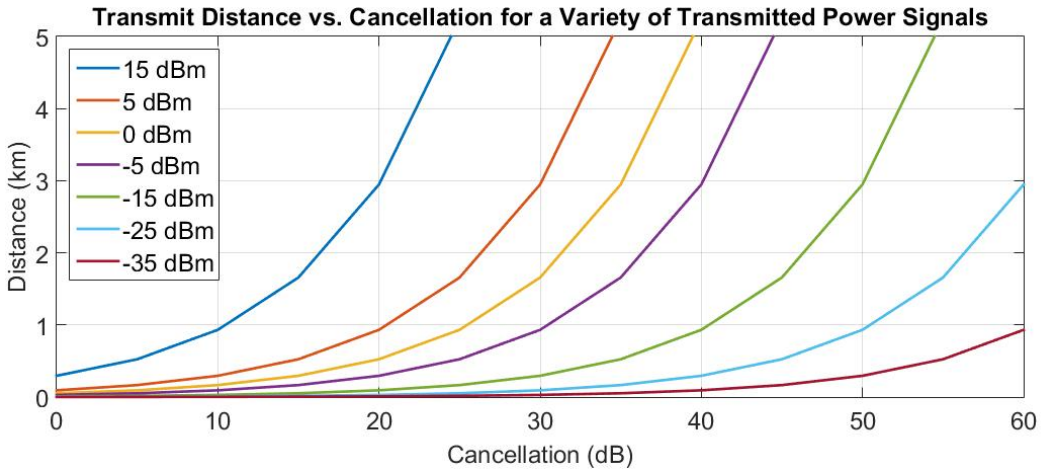

Figure 2.3: Transmission Distance vs. Cancellation

2.4 Chapter Closing Summary

A useful tool to determine the ideal phase and amplitude error tolerances has been presented in Chapter 2. The cancellation performance as a function of error can be used to predict possible performance and in turn be used to predict the increase in communication distance. The following chapter reviews the literature topics required in the design of the system.

Chapter 3

Literature Study

3.1 Chapter Summary

Chapter 3 contains a literature review of the theoretical concepts covered throughout the text. It serves as a reference chapter to refer back to in the event that the reader is unfamiliar with a concept described within the text.

3.2 Theory Components

3.2.1 Noise Cancellation

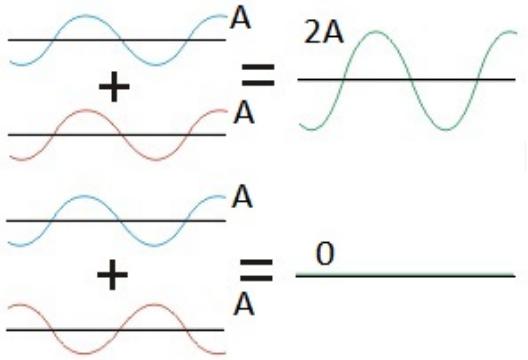

Figure 3.1: Wave superposition principle

Anti-phase cancellation can be achieved through the phenomenon of wave superposition. Waves added in phase constructively add while waves out of phase (180°), result in signal cancellation. The addition of an interference signal and an equivalent out of phase version of the interference signal, will result in the cancellation of the signal [41]. The wave concept is demonstrated

in Figure 3.1. Figure 3.2 is a basic block diagram illustrating the use of wave superposition in noise cancellation.

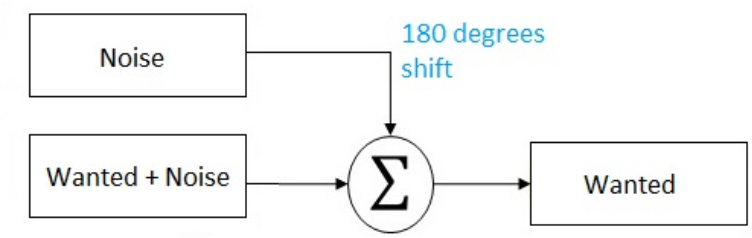

Figure 3.2: Anti-phase cancellation concept

3.2.1.1 Adaptive Noise Cancellation

Adaptive interference cancellation incorporates the use of an error signal along with the system described in Figure 3.2. The error signal is a measure of the cancellation performance level. Adjustment of the cancellation signal until the error signal is at a minimum allows for continual adaptation of the cancellation process in a dynamic environment.

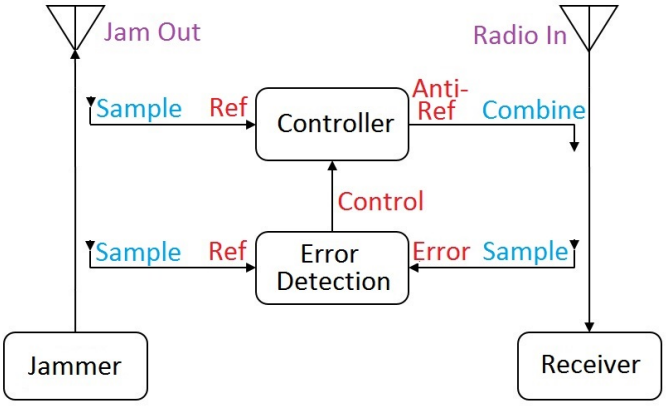

Figure 3.3: Block diagram illustrating adaptive cancellation

Figure 3.3 is a block diagram representation of an adaptive canceller system. The jammer/interference channel is a representation of the source of the noise. This source represents any form of noise, including jamming signals and internal power amplifier noise coupled over from the jammer outgoing antenna to the receiver incoming antenna. The interference source is sampled and fed into the controller block. Here the signal is converted into an anti-phase version of the reference-interference signal. The resultant signal is fed into the receiver channel resulting in cancellation, with the Signal of Interest (SOI)

and the residue error signal remaining. The error signal is sampled and passed into the error detector block. This block creates a control signal that updates the control block to continually adjust the phase and amplitude of the anti-reference signal for optimal cancellation as the system continually attempts to minimise the error.

3.2.2 Digital vs. Analog

At multiple points in the design of the canceller system, a choice will be made between digital or analog components at different steps of the design process. Comparing the advantages and disadvantages of each approach will allow for better decisions to be made throughout the design process that takes into consideration the most sensitive parameters and which design approach will suit them best.

Some of the parameters that are important factors to consider in a Radio Frequency (RF) design system are complexity, latency, tolerance, as well as radiation sensitivity. Analog devices are by nature easier to implement, while digital implementations often require additional information to implement a new learning curve, however, this increased difficulty in implementation allows for easier changes and adaptation of the system to a new function than that of an analog system [2].

The use of development boards, such as Arduino, to create an interface between computer software and the hardware, adds to the complexity of the system. An analog feedback system will adapt autonomously once the correct hardware has been implemented. The use of software or digital approaches will require programming and software development, but once completed, should be able to be easily re-purposed to perform a different task or shift the frequency scope of the application whereas hardware would need to be re-implemented, further adding to the costs.

Digital systems often suffer more from latency. Digital systems require signals to be digitised and quantised before the signal can be processed. Furthermore, the use of user-end software requires the use of serial communications between the hardware and software. Although large amounts of data bits can be transmitted serially, the true rate of useful data transfer is not as impressive. Multiple characters are required per piece of information transmitted over the serial link in order to parse the data and distinguish between relevant information pieces required at any one moment. Combined with the time taken for the system loop to complete and perform all the necessary calculations to perform the cancellation process, the time factor significantly increases, especially in lower performance standard devices such as Arduino boards.

Digital systems are also much more prone to radiation sensitivity. External sources of noise and radiation have a more pronounced effect on digital systems than that of analog systems, whereas analog systems are more affected by drift, mainly through temperature fluctuations.

3.2.3 Noise Figure

All components have a measure of noise contribution to a system. Noise Figure (NF) describes the degradation of the Signal to Noise Ratio (SNR) from the input to the output of the Device Under Test (DUT) [1]. NF is expressed in (3.1).

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{3.1}$$

The noise figure of a device is related to its noise temperature. The noise temperature of a device is a temperature equivalent representation of the spectral noise contribution of the device. The equivalent temperature of a device can be related to its noise figure by (3.2).

$$NF = 1 + \frac{T_e}{T_0} \tag{3.2}$$

where,

T_0 = Standard Noise Temperature

T_e = DUT Thermal Noise

NF = Noise Figure

For cascaded devices, the total noise factor, according to Friis' formula for noise, is shown in (3.3). This equation is for a n-cascaded system. It can be noted that the noise figure effect of a device decreases further in the cascade chain with consequent amplifiers present. With cascaded amplifiers, addition of higher noise amplifiers further down in the chain will result in an overall lower cascaded noise figure due to the division of consequent terms by the total cumulative gain of the previous elements. Attenuators or loss components can have a negative effect by dividing consequent component noise figures by values less than one, resulting in a large effect noise figures. Optimising the sequence of components in a cascaded system, where possible, can greatly benefit the noise figure of the system.

$$NF = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 G_3 ... G_{n-1}}, \tag{3.3}$$

where,

G_n represents the gain of each cascaded element.

F_n represents the noise figure of each cascaded element.

3.2.4 Non-linearity

Non-linear circuit behaviour is an important characteristic that needs to be considered in any RF circuit design. An in depth understanding of the limitations of circuit components due to non-linear effects is useful in avoiding system design issues. Designing systems using computer software modelling or calculations do not always take into account the effects of component non-linearities and limitations.

3.2.4.1 Non-linear infinite exponential series

In a linear system, the output variables are linearly related to the input variables in the form,

$$y = a + bx + cx + ... \tag{3.4}$$

where the relationships between currents and voltages are linear. Non-linear current and voltage relationships result in an infinite series of weighted input exponentials, such as the equation,

$$y = g_1 x + g_2 x^2 + g_3 x^3 + ... \tag{3.5}$$

where x is the input signal to the system, g_n are the gain and distortion coefficients and y is the output [29].

3.2.4.2 Harmonic Distortion

A sinusoid input signal, $x = acos(2\pi f_a t)$, outputs a signal, $y = g_1 acos(2\pi f_a t)$, when the system is linear. When applied to a non-linear system,

$$y = g_1 acos 2\pi f_a t + g_2 a^2 cos^2 2\pi f_a t + g_3 a^3 cos^3 2\pi f_a t + ... \tag{3.6}$$

These occurrences are characteristic of components such as mixers or diodes which are non-linear. The single frequency centered base-band signal has

numerous surrounding harmonic components when mixed up to the RF signal. The second and third terms are representative of the second and third harmonic distortion components. In Figure 3.4, the second and third harmonic terms for 2 sinusoid signals, f1 and f2, can be seen.

3.2.4.3 Inter-Modulation Distortion (IMD)

The Harmonic distortion terms are not sufficient to model or characterise the distortion of a system. When two or more signals (different frequencies) are frequency multiplied by a non-linear system, terms not harmonic to the base term are formed. They are referred to as inter-modulation distortion products [1; 33]. A double-tone frequency, with closely spaced frequencies, ω_1 and ω_2,

$$V_i = V_0(cos\omega_1 t + cos\omega_2 t), \tag{3.7}$$

when entered into a non-linear system as in (3.5), will result in,

$$\begin{aligned}
v_0 &= a_0 + a_1 V_0(\cos\omega_1 t + cos\omega_2 t) + a_2 V_0^2(cos\omega_1 t + cos\omega_2 t)^2 \\
&\quad + a_3 V_0^3(cos\omega_1 t + cos\omega_2 t)^3 + \dots \\
&= a_0 + a_1 V_0 cos\omega_1 t + a_1 V_0 cos\omega_2 t + \frac{1}{2} a_2 V_0^2(1 + cos2\omega_1 t) + \frac{1}{2} a_2 V_0^2(1 + cos2\omega_2 t) \\
&\quad + a_2 V_0^2 cos(\omega_1 - \omega_2)t + a_2 V_0^2 cos(\omega_1 + \omega_2)t \\
&\quad + a_3 V_0^3 \left(\frac{3}{4} cos\omega_1 t + \frac{1}{4} cos3\omega_1 t\right) + a_3 V_0^3 \left(\frac{3}{4} cos\omega_2 t + \frac{1}{4} cos3\omega_2 t\right) \\
&\quad + a_3 V_0^3 \left(\frac{3}{2} cos\omega_2 t + \frac{3}{4} cos(2\omega_1 - \omega_2)t + \frac{3}{4} cos(2\omega_1 + \omega_2)t\right) \\
&\quad + a_3 V_0^3 \left(\frac{3}{2} cos\omega_1 t + \frac{3}{4} cos(2\omega_2 - \omega_1)t + \frac{3}{4} cos(2\omega_1 + \omega_2)t\right) + \dots
\end{aligned} \tag{3.8}$$

The expansion of the quadratic term results in $(\omega_1 \pm \omega_2)$, second-order harmonic terms, while the cubic terms result in $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ components, known as the third-order inter-modulation terms. The expansion of (3.5) results in an infinite series, where the nth term results in the nth order inter-modulation products [32].

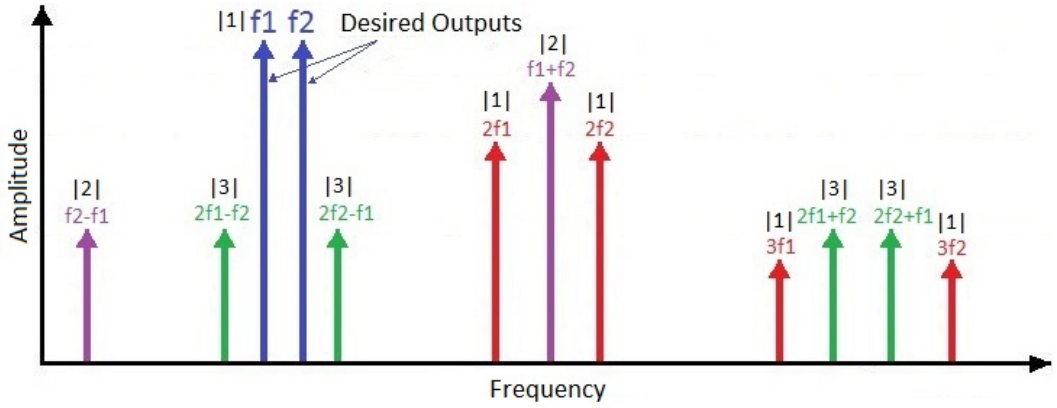

Figure 3.4: Intermodulation products

Inter-modulations for two fundamental frequencies, f1 and f2, are plotted in Figure 3.4. They are labelled as follows:

1. Fundamentals and Harmonics
2. Second Order IMD products
3. Third order IMD products

3.2.4.4 1-dB Compression Point

The 1 dB, or Gain Compression Point, is the point 1 dB below the predicted linear gain line of an amplifier, to the actual gain line as it begins to reduce as a result of saturation. This phenomenon is depicted in Figure 3.5. The value for the 1 dB compression point is denoted by input power, IP1, or by output power, OP1, but typically the larger one of these options [1]. Operating a device beyond the 1 dB compression point will result in signal clipping.

A multiple component system 1 dB compression point is defined as the compression point of the lowest relative (component gains links components to each other) 1 dB compression point device in the circuit. As the first system component reaches saturation, the system is said to be saturated.

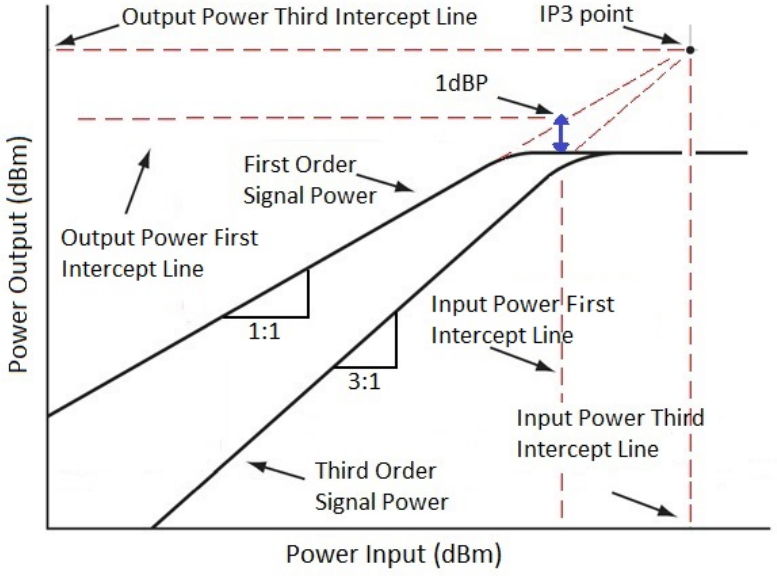

Figure 3.5: Definition of 1 dB Compression and IP3 Points

3.2.4.5 Third Order Intercept Point (IP3)

The coefficients of all the expansion terms of a non-linear system as in (3.5), are dependant on the input power, V_0. The increase of input power for the third order inter-modulation terms are cubic as the coefficient to the third order terms are V_0^3, an exponential relationship. The third order terms quickly increase to meet with the lower order terms. The point where the first order, linear predicted line gain, and the third order coefficient predicted lines intersect, is known as the third-order intercept point [1]. The third-order intercept point is shown in Figure 3.5.

3.2.5 Directional Couplers

Couplers are passive devices used in high frequency applications to sample an input signal by separating a predefined amount of signal power to be used in another part of the circuit. The device can be used in reverse to combine signals as well.

$$C_{3,1} = 10\log\left(\frac{P3}{P1}\right) dB \tag{3.9}$$

These 3 port devices are characterised through a coupling factor/gain C, defined in dB, which defines the coupling path from port 1 to port 3 as observed in Figure 3.6 through (3.9). The through path gain is defined as $1 - C$ from port 1 to port 2. A coupler is generally constructed with

close proximity transmission lines that allow for predetermined electromagnetic coupling between the lines.

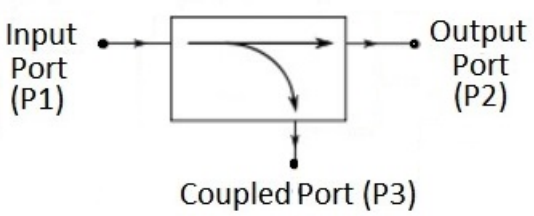

Figure 3.6: Directional coupler port model

Ideally all power should be transferred from P1 to P2 and P3 as defined by the coupling factor C. This however, is not the case as some of the power is transferred to an internally isolated port, P4, and some power is lost through copper losses. The definition of coupler power transfer ratios are defined in (3.10) [1].

Directional coupler characterising equations:

$$\text{Insertion Loss (L)} = 10\log\left(\frac{P2}{P1}\right) = 20\log|S21| \text{ dB} \tag{3.10a}$$

$$\text{Isolation (I)} = 10\log\left(\frac{P4}{P1}\right) = -20\log|S41| \text{ dB} \tag{3.10b}$$

$$\text{Coupling (C)} = 10\log\left(\frac{P3}{P1}\right) = 20\log|S31| \text{ dB} \tag{3.10c}$$

$$\text{Directivity (D)} = 10\log\left(\frac{P4}{P3}\right) = 20\log\left(\frac{|S31|}{|S41|}\right) \text{ dB} \tag{3.10d}$$

3.2.6 Propagation Loss

Transmitted power radiates in a spherical motion outward from the source into space in a 3-D environment. If the total transmitted power is defined by P_t, that has directional gain of G_t, the power density (p) can be defined through distance as [31; 30],

$$p = \frac{P_t G_t}{4\pi d^2} \tag{3.11}$$

The receiver end antenna has an effective receiver gain based on the antenna dimensions and efficiency. The effective antenna area of the receiver, A_e, through receiver antenna gain G_r, is defined as,

$$A_e = G_r \frac{\lambda^2}{4\pi} \tag{3.12}$$

The total received power at the receiver is thus,

$$P_r = pA_e = G_r G_t \frac{\lambda^2}{4\pi} \frac{P_t}{4\pi d^2} \tag{3.13}$$

Free space loss is defined as the ratio of received power over transmitted power, $\frac{P_r}{P_t}$. Taking into consideration the gain for isotropic antennas, $G_r = 1$, $G_t = 1$, resulting in Free Space Propagation Loss (FSPL),

$$FSPL = \left(\frac{\lambda}{4\pi d}\right)^2 \tag{3.14}$$

Noting λ is frequency dependant and converting FSPL into dB with distance d, in km and frequency f, in MHz, results in 3.16.

$$FSPL = \left(\frac{c}{4\pi df}\right)^2 \tag{3.15}$$

$$FSPL(dB) = 32.4 + 20\log(f) + 20\log(d) \tag{3.16}$$

3.2.7 Dynamic Range and Saturation

3.2.7.1 Saturation

Receiver chains in communications are limited in the size of signals which they can receive. If a signal received surpasses the 1 dB compression points of any of the devices in the receive chain, such as mixers, Low Noise Amplifiers (LNA's) and filters, the receiver is considered as saturated. The device with the lowest 1 dB point is the limiting factor in the circuit.

A signal input beyond the 1 dB compression point of a device clips the signal to the saturation ceiling. This distorts the signal and induces harmonics not present in the original signal. This phenomenon limits the capabilities of the receiver in an arena of high intensity, close proximity sources of noise and interference. For this reason, the cancellation system must be implemented before the receiver to avoid saturation from high power interference signals.

This phenomenon can also be described in terms of desensitisation. Any large level signals that can cause the receiver internal thermal noise to increase, directly increase the Minimum Detectable Signal (MDS) of the device.

3.2.7.2 Dynamic Range

Dynamic Range (DR) is a measure that can be characterised by receiver characteristics elements. Dynamic range can be defined as the range of operation in which a device can perform in its desired manner [1].

It is physically defined by the minimum detectable signal and maximum receivable signal that a component can detect while performing as desired. The lower range is generally limited by the sensitivity of the device while the maximum is limited by the power overload and saturation capabilities of the device. In Figure 3.5, the dynamic range is defined as the point between the 1 dB compression point and the noise floor (or the 12 dB SINAD point).

Dynamic range has an important effect on Analog to Digital Converters (ADC's). The range of received amplitudes are quantised into a set number of equally spaced amplitude values expressed in bits. If both large and small signals are received, the large signal would force the quantisation bits to be spread over a large range, causing large inaccuracies when quantising the small signals, rounded to the nearest quantisation level that has been set wide by the large received signal. This concept is taken into consideration if a digital cancellation system is to be considered.

3.2.7.3 Spurious Free Dynamic Range

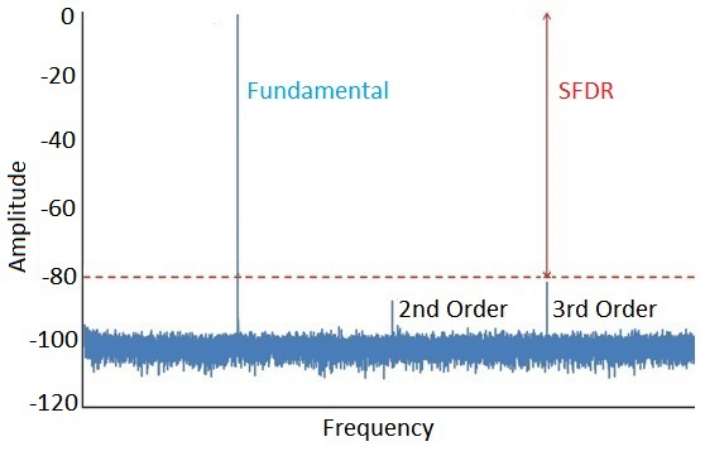

Figure 3.7: Spurious Free Dynamic Range for an amplifier

Where dynamic range is defined as the largest and smallest processable signals, Spurious Free Dynamic Range (SFDR) is defined as the ratio between the fundamental SOI and the largest spur in the band of operation. SFDR can be defined over a bandwidth and all spurs outside this band will not be considered. SFDR can also be sub-categorised into the second-order and third-order SFDR values that refer to the ratio between second-order and third-order terms to the fundamental respectively. Representations of such measures are plotted in Figure 3.7 and Figure 3.8. The first is a frequency spectrum plot showing fundamentals and harmonics while the second figure is a plot of input power vs. output power. In Figure 3.8, the noise floor is the lower reference point.

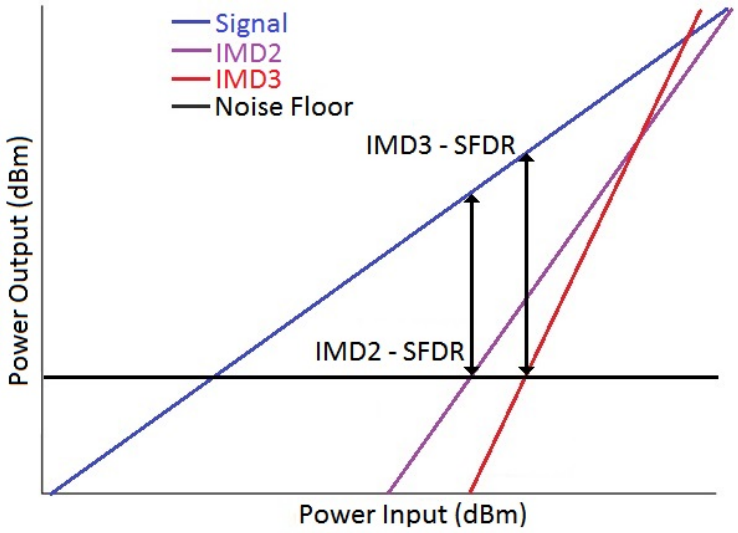

Figure 3.8: Dynamic range for an amplifier

3.3 Chapter Closing Summary

From the literature review chapter, the text continues into Chapter 4 where the numerous design options for a first iteration prototype are discussed.

Chapter 4

Canceller Design Options and Specifications Thereof

4.1 Chapter Summary

Chapter 4 summarises the basic building blocks required to create a noise and interference cancellation system. A summary of the available design options for each of these basic design blocks, based on a literature review of current and novel technologies, is presented [16]. The final section presents the chosen initial prototype design choices for each of the design blocks presented throughout the chapter.

4.2 Pre-Design Considerations and Background

4.2.1 Base Canceller Component Blocks

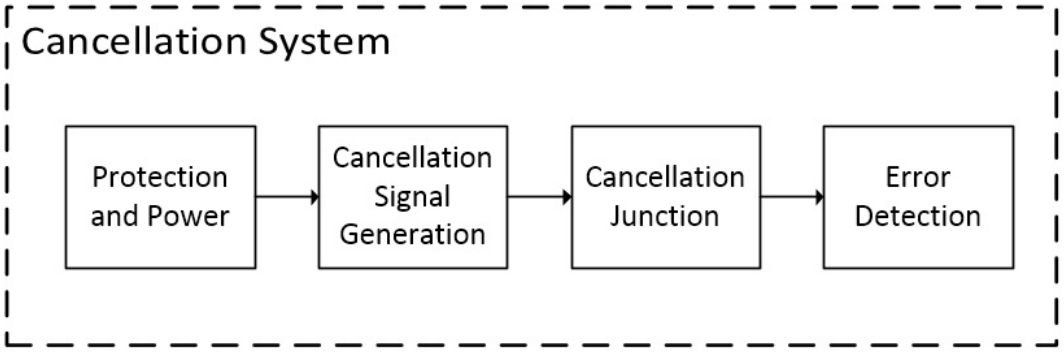

Figure 4.1: Basic canceller system component blocks

The basic design requirements for an adaptive cancellation system can be summarised into 4 main divisions:

1. Correlation and Error Detection
2. Cancellation Junction
3. Cancellation Block
4. Protection and Power

4.2.2 Component Block Descriptions

The operation and purpose of each of these blocks are summarised in order to create background on the purpose of each. Figure 4.1 presents a flow diagram of the connections between the 4 base design blocks.

Correlation and Error Detection - Changes in the environment around radio antennas as well as numerous other unpredictable changes in the circuitry require the controller to continually update the anti-phase signal. In order to continually generate a precise anti-phase version of the noise, an error signal representative of the cancellation error is required. It is this error signal, generated by the error detection/correlation circuit, which drives the controller in order to minimise the cancellation error and maximise cancellation.

Cancellation Junction - The second consideration is that of the Receive Chain/Cancellation Junction. The receive chain consists of the signal summation and splitting junctions such as the 4 points labelled in blue in Figure 3.3. Although the topology for the receive chain is inherently specific to the error detection method chosen, the basic components used remains the same. At multiple sections of the circuit, reference signals are required to generate the anti-phase noise signal as well as the error signal. This application requires the use of signal splitters/combiners or directional couplers. At the summation junction where the noise and anti-noise are combined, a splitter/combiner or coupler can once again be used in a reverse topology. Figure 3.3 of a basic adaptive cancellation system block diagram highlights the use of sampling and summation junctions as described clearly.

Cancellation Block - The cancellation block and controller are considered the most important components of the cancellation system. The cancellation block is directly responsible for the generation of the anti-phase signal through amplitude and phase variation of a reference noise signal. The resolution of

the phase and amplitude variations that the chosen topology is capable of will have a direct effect on cancellation performance. Bandwidth considerations and most importantly, dynamic range, are important considerations.

Protection and Power - As in all circuit design applications, most devices and components require a supply voltage to operate. In conjunction with this requirement is the need for circuit component protection in the event of a fault in the supply voltage. The design of stable and reliable power sources will ensure stable circuit operation while protection circuitry protect sensitive devices during operation as well as testing and adjusting. Replacing a protection component is much easier than replacing an entire Printed Circuit Board (PCB) if a fault were to occur during the design and testing process.

4.3 Correlation and Error Detection

A variety of error detection methods are used in literature and in current cancellation technologies that are applicable to the cancellation system to be designed. Three options that are viable for the proposed cancellation system are assessed.

4.3.1 Mixer Correlator

An adaptive detector is proposed [14], whereby the reference interference signal is frequency mixed with the signal after cancellation at the cancellation junction. This will result in a baseband signal proportionate to the correlation of the remaining interference in the cancelled signal. If cancellation is imperfect, a small part of the interference will remain in the signal after cancellation. Mixing this post-cancellation signal with a pure interference reference will result in a baseband signal with an amplitude proportionate to error of cancellation (signals are correlated). This baseband signal is accumulated in an integrator in order to sustain its value. The resultant Direct Current (DC) value can be used to adjust the phase and amplitude control of the circuit until the value is at a minimum, a representation of maximum cancellation. This is demonstrated in Figure 4.2

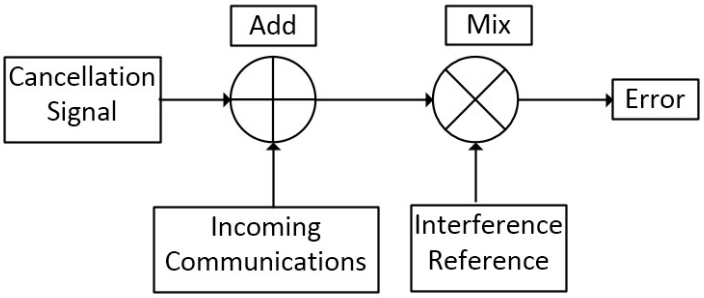

Figure 4.2: Mixing the cancelled signal with a reference of the interference signal

A similar concept [14] uses a different sampling structure. Figure 4.3 is a representation of the error detection structure, whereby post and pre-cancellation signals are mixed and sent to the error detection block where the control signal to the canceller is generated.

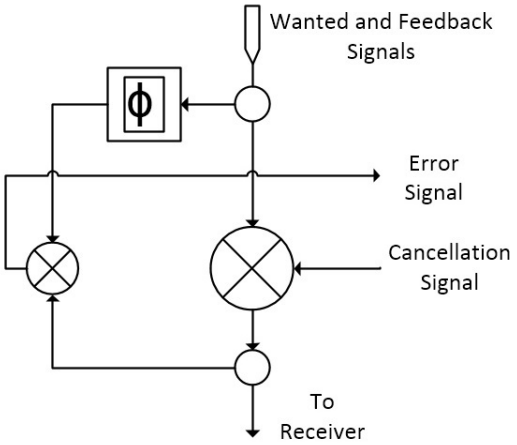

Figure 4.3: An alternative error detection block [14]

4.3.2 IQ demodulator

A basic correlator is essentially a multiplier and an integrator [11]. A reference signal and error signal are the inputs. Multiplication of two same frequency signals will result in a baseband signal at DC. The integrator allows for the value to be maintained (averaged) through cumulative samples of the DC value. It is this value that drives the cancellation controller to adapt the phase and amplitude of the anti-phase signal generated.

The multiplier can be implemented in many ways, one being a quadrature mixer. A quadrature mixer will frequency mix the RF input error signal with

an in-phase (I) and quadrature (Q) version of the reference signal to create two control signals, the I and Q control signals. This result is useful if the cancellation signal is generated by a vector modulator. A Low-Pass Filter (LPF) can operate as the integrator with the implementation of a RC LPF or an op-amp driven active LPF [22; 21; 19; 20].

4.3.3 Power Sensor

A power sensor is an alternative to the use of frequency mixers in order to obtain an error signal. This method measures the power of the noise within a narrow frequency band adjacent to the SOI. If the cancellation is accurate, the power levels of the noise adjacent to the SOI should be minimal. Continual measurement of this noise band and controller adjustment to minimise it should allow for the best cancellation at the center frequency where operation occurs and the SOI is transmitted.

4.4 Receive Chain

4.4.1 Correlator Receive Chain

The receive chain requires the use of three sampling devices if the frequency mixer topology is to be implemented. The first is for obtaining a reference of the jamming/noise signal from the jammer transmitter to generate the cancellation signal. The error signal requires two samples, one the same as for the cancellation signal reference, the other taken from a point after the summation junction where cancellation has occurred [15]. A combination component is required where the noise and anti-noise signals are to be combined for cancellation at the summation junction. Figure 3.3 describes the correlator based layout with two references from the noise/jammer channel.

4.4.2 Power Sensor Receive Chain

The main difference between the correlator based approaches and the power sensor is that the power sensor does not require a sample of the noise reference in order to generate an error signal. The power sensor error detector does not compare the cancellation output to a reference but rather measures the power in the sideband and makes a decision based on the power levels found here alone. It therefore requires two sampling points and one combination point at the summation junction where cancellation will occur.

An important decision to be made regarding the receiver chain is the coupling factor to be used in obtaining signal references. At the summation junction, a reference signal is taken to determine the error signal. This sample signal not only contains the cancellation error, but the SOI as well. If a larger

value reference is coupled, more of the SOI is lost. Noise generated by the cancellation circuit is added via the coupler at the summation junction. A minimal coupling is therefore optimal in this case. An optimum value for the coupler can be used by optimising the Signal to Interference and Noise Ratio (SINR) function of the system.

4.5 Cancellation and Control

4.5.1 Line Stretcher

An Electronic Line Stretcher (ELS) is a device typically used to classify Voltage Controlled Oscillators (VCO's) [38]. It replaces the conventional mechanical line stretcher method with an automated VCO classification system. Adjusting the control DC voltage of the ELS shifts the phase of the reflected signal. The output of the ELS is a sample of the reflected, phase shifted input.

This phase shifting principle at the output can be utilised in order to create the phase shift required in order to create an anti-phase version of the noise and interference present in the receiver. Correct adjustment of the amplitude through the use of variable amplifiers and variable attenuators in conjunction with the phase shift properties of the ELS, will serve as a basic cancellation system.

Many novel phase shifting approaches can be implemented as an alternative to an electronic line stretcher. Alternatives incorporate transmission line matching and reflection principles. The phase velocities and matching of different transmission line structures are altered through capacitors and varactors to achieve the desired phase shift [4; 6; 7; 8].

4.5.2 Vector Modulator

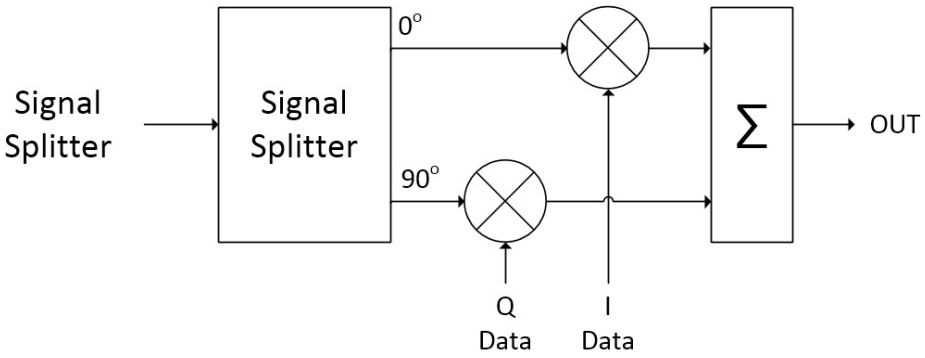

Figure 4.4: Vector modulation principle block diagram

A vector modulator is more typically used in cancellation applications than line delay devices. A vector modulator performs modulation on the RF input by splitting it into two channels, the in-phase channel and the quadrature channel. By modulating the RF input I and Q channels with DC signals, we are able to control the amplitude and phase of the RF signal.

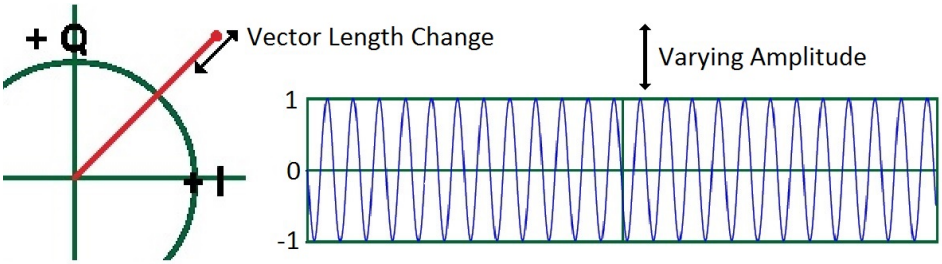

Figure 4.5: Vector modulation amplitude variation

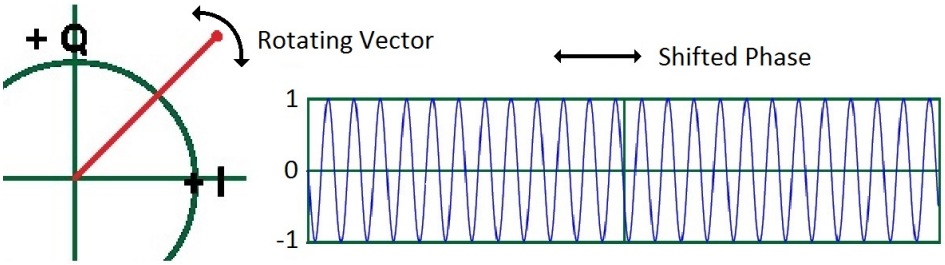

Figure 4.6: Vector modulation phase shifting

By changing the amplitudes of the I and Q channels equivalently, we are able to change the amplitude of the RF input [5]. If we vary the amplitudes of the I and Q control signals in a trigonometric fashion whereby one amplitude decreases and the other increases while maintaining a uniform total amplitude, we can exclusively shift the phase of the RF input signal. These two principles can be described as either changing the length of a vector (Figure 4.5) and rotating a uniform vector (Figure 4.6), respectively.

A combination of these effects allow us to create an accurate anti-phase version of the reference noise and allow for better cancellation. Vector modulators have excellent dynamic range and can operate over a wide bandwidth [12].

4.6 Design Choices

From the many design solution possibilities that were discussed in Chapter 4, a selection has been made for the preferred design topologies for each design section. These first build design choices are justified below. Figure 4.7 describes the chosen topology.

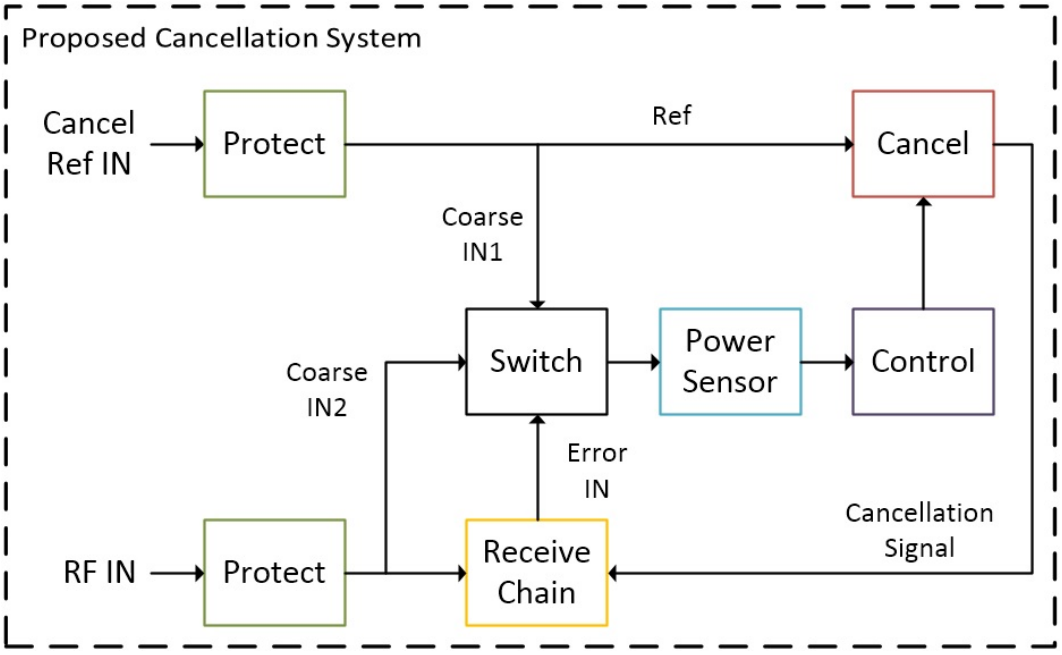

Figure 4.7: Top level block diagram of proposed cancellation system

Error Detection - The error detection topology chosen is that of the Power Sensor method. Power sensor dynamic range does not go to a low enough level to measure the cancelled power levels, however through frequency selection and amplification, a solution can be found.

The use of correlation based error detection isn't fully realisable due to the high power levels that are required to drive the mixer. This approach is commonly used in radars where the pulse signal is of a high enough magnitude to drive a frequency mixer. (Mixers generally require large LO signal levels to function properly.) In this case, no radar pulse is emitted and only very small amplitude signals are available. A further disadvantage is the slightly more complicated control of the cancellation signal, as defining an I/Q control signal as a function of a DC signal, could prove difficult. An advantage of this layout is that one fewer coupler/splitter is required.

Receive Chain - The receive chain topology is dependant on the error detection topology choice. The use of three devices will be implemented, 2 of which serve as signal extraction devices and the third as a summation junction where cancellation occurs. The standard cancellation block diagram of Figure 3.3 is implemented without the sample point, fed from the jammer line to the error detection block. This point is not required with the power sensor error detection method.

Cancellation Block - A vector modulator will be used for its dynamic range capabilities and large operational bandwidth. It is also the preferred option as it has the ability to control amplitude and phase simultaneously.

4.6.1 Design Summary

The first iteration design is presented in Figure 4.7. The reference port where a sample of the jammer is received, as well as the RF input signals from the receiver antenna, will have a protection circuit present. Samples of each of these channels (Coarse In1 and Coarse In2), will be taken to the power sensor circuit for coarse amplitude adjustment through the use of an amplitude and attenuation circuit.

The vector modulator then performs the required phase shift and fine amplitude adjustment in order to generate a near to perfect cancellation signal. Coarse amplitude control will alleviate some of the work performed by the vector modulator

The generated signal and input RF signals are summated at the summation/cancellation junction. A further power sample is taken post-cancellation in order to generate the error signal used to adaptively tune the vector modulator and coarse amplitude control circuits.

Chapter 5

Complete System Design and Integration

5.1 Chapter Summary

Chapter 5 details the component designs for each of the design blocks as they were presented in Chapter 4. Where applicable, and where the complexity of the design block is high, the block will be divided into subsections. Each section is designed individually and where possible, simulations as well as measurements will be included. The final product photographs will also be presented.

Figure 5.1 is the top level block diagram of the proposed cancellation system (also presented at the end of Chapter 4). Following Figure 5.1, is Figure 5.2. It is a photograph of the completed cancellation system that has been integrated with Figure 5.1. It has been presented such that the design blocks of Figure 5.1, align with colours of the blocks on the completed physical system. It serves as a reference to the reader throughout the numerous design sections detailed in the chapter. Each of the main design blocks in this figure are handled in separate sections within the chapter.

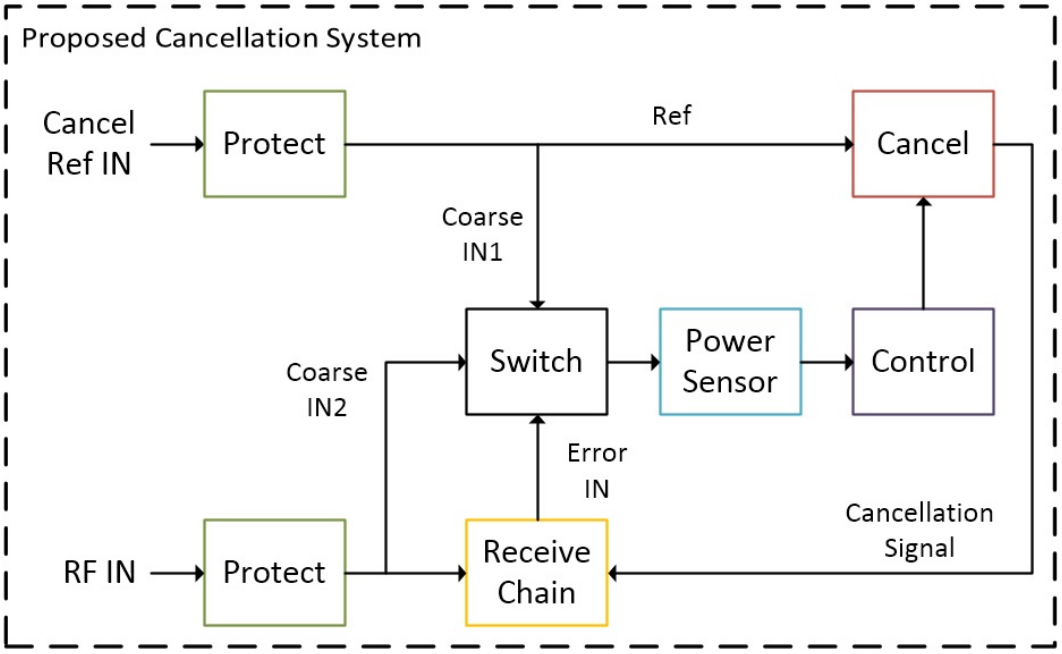

Figure 5.1: Top level block diagram of proposed cancellation system

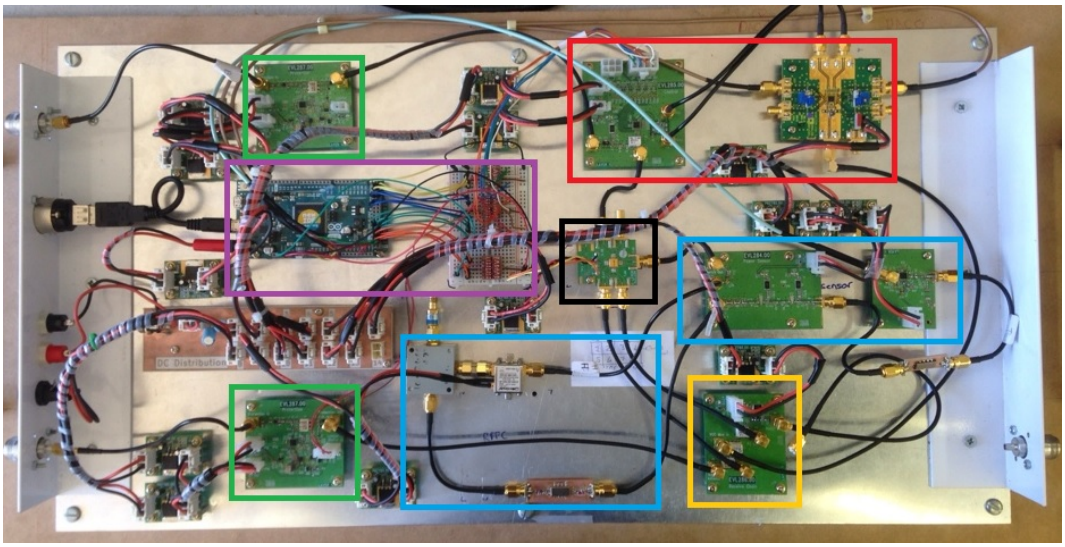

Figure 5.2: Top level block diagram representation colour coded to complete system design photograph

5.2 Manufacturing Standards

Each design section of the canceller system is designed and manufactured on Printed Circuit Boards (PCB's). The schematic and PCB layouts for the

designs were performed by Jan Roux from GEW Technologies. The complete design schematics can be viewed in Appendix B and the PCB layouts as well as the photographs of the designs will be detailed in this chapter. The PCB's used have the following properties:

Parameter	Value
Substrate type	FR4 - coplanar double layer
Substrate thickness	0.5mm
Substrate permittivity	4.1
Conductor material	Gold
Conductor thickness	35μm
Track width	0.889mm
Gap width	0.381mm

Table 5.1: Table presenting PCB design specifications and attributes

5.3 Protection Circuit Design

A good circuit design would not be complete without protection circuitry. The use of protection circuitry safeguard circuit components from a wide range of possible fault situations. These faults include voltage and current surges in the case of faulty sources, short circuits, and the user incorrectly connecting the sources. In other applications, power limiting can be implemented to protect components within a certain threshold of what they can operate within.

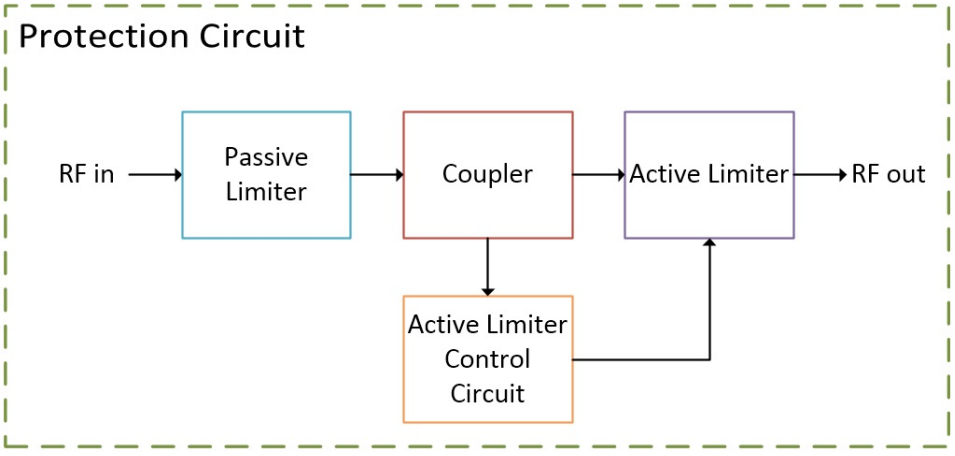

Figure 5.3: Top level protection design block diagram

Two levels of limiting will be implemented to ensure correct power limiting in the circuit. The first stage is a passive limiter, whose purpose is to limit

the input power passively as defined by its specifications. The second stage, the active limiting stage, will implement a power sensing network prior to the active limiter diode. This network will sense the incoming power and actively bias the active limiter PIN diode. A voltage reference Integrated Circuit (IC) will decide on the active power limit. Once the DC output from the power sensor bypasses the reference voltage, a comparator IC will force the diode to limit. At the same time the comparator will trigger a timer IC to maintain the active limit for a predetermined amount of time to ensure the incoming power surge has passed. In the event that the large incident power continues, the circuit will re-trigger the timer and active power limiting will remain in effect. The passive stage, active control and active limiter stages will be designed. These three design blocks complete the Protection Circuit as described in Figure 5.3.

5.3.1 Passive Limiter

The passive limiter stage design can be seen in Figure 5.4. An Electrostatic Discharge (ESD) protection anti-parallel configuration diode pair, D1, will be implemented at the input of the protection circuit with a parallel to ground inductor, L1, required to allow for a free path of current in the event that the device is activated. The ESD device chosen for the design is the Infinion ESD0P4RFL. The inductor value is chosen as 36 nH to serve as the current path as well as a RF choke for the frequency of operation.

The cut-off power threshold that will be implemented is 15 dBm. All subsequent circuit components will be protected by this threshold level while simultaneously allowing all signals of interest to pass unhindered. The PIN diode selected to allow for a 15 dBm limit threshold, D2, is the Skyworks CLA4606-08LF [34]. D2 also requires a free current path through inductor L2, that also forms part of the filters.

Incorporated into the passive limiting stage will be a high-pass and low-pass 3rd order filters. The filter will be designed for a wide pass-band. The filter stage will consist of 2 third-order Butterworth Tee filters.

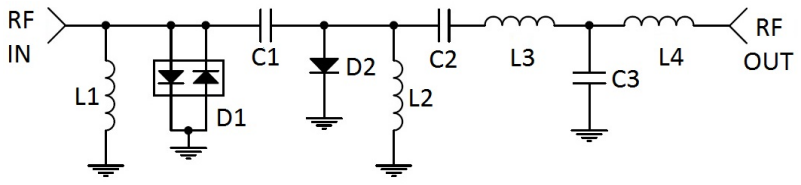

Figure 5.4: Passive limiter design

5.3.1.1 Filter Design

Figure 5.5 shows the response of a 3rd order Butterworth Low-Pass Filter (LPF) and High-Pass Filter (HPF) plotted against frequency. The LPF has a -3 dB cut-off of 525 MHz while the HPF has a -3 dB cut-off frequency of 375 MHz. The filters are added in seri es to create a low order band pass filter with a calculated bandwidth of 150 MHz.

The simulated frequency response of the cascaded LPF and HPF can also be seen in the figure. The center frequency is at 450 MHz with a S21 of -3.2 dB as simulated in Advanced Design Studio (ADS). Parasitic component effects were added in the simulation.

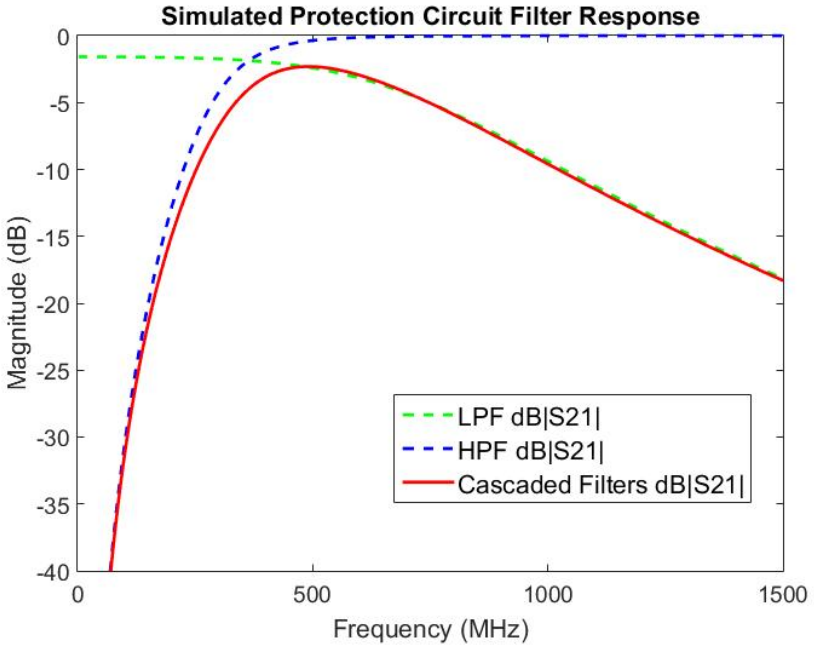

Figure 5.5: Simulated frequency response of cascaded HPF and LPF

5.3.2 Active Limiter

A second stage of PIN diode based limiting is implemented following the passive limiting stage. This stage will be hard driven by a control signal from a series of power sensing and timer IC's. Once the signal power bypasses a predetermined power level designed into the active control circuitry, the active protection PIN diode will be activated with a current free-flow path through a Schottky diode to ground.

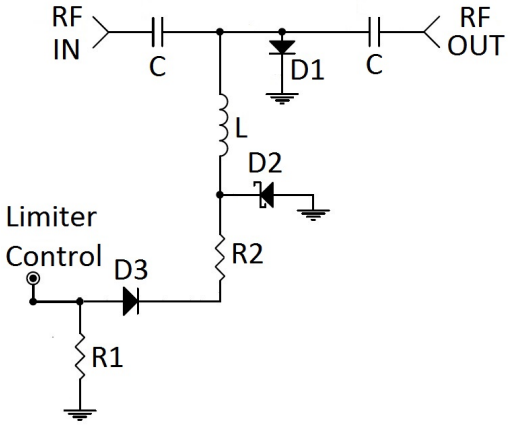

Figure 5.6: Active limiter design

In Figure 5.6, the PIN diode is directed to ground from the RF signal path. Increased input power will allow for the mismatch of the PIN diode to increase, thus limiting the input power. A line connects next to the PIN diode to the RF line that will cause active limiting. DC capacitors are placed on either side of this addition to prevent any of the DC control signals to enter the RF stream. Likewise, a RF Choke inductor is added to prevent RF signals from short circuiting through the active limiter control circuit. The DC blocking capacitors are 100 nF while the inductor value is 36 nH.

R1 is a 10 kΩ resistor added to act as a load for the Limiter Control input. D3 is a diode added to prevent current flow back into the Limiter Control point from the rest of the circuit. R2 controls the current flow with a value of 27 Ω. D2 is a BAT165 Schottky diode used to regulate the output voltage and prevent a negative voltage from creating reverse flowing current. D1 is a CLA4606-08LF PIN diode.

5.3.3 Active Limiter Control Circuit

The active limiter PIN diode is activated through a control circuit. This circuit measures the incoming RF power and triggers a timer circuit that holds the active limiter PIN diode in an active state for the duration of the timer trigger period until the high incident power signals are no longer present. The block diagram of Figure 5.7 displays the different segments of the active limiter control circuit in red.

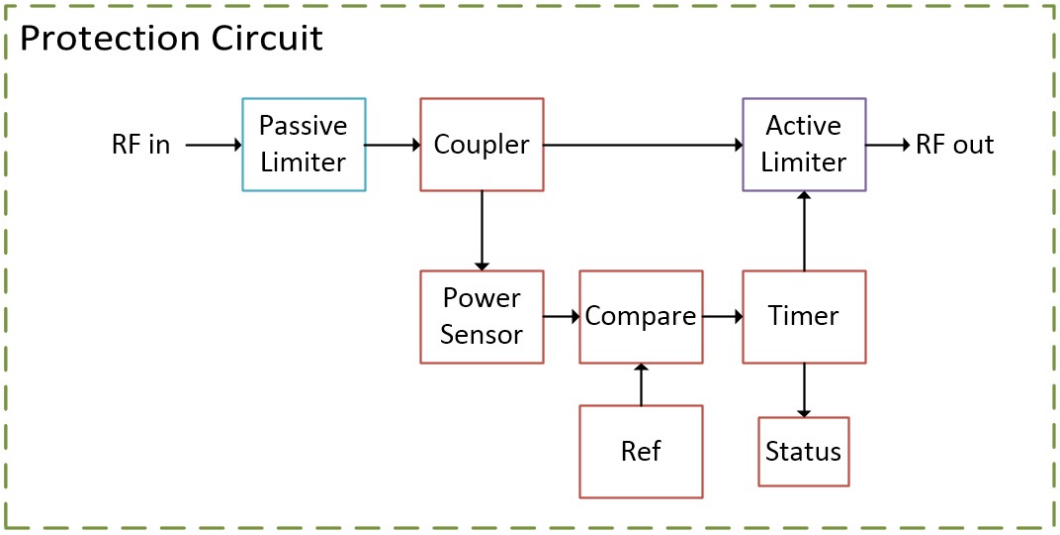

Figure 5.7: Active limiter control circuit block diagram

The first component of the active limiter control stage is the coupler. The coupler needs to sample the RF channel in order to determine the power level present. The coupling value should be small to ensure minimal RF channel power loss. The higher the coupling value, the more of the SOI is also lost. A 20 dB coupler value was chosen to allow for minimal signal loss and ensure a high enough value is chosen that falls in the dynamic range of the power sensor. The coupler chosen is a Mini Circuits ADC−20 − 4+ 20 dB surface mount coupler with an insertion loss of 0.4 dB at 450 MHz.

5.3.3.1 Power Sensor

The next component in the active limiter control circuit is a power sensor. Analog Devices ADL5906 TruPower is a true Root Mean Square (RMS) power sensor that has a wide dynamic range. It gives a DC voltage between 0 and 5 V for RF input signals between -60 dBm and 0 dBm [42]. The relationship between the RF power and the corresponding DC voltages is linear (logarithmic detector). The data sheet for the device provides a schematic diagram for basic power measurement operations. Some components require design for the type of application to be performed by the user. Figure 5.8 shows the power sensor design schematic.

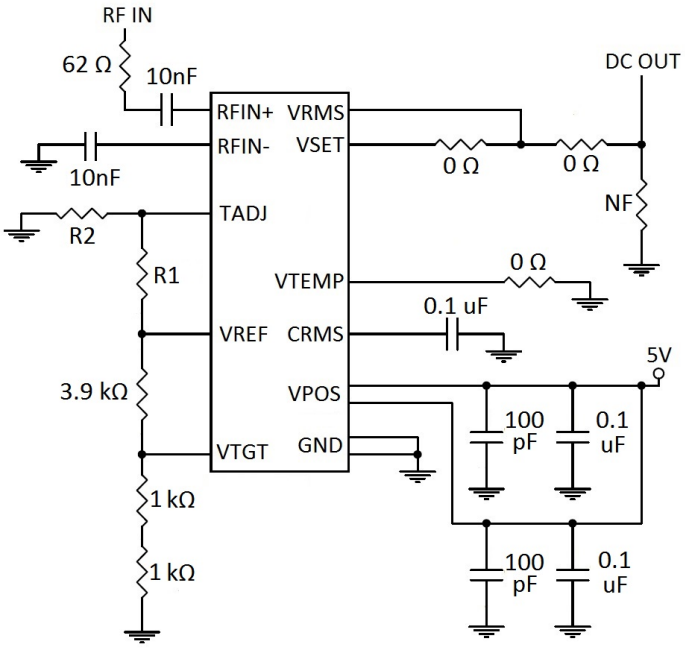

Figure 5.8: Power sensor design schematic

The values for R1 and R2 are dependant on the bandwidth of operation. V_{TADJ} determines the offset due to temperature. For 10 MHz to 2.14 GHz, $V_{TADJ} = 0.35\ V$. Therefore, $R1 = 1.5\ k\Omega$ and $R2 = 270\ \Omega$. The resistors at outputs V_{SET} and V_{RMS} can be changed if the user wishes to change the output slope of the device. All other values are used as recommended by the data sheet for basic measurement operation.

5.3.3.2 Reference and Comparator Block

The reference block IC, IC1, is required to give a reference voltage where we wish for the active protection to activate. It will be used in conjunction with a comparator IC, IC2, which will trigger the circuit once the power sensor voltage bypasses the reference IC voltage. We will design the reference output with a voltage divider potentiometer in order to allow for the power threshold to be adjustable.

$$\begin{aligned} 15\ \text{dBm} - 20\ \text{dB(coupler)} &= -5\ \text{dBm} \\ -5\ \text{dBm} &= 3.5\ V\text{(Power Sensor)} \\ 4.09 * \frac{R}{10 - R} &= 3.5\ V \\ R &= 4.611\ k\Omega \end{aligned} \tag{5.1}$$

For a 15 dBm threshold, the power sensor will need to trip at -5 dBm. The value it gives at -5 dBm is 3.5 V. The reference IC has an output of 4.09 V that needs to be voltage divided to achieve a 3.5 V level. A resistor value of 4.611 kΩ is required. Small changes in the reference voltage as a result of temperature can be accounted for by slightly adjusting the potentiometer. The reference IC and the comparator setup are shown in Figure 5.9.

R1 and R3 are 10 Ω resistors that add current limiting and combine with the capacitor to form a RC filter that filters unwanted components in the supply line. They have little effect on the voltage during normal operation, however, if the current were to increase, the resistors with a power rating of 0.25 W will fail and protect the rest of the circuit from harm. C1 and C3 are coupling capacitors of 100 nF that couple any unwanted non-DC frequency components to ground. C2 is an additional coupling capacitor with a value of 1 uF. R2 is a 10k potentiometer.

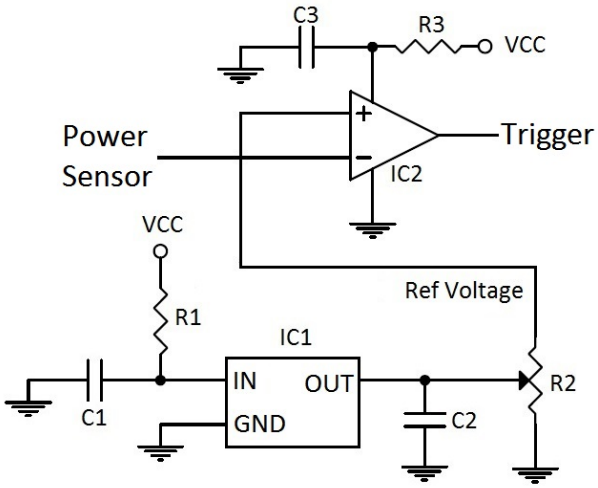

Figure 5.9: Trigger level: Reference and comparator IC's design block

A MCP1541, 4.096 V reference IC was chosen for IC1. IC2 was chosen to be a Texas Instruments TLV3201 Push-Pull comparator.

5.3.3.3 Timer and Trigger

Following the comparator IC is the timer block. The purpose of the timer block is to push the active limiter for a set duration chosen by the user. This is to ensure that the limiter is active long enough for the high incident power to pass or dissipate. The comparator output will split between the timer block and an OR gate. The timer output will join to the second input of the OR gate. This is to ensure that the limiter is activated directly via the comparator

while the timer activation delay passes from where the timer will continue to hold the limiter.

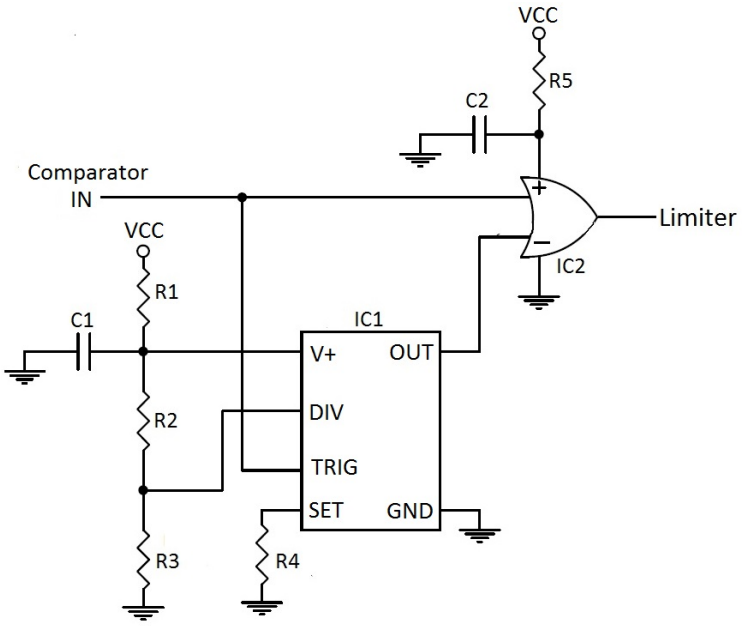

Figure 5.10: Protection circuit timer design schematic

5.3.3.4 Timer IC

R1 and R5 are the 10 Ω supply protection resistors forming RC filters along with capacitors C1 and C2 with values of 100 nF for the Timer block IC1 and the AND gate IC2. IC1, the timer block, is an LTC6993IS6-2 from Linear Technologies. The timer is programmable by using the correct biasing resistors values to determine the timer duration trigger and timer characteristics.

For a trigger duration of 70 ms, a value chosen arbitrarily to not be too long so that it blocks communications unnecessarily, while at the same time not being too short, requiring the protection circuit from having to re-trigger. To program the DIVCODE of the IC, the datasheet is used [43]. For a trigger time between 32.77 ms and 524.3 ms, a DIVCODE of 5 is required.

Resistors R2 and R3 are therefore chosen as 1 MΩ and 523 kΩ respectively. The calculating of R4 to set the IC to trigger for 70 ms is given:

$$R_{set} = \frac{50\text{k}}{1\mu s} \times \frac{t_{OUT}}{N_{DIV}}$$

$$R_{set} = \frac{50\text{k}}{1\mu s} \times \frac{70\text{ms}}{32768}$$

$$R_{set} = 106.8k\Omega \tag{5.2}$$

A standard resistor value of 115 kΩ is chosen for R4 resulting in a trigger time of 75.3 ms. IC2 is a standard push-pull OR gate. The OR gate chosen is Texas Instruments SN74LVC1G32. It has a high output state if either or both of its inputs states are high and has a low output if both inputs states are low. This allows for it to drive a high output as soon as the comparator has a high output. The OR gate output remains high as the timer is triggered and still remains high when the comparator output drops.

5.3.3.5 Limiter Driver and Limiter Status

From the OR gate we add two AND gate IC's. The first is a buffer between the OR gate and the Active Limiter portion of the protection circuit as was designed in Section 5.3.2, while the second AND gate, parallel to the first, is required to drive a Light Emitting Diode (LED) and an output port that will be fed to the controller. The LED and the output port to the controller serve as limiter status indicators for the user to observe.

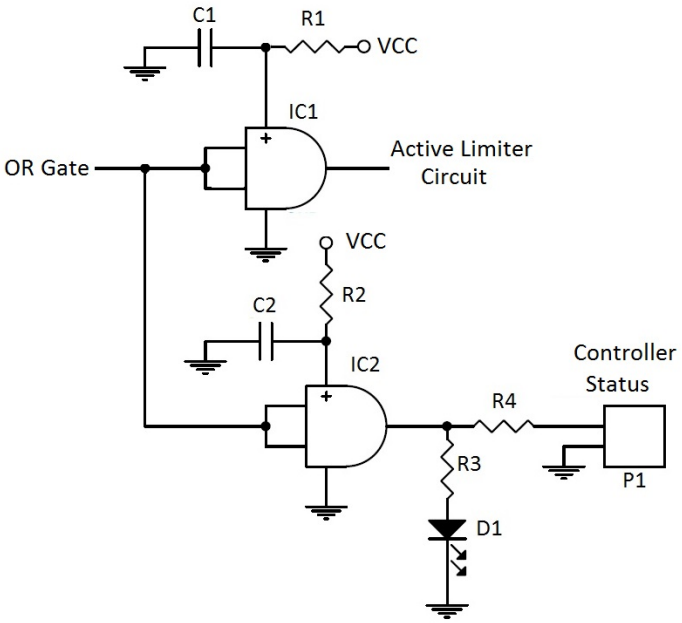

Figure 5.11: Buffer gates and status driver IC design schematic

Once again we add 10 Ω resistors at positions R1 and R2 and 100 nF capacitors to C1 and C2 as part of the IC voltage supplies. The LED, D1, is a red 0805 surface mount led. R3 is a 390 Ω, 0.25 W resistor to allow for 3.5 mA to flow through the diode with a voltage drop of 2 V. R4 is a standard 33 Ω resistor connected to a digital input of the Arduino.

5.3.4 Final Product

Figure 5.12 is the top view PCB layout for the protection circuit. It is followed by a photograph of the assembled protection circuit PCB in Figure 5.13.

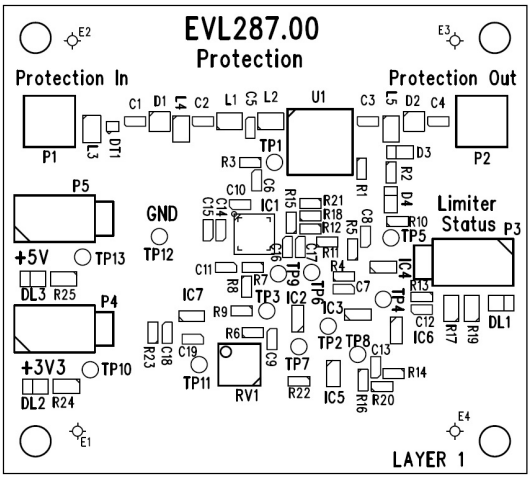

Figure 5.12: Top layer protection circuit PCB layout

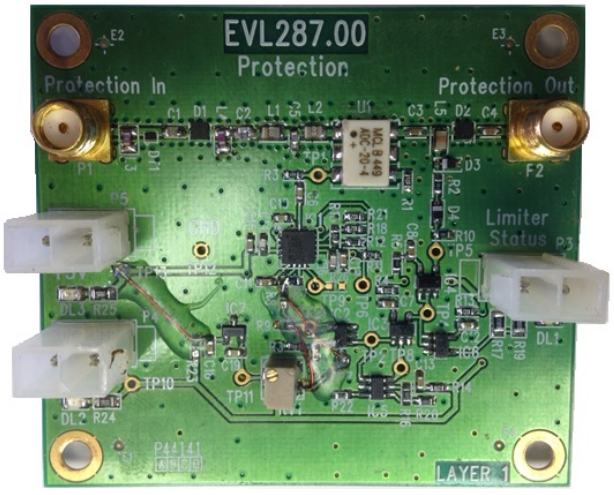

Figure 5.13: Photograph of protection circuit PCB

5.3.5 Testing

The network parameters S11, S21 with no limiting, and S21 with hard limit, for the protection circuit are plotted in Figure 5.14. The figure for only one of the protection circuits are plotted as they have been identically manufactured.

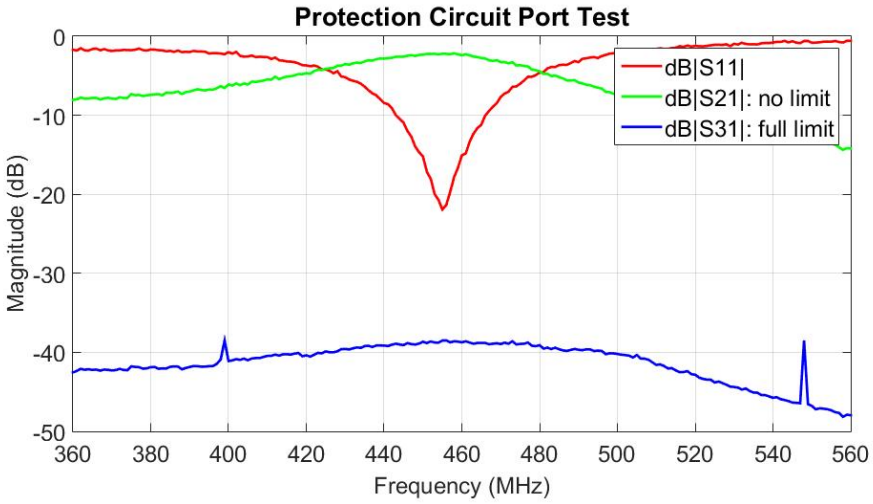

Figure 5.14: Measured frequency response of protection circuit

5.4 Power Sensor Circuit Design

The power sensor circuit performs the error signal generation task in the system. It is the error signal that drives the controller and allows for the system to perform maximum cancellation at any time in a dynamic environment. The reliability and accuracy of the error signal has a direct result on the cancellation performance. The power sensor is designed in 4 steps as presented in Figure 5.15.

It low pass filters the input, after which the signal is passed off the PCB onto the mixer stage. From here, the signal is passed back to the PCB where it is then filtered by a narrow band filter, amplified, and passed to the power sensor IC.

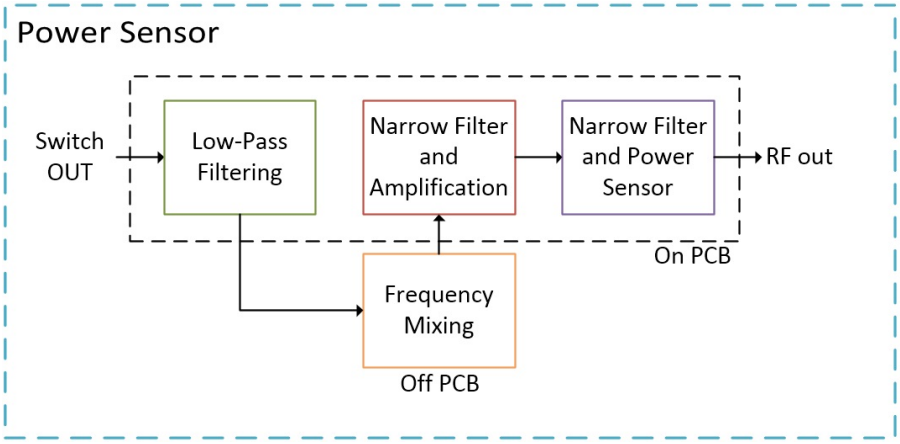

Figure 5.15: Top level design block diagram of the power sensor circuit

5.4.1 Power Sensor Operation

5.4.1.1 Switching

The power sensor approach to calculating the error of cancellation has been chosen. The power sensor is preceded by a 4 way Single Pole 4-Throw (SP4T) RF switch. The purpose of this switch is to allow for numerous power sensor measurements to be made from multiple parts of the circuit without the need for multiple power sensor circuits.

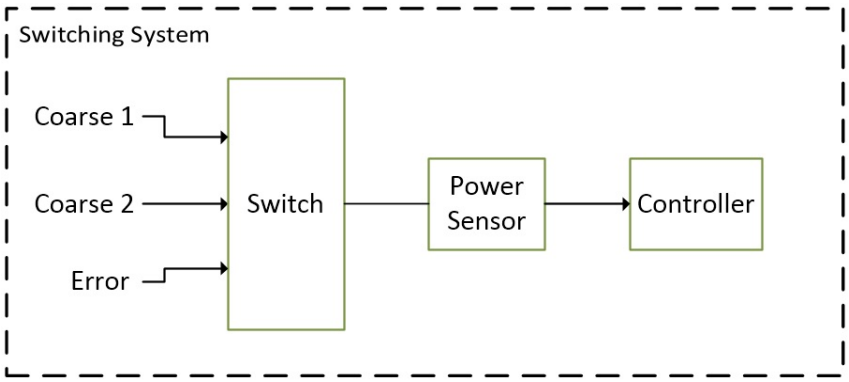

Figure 5.16: Block diagram of switch as incorporated with power sensor circuit

5.4.1.2 Measurement Points

Three power measurements will be made of which the first two are for the purpose of coarse cancellation. The coarse cancellation power measurement points are just after the protection circuit on the reference line and the other just after the protection circuit on the RF IN communications receiver line. The difference between these two measurements will adjust the digital attenuator in the cancellation circuit accordingly to ensure the levels of the incoming and reference lines are within a 0.25 dB level from each other. This will relieve the amplitude modulation requirements on the vector modulator.

The third measurement is the error measurement after cancellation. The error is the remaining noise power after cancellation and will drive the controller.

5.4.1.3 Power Sensor Operation - Spectrum

The power sensor circuit filters the incoming RF signal and noise. The RF communications band is mixed down to a lower frequency band through the use of a frequency mixer. The Local Oscillator (LO) will be chosen so that the 460 MHz SOI will be mixed down, just adjacent to a sharp cut-off SAW filter. This will allow for the noise and interference to fall into the band of the SAW filter and the communications SOI to be filtered out. The power measurement

will therefore be of the noise adjacent to the SOI and an indication of the level of cancellation. Figure 5.17 to 5.19 demonstrates this concept further.

By mixing down to a predetermined signal, the system can be adapted to any communication frequency system by simply adjusting the LO.

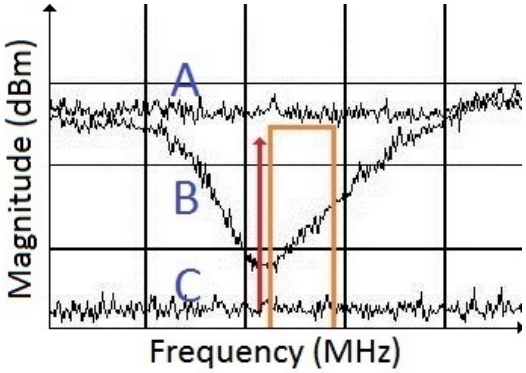

Figure 5.17: Power sensor concept - Perfect cancellation

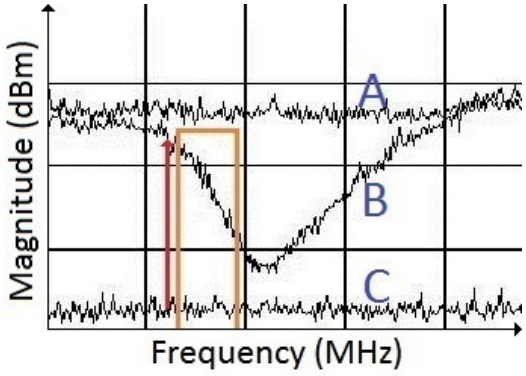

Figure 5.18: Power sensor concept - Near cancellation

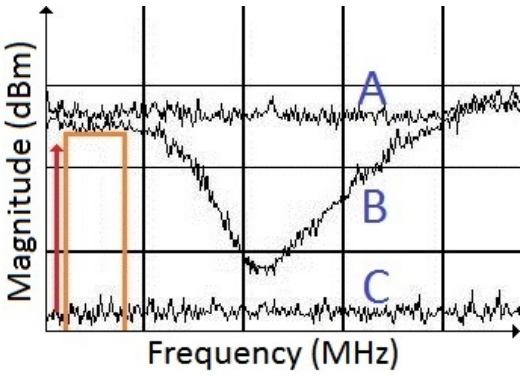

Figure 5.19: Power sensor concept - Total non-cancellation

The red arrow is indicative of the SOI in the system with the orange band representative of the SAW filter pass band. Signal C is the noise floor for the receiver, while signal A at the top is the new noise floor with the Power Amplifier (PA) switched on. Signal B is when the PA is active and the cancellation system active (and actively cancelling). All signals are presented in the frequency spectrum and are not in scale to the actual signal and SAW filter bandwidths.

Measurement of the RF power of signal B within the band of the SAW filter, is fed to the controller. Adjustments to the cancellation parameters are made based on the level of the power detected within the SAW filter pass-band. The power level detected is at a minimum in the event of maximum cancellation performance and at a maximum at minimum cancellation performance.

Two observations can however be made on the requirements for optimal cancellation; the first is that the absolute minimum measure within the SAW filter pass-band is made with the filter directly over the cancellation minimum peak. In this case the SOI is not at the minimum peak as would be required for maximum cancellation. Care should be taken to deal with this slight offset required for maximum cancellation.

The second observation is that the change in measured power within the SAW filter band changes quickly for cancellation within close proximity of the SOI due to the sharp gradient of the cancellation dip. The change of power measured within the SAW filter band due to canceller adjustments is not as pronounced when the cancellation is off by a large amount, due to the flat top of the spectrum outside the cancellation bandwidth.

5.4.2 Low-Pass Filtering

Before the mixer stage, a fifth-order LPF to clean the spectrum above 500 MHz, is implemented. Figure 5.20 shows the design schematic.

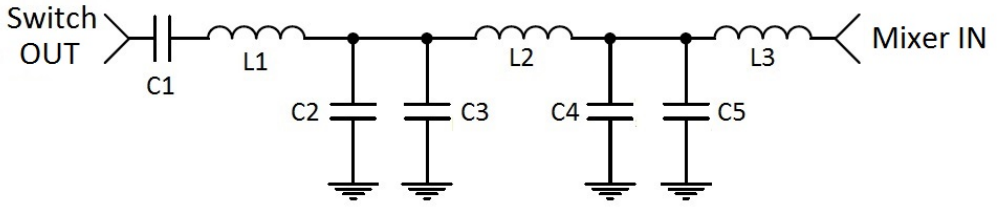

Figure 5.20: Design schematic for the input filter

C1 is a DC block capacitor to remove any DC components in the channel. L1, L2, L3, C2 and C4 are the five components that form the fifth-order LPF. C3 and C5 are parallel to the shunt capacitors C2 and C4 in the event of the filter characteristics need to be changed or component tolerances need to be compensated for. Open pad allocations are made for C3 and C5.

For a cut-off frequency of 500 MHz, the values for the filter components are the following:

LPF		
Name	Value	Unit
L1	15	nH
L2	27	nH
L3	15	nH
C2	8.2	pF
C4	8.2	pF

Table 5.2: Low-Pass filter component values

The simulated response of the Filter dB|S21| is plotted in conjunction with the actual measured dB|S21| and dB|S11| in Figure 5.21. The measured filter has a slightly lower cut-off frequency, probably due to component tolerances, however, the center of 460 MHz still passes relatively unhindered with a loss of only 0.5 dB.

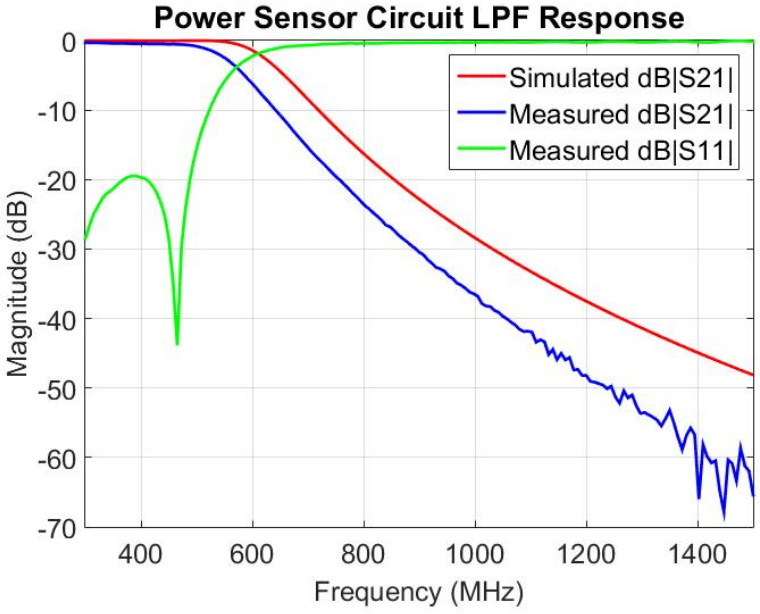

Figure 5.21: Measured response of power sensor 460 MHz LPF

5.4.3 Frequency Mixing

Once the signal has been filtered by the LPF, it is stepped down by a frequency mixing stage. Mixing up complicates the process as manufacturing or purchasing a filter with good out of band rejection and a narrow enough bandwidth is challenging. The design of an in-house manufactured 5th order coupled microstrip filter is added to Appendix A.4 to demonstrate the physical dimensions required to create a good performance filter using a LPKF milling machine.

The mixing stage consists of a connectorised Mini-Circuits amplifier (ZX60-3018G-S+) into a connectorised Mini-Circuits frequency mixer (ZFY-11). The output from the mixer, as determined by the frequency of the LO, is passed back to the power sensor PCB into the filter and amplifier stage and onto the Power Sensor IC.

The amplifier used in conjunction with the mixer is used to regain the signal power lost through mixer conversion losses and forms part of the mixing stage.

The power measurement performed by the power sensor IC will take place in a lower frequency band. In order for the signal to be measured, it has to be amplified to fit into the operation range of the power sensor IC. Filtration is required before amplification to clean the spectrum resulting from frequency mixing, as well as after the amplification stage to limit the bandwidth of noise

being measured to a small band adjacent to the SOI. The use of a mixer allows for the cancellation process to be adapted to any frequency SOI by simply adjusting the mixer LO.

5.4.4 Filtering and Amplification

5.4.4.1 Narrow Filter

The filter used post-mixing is an 86.85 MHz PX1002 SAW filter with a narrow, sharp cut-off pass-band. The power sensor band to which the LO is tuned was chosen at this frequency simply due to the availability of the PX1002 filter and the performance it delivers. The measured frequency response of the filter is plotted in Figure 5.22

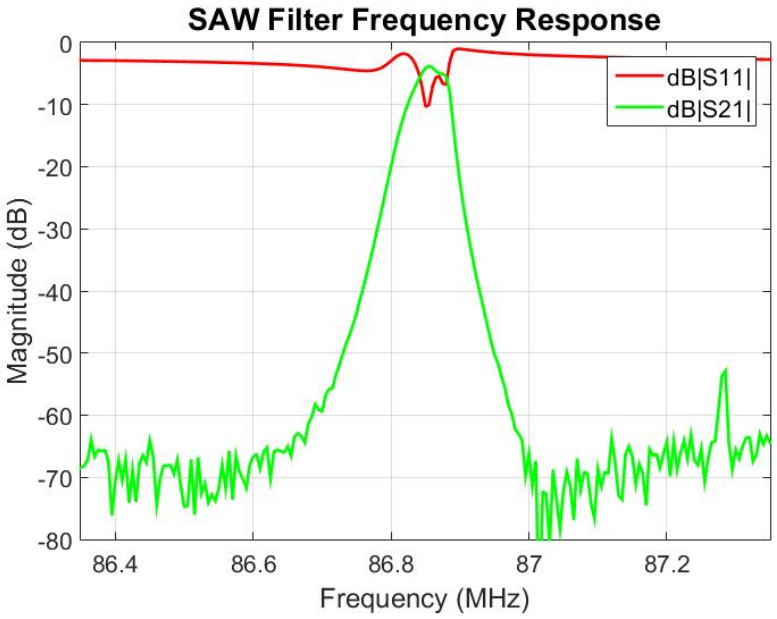

Figure 5.22: SAW filter frequency response

5.4.4.2 Cascaded Amplifier Stage

Due to the limited dynamic range of the power sensor with a maximum sensitivity of -60 dBm, a large level of amplification of the RF signal is required. The typical level for the PA heightened noise floor is between -80 and -90 dBm. With cancellation of 30 dB, the noise levels drop to below -100 dBm. To compensate for the lower minimum threshold of the power sensor, a level of amplification is needed in order to fall into the dynamic range of the power sensor. Figure 5.23 is an insert of a single amplification level as part of the cascaded amplifications stage.

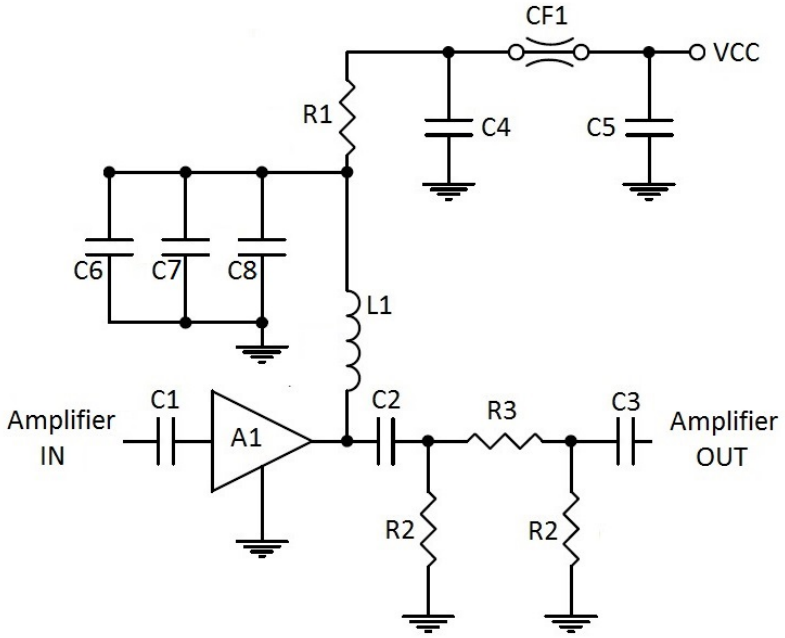

Figure 5.23: Single amplifier design schematic

The amplifier A1, is a Mini-Circuits GALI-3+. The amplifier has an operating bandwidth of DC to 3 GHz with a typical noise figure of 3.5 dB. The gain at the operating frequency of 450 MHz is roughly 21.75.

The cascaded amplifiers stage will consist of three amplifiers as in Figure 5.23. A high level of amplification will be achieved, but at the same the system would be at risk of oscillating due to the high levels of gain. Two steps are taken to improve the circuit stability and reduce the chances of oscillation.

The first is a power supply to the amplifier with adequate filtering capacitors to remove any non-DC signals. C6, C7 and C8 are coupling capacitors slots kept empty for additional filter addition. C4 and C5 couple to ground with a series NFE31PT222Z1E9L noise suppression component from Jameco, added in between to couple any further unwanted RF to ground and block RF from passing to the amplifier. Another RF choke inductor is added into position L1 with a value of 27 nH. C1 and C2 are standard DC blocking capacitors, each with a value of 100 nF.

The second measure undertaken is the use of resistive pi-attenuators between each amplifier. These attenuators will remain unimplemented with a 0Ω resistors placed in position R3 and NF allocations at positions R2. In the event of oscillation, the attenuators can be implemented to reduce the gain and

buffer the stages, bringing the gain out of the unstable region. The equations for implementing the pi-attenuators, with C as attenuation in dB, is as follows:

$$R1 = \frac{Z_0\left(10^{\frac{C}{20}} - 1\right)}{10^{\frac{C}{20}} + 1}$$
$$R2 = \frac{2Z_0\left(10^{\frac{C}{20}}\right)}{10^{\frac{C}{20}} - 1} \tag{5.3}$$

Resistor R1 is chosen to optimally bias the amplifier. For a supply voltage of 7.5V, as will be applied in this case, the resistor value is chosen as recommended by the data sheet [44], as 120 Ω.

5.4.5 Filtering and Power Sensing

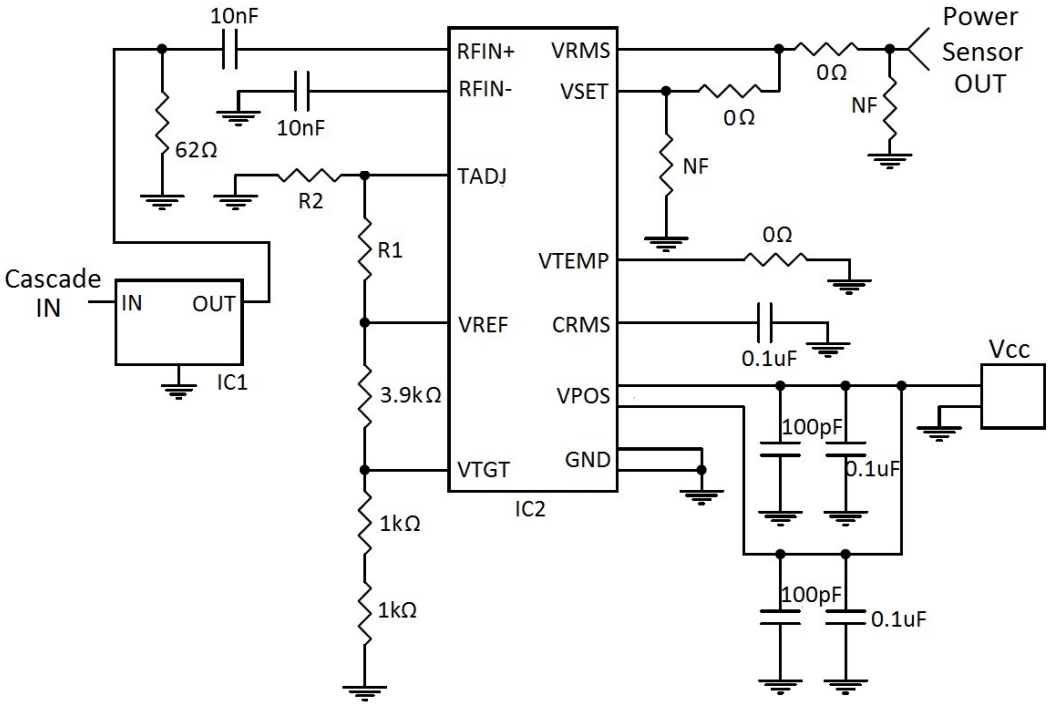

Figure 5.24: SAW filter and power sensor design schematic

The addition of a second filtration stage as the one implemented in the Filtering and Amplification section (5.4.4), has been included, labelled IC1, as a secondary measure in the event that the suppression of side-band interference

by the first filter stage is not sufficient. The Power sensor is designed exactly as in Section 5.3.3.1.

5.4.6 Final Product

Figure 5.25 is the top view PCB layout for the receive chain circuit. It is followed by a photograph of the assembled power sensor circuit PCB in Figure 5.26. As seen in the power sensor photograph, the PCB was split between the amplifier stage and the SAW filter to allow for easier testing. The changes from the original design and the photograph, is the removal of one amplification stage, replaced by the use of a connectorised Mini-Circuits amplifier, as well as the splitting of the PCB where the amplifier stage used to be.

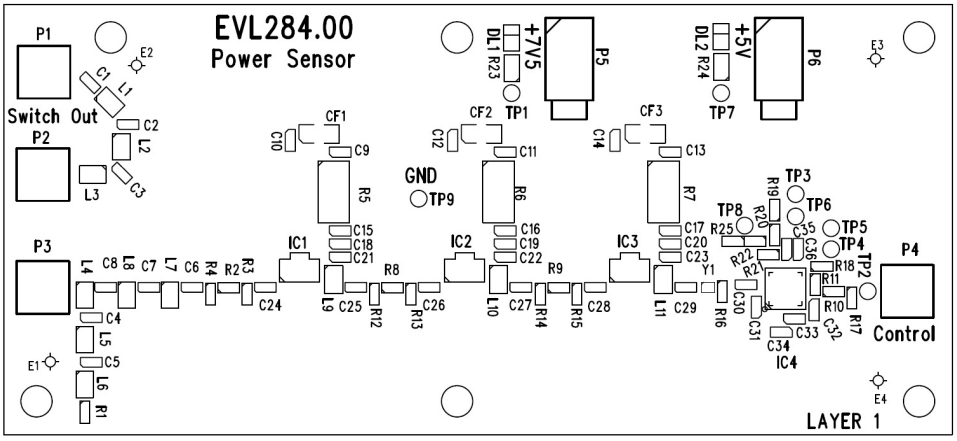

Figure 5.25: Top layer power sensor circuit PCB layout

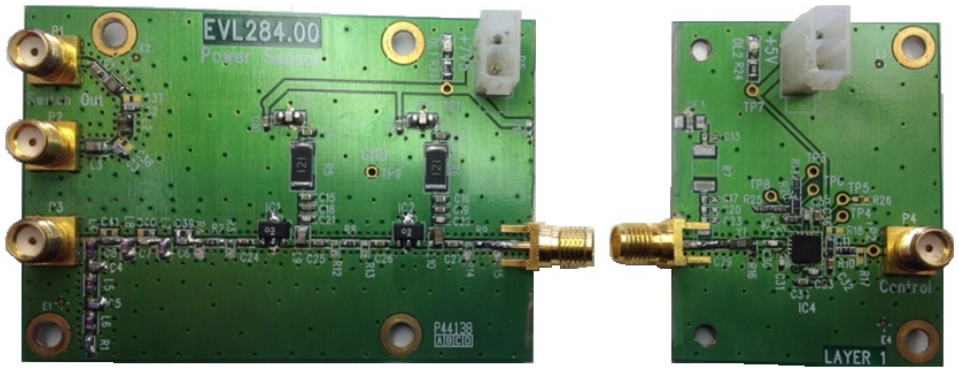

Figure 5.26: Photograph of power sensor circuit PCB

5.4.7 Testing

The two-port parameter readings, dB|S11| and dB|S21|, for the cascaded amplifier and narrow filter stage are plotted in Figure 5.27.

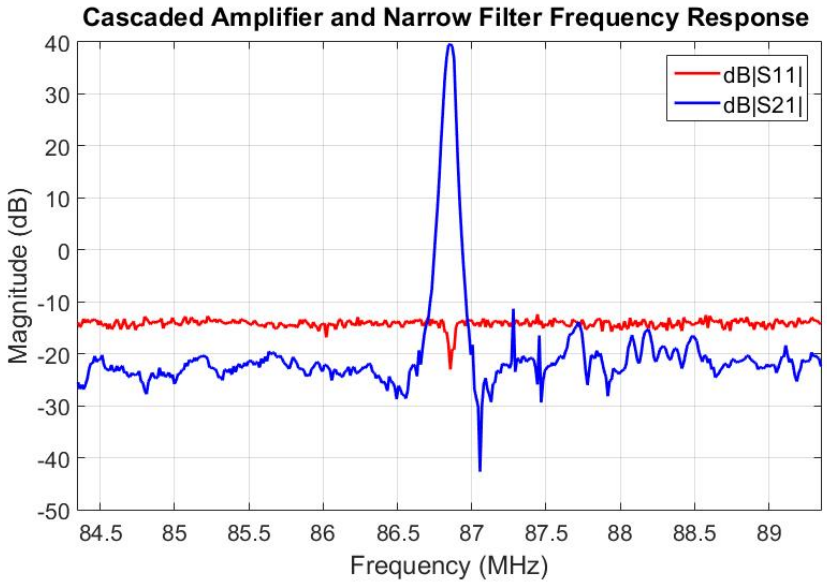

Figure 5.27: dB|S11| and dB|S21| of cascaded amplifier and Narrow Filter Stages

A sinusoidal signal of 460 MHz is fed into the power sensor circuit with the power level at the power sensor recorder for every 5 dBm step in amplitude of the sinusoid. The results are recorded and plotted in Figure 5.28.

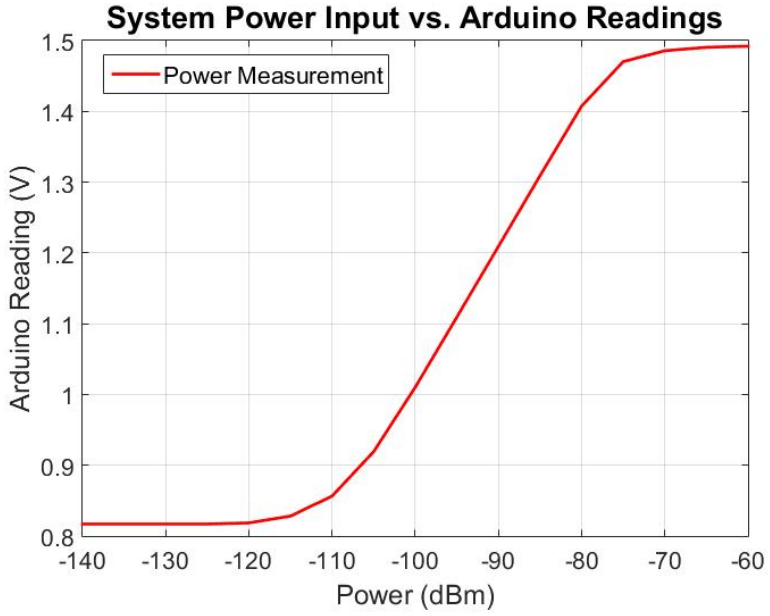

Figure 5.28: Input Sinusoid Power vs. Power Sensor Output Plot

5.5 Cancellation and Control Circuit Design

The cancellation block is one of the most essential parts of the cancellation system. The cancellation system is responsible for correctly generating an anti-noise signal that is correct in amplitude and phase. The error in phase and amplitude is directly responsible for the level of cancellation possible in the system. The resolution of the phase and amplitude modulation performed in the canceller, as well as the ability of the controller to adjust for the error, will determine the level of cancellation, as investigated in Section 2.2.

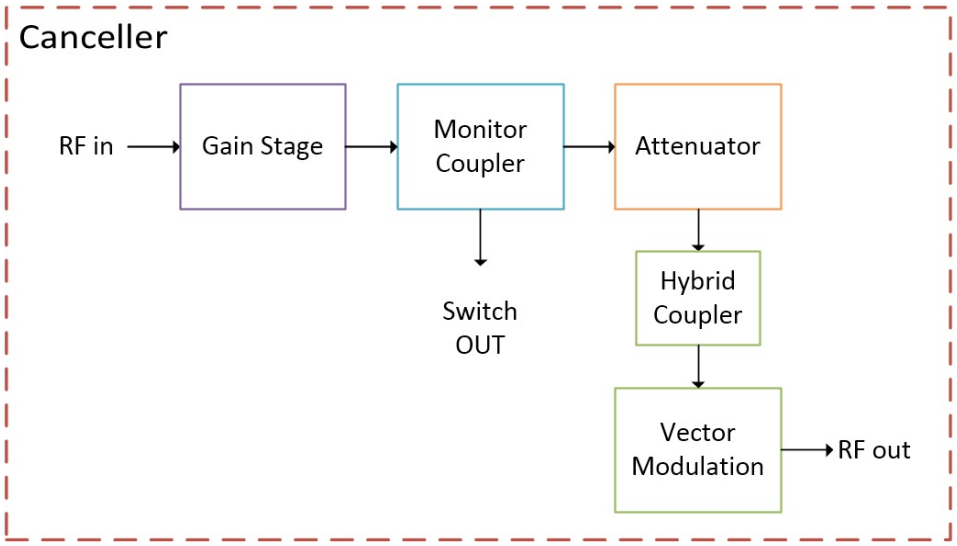

Figure 5.29: Top level block diagram of canceller circuit

Figure 5.29 is a block diagram representing the basic building blocks of the canceller system. The canceller system coarsely adjusts the amplitude of the cancel signal from where the vector modulator does fine amplitude adjustment and phase adjustment.

5.5.1 Amplification and Coupler

5.5.1.1 Amplification

The amplification stage in the canceller block works in conjunction with the digital step attenuator block. The attenuator is responsible for attenuating the signal to the same amplitude as the RF In communications signal. In order for the attenuator to operate correctly, the amplifier is required to amplify the incoming signal and allow for a buffer region wherein the attenuator can operate. The amplification stage design is the same as for a single stage in the cascaded amplification stage in Section 5.4.4.2.

5.5.1.2 Coupler

In order for the coarse amplitude adjustment stage to work correctly, the power at the PA reference point and the power of the RF In signals need to be compared. The coupler, or rather power splitter, as it has a 3 dB coupling factor, splits the signal equally. The outgoing signal continues on its path toward the attenuator whereas the coupled signal passes over to the input of the power sensor circuit through a 4 way SP4T RF switch. The controller switches between the different switch inputs to get a power reading at different points of the circuit.

The coupler used is a Mini-Circuits JPS-2-1W+ 3 dB power splitter. The package is a 6pin surface mount device.

5.5.2 Digital Attenuator

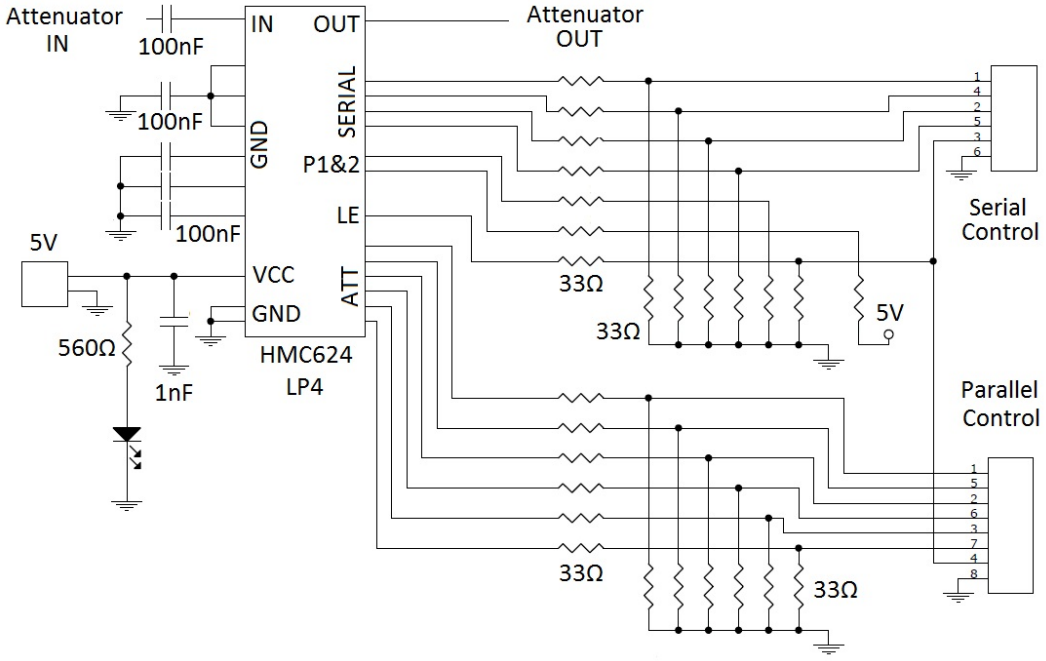

Figure 5.30: Design schematic of the digital step attenuator

The digital step attenuator chosen to perform the attenuation task is a HMC624LP4 IC. The package has two control method capabilities, serial and parallel. The parallel approach is chosen to control the attenuator but a control interface for both the serial and parallel interfaces are created in the event that the control method is required to change.

The IC attenuates from the IN port through to the OUT port. Various ground pins are required to allow for the attenuated signal to be dissipated. The IC requires a 5 V supply. The ATT pins are parallel control lines while the SERIAL lines control the serial communications. The pins P1 and P2 are set on device start-up to allow for a default power up attenuation level of 8, 16, 24 or 31.5 dB attenuation. LE is set low to allow for the start-up attenuation to be activated with P1 and P2 set to 8 dB.

All pins are serially driven through a 33Ω resistors. They are connected to either ground or 5 V in the event that no control line is connected, preventing any lines from floating.

5.5.3 Hybrid Coupler

The signal passes from the digital attenuator to the vector modulator where the refined phase and amplitude adjustments are performed. The vector modulator requires quadrature input signals in order to allow for the phase and amplitude to be adjusted through 2 DC control signals. A hybrid coupler, implemented with micro-strip and passive components to minimise the physical dimensions, is designed and implemented into the PCB to allow for the input signal to be split into its in-phase and quadrature components.

The test design is composed in ADS and optimised to have optimal reflection coefficients, minimal losses, as well as a 90° difference between output ports over the widest band possible. The resulting layout as generated by the software is plotted in Figure 5.31.

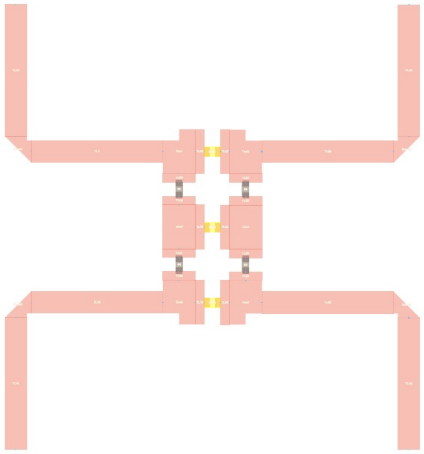

Figure 5.31: ADS layout of hybrid coupler

The design is manufactured using a Computer Numerically Controlled (CNC) milling machine onto a FR-4 substrate. The resulting circuit is represented in Figure 5.32.

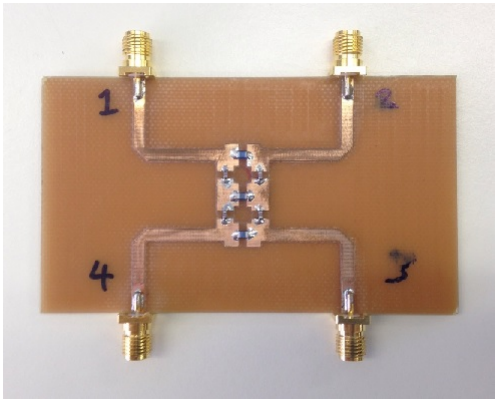

Figure 5.32: Image of final manufactured lumped hybrid coupler

The coupler is connected to a VNA and the performance of its operation is tested. dB|S11| and the balanced amplitude split at 460 MHz between the 2 output ports (dB|S21|, dB|S31|) are plotted in Figure 5.33. The phase balance between the 2 output ports is plotted in Figure 5.34. The difference equates to an almost perfect 90° split over a wide bandwidth.

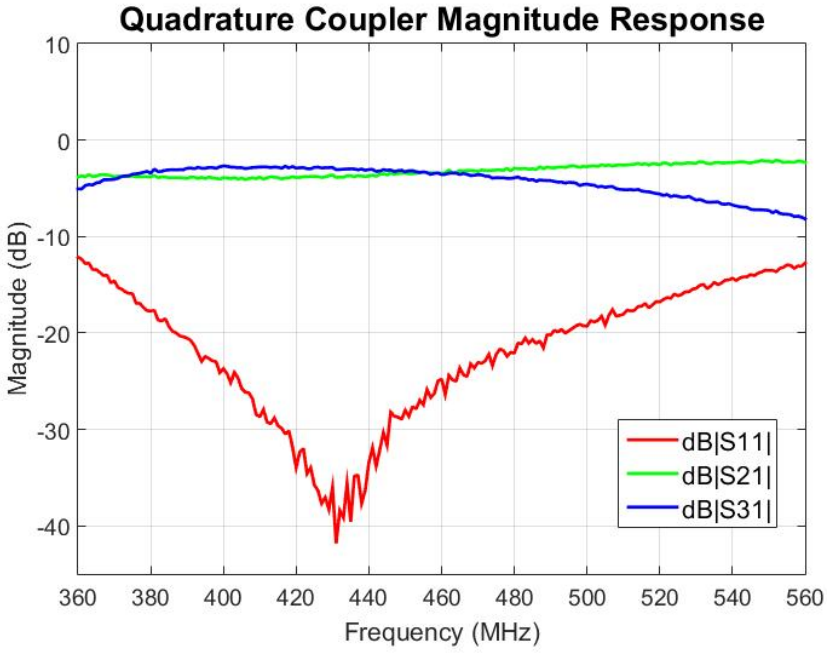

Figure 5.33: S parameters performance measurements of Hybrid Coupler

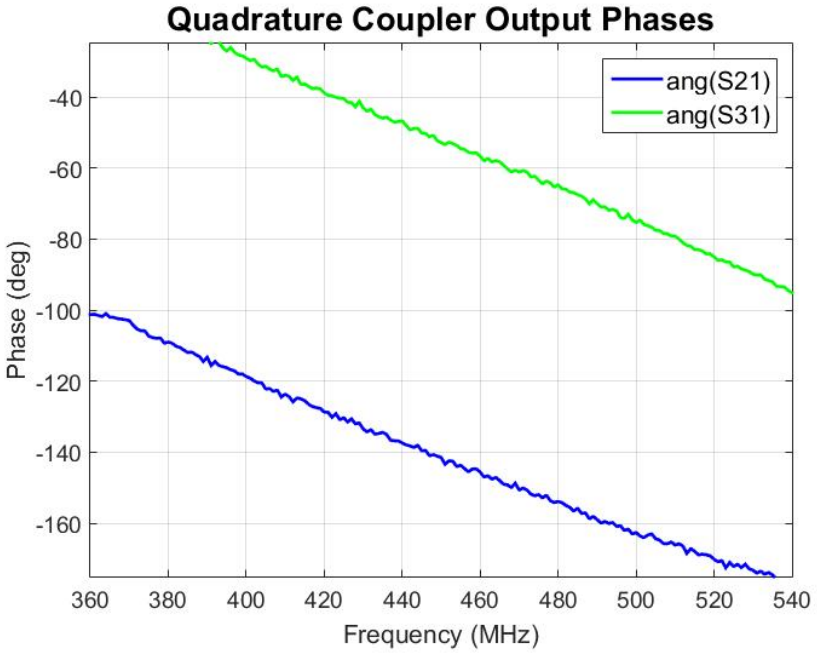

Figure 5.34: Hybrid coupler phase balance

The design is then successfully re-optimised to be suitable for the substrate onto which the PCB's will be manufactured as described in Section 5.2.

5.5.4 Vector Modulator

The vector modulator that will perform the fine amplitude and phase control is an evaluation board version of an ADL5390 vector modulator chip. The vector modulator is not implemented onto the cancellation control circuit board. The use of an evaluation board ensures that the IC is properly implemented and set up on a high standard PCB. The board has SMA connectors fitted along with all the required biasing and power points to allow for easy integration. Figure 5.35 is a photograph of the evaluation board.

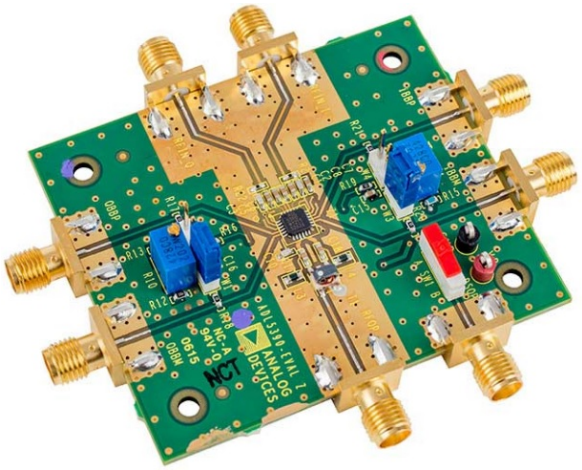

Figure 5.35: Photograph of ADL5390 vector modulator evaluation circuit

5.5.5 Final Product

Figure 5.36 is the top view PCB layout for the control circuit. It is followed by a photograph of the assembled control circuit PCB in Figure 5.37.

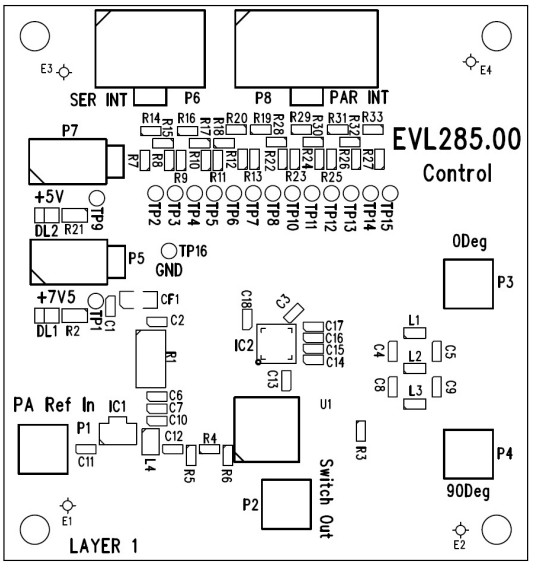

Figure 5.36: Top layer control circuit PCB layout

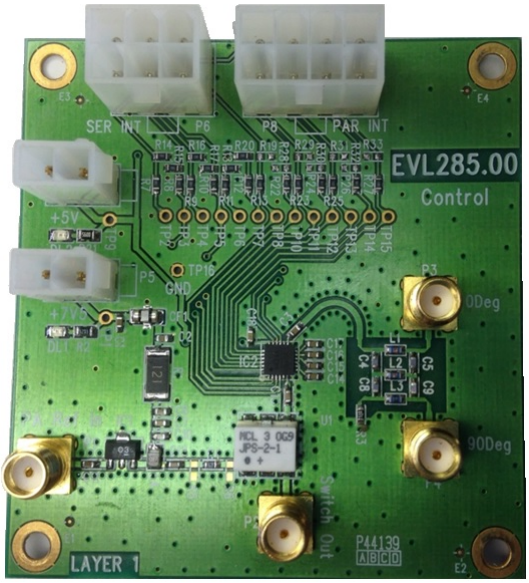

Figure 5.37: Photograph of control circuit PCB

5.5.6 Testing

The PCB for the cancellation control circuit is tested with a VNA to test the phase and amplitude balance from the input to the two output ports of the PCB. The input reflection coefficient S11 is also plotted in dB. The measurement does not include the vector modulator.

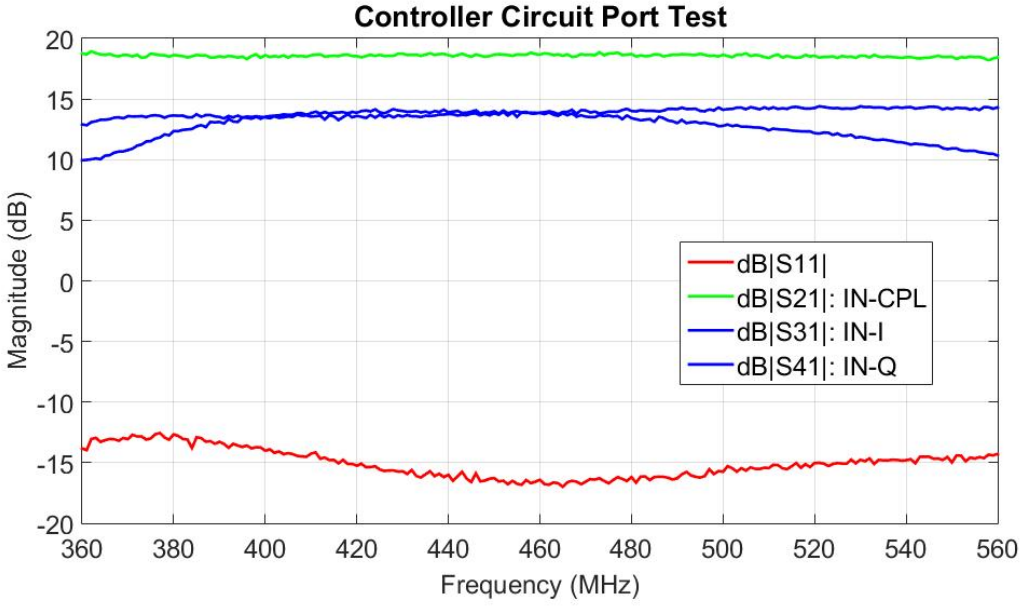

Figure 5.38: Port parameters of canceller PCB

5.6 Receive Chain Circuit Design

The Receive Chain circuit is a collective of power splitters and combiners, combined into a single PCB to perform the cancellation summation as well as signal sampling for use by the power sensor circuit.

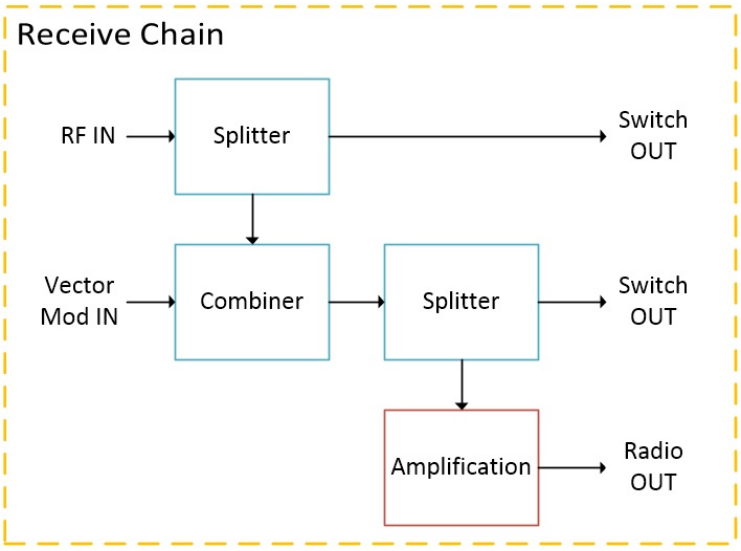

Figure 5.39: Top level block diagram of receive chain

5.6.1 Coupler Chain

The Receive Chain makes use of three JPS-2-1W+ power splitter/combiners. The first splits the incoming received signal line. The 3 dB split results in a signal that remains on the original path while the second part is passed to the power sensor as part of the coarse amplitude control system.

The second JPS-2-1W+ is used as a summation junction. It is at this point where the signal passed through from the previous splitter, and the cancellation signal resulting from the cancellation circuit, will combine. It is at this point where the cancellation occurs.

The final JPS-2-1W+ once again splits the signal as with the first. One half passes to the power sensor to compute the remaining power of noise within the band of operation while the other component from the splitter continues to the receiver radio where the receiver will demodulate the signals into audio speech signals.

5.6.2 Amplification

A final level of amplification, to the signal intended for the receiver, is implemented. The setup is a duplicate of the amplifier setup as performed in Section 5.4.4.2.

5.6.3 Final Product

Figure 5.40 is the top view PCB layout for the receive chain circuit. It is followed by a photograph of the assembled receive chain circuit PCB in Figure 5.41.

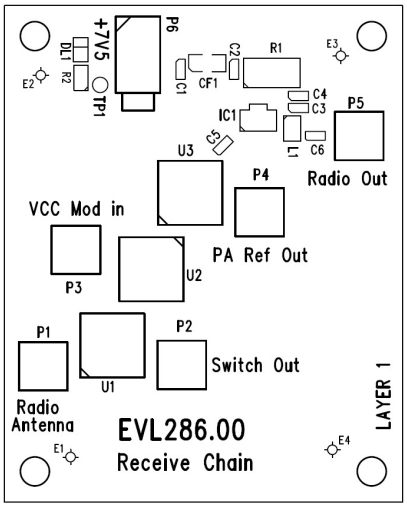

Figure 5.40: Top layer receive chain circuit PCB layout

Figure 5.41: Photograph of receive chain circuit PCB

5.6.4 Testing

Figure 5.42 is a network analyser frequency plot for the receive chain circuit connection points. The analyser is connected to the input, the two switch sample point outputs, PA Ref Out and Switch Out, as well as the circuit output. The VCC Mod In port is terminated with a 50Ω load. The drop of signal level for each coupler can be observed as well as the gain provided to the output by the output amplifier.

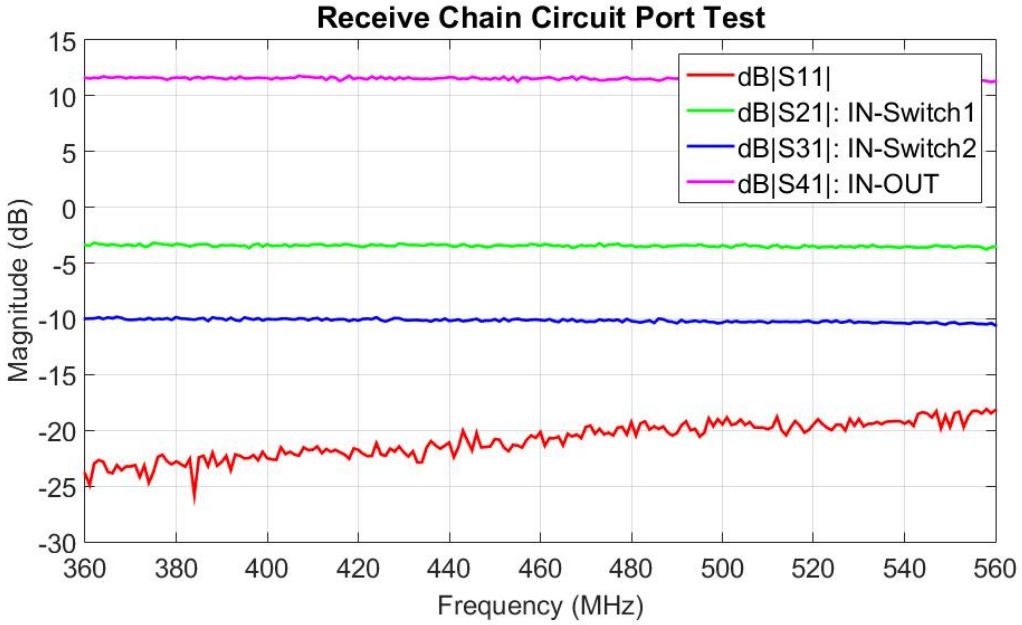

Figure 5.42: Measured frequency response of receive chain circuit

5.7 Controller - Arduino Implementation

5.7.1 Pin allocations

The purpose of the controller circuit is to combine and process all information generated by the circuit components and create outputs for the user to observe, trigger essential circuit components and adaptively adjust cancellation parameters.

A few essential requirements for the controller are a processor to perform instructions coded by the user, sufficient input and output pins, as well as Digital to Analog (DAC's) converters to perform the conversion of the digital logic data into a usable analog signal to adjust the I/Q values of the vector modulator. The Arduino Due project board has an IDE with an easily implementable C code environment, as well as 2, 12-bit DAC channels to

Requirement	Number of Pins	Connection Type
Attenuator Serial Connection	6	Digital Output
Attenuator Parallel Connection	8	Digital Output
Limiter Status	2	Digital Input
Switch Control	2	Digital Output
Power Sensor Measure	1	Analog Input
Vector Control	2	Analog Output

Table 5.3: Arduino pin requirements

perform the I/Q channel control. It is selected for its ability to convert digital to analog conversion, its ease of access, as well as cost. A breakdown of the pins required for operation are as follows:

Figure 5.3 labels all the required pins as they have been allocated on the Arduino Due according to Table 5.3. Some other critical components are also labelled.

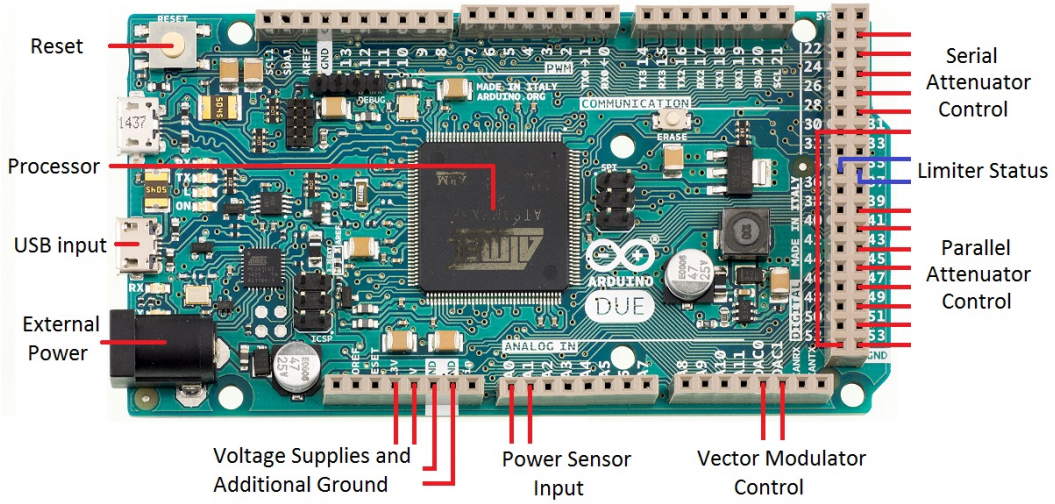

Figure 5.43: Arduino Due with essential pins labelled

5.7.1.1 Switch Control

Three different measures of power occur in the system. The first two being the coarse amplitude control measures with the third being the post cancellation power measurement. As mentioned in the power sensor design chapter, the power sensor circuit consists of one measurement line in order to prevent redundancy. The use of a 4 way non-reflective RF switch allows for the controller to switch the input to the power sensor circuit between all three power measurement requirements using 2 digital lines. A HMC244 evaluation circuit was available and implemented.

5.7.1.2 Attenuator Control

The switching between the switch inputs allows for the controller to acquire the level of power in the input and reference channels in order to perform coarse amplitude control. The power sensor DC power level indication from the ADL5906 is received at the analog in port A0 (A1 spare) as indicated in Figure 5.43. It will compare the two coarse adjustment power measurements and implement the necessary attenuation according to the power sensor output slope.

The attenuator will connect via ribbon cable to the ports as indicated in Figure 5.43. Lines for serial and parallel control will be implemented with the parallel approach active.

5.7.1.3 Vector Modulator Control

Once the coarse amplitude control is completed, the power is measured at the point after signal cancellation has occurred. From here the controller will drive the I and Q analog DC control lines of the vector modulator in order to adjust the phase of the reference signal as well as its amplitude. The cancellation process is continually repeated throughout the cycle of the controller in order for the reference signal to adapt to any changes that affects cancellation accuracy.

5.7.1.4 Protection Limits

A single pin is allocated for each protection circuit. If the hard limit of the active limit stages on the protection circuits are activated, the user interface will inform the user and prevent the controller from making large incorrect changes based on the drop of input due to the limiting of the power sensor circuits.

5.7.2 Arduino Level Converter Interface

The use of an Arduino Due in order to make use of the build in DAC features, also has a drawback. The maximum input voltage tolerated by the Arduino input ports is 3.3 V, compared to the standard 5 V as with all other Arduino boards. In order to allow for the Arduino to receive and read 5 V signals, as well as output 5 V signals for use in the system, a voltage interchange interface is required.

A SparkFun BSS-138 bidirectional level converter interchanges levels according to the reference voltages supplied to the circuit. By using the 3.3 V and 5 V supply output pins on the Arduino Due as reference lines connected to the LV and HV lines of the BS-138 respectively, it would be possible to perform

all 5 V system operations while still maintaining 3.3 V input and output levels at the Arduino ports.

The multiple level converters required are mounted on a breadboard.

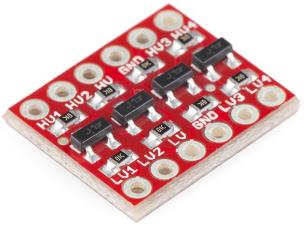

Figure 5.44: SparkFun level converter image

5.8 Supply Network Design

The purpose of the supply network is to provide power to all the components and circuits in the system from a single DC input power supply. The power network is divided into three main components.

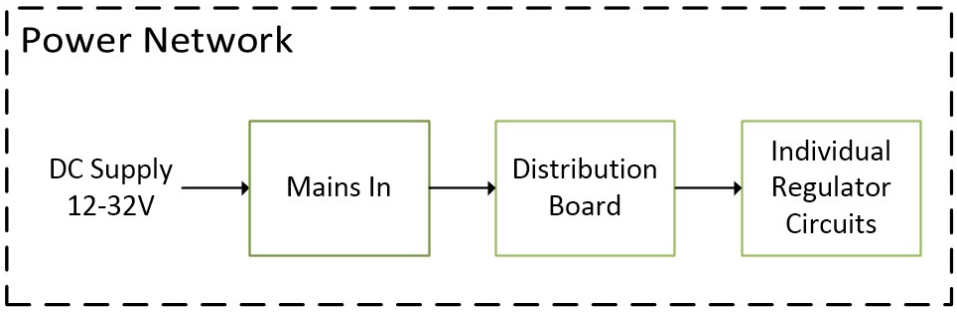

Figure 5.45: Block diagram of power network layout

5.8.1 Main Supply

The main supply circuit receives the DC supply, in the form of a DC laboratory power supply, and adds fault protection. The use of the built in current limiter of this device is an additional fault protection mechanism.

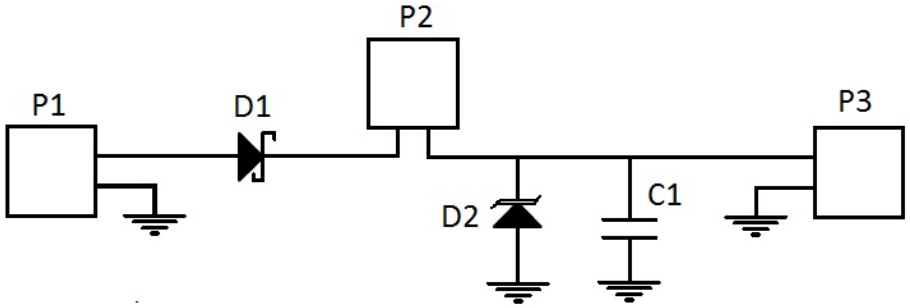

Figure 5.46: Power network mains

P1 is the DC input point. The standard DC supply banana plug interface will be used at this point. D1 is chosen as a SS1P4L-M3 Vishay Schottky diode. It prevents current flow in the event that the supply polarity is incorrectly connected.

P2 is a Molex Minifit JNR connector that wires to a fuse mounted on the system enclosure. The fuse is a 1A cartridge fuse. The total current draw for the circuit is roughly 0.5A allowing for a buffer in the event that more current is required up to 1A.

D2 is a SMAJ33A transient voltage diode that clamps any supply voltage levels above 33 V in order to protect the subsequent LM317 regulator circuits.

C1 is a decoupling capacitor with a capacitance value of 68uF and a voltage rating of 63 V. P3 is a representation of the distribution circuit connection point.

5.8.2 Distribution Circuit

The distribution circuit is a simple connector board with the sole purpose of splitting the mains supply line into multiple plug points into which the numerous regulator circuits for each component can connect. The board will accept the output from the board in Figure 5.46 and split it into multiple Minifit JNR receptacles. The distribution circuit will require a minimum of 12 receptacle points for the components of the system. Allocations for 14 receptacles will be made to allow for future connections.

5.8.3 Regulator Circuits

Each supply voltage requirement for each sub-circuit will be allocated a separate voltage regulator circuit. They will be supplied via the output ports of the distribution circuit. The modular nature of the regulator boards allow

them to be placed in close proximity to the device they will power and allow for them to be moved around within the enclosure of the canceller system to allow for space optimisation.

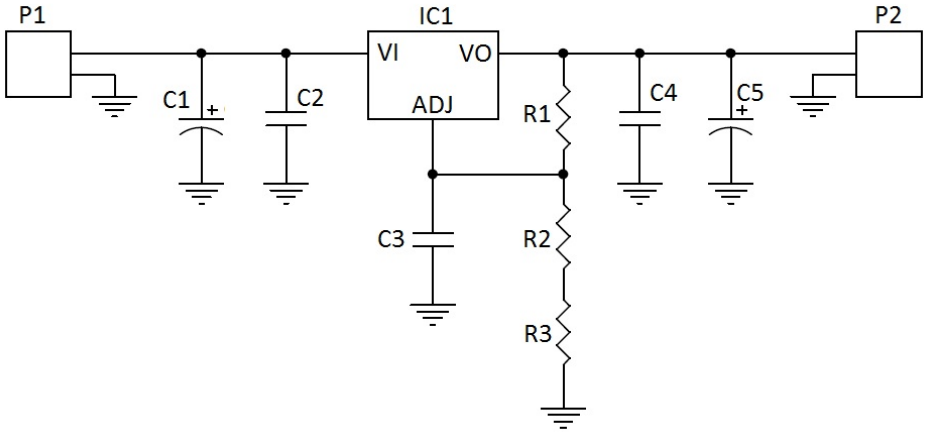

Figure 5.47: Regulator design schematic

The regulator circuit in Figure 5.47 is a LM317 based regulator circuit that can be setup to provide 1.5A over an output voltage range of 1.2 V to 37 V. The output voltage level is controlled by the resistor values R1, R2 and R3. R1 is kept constant at 240 Ω. Solving for R2 and R3 to allow for 3.3 V, 5 V and 7.5 V regulated voltages is done as follows:

$$V_{OUT} = 1.25V\left(1 + \frac{R2 + R3}{R1}\right)$$
$$R2 + R3 = \left(\frac{V_{OUT}}{1.25} - 1\right)R1 \tag{5.4}$$

5.8.4 Final Product

Figure 5.48 contains the top layer PCB for the cascaded Main Supply and DC distribution circuit. Figure 5.49 is a photograph of the Main Supply and DC distribution PCB manufactured in-house using a LPKF100 PCB milling machine. It is followed by the top layer PCB layout of the LM317 based regulator circuit and a photograph of the regulator circuit in Figures 5.50 and 5.51 respectively.

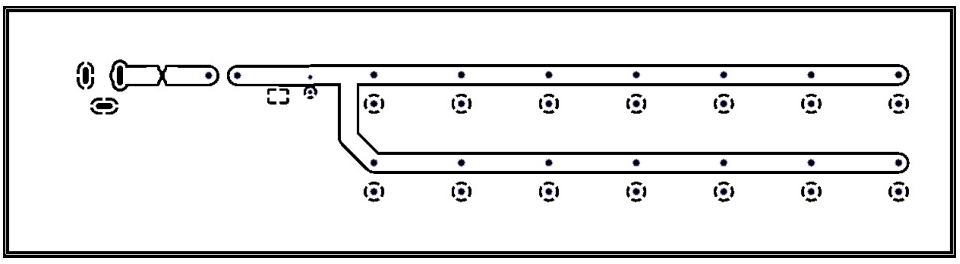

Figure 5.48: Top layer DC distribution circuit PCB layout

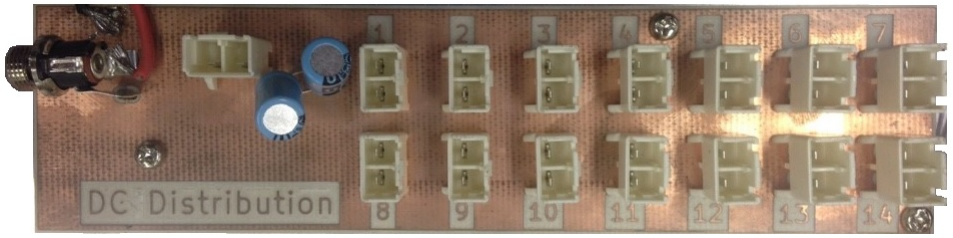

Figure 5.49: Photograph of DC distribution circuit PCB

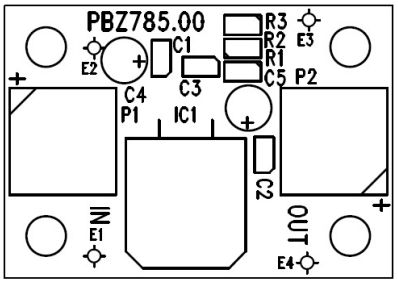

Figure 5.50: Top layer regulator circuit PCB layout

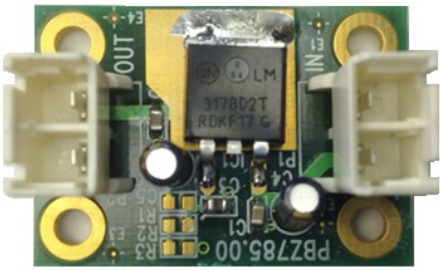

Figure 5.51: Photograph of regulator circuit PCB

5.9 Controller Code Structure

5.9.1 Controller Code Design

The cancellation system makes use of two programmed interfaces; The Arduino embedded code and the GUI code. The GUI receives instructions from the user which it passes to the Arduino. The Arduino will perform the relevant action as commanded by the user and return the resultant data via the user interface in the form of a data feed or graphical plots. The communication flow is described in Figure 5.52.

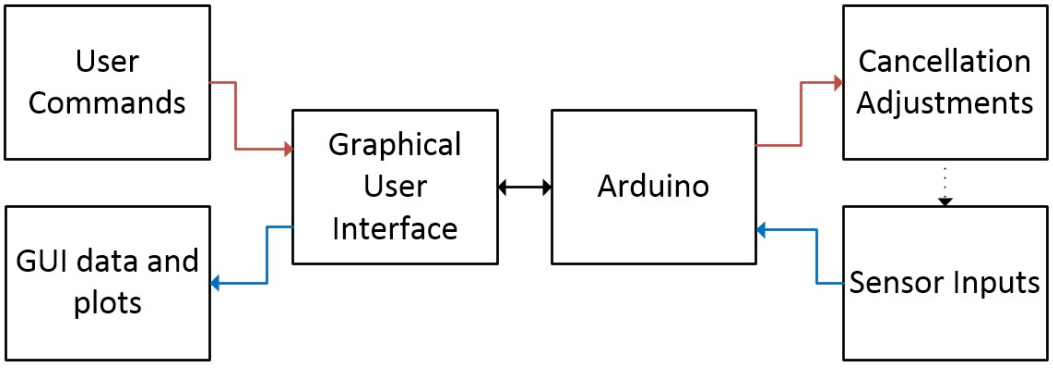

Figure 5.52: Block diagram of data flow and communication interface

The Arduino code utilises 6 basic functions. All functions are encapsulated into a single case statement. The code performs each function once (except for autonomous mode), and returns to the top of the case awaiting the next function instruction. After each execution of a single function, a set of uniform results is returned. The functions are:

1. Autonomous Cancellation Mode
2. Digital Attenuator Manual Mode
3. Digital Attenuator Auto Mode
4. Vector Modulator Magnitude Change
5. Vector Modulator Phase Change
6. Switch Read

5.9.1.1 Autonomous Mode

In autonomous mode, the user selects the Auto Cancel button on the GUI. The autonomous digital attenuator coarse amplitude control (3) function is run once. The Arduino then reads the cancellation error power sensor output. It makes a series of stepped changes to the vector modulator amplitude with the steps defined by the measured error range. For every modulator adjustment, the error level is read and the minimum error value recorded. The vector modulator is then set to the value that achieved the minimum. The process is repeated for the phase. The entire process is then repeated until the cancellation is at a maximum.

Every change made to the vector modulator I and Q values and error measurement is passed to the GUI and plotted.

5.9.1.2 Digital Attenuator Manual

Once the user activates any of the sliders or spinners on the GUI that adjust the digital step attenuator, the Arduino is passed into the case statement encapsulating the manual digital attenuator code. The code then awaits the value to which the attenuator is to be adjusted. Each adjustment returns the power sensor error value and plots it for each attenuator change.

5.9.1.3 Digital Attenuator Auto

By selecting the Auto Coarse Cancellation Button on the GUI, the Arduino measures the power in each channel of the system. It then calculates the correct attenuator level based on the difference and sets the attenuator to this level. It is this function that is performed by the autonomous cancellation mode as a precursor to autonomous vector adjusting by the vector modulator.

5.9.1.4 Vector Modulator Manual

For both functions 4 and 5, the vector modulator I and Q values are adjusted in order to change the vector modulator vector amplitude and phase respectively. The user enters a value into either the magnitude or phase boxes. By selecting one of 4 buttons, the user can increase or decrease the amplitude or phase by the value that has been entered. The values for the new updated I and Q values are plotted for each change the user makes. The power sensor output for the error plot is also updated for each user change. These functions, along with function 2, allows for complete manual cancellation. To change the magnitude, the vectors are changed trigonometrically by the code in order to maintain the vector angle. The same applies to changing the phase, whereby the vector magnitude is kept constant while the vector is rotated.

5.9.1.5 Switch Read

The Switch Read function rotates through each of the switch inputs, records the results, and returns the result to the GUI where it is printed in the data feed. It is used as a troubleshooting tool and allows the user to get a sense of the levels of signals around the circuit.

5.10 Additional Test Rig Components

5.10.1 Lines and Connects

Interconnects between the numerous PCB's and connection points of the circuit are LMR-100-UF coaxial lines. The final layout design of the PCB's and components on the test rig is compiled and line distances between the numerous connection points measured. The coaxial lines are then constructed to specification with straight or right angle SMA connections, depending on which is more suitable.

5.10.2 RF channel delay

An important component of the final system build is the coaxial interconnects between the multiple PCBs and external connection housings. The reference channel and the RF IN channel need to have the same delay in order for cancellation to be successful. The signals involved are non-periodic, indiscriminate signals. For cancellation to be possible, the anti-phase version of the noise at the summation junction needs to be coherent in delay. If the anti-phase signal generated by the cancellation circuit is behind, due to the delay of the numerous cancellation components, cancellation will not be possible. The phase of the cancellation can be altered by the vector modulator in order to perfect cancellation, however, it cannot advance the signal in time.

To allow for the signals to align in time, a delay line is required on the RF IN line to allow for the signal to be delayed until it reaches the summation junction. A single coaxial line, long enough to provide sufficient delay, is inserted between the input of the RF IN channel and reference coupler through output.

5.11 Complete Canceller Rig

A sturdy enclosure or mount for all the components of the total system is required to allow for continual transport, fault finding and testing. By mounting all the components on a sturdy surface, the results will be repeatable and most of the strain on the components removed. By adding a connection

front end to the mount, no repetitive connections are required on the fragile PCB's, but will instead be connected to sturdier front end connectors.

A hard wood board, roughly 10 mm thick, will be used as the base. The individual components will be mounted onto a steel sheet using M3 standoffs, nuts and bolts, which in turn will be bolted to the wood surface. This approach will allow for design flexibility as well as an electrical ground plane for the devices. The standoffs are plastic or steel depending on the grounding required.

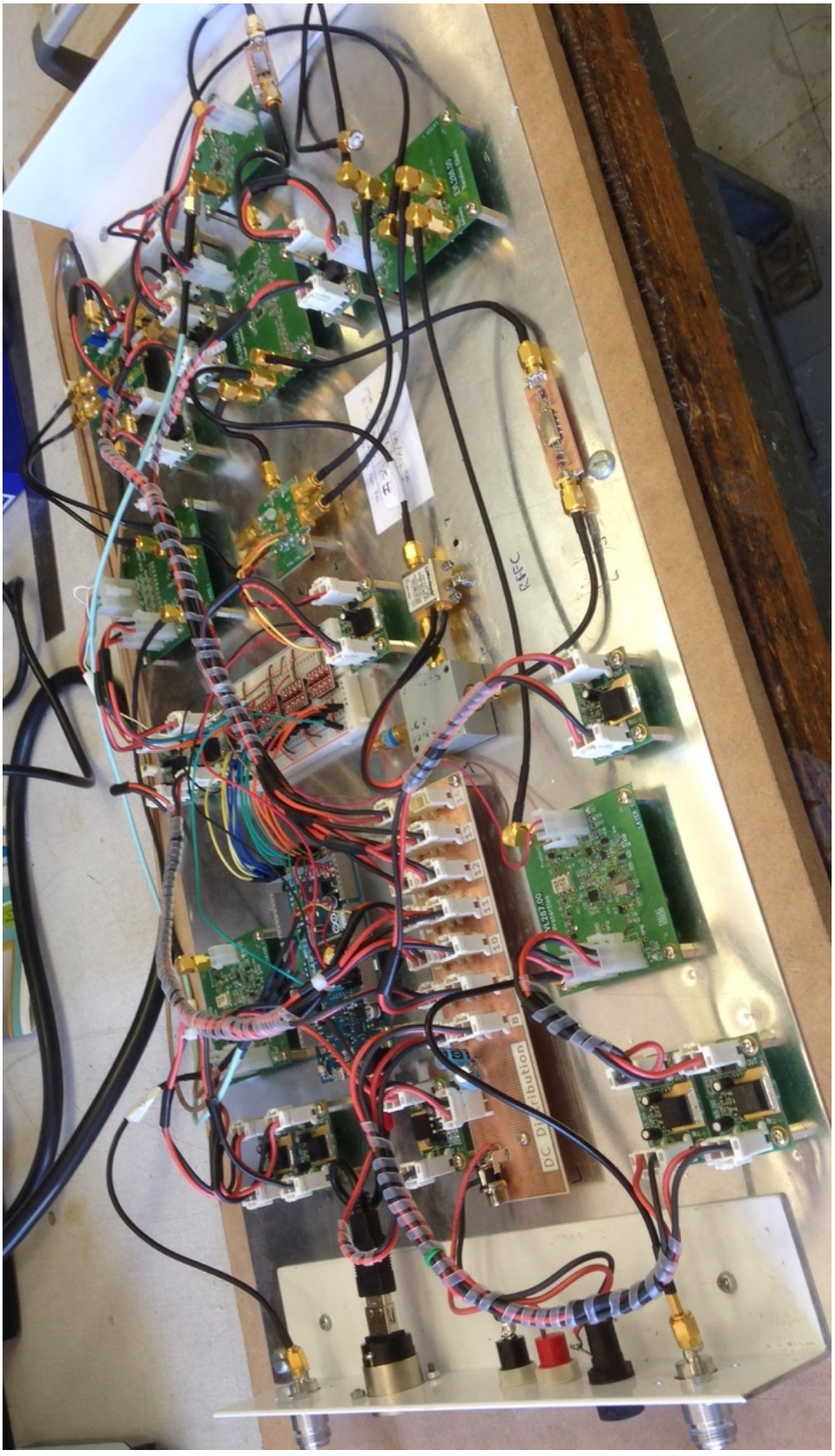

Figure 5.53: Top view photograph of complete canceller mount

Figure 5.53 is a top view photograph of the entire cancellation system with all components in place and connected. Figure 5.54 is a front view of the rig demonstrating the connection plate. This 90° bend steel plate houses all the connectors that extend into the relevant connection points on the circuit components. It improves appearance and allows for a sturdy connection point that will alleviate repeated connection and disconnection strain from the circuit components. Handles were also added for easier carrying.

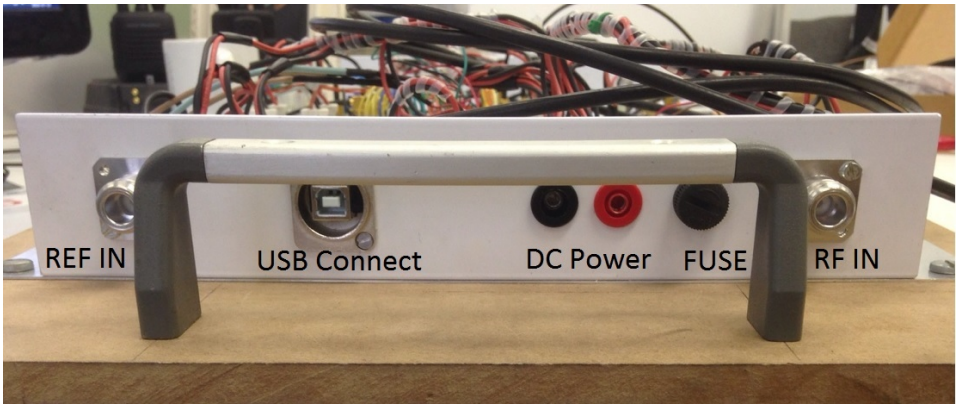

Figure 5.54: Front view photograph of canceller mount front connection end

5.12 Chapter Closing Summary

The chapter has detailed the design of all the design blocks and sub design blocks of the canceller system. The complete design schematics can be seen in Appendix B. The following chapter will mathematically reduce the system block diagrams into equations, allowing for optimisation of the canceller for future development.

Chapter 6

Optimisation and Further Considerations

6.1 Chapter Summary

Characterisation of circuit parameters such as the third intercept point for the circuit, as well as the noise figure of the whole system, is an important tool that could be used to optimise component choices and the sequences in which they appear in the design. Mathematical analysis of these system characteristics will be instrumental in identifying the role of each of the circuit parameters for future product development.

The Noise Figure (NF) of the cancellation channel system is analysed, followed by a derivation for the system Third Intercept Point (IP3) as well as SINR. A function that can be used for determining the optimum coupling factor is also derived. These considerations were not implemented in the design as presented in Chapter 5, as the design took place in the early stages of the project in order to meet the project time deadlines.

6.2 System Noise Figure Analysis

An important goal is to limit the contribution of the canceller to the noise figure of the total system. Design and optimisation of canceller components to limit their noise contribution will effectively increase the amount of cancellation possible by minimally degrading the sensitivity of the receiver [18].

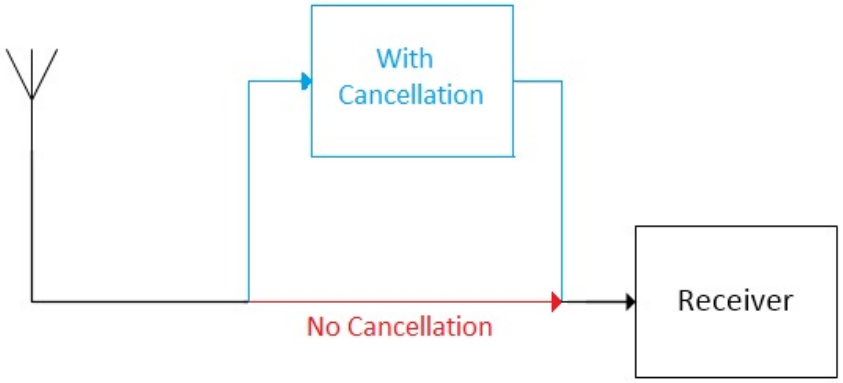

Figure 6.1: Signals received via cancellation channel

Figure 6.1 represents a system with two path possibilities. The first path possibility, coloured in red, is a receiver without the presence of a cancellation system. The incoming signals from the receiver antenna go directly to the receiver. A simplified presentation of the system, with the cancellation system present, can be observed as the path that is blue in colour. The cancellation block in this figure represents a cascaded chain of devices and circuitry that make the cancellation of interference signals possible, however, the presence of each of the components adds to the degradation of the signal to noise ratio of the system.

The radio receiver, such as the Vertex Standard VX-160EU, has a 20 dB SINAD of -111 dBm, a standard receiver integrity test. This allows for the radio to receive signals with a minimum power of -111 dBm while maintaining a signal to noise ratio of 20 dBm. The complication of this phenomenon limits the amount of noise that can be added by the introduction of the cancellation blocks prior to the receiver without reducing the minimum detectable signals too considerably. The noise contributions of components must be weighed against their ability to add to the overall cancellation effectiveness. At some point, the cancellation a device can provide, is outweighed by the noise it contributes to the system.

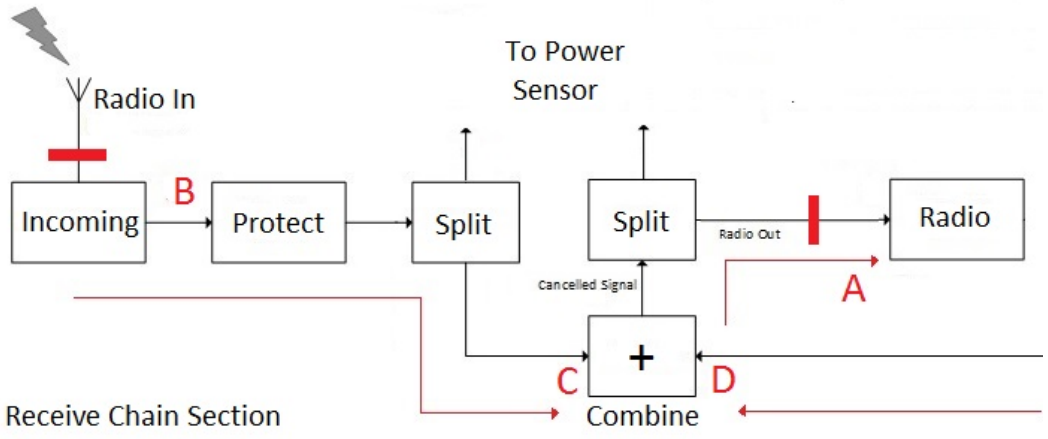

Figure 6.2: Insert of the block diagram of the cancellation system

Figure 6.2 is an insert of the receiver section of the cancellation block diagram. If the cancellation system was absent, the points A and B would be directly connected to the effect of the red line in Figure 6.1. The signals from the antenna would be directly received. The presence of the cancellation systems allows for extra noise to be injected into the receive chain. Cascaded noise at points C and D due to cancellation system components, are added in the combiner and added to point A. This added noise should be minimised where possible to allow for the cancellation system to affect the receiver as little as possible.

6.2.1 Canceller Circuit Component Sequence Optimisation

An important factor, along with shielding, individual component noise figures, and RF build techniques, is component sequences. The order of a cascaded group of circuit components, by the cascaded noise figure equations, can have an astounding effect on the overall cascaded noise figure of the component group. The cancellation circuit, namely the digital attenuator, amplifier, coupler, and vector modulator will be considered as listed below.

1. Amplifier
2. Attenuator
3. Coupler
4. Vector Modulator

Component	Gain (dB)	Noise Figure (dB)
Amplifier	20.1	3.5
Coupler	-3.5	3.5
Attenuator	-16.6	16.6
Vector Modulator	0.5	20.5

Table 6.1: Cascaded cancellation components gains and noise figures

Sequence	Noise Figure (dB)
1	20.5
2	25.3
3	20.5
4	23.3
5	7.4
6	6.2

Table 6.2: Cascaded noise figure for different component sequences

Table 6.1 contains the gain and noise figure levels for the various components as used in the system design. Where the noise figure or gain values were not supplied by the datasheet for the specific operating conditions, they were measured. The cascaded noise figure equation in the literature study of Chapter 3.2.3 is applied to these values using a basic MATLAB script.

The various sequence sets that were tested are displayed below. Not all of the sequences are logically valid for the operation of the circuit, but aim to indicate the vast effect component sequences can have.

1. Gain - Coupler - Attenuate - Vector Modulation
2. Attenuate - Coupler - Gain - Vector Modulation
3. Gain - Attenuate - Coupler - Vector Modulation
4. Attenuate - Gain - Coupler - Vector Modulation
5. Gain - Coupler - Vector Modulation - Attenuate
6. Gain - Vector Modulation - Attenuate - Coupler

The cascaded noise figure for each of the combinations from the list above are as follows:

From the results in Table 6.2, it is obvious that the final sequence will have the lowest cascaded noise figure. Referring to (3.2.3), it is clear that the

effects of each component in the chain is dependant on the gain of the previous elements. The vector modulator has a large noise figure, whose effects can be greatly minimised by preceding it with high gain components. (Moving the attenuator as far back as possible). The very large noise figure of the attenuator is then reduced by its division by the cumulative gains of the previous elements. All the elements preceding the attenuator have greater gains. These factors all contribute to sequence 6 being the most effective.

The sequence that was manufactured was sequence 1. If the sequence of the components were redesigned to match that of sequence 6, the total noise figure could be reduced by three-fold. These design considerations will be useful for a second iteration build along with additional considerations made in Section 8.2.

6.2.2 Total System Noise Figure

The analysis of the entire cancellation branch will allow for the characterisation of each of the components in the overall noise figure. By mathematically reducing the cascaded noise figure of the system into a single equation, we will be able to identify which components have the largest effect on the noise figure [37]. Minimisation of this noise figure will allow for increased cancellation performance by eliminating unnecessary noise introduced in the cancellation chain.

The inclusion of the couplers that provide signal power splitting and summation into the equation will allow for the optimal coupling value to be calculated, further increasing the level of cancellation. The total system is presented as a flow diagram and reduced until a single noise figure equation can be calculated. This process is described in Figures 6.3 to 6.5.

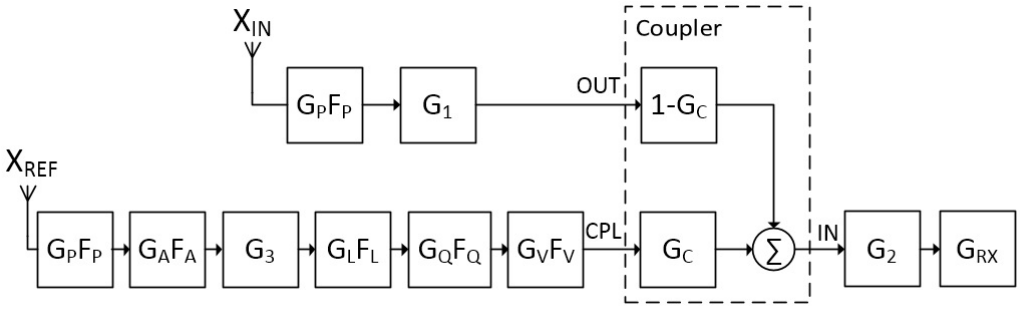

Figure 6.3: Step 1 of circuit noise figure analysis breakdown

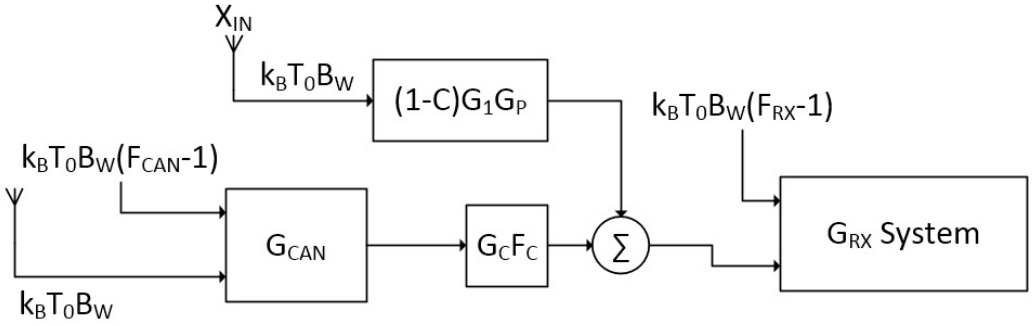

Figure 6.4: Step 2 of circuit noise figure analysis breakdown

In Figure 6.4, the system is reconstructed into simplified equivalent blocks. The blocks are assumed ideal with no internal noise, but rather with the noise specified at the inputs. The total noise for the lower branch is combined into a combined noise figure block, G_{CAN}.

$$G_{CAN} = G_P G_A G_3 G_L G_Q G_V \tag{6.1}$$

$$F_{CAN} = F_P + \frac{F_A - 1}{G_P} + \frac{F_3 - 1}{G_P G_A} + \frac{G_L - 1}{G_P G_A G_3} + \ldots \\ \frac{F_Q - 1}{G_P G_A G_3 G_L} + \frac{F_V - 1}{G_P G_A G_3 G_L G_Q} \tag{6.2}$$

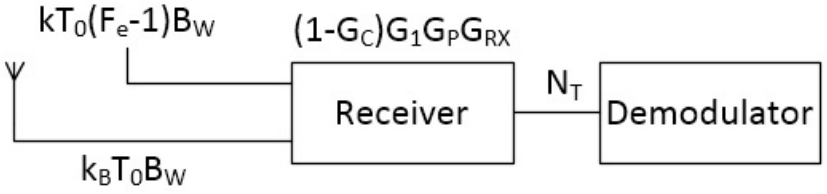

Figure 6.5: Step 3 of circuit noise figure analysis breakdown

Figure 6.5 is a further condensed formulation of the system, with total noise N_T at the demodulator,

$$N_T = k_B T_0 B_W G_{RX}(G_{CAN} F_{CAN} G_C G_2 + (1 - G_C) G_1 G_P G_2 + F_{RX} - 1) \quad (6.3)$$

This equation can be reformulated in terms of the total noise figure of the system, F_e, as shown in figure 6.5. If we rewrite (6.3) in terms of the effective total noise figure,

$$N_T = [k_B T_0 B_W + k_B T_0 (F_e - 1) B_W](1 - G_C) G_P G_1 G_{RX} \quad (6.4)$$

F_e, from (6.3) and (6.4), is given by,

$$F_e = \frac{G_{CAN} F_{CAN} G_C G_2 + (1 - G_C) G_1 G_P G_2 + F_{RX} - 1}{(1 - G_C) G_P G_1} \quad (6.5)$$

The total noise figure decreases with a decrease in the coupling level of G_C.

6.3 Third-order Intermodulation Analysis

6.3.1 Third-order Intercept Point

This section of the text derives an expression for the IP3 point of the cancellation system [37]. A block diagram representation will be used to determine the expressions.

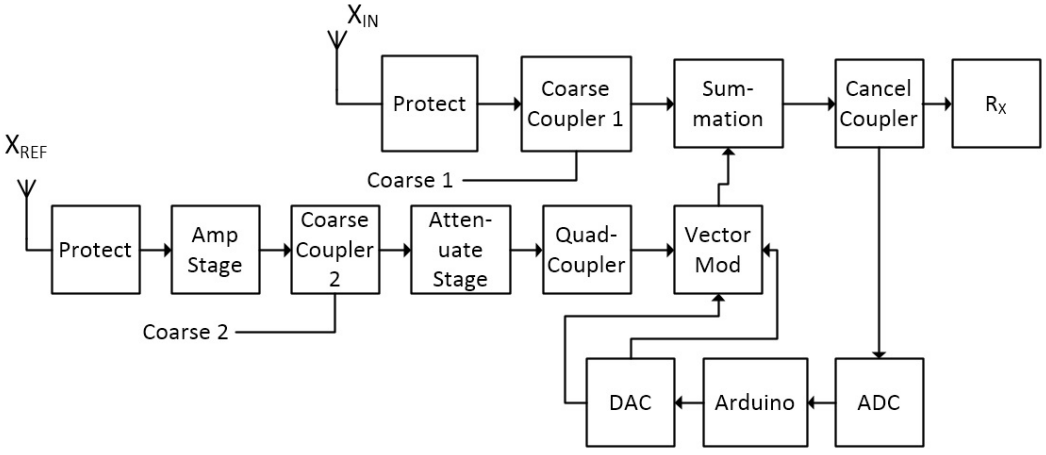

Figure 6.6: Step 1 of IP3 analysis breakdown

Figure 6.6 is a block representation of an I and Q channel controlled vector modulator based cancellation system. In order to analyse the system, it is redrawn as presented in Figure 6.7. The coupler that performs the summation of the signals X_{IN} and X_{REF}, as well as the couplers, G_1, G_2, and G_3 are redrawn in the figure. The summation coupler is restructured into a coupling path gain of G_C and through path gain of $1-G_C$. Only the through path gain of the remaining couplers are considered as G_1, G_2 and G_3.

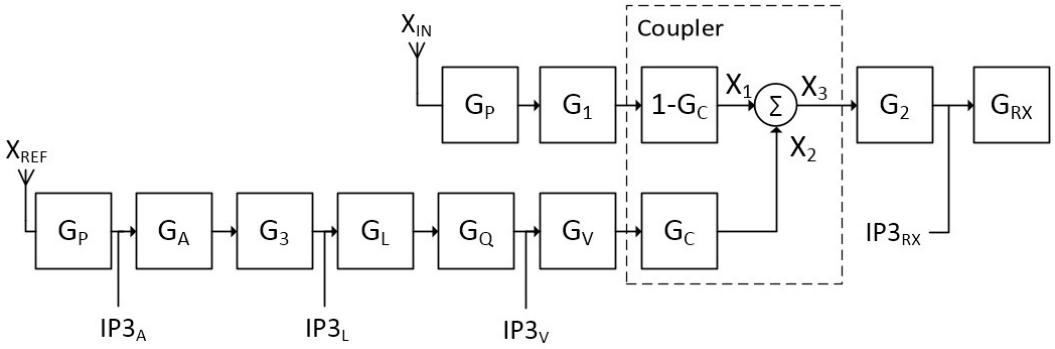

Figure 6.7: Step 2 of IP3 analysis breakdown

The system is simplified with a single input in Figure 6.8. Passive devices such as couplers, attenuators and the protection circuits (active limiting state not considered) do not have IP3 values, and so, the cascade of the coupler, attenuator and quadrature couplers are reduced into an equivalent block, G_{INT}.

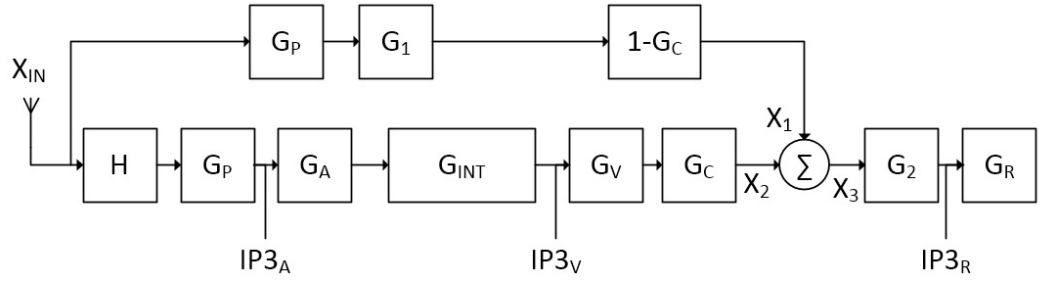

Figure 6.8: Step 3 of IP3 analysis breakdown

with,

$$H = \frac{X_{REF}}{X_{IN}} \tag{6.6}$$

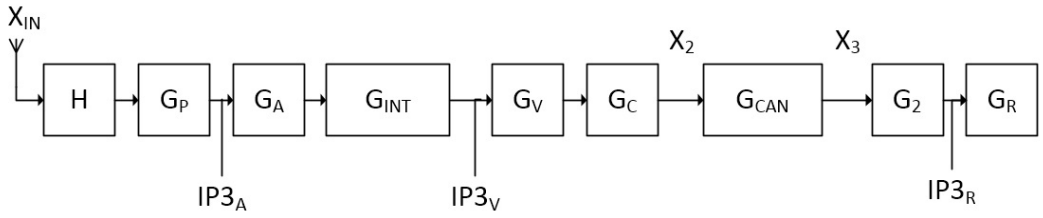

Figure 6.9: Step 4 of IP3 analysis breakdown

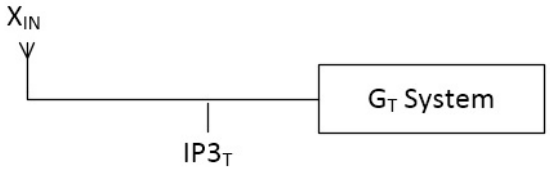

Figure 6.10: Step 5 of IP3 analysis breakdown

In Figure 6.9, the two paths that combine at the summation junction are redrawn as a single branch with a compensation block G_{CANCEL}, added for this simplification. G_{CANCEL} is calculated,

$$\begin{aligned} G_{CAN} &= \frac{X_3}{X_2} = \frac{X_1 - X_2}{X_2} \\ &= \frac{G_P G_1 (1 - G_C) - H G_P G_A G_{INT} G_V G_C}{H G_P G_A G_{INT} G_V G_C} \\ &= \frac{G_P G_1 (1 - G_C)}{H G_P G_A G_{INT} G_V G_C} - 1 \\ &= \sqrt{\left(\frac{G_P G_1 (1 - G_C)}{H G_P G_A G_{INT} G_V G_C} - 1 \right)^2} \end{aligned} \tag{6.7}$$

The system is simplified into a single block in Figure 6.10. The total IP3, namely $IP3_T$, with a total gain of G_T is derived.

$$G_T = H G_P G_A G_{INT} G_V G_C G_{CAN} G_2 G_R \tag{6.8}$$

$$\frac{1}{IP3_T} = \frac{HG_P}{IP3_A} + \frac{HG_PG_AG_{INT}}{IP3_V} + \frac{HG_PG_AG_{INT}G_VG_CG_{CANCEL}G_2}{IP3_R} \quad (6.9)$$

For the purpose of the study, the value for G_{CANCEL} is set to zero, as this represents perfect cancellation. Substituting (6.7) into (6.9),

$$\frac{1}{IP3_T} = \frac{HG_P}{IP3_A} + \frac{G_1(1-G_C)G_P}{G_VG_CIP3_V} \quad (6.10)$$

,yields the equation for the total system IP3. The total system IP3 is reduced with a decrease in the coupling factor of G_C. This is an inverse response to the effect of the coupling factor on the noise figure.

6.3.2 Third-order Intermodulation Distortion and SINR

Expressions for intermodulation distortion and noise at the receiver will allow for the derivation of an expression for SINR. This equation related the noise and intermodulation distortion at the receiver and will allow for the calculation of the optimum coupling value at the cancellation junction [36] as the equation for SINR encapsulates both signal and distortion/noise components.

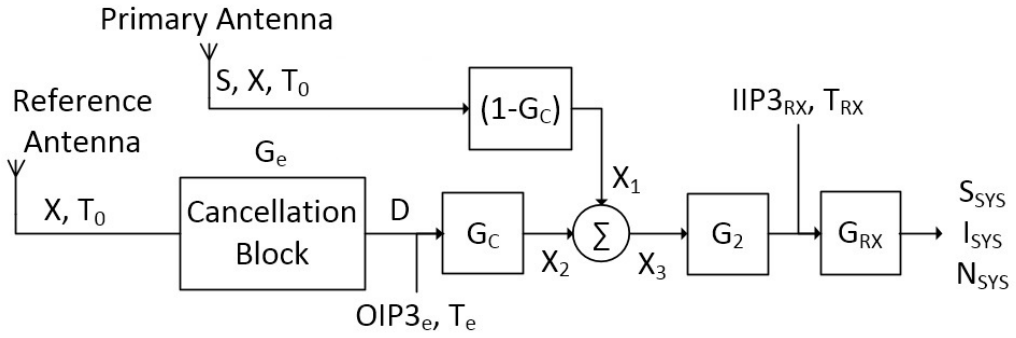

Figure 6.11: IP3 distortion calculation block diagram

In Figure 6.11, the value of $OIP3_e$ is specified at the output of the cancellation system block as this makes the value independent of gain of the internal blocks, such as the vector modulator.

For simplification, the protection circuit and coarse amplitude control couplers are removed which appear in both the reference in primary branches. The levels of the jamming signals (X) for the reference and primary paths are

also assumed equal, resulting in $X_3 = 0$. To allow $X_3 = 0$, the gain of the cancellation block is therefore,

$$G_e = \frac{(1 - G_C)}{G_C} \tag{6.11}$$

When $X_3 = 0$, third-order modulation distortion is only produced by the cancellation block and no modulation distortion is produced by the receiver. The third order distortion of the cancellation block, at point D, is calculated as follows,

$$D = \frac{G_e^3 X^3}{OIP3_e^2} \tag{6.12}$$

The third order intermodulation distortion level at the receiver output is calculated as follows,

$$I_{SYS} = \frac{G_{RX} X^3 (1 - G_C)^3}{OIP3_e^2 G_C^2} \tag{6.13}$$

With the intermodulation distortion at the output of the receiver defined, the SINR at the receiver can be calculated if the signal power S, and the noise power N, are defined at the receiver.

$$S_{SYS} = S(1 - G_C)G_{RX} \tag{6.14}$$

$$N_{SYS} = k_B B_W G_{RX}(T_{RX} + T_e G_C + T_0) \tag{6.15}$$

By combining the expressions for the signal power, the noise power and the interference power, the SINR can be defined,

$$SINR_{SYS} =$$

$$\frac{S(1 - G_C)G_{RX}}{\frac{G_{RX} X^3 (1-G_C)^3}{OIP3_e^2 G_C^2} + k_B B_W G_{RX}(T_{RX} + T_e G_C + T_0)} \tag{6.16}$$

6.4 Optimum Cancellation Coupling

With the definition of a SINR expression for the cancellation system, we can optimise the coupling value for the cancellation junction coupler by maximising SINR [36]. To find this coupling value, the expression for SINR will be differentiated in terms of G_C,

$$\frac{dSINR_{SYS}}{dG_C} = \frac{d}{dG_C}\left(\frac{A(1-G_C)}{B(\frac{(1-G_C)^3}{G_C^2}) + C(D+EG_C)}\right) \tag{6.17}$$

with,

$$A = S \tag{6.18a}$$
$$B = \frac{X^3}{OIP3_e^2} \tag{6.18b}$$
$$C = k_B B_W \tag{6.18c}$$
$$D = T_{RX} + T_0 \tag{6.18d}$$
$$E = T_e \tag{6.18e}$$

By substituting unimportant terms as in (6.17), the differentiation process in greatly simplified. To complete the differentiation, the quotient rule is used:

$$D\left(\frac{f(x)}{g(x)}\right) = \frac{g(x)f^{'}(x) - g^{'}(x)f(x)}{g^2(x)} \tag{6.19}$$

The result, with the squared denominator term removed due to the equation being set to 0 in order to find a peak on the curve, is the following:

$$\begin{aligned} 0 = &\left[B\frac{(1-G_C)^3}{G_C^2} + C(D+EG_C)\right][-A]\ldots \\ &+ [A(1-G_C)]\left[B - \frac{3B}{G_C^2} + \frac{2B}{G_C^3} + CE\right] \end{aligned} \tag{6.20}$$

resulting in the equation,

$$\frac{dSINR_{SYS}}{dG_C} = \frac{(S \cdot OIP3_e^2 C(2(1-G_C)^3X^3 - k_B B_W OIP3_e^2 C^3(T_0+T_e+T_{RX}))}{(k_B B_W OIP3_e^2 C^2(T_0+CT_e+T_{RX}) + (1-G_C)^3X^3)^2} \tag{6.21}$$

The equation is set to zero in order to find the minima, resulting in the denominator falling away. For $0 < G_C < 1$,

$$\frac{1-G_C}{G_C} = \sqrt[3]{\frac{k_B B_W OIP3_e^2(T_0+T_e+T_{RX})}{2X^3}} \tag{6.22}$$

The real valued root is of interest in determining the optimal coupling for power gain values, thus,

$$G_C(opt) = \frac{2^{1/3}X}{(k_B B_W OIP3_e^2(T_0+T_e+T_{RX}))^{1/3} + 2^{1/3}X} \tag{6.23}$$

6.5 Chapter Closing Summary

With the derivation of expressions for the system noise figure, IP3, optimisation of component sequences for noise figure, and the derivation of the optimal coupling equation for the cancellation coupler, a better design can be implemented. The following chapter continues onto testing of the system as it was designed in Section 5.

Chapter 7

System Measurements

7.1 Chapter Summary

The testing chapter details the numerous test procedures that will be used in order to quantify the performance of the prototype. Results are detailed along with the test descriptions. The GUI link between the user and the hardware is also reviewed in the chapter.

7.2 User Interface Design

The user interface design is required to have the following features:

1. Arduino Connection Interface
2. Coarse Attenuation Control Interface
3. Vector Modulation Control Interface
4. Vector Modulator Control Line Plot
5. Switch Readout Function
6. Power Sensor Level Plot
7. Auto Cancellation Function
8. Information Display Feed

Figure 7.1 is a screenshot of the graphical user interface designed in Qt, a GUI creation software designed by Nokia. The code is based on C++ as the compiler is run by Microsoft Visual studio. The various functions listed above are labelled in Figure 7.1.

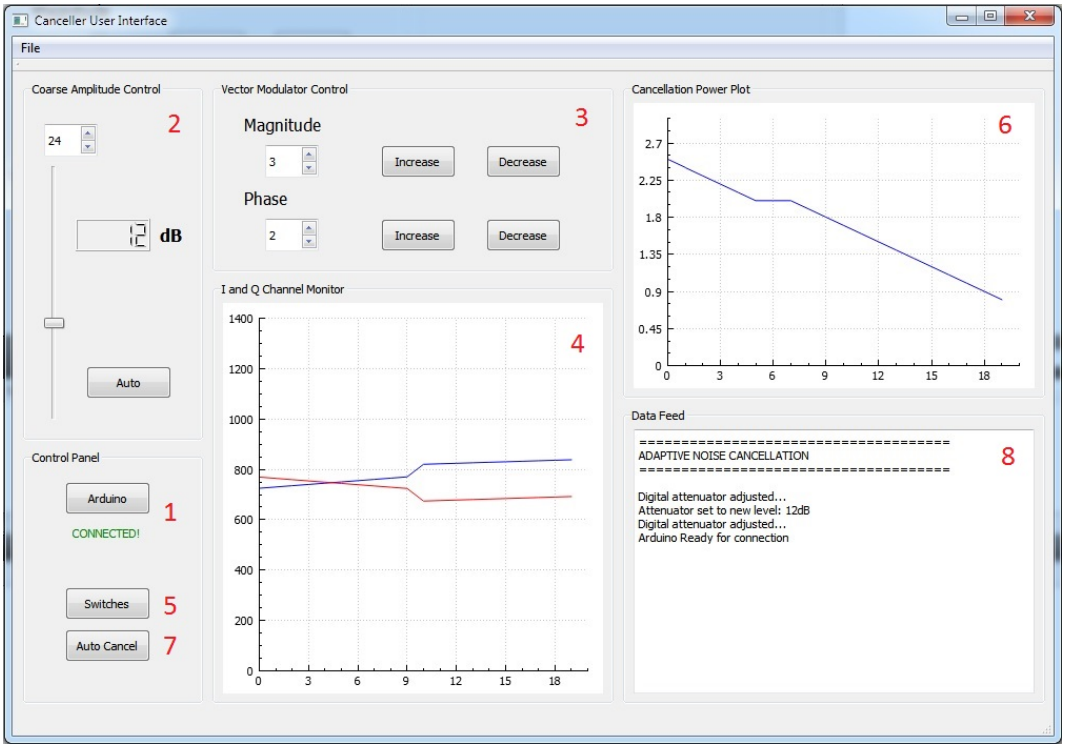

Figure 7.1: Screenshot of Graphical User Interface

1 : The Arduino connect button seeks out the COM port that contains the vendor and product ID that matches that of the Arduino Due board used. If present, a serial object is created and initialised. If the device is not found, the software debug window will display a list of all the available devices.

2 : The coarse amplitude control panel gives the user the option of manually selecting the level of cancellation or performing the calculation automatically.

3 : The vector control panel allows the user to adjust the I and Q vectors up or down by the amount specified in the spin boxes. Amplitude varies the I and Q vectors equivalently while phase varies the vectors inversely.

4 : The I/Q plot panel gives a real time plot of the I/Q vectors. In manual cancel mode, the graph updates with every user adjustment while in auto mode, the values for I and Q are constantly updated by the Arduino function loop.

5 : The switch function gives a printout of the level of power measured by the power sensor from each switch input. It serves as a useful debugging tool and monitor of circuit occurrences.

6 : The power plot graph performs a task identical to the graph in '4'. Its purpose is to plot the post cancellation power level (error), and allow for the user to track the progress of the cancellation performance.

7 : The auto cancel switch initiates the Arduino auto control function. Manual control is deactivated for this instance until the switch is pressed again. In auto cancellation mode, the Arduino code attempts to minimise the cancellation power output by adjusting the coarse amplitude control attenuator as well as the vector modulator.

8 : The data feed outputs the actions of the user as well as the power levels at the switches if function '5' is performed.

7.3 Single Signal Test

A single frequency signal can be generated by a signal generator and in turn cancelled again as a test measure. Additionally, a vector network analyser can be used to perform the same task but over a swept bandwidth of single frequencies.

7.3.1 Signal Generated

A single sinusoid signal is generated, 20 dB of the signal is coupled to the canceller reference input while the rest is passed through to the RF input of the canceller. The output signal power is measured with no cancellation present and then again with maximum cancellation in order to determine the maximum cancellation level. The diagram showing the test setup is displayed in Figure 7.2.

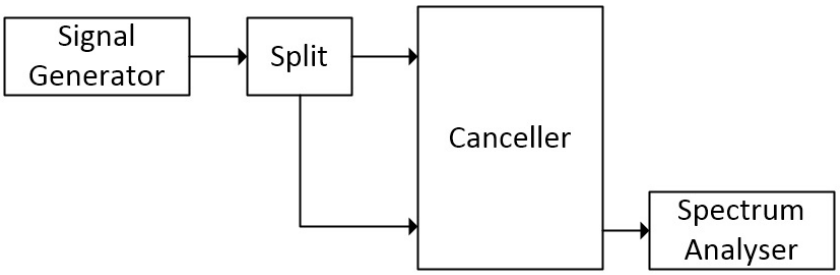

Figure 7.2: Signal generator input sinusoid test setup

The results for the test are plotted in Figure 7.3. The single sinusoid of 460 MHz with an amplitude of -35 dBm is passed to the canceller system. The no cancellation level is higher as a result of amplification at the end of the receiver chain output before the signal passes to the spectrum analyser. With cancellation at almost maximum, the level of the signal that remains is roughly -98 dBm. The total cancellation, the difference between the two signal power levels, is 73 dB.

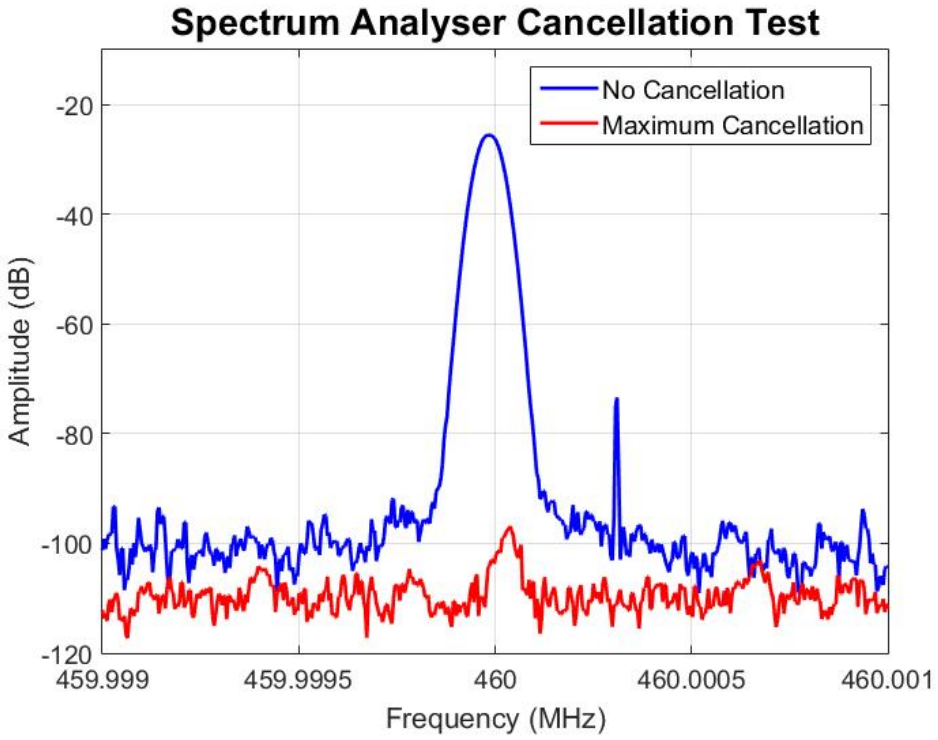

Figure 7.3: Signal generator cancellation test results

7.3.2 Vector Network Analyser Test

By splitting the output from Port 1 of a network analyser as in the test above, the signal can be cancelled and it will reflect as a dip in the dB|S21| characteristic at the frequency of cancellation. The difference between the dB|S21| level before cancellation and the level after cancellation is the total cancellation performed by the system. The test setup is described in Figure 7.4.

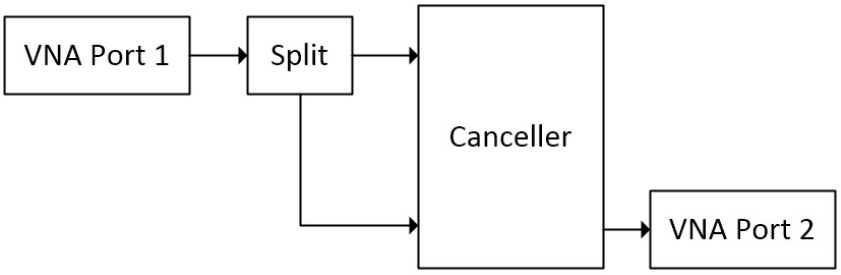

Figure 7.4: VNA cancellation test setup

The test results for the VNA test are displayed in Figure 7.5. The VNA dB|S21| is equal to roughly 10 dB with no anti-interference signal present. The gain can be accounted for by the amplifier stage at the end of the receiver chain output. This positive 10 dB gain is added to the cancellation total as the gain also affects the communication signal amplitude.

The level of cancellation achieved was between -60 dB and -70 dB. Added to the positive initial 10 dB gain, the total cancellation achieved for the test was roughly 80 dB. This is a substantial reduction in interference signal level. This value however, will not be the performance at all times. Referring back to Figure 2.2 in Chapter 2.2, a variation of amplitude or phase of the smallest magnitude will greatly affect the cancellation level.

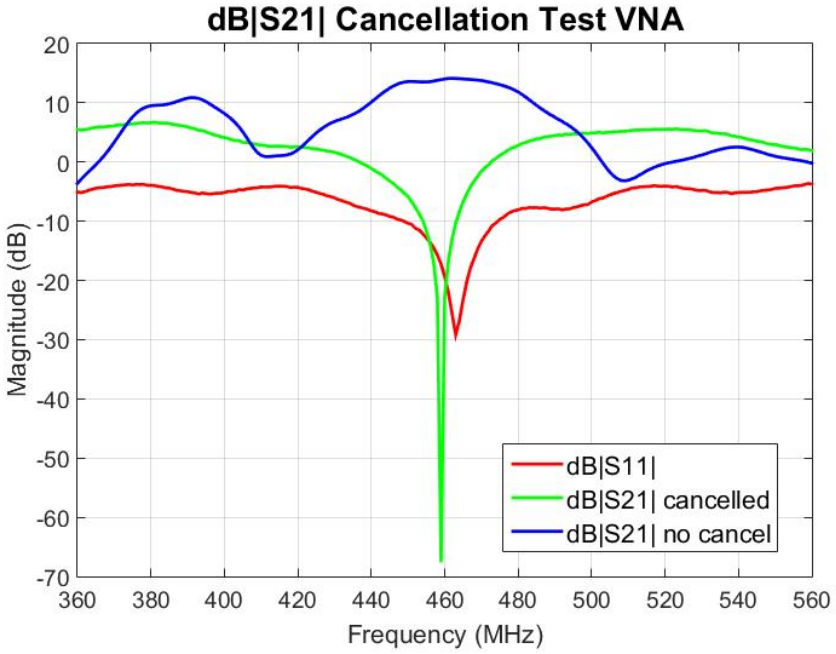

Figure 7.5: VNA cancellation test results

7.4 Audio Cancellation Test

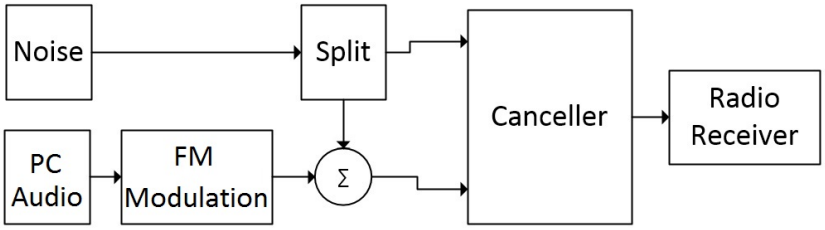

Figure 7.6: Audio and noise test setup

The audio cancellation procedure is the first practically applicable test that will be performed to characterise the system cancellation performance. A test radio communication signal is generated, attenuated, and added to a high power noise signal (Section A.3) to simulate the real life situations of a co-located communications and jammer system. A diagram representation of the audio cancellation test procedure is displayed in Figure 7.6.

The audibility of an audio signal with an amplitude of -70 dBm in the presence of a -20 dBm signal equates to a cancellation level of up to 50 dB.

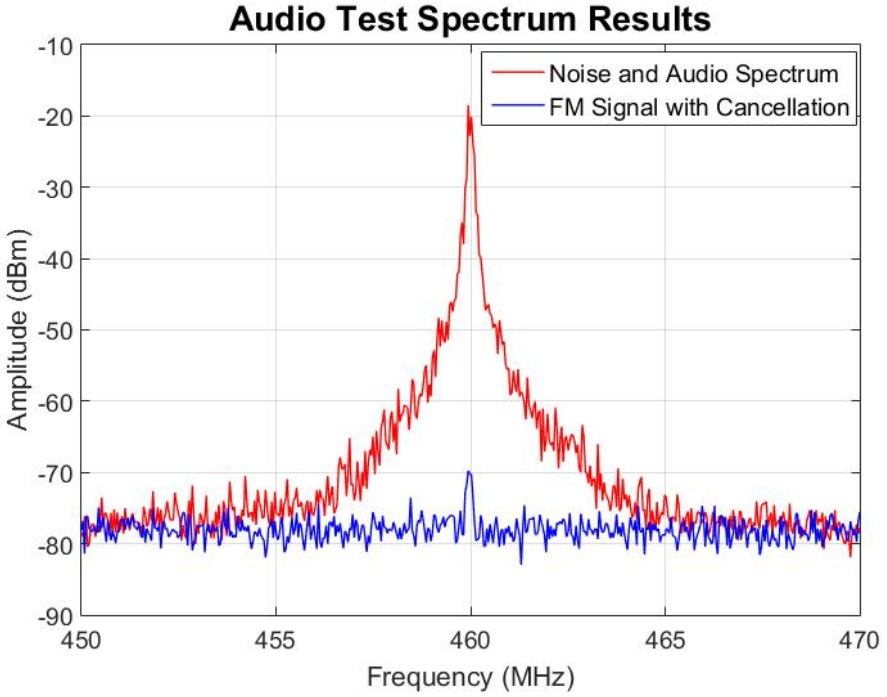

Figure 7.7: Audio and noise test results

In Figure 7.7, the plot shows two signal spectra plotted together. The larger of the two is of the noise added to the FM modulated signal, with the second of the audio signal with cancellation active. The audio is audible with cancellation on as almost all the noise has been cancelled. With the canceller turned off, audio is completely lost in the noise.

7.5 Sensitivity Performance Test

A complete system sensitivity test will be performed to demonstrate the effects of the canceller on the system as well as its ability to cancel noise. It is a comprehensive test procedure that most accurately represents a practical application of the system. 20 dB SINAD measurements are done at different points of the system by performing a series of different tests.

The first is to measure the radio sensitivity as a baseline. From here, the sensitivity of the radio is measured through the cancellation circuit to demonstrate the degradation of the signal to noise ratio of the radio due to canceller noise figures. The same measurement is then made with the canceller reference channel (anti-ref generating circuit) disconnected in order to demonstrate the noise figure effect of the cascaded cancellation components as done in Section 6.2.

Noise is then added to the system and a sensitivity measurement of the radio is done without the canceller connected in. The canceller is then connected in before the radio and a sensitivity measure is done with the system performing adaptive cancellation in the presence of noise.

7.5.1 SINAD measurement

The SINAD measurement is made with a VX-160EU antenna as a baseline. All measurements are ported directly through the radio antenna port from where the demodulated audio signal is passed to a HP communications analyser. Figure represents the SINAD measurement test setup.

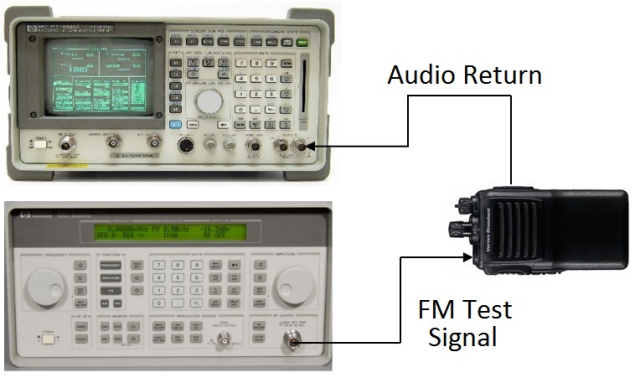

Figure 7.8: SINAD measurement setup concept

7.5.2 Results

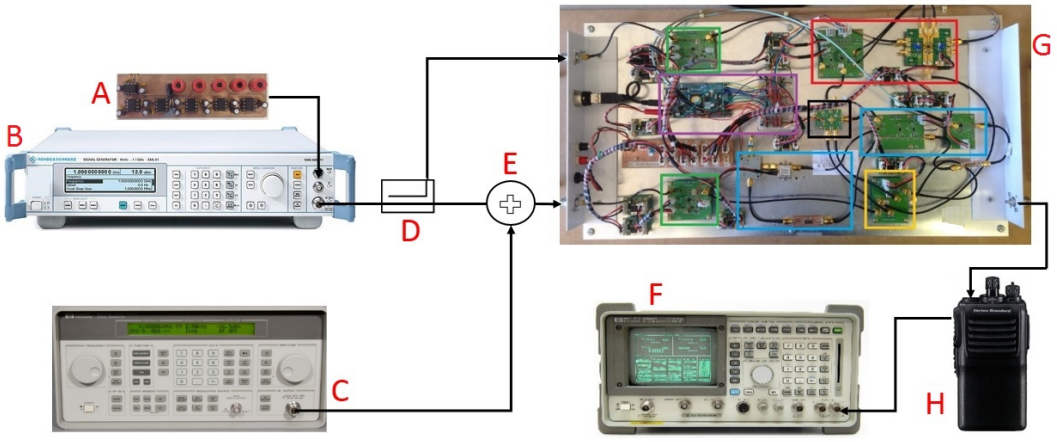

Figure 7.9: Full system cancellation SINAD measurement test setup

In Figure 7.9, the complete test setup for the cancellation sensitivity performance is characterised. 'A' is the baseband OP-AMP based noise source that is FM modulated to 460 MHz through the use of 'B', a Rhode and Swartz SML 03 signal generator. The noise generated has an amplitude of -55 dBm. 'C' is a HP 8647A signal generator used to generate a 1 kHz signal FM modulated to 460 MHz with a FM deviation of 2 kHz. The amplitude of the signal generated by 'C' will be adjusted until a 20 dB SINAD level is achieved, resulting in a reading for the sensitivity of the system. 'D' is a ZX30-20-4-S Mini-Circuits 20 dB coupler used to provide the canceller 'G', with a reference of the noise in order to generate an anti-noise signal. 'E' combines the noise generated with the FM test signal generated by 'C'. The output of 'G' is passed to a VX-160EU handheld radio where the received signal is demodulated and fed to 'F'. 'F' is a HP 8920A communications tester that will be used to generate the SINAD value of the received signal.

The different measurement results to classify the sensitivity at different points in the circuit are displayed in Table 7.1.

Test	Results (dBm)
Radio Only	-110
Radio with full canceller	-82
Radio with canceller - no cancellation channel	-99.5
Radio with noise	-52.9
Radio with noise and adaptive cancellation	-80.7

Table 7.1: SINAD measurement results

It can be observed that the addition of the canceller system severely degrades the signal to noise ratio of the system. By disconnecting the vector modulator output at the receive chain circuit, the effects of the cancellation circuit consisting of the digital attenuator, amplifier, coupler and vector modulator can be seen. This difference is roughly 20 dB, which was confirmed by the noise figure sequence optimisation performed in 6.2.

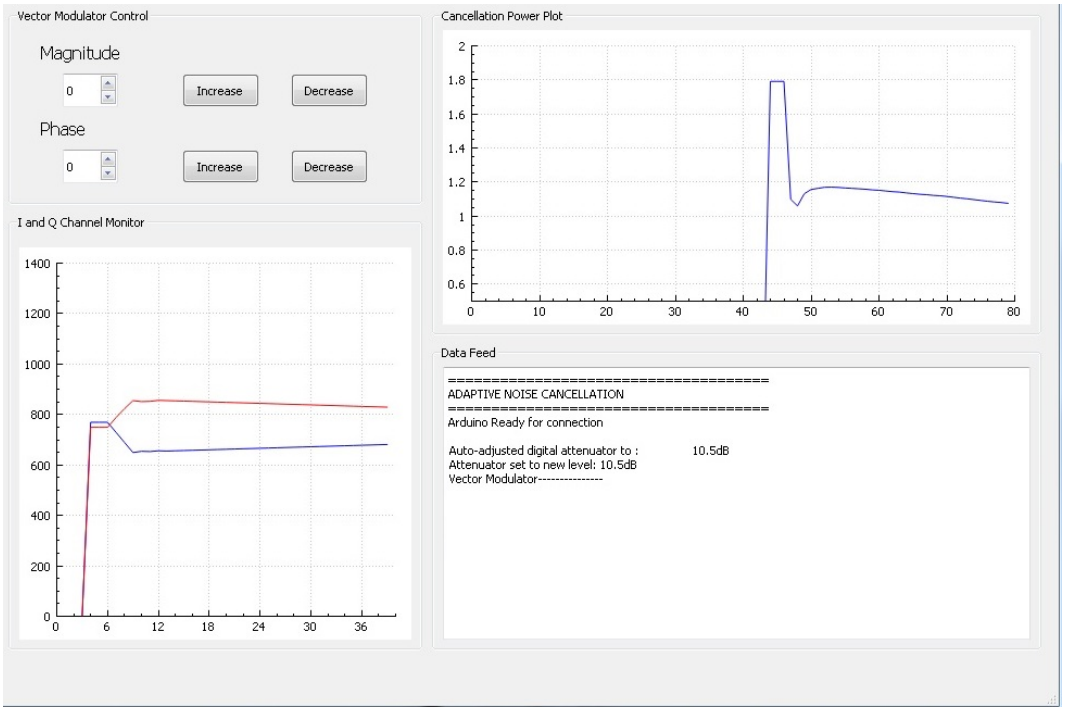

Figure 7.10: Cancellation sensitivity controller response as observed through user interface

Once noise is added to the radio, the SINAD is degraded to -52.9 dBm. The addition of the canceller circuit results in a SINAD reading of -80.7 dBm, a 30 dB cancellation result, with adaptive cancellation active. The response of the controller to autonomous cancellation is presented as a screenshot of the user interface in Figure 7.10. The procedure takes roughly 1 second.

7.5.2.1 Results with Antennas

The test performed as described above in Figure 7.9 does not take into the effect the influences of antenna propagation. The test is repeated with the implementation of antennas over a large room expanse as presented in 7.11. The test is performed in order to validate that the lab results of Figure 7.9 are not unrealistic.

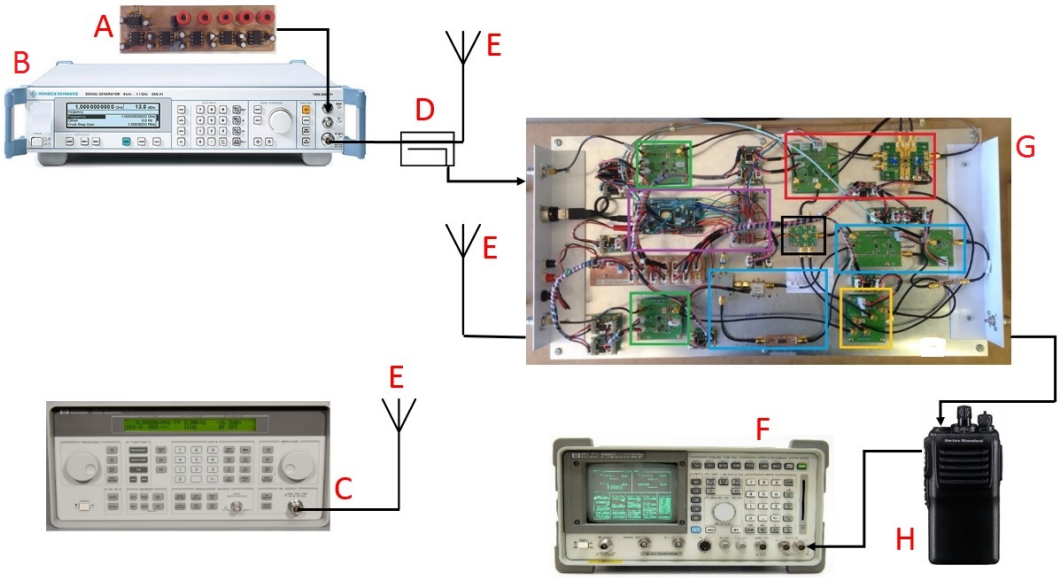

Figure 7.11: SINAD sensitivity test setup through use of antennas

The use of antennas requires the FM test signal to be transmitted through a rubber ducky monopole antenna and received through an identical antenna at the radio. The propagation loss through this cordless transmission must be characterised and used to offset the results achieved through the repeated tests of Section 7.5.2, on the setup described in Figure 7.11. All labels are identical in Figure 7.9 and 7.11, except for 'E', where the combiner has been replaced by rubber ducky monopole antennas to combine signals as required.

A signal splitter is inserted between the radio input port and antenna. Half of the signal is passed to a spectrum analyser. The difference between the amplitude of the test signal that is being transmitted and the signal power received at the radio (taking into effects the splitter), is the total attenuation through antenna propagation. The attenuation is recorded as 42.5 dB.

Test	Results (dBm)
Radio Only	-67
Radio with full canceller	-38
Radio with canceller - no cancellation channel	-53
Radio with noise	-1
Radio with noise and adaptive cancellation	-32

Table 7.2: SINAD measurement results for Antenna Test

From the results presented in Table 7.2, it is apparent that the results correlate to the connectorised sensitivity test performed in Section 7.5.2 with the difference equivalent to the recorded antenna propagation losses.

7.6 Closing Summary

With the testing methods having been described and the results for each presented, conclusions need to be made on the performance of the system. In the following chapter, the possible changes to design, optimisation considerations, and improvements to the design are discussed. From here, conclusions will be drawn on the current performance as well as the predicted improved second iteration performance on the overall validity and feasibility of the system.

Chapter 8

Conclusions and Recommendations

8.1 Chapter Summary

The chapter consists of a future development section as well as a conclusions section. Improvements and optimisations that are applicable to a second iteration prototype are discussed in detail. The complete system design process and the results achieved are then discussed.

8.2 Future Considerations

The future development components for the project presented during testing, construction and optimisation of the design parameters are discussed in the section. These second iteration build components will allow for the system performance to improve.

8.2.1 DAC and ADC resolution

The Arduino controller makes use of two built in DAC circuits. These devices have a resolution of 12 bits, equating to 4096 levels over a voltage of 0 V to 5 V. Each step of the DAC is therefore equivalent to a voltage change of roughly 1.2 mV.

The use of an Arduino is an easily implementable and cost effective method of control, processing and digital to analog conversion, however dedicated digital to analog circuitry and improved processing performance, will allow for faster and more accurate control of the cancellation signal generated by the vector modulator.

8.2.2 RF Switch Port-to-Port Isolation

The RF switch responsible for switching between the numerous power sensing points in the cancellation system, just as with most RF devices, has a port to port isolation rating. This quantity, often defined on the device datasheet, described the amount of signal that leaks through from one input port to the output or another input.

The isolation below 1 GHz is roughly 45 dB as specified by the datasheet. The power sensor circuit is required to measure signal power down to -120 to -110 dBm. Any power levels present at any of the switch inputs above -80 dBm, as is the case in most instances, will reflect in the power sensor, essentially lowering the dynamic range of the power sensor.

8.2.3 Mixer Improvements

An improvement in mixer performance and the improvement of additional circuitry associated with the frequency mixing process will improve system performance. The mixer is responsible for frequency mixing the power sensor signal up or down into the desired band of the power sensor filters and the band of its frequency operation.

The filter used in the system is an older model Mini-Circuits ZFY-11 frequency mixer. It is a level 23 mixer which requires a LO power of 23 dBm in order to perform as specified on the datasheet. It is generally recommended to use a mixer with a level just above the maximum anticipated input level expected. As the signals we anticipate are very low level signals, a mixer with the lowest level would prove the most successful whereas the ZFY-11 is a very high LO level mixer.

Signal generators do not generate perfect LO signals as the spectrum often contains intermodulation distortion components. By filtering the spectrum and allowing a good LO to pass to the mixer, fewer unwanted signals will be present at the mixer output. The same applies to the output in order to filter out leakage signals and intermodulation distortion where possible. Buffering the LO with an attenuator to decrease the VSWR will also improve mixer performance.

8.2.4 Lower NF components

The optimisation processes followed in Chapter 6.1 details the reduction of the system noise figure by optimisation of component sequences as well as coupling values and component parameter choices. Another improvement that can be made based on these results and the numerous equations derived in this chapter, is the selection of lower noise figure components at all sections of the

system. This includes further searching for possible components with lower noise figures and generally improved performance parameters.

8.2.5 Coupler Optimisation

The equation for SINR derived in Chapter 6.1 can be derived into an equation to optimise the summation coupler value to maximise the SINR of the system. By replacing the coupler in the circuit with the calculated coupler value, the system performance will be improved upon.

The same analysis can be applied to the sampling couplers that sample the RF and REF channels in order to perform coarse amplitude cancellation. The design incorporates 3 dB couplers of which there are two in series in the RF channel. The losses for the incoming signals are therefore upward of 7 dB, which should be avoided. The sample coupler values were chosen high to compensate for the power sensor measurement range and to alleviate some of the amplification needed in the power sensor circuit. This alleviation in amplification cannot however be justified by the level of signal loss in the RF channel and should be optimised or decreased.

8.2.6 NF Sequence Optimisation

By applying the optimal component sequence for noise figure calculations performed in Chapter 6.1, the performance of the canceller can be greatly improved. The effects of the high noise figure that the system adds due to the component sequences has a large effect. A spectrum analyser is used to compare the noise floor levels of the system with the noise on as well as off. Refer to Figure 8.1.

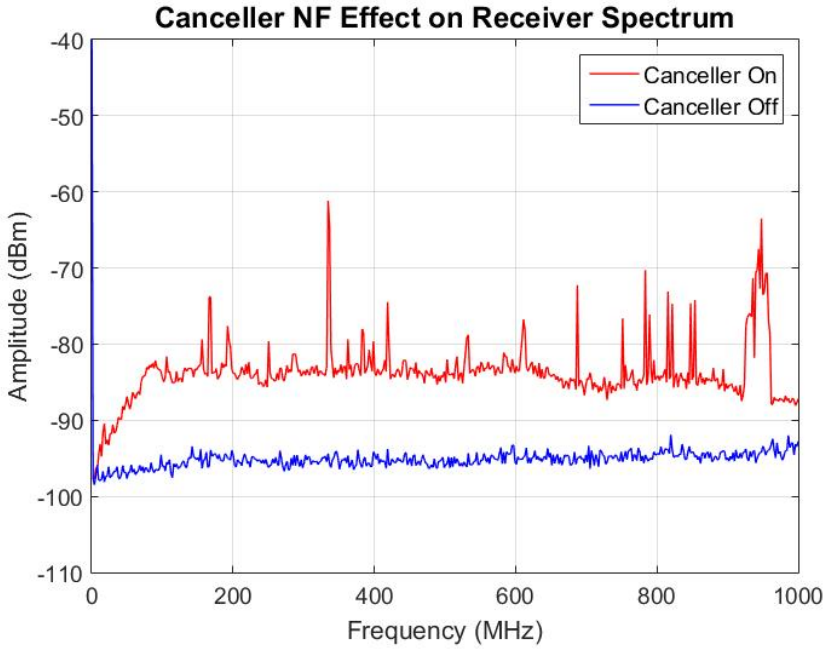

Figure 8.1: Noise floor of the canceller system

The system should add minimal noise to the RF signal input channel. Every dB of noise added is essentially removing a dB of cancellation that would have been possible. By raising the noise floor, the canceller is essentially limiting the smallest detectable signal that the receiver can demodulate.

An additional observation that can be made from Figure 8.1, is that the raised spectrum, due to the canceller circuit input, has numerous signal spikes. These signal spikes are a result of insufficient shielding. The PCB tracks and connection wires spread across the test rig act as small antennae, intercepting signals around the vicinity where the measurements were made. The largest spike on the furthest right side of the plot, in the 980 MHz region, is due to the system receiving cellular communications as a result of insufficient shielding. These effects can be minimised by encapsulating the system in a shielded enclosure.

8.2.7 Singular PCB and Shielding

Once the optimisation improvements and performing increasing changes have been made and tested, all the sub-circuits and circuit blocks can be combined and manufactured into single PCB circuit. The first iteration prototype was manufactured into separate blocks to allow for ease of testing and troubleshooting as well as easing the ability to characterise each of the design elements separately. At the same time however, the modulator implementation

of the design greatly increases the system physical size, requiring large amounts of interconnect cables to run all along the rig as well as multiple, repeated power supply circuits.

By manufacturing one PCB, the total noise radiating from wires and coaxial lines, as well as power lines running all over the circuit can be greatly reduced.

8.2.8 Tuneable Delay Line

As mentioned in Section 5.10.2, a delay line is required to phase align the RF IN channel and the reference channel by delaying the RF IN signals. The system made use of a single coaxial line with a specific length in order to achieve the correct coarse delay. By changing some of the canceller coaxial lines and arrangements in order to perform specific tests, the delay line must be adjusted accordingly.

As an alternative to arranging the various different coaxial lines available until a correct delay is found, a tuneable delay line component can be implemented to ease the cancellation process. It can be controlled by the controller and serve as a coarse phase adjustment device, similar to the purpose of the coarse amplitude attenuator for coarse amplitude control.

8.2.9 Error/Correlator Design Revision

The use of a power sensor correlator circuit is a novel approach to obtain and minimise the cancellation error signal. Multiple different technologies are available that could improve performance and simplify the cancellation process. Furthermore, as an alternative to changing the cancellation correlator/error detection circuit, a second stage of digital cancellation after the analog stage could be implemented to improve performance [18].

8.2.10 Additional Physical Cancellation Implementations

The design of the system only considers the electrical cancellation procedure through wave superposition. As an added consideration for cancellation improvement, the physical setup and location of antenna and components on the vehicle can be assessed.

Optimal positioning of devices for minimal jammer coupling into the communications channel should be considered alongside possible antenna nulling and shielding to minimise the effects of the jammer.

8.2.11 Analog and Digital Comparison

Cancellation in the digital domain can provide great performance improvements. A digital approach is often very expensive if sophisticated ADC and DAC circuitry is implemented. The use of much higher performance processing will also be required.

Even with the costs and latency issues of a digital system, analysis in the digital domain effectively removes the electrical aspect of the data and presents it in a very pure form. Powerful algorithms and high speed processing will allow for high levels of performance to be achieved. Furthermore, combinations of analog and digital cancellation interfaces will prove very successful.

8.3 Conclusion

8.3.1 Objectives of the Study

The objectives of the study were met. Cancellation technologies and novel approaches to noise and interference cancellation were studied and reviewed. A complete, operational first iteration canceller system was designed and constructed and tested for its ability to cancel noise and interference in a dynamic environment. Mathematical analysis was performed and numerous system parameters such as NF, IP3 and SINR being presented as functions.

8.3.2 System Performance

The performance of the system achieves cancellation results of up to 50 dB in a non-dynamic environment. In a fully dynamic environment, results of cancellation of up to 30 dB have been achieved. This performance is equivalent to 0.001% of noise subjected to the system allowing to pass to the receiver allowing for a considerable increase in communication distance.

By referring to the plot in Figure 2.3, in an environment with a noise floor of -80 dBm, a 0 dBm transmitted signal will be able to be received at an estimated distance of 250 m. With 30 dB cancellation, this distance increases to an estimated distance of over 1.5 km.

8.3.3 Future Development

The degradation of the signal to noise ratio caused by the components in the cancellation system directly decrease the cancellation performance. With the optimisation of the cancellation chain as presented in Section 6.2, the cancellation performance will be improved upon by an amount equivalent to the decrease in the noise figure.

Incorporation of the design into a singular shielded PCB, and implementation of the topics discussed in Section 8.2, can allow for a great improvement in cancellation performance.

8.3.4 Feasibility

The concept of adaptive noise cancellation has been implemented and proved to work with good results. By considering the current system performance, as well as considering the possible performance increase of a second iteration system build, the project is deemed successful and feasible for implementation in real world scenarios.

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Appendices

Appendix A

Additional Component Design

A.1 Chapter Summary

During the design and testing of the canceller system numerous additional components were required in concept testing or in the final test setup itself. The design of these initial components are described in this chapter.

A.2 Wilkinson Combiner/Splitter

The Wilkinson power divider is a lossy three-port network with all its ports matched and isolation between output ports. It is most often created using microstrip lines and can be designed to have an arbitrary split in power. The case considered here is an equal split Wilkinson power divider. The device uses 50Ω ports, a quarter wave length transfer split branch with an impedance of $\sqrt{2}Z_0$. A depiction of this configuration can be seen in Figure A.1. The design will then be further compacted by transforming sections of the microstrip into lumped elements according to their capacitive and inductive equivalent model [24].

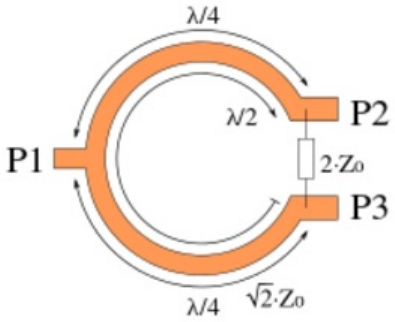

Figure A.1: Wilkinson Divider Microstrip Form

A.2.1 Design

The component design was performed using ADS. Schematic components and sections are plotted from libraries in the schematic editor. Parameters are set to values between a viable range corresponding to the correct dimensions for micro-strip operation at the correct frequency and desired impedance (50Ω). The software will be used to optimise the dimensions of the circuit in order to achieve the user defined goals using the built in optimiser console. The circuit as designed in the software is displayed in figure A.2.

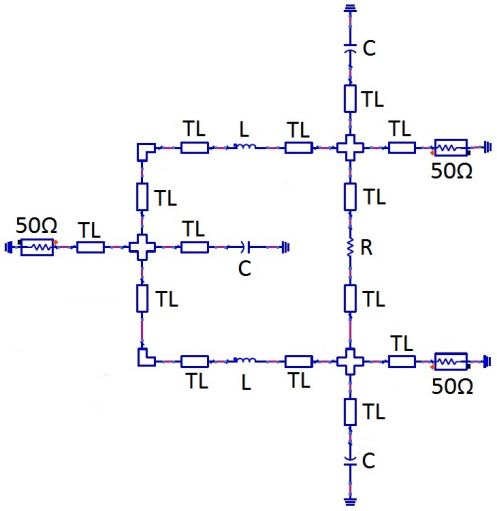

Figure A.2: ADS schematic of Wilkinson Divider circuit

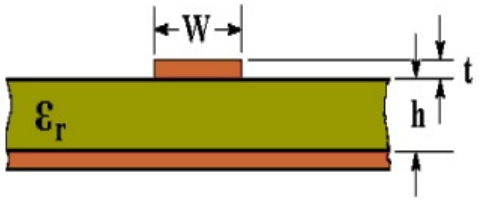

Figure A.3: Microstrip cross-section parameter definitions

$$Z_0 = \frac{87.0}{\sqrt{\epsilon_r + 1.41}} x \ln \frac{5.98h}{0.8W + t} \tag{A.1}$$

The starting value for the optimisation is calculated in A.1 [25]. The calculation is based on FR-4 substrate which is available in the milling

laboratory. The values are substituted and W is solved for. The substrate parameters are the following:

1. h = 1.6mm
2. er = 4.4
3. t = 35um

The optimisation process yields a structure with desirable reflection coefficients at all ports in order to allow performance as a splitter as well as a combiner. The layout is automatically generated by the software and the resulting layout is plotted after a few minor alterations. The layout can be seen in Figure A.4 while Figure A.5 is a photograph of the final milled circuit.

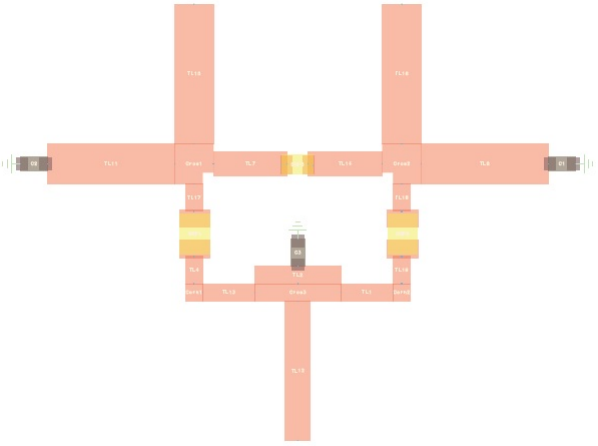

Figure A.4: ADS generated layout of microstrip Wilkinson divider

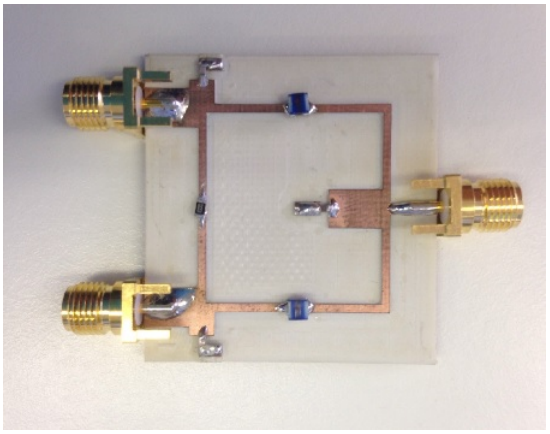

Figure A.5: Final device after manufacturing

A.3 Operational Amplifier Noise Source

All electrical charge experience random statistical variations and fluctuations that form the basis of noise analysis. The most common sources of noise in electrical sources are the following [27; 28]:

- Shot Noise
- Thermal Noise
- Flicker Noise
- Burst Noise
- Avalanche Noise

Operational amplifier noise can be analysed through superposition, whereby each noise source is isolated and all other sources of noise assumed to be noiseless. Op-amps are cascaded in order to continually multiply and add to the internal noise of the device. A cascaded network of 5 Op-amps is constructed and simulated in LTSpice. The setup is as shown in Figure A.6.

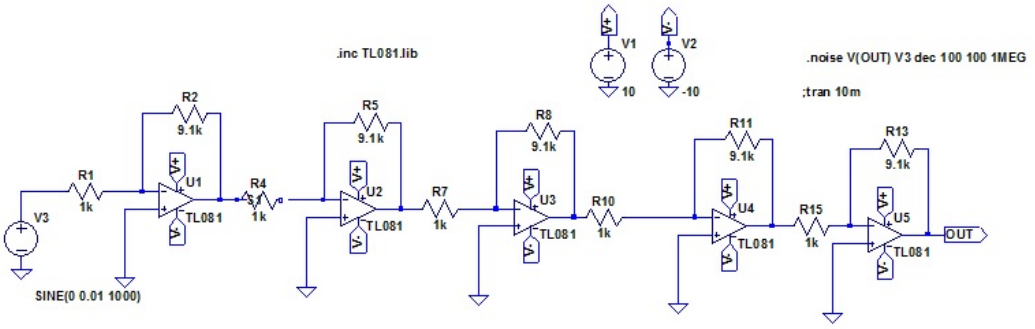

Figure A.6: LTSpice setup configuration for noise analysis

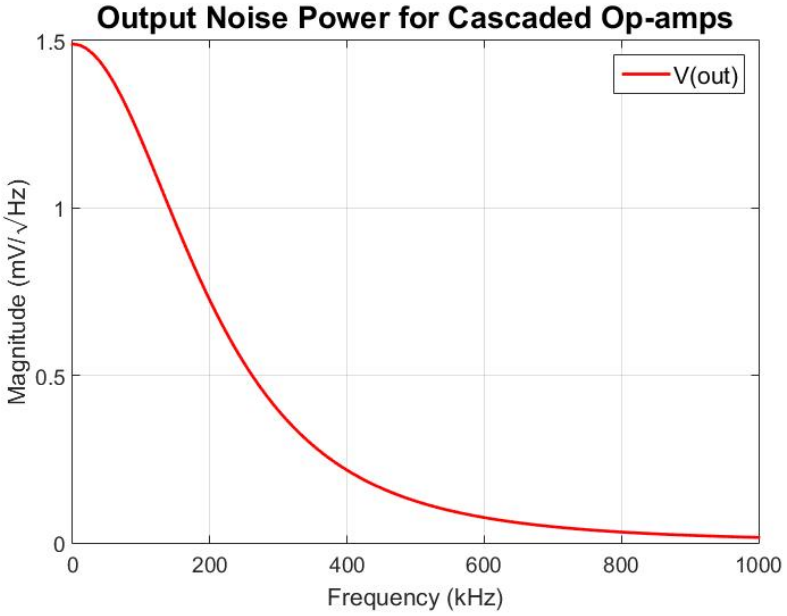

Figure A.7: Voltage sepctral density plotted from Spice simulation

LTSpice simulation has a domain analysis noise analysis tool that takes into account thermal noise as well as shot and flicker noise. This Op-amp configuration yields a noise density plot as seen in Figure A.7. The model for the TL081 Op-amp as was used in the practical circuit was imported. The theoretical RMS noise voltage for the configuration can be calculated by integrating the spectral density plot from Figure A.7 to yield the power density [26].

$$\int_{fL}^{fH} (voltage - spectral - density)^2 df$$

The aim is to cascade multiple Op-amps and rely on the cascaded amplification of internal noise in order to create a source of random or white noise. This noise source is a safer alternative to the use of high power RF amplifiers when measurements and tests with existing hardware are to be performed on expensive testing and measurement equipment.

A PCB of the Op-amp noise source will be designed in KiCAD. The PCB layout for the design is shown in Figure A.8. As shown in the figure, the circuit has been decoupled with a large and small decoupling capacitor at both positive and negative source ports as close to the Op-amp terminals as possible. This, in conjunction with the use of a ground plane PCB and slightly lower amplification per Op-amp level, ensures oscillations and instability as observed in previous versions of the design, have been eliminated.

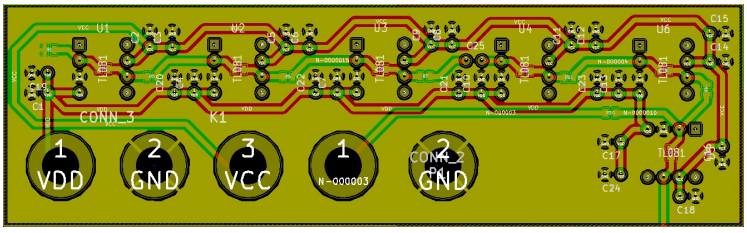

Figure A.8: KiCAD PCB layout for Noise Source

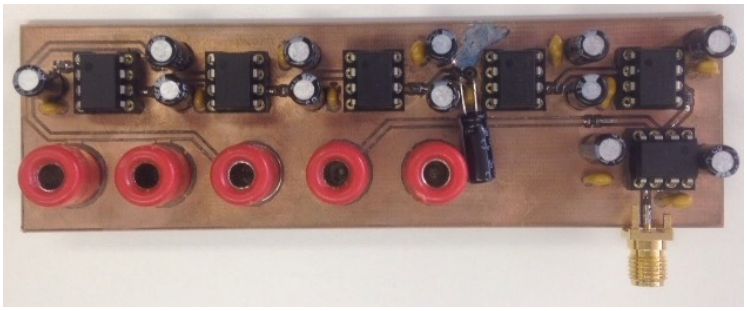

Figure A.9: Photograph of final Noise Source design

A photograph of the final manufactured design is displayed in Figure A.9. The device was tested using an oscilloscope to measure the transient response, and a spectrum analyser was used to plot the spectral density of the noise. These measurements are present in Figure A.10 and Figure A.11 respectively.

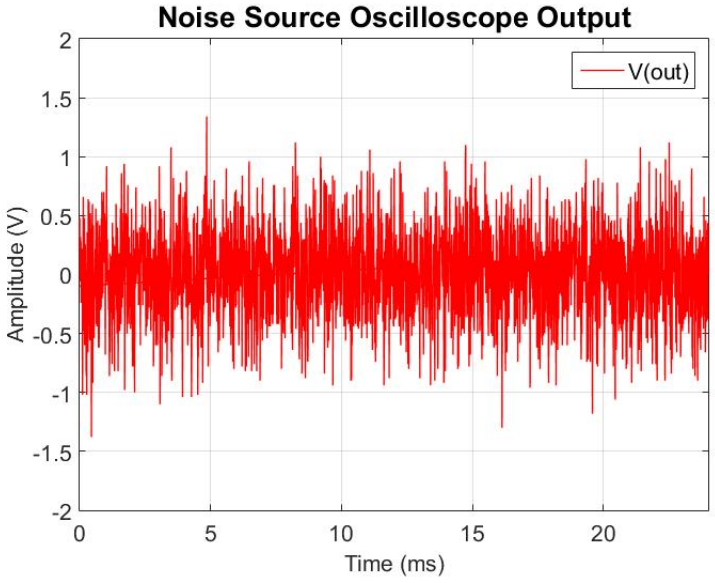

Figure A.10: Transient noise voltage generated by Noise Source

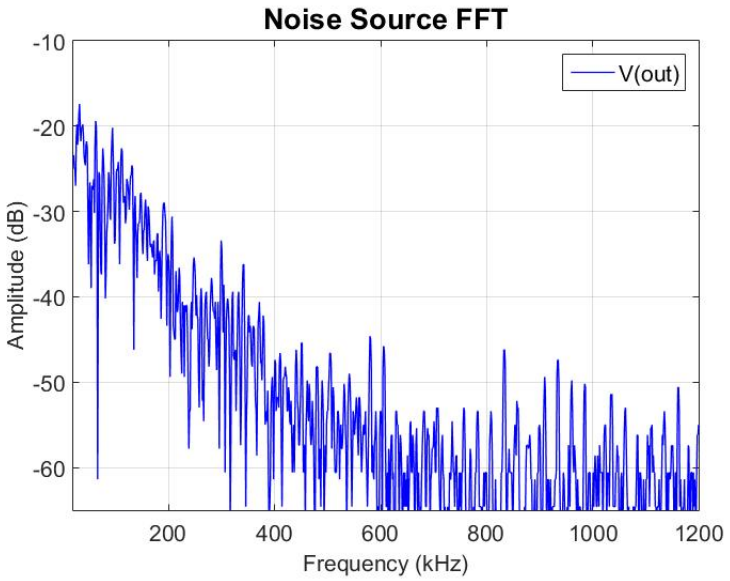

Figure A.11: Frequency Spectrum of Noise Source

A.4 Microstrip GPS Filter

During the testing of the power sensor circuit, a higher order filter with a narrow bandwidth was needed to shrink the spectrum of noise and signal passed through to the power sensor. The sensor makes a RMS measurement, allowing the noise and signals passing through the filter band to contribute to the measurement. Limiting the signals passed through will improve power sensing

The microstrip filter was designed using AWR Filter Design Wizard. The center frequency is 1575.42 MHz with a BW of 50 MHz. In order to achieve a sharp enough cut-off a 5th order filter is required. The substrate is a 1.524mm thick Rogers 4003C substrate with a 35μm copper thickness. The PCB layout is presented in Figure A.12. A photograph of the filter follows in Figure A.13.

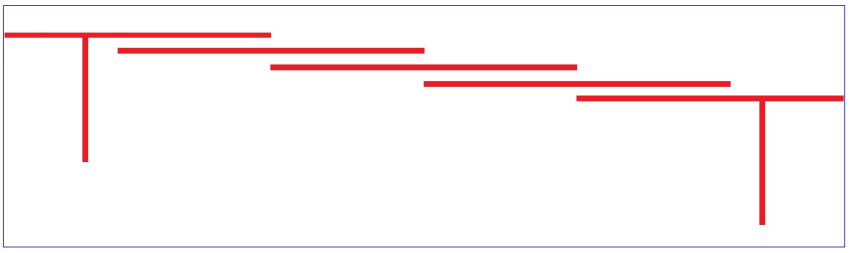

Figure A.12: Microstrip Filter Layout

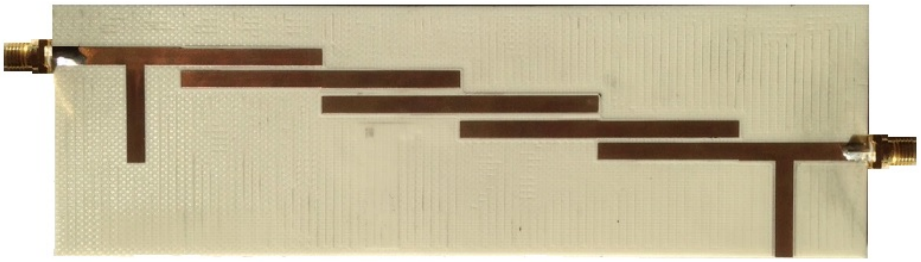

Figure A.13: Microstrip Filter Photograph

A.5 Power Amplifier Enclosure

The construction and testing of a canceller system requires a source of noise and interference that best represents the PA and its contributions. This section covers the construction and testing of a PA enclosure complete with power, heat management and connections for RF applications. An operational amplifier based noise source was also constructed due to time and cost implications during the early stages of the project. The design of this source is detailed in Section A.3.

N-type connectors form the input and output to the amplifier to allow for a rugged operating environment, while SMA coaxial cable connects the N-type sockets to the amplifier internally. Fans are inserted strategically around the case to allow air flow through the large heat-sink attached to the power amplifier. The 3D design are courtesy of GEW Technologies and was used to construct the device. The 3D model is displayed in Figure A.14.

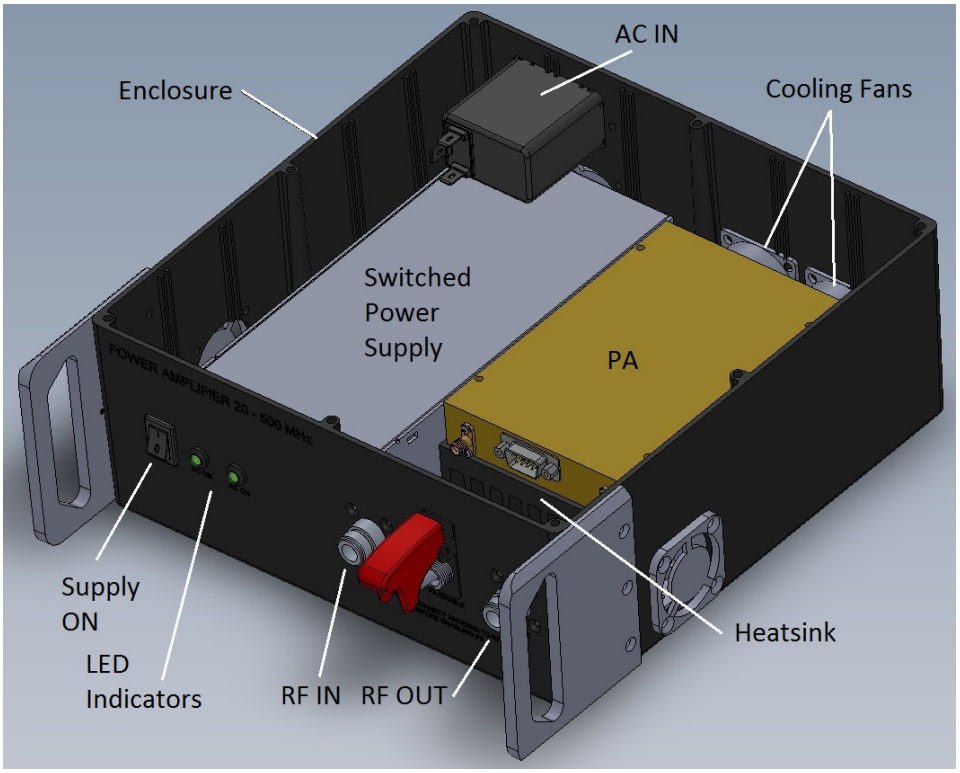

Figure A.14: 3D Model of power amplifier enclosure

Appendix B

Schematics

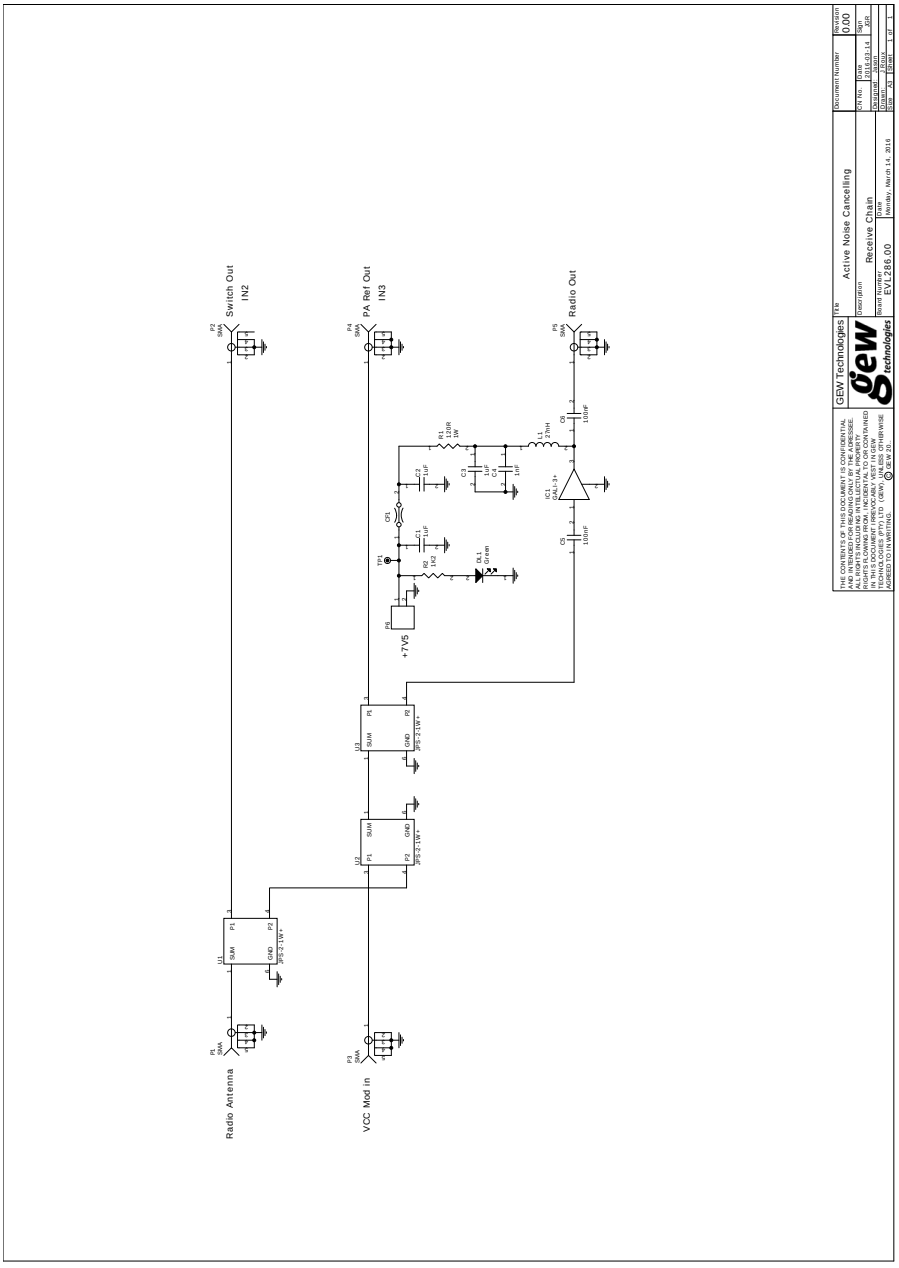

Figure B.1: Receive Chain Final Design Schematic

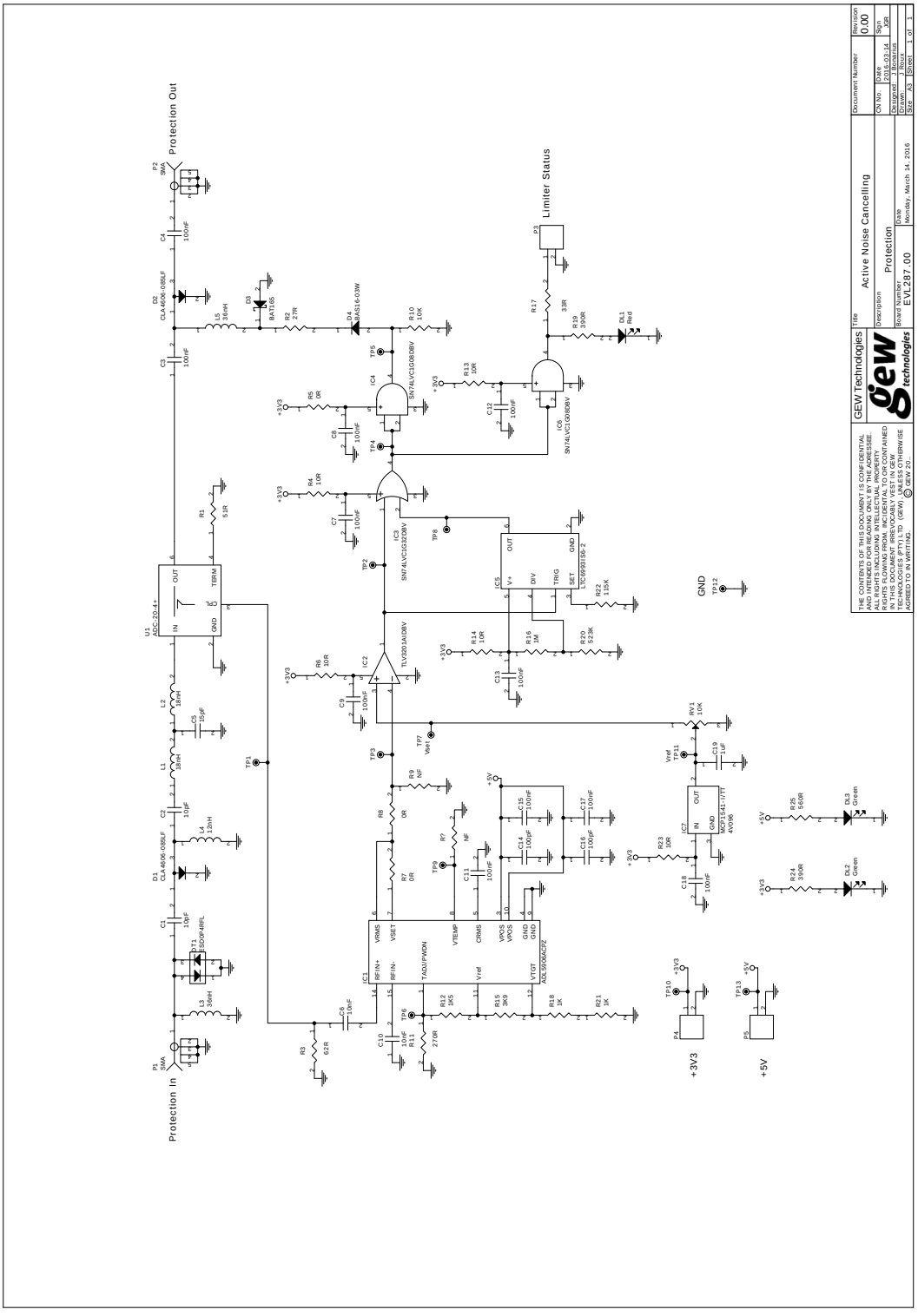

Figure B.2: Protection Circuit Final Design Schematic

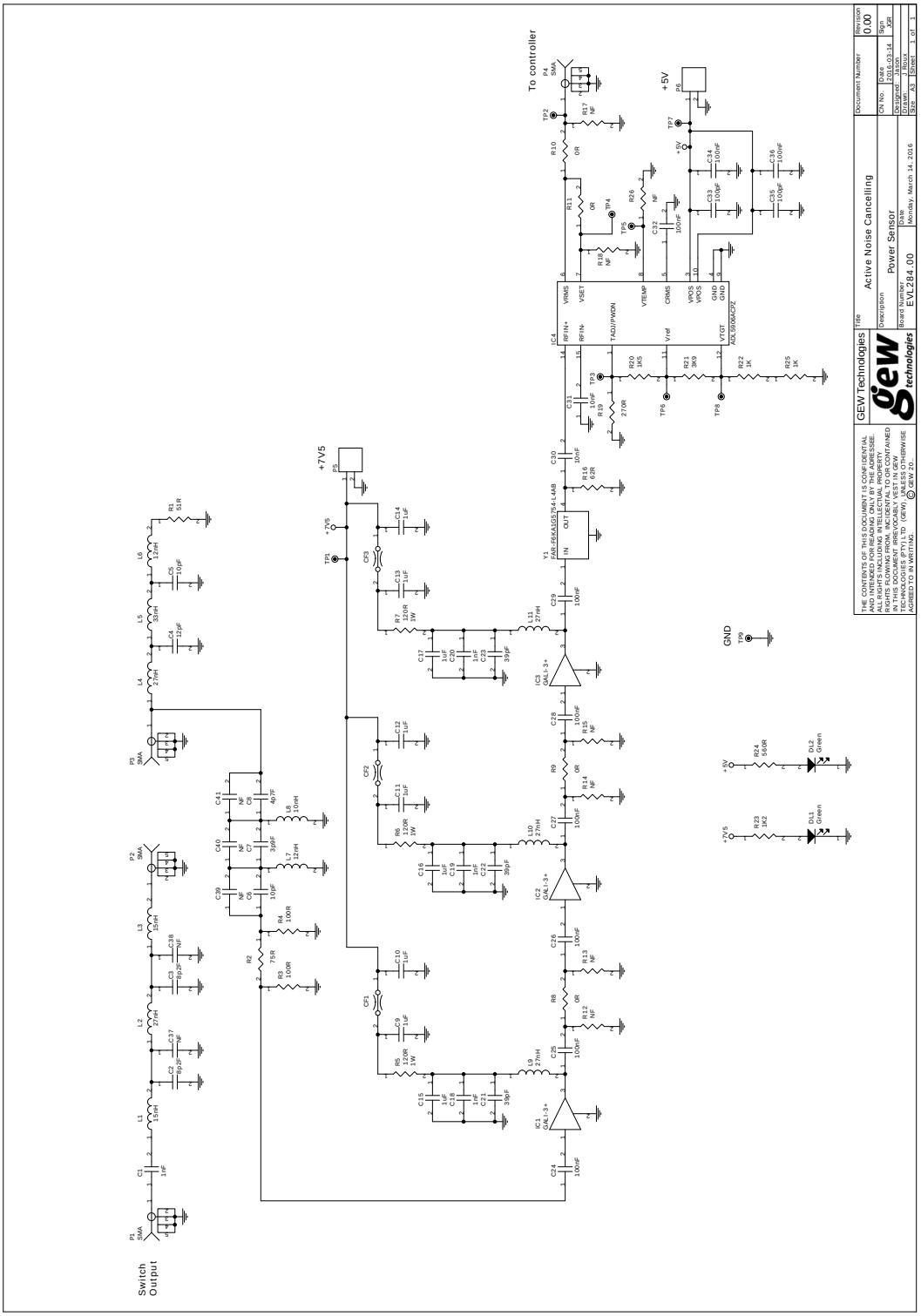

Figure B.3: Power Sensor Final Design Schematic

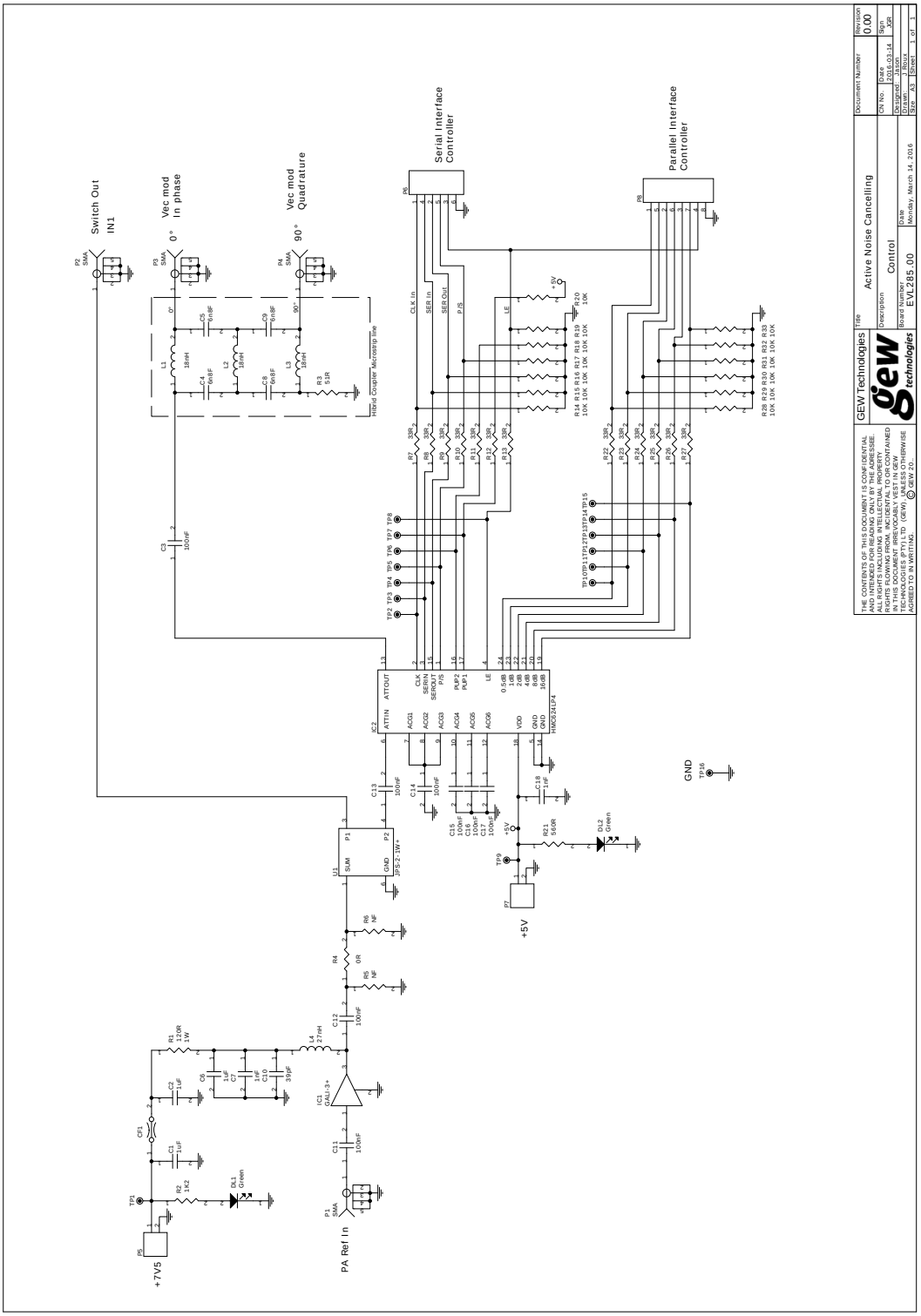

Figure B.4: Canceller Final Design Schematic